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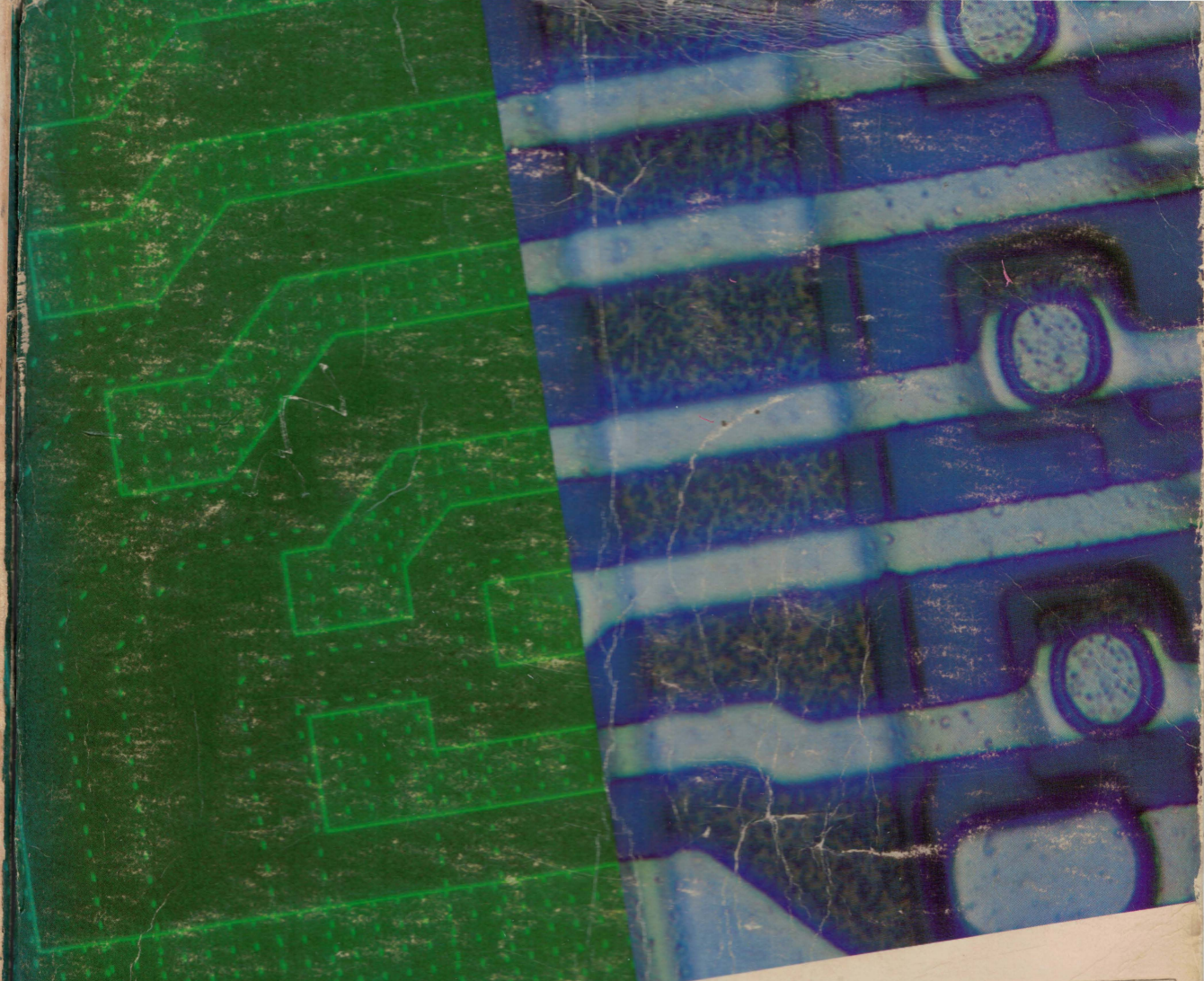

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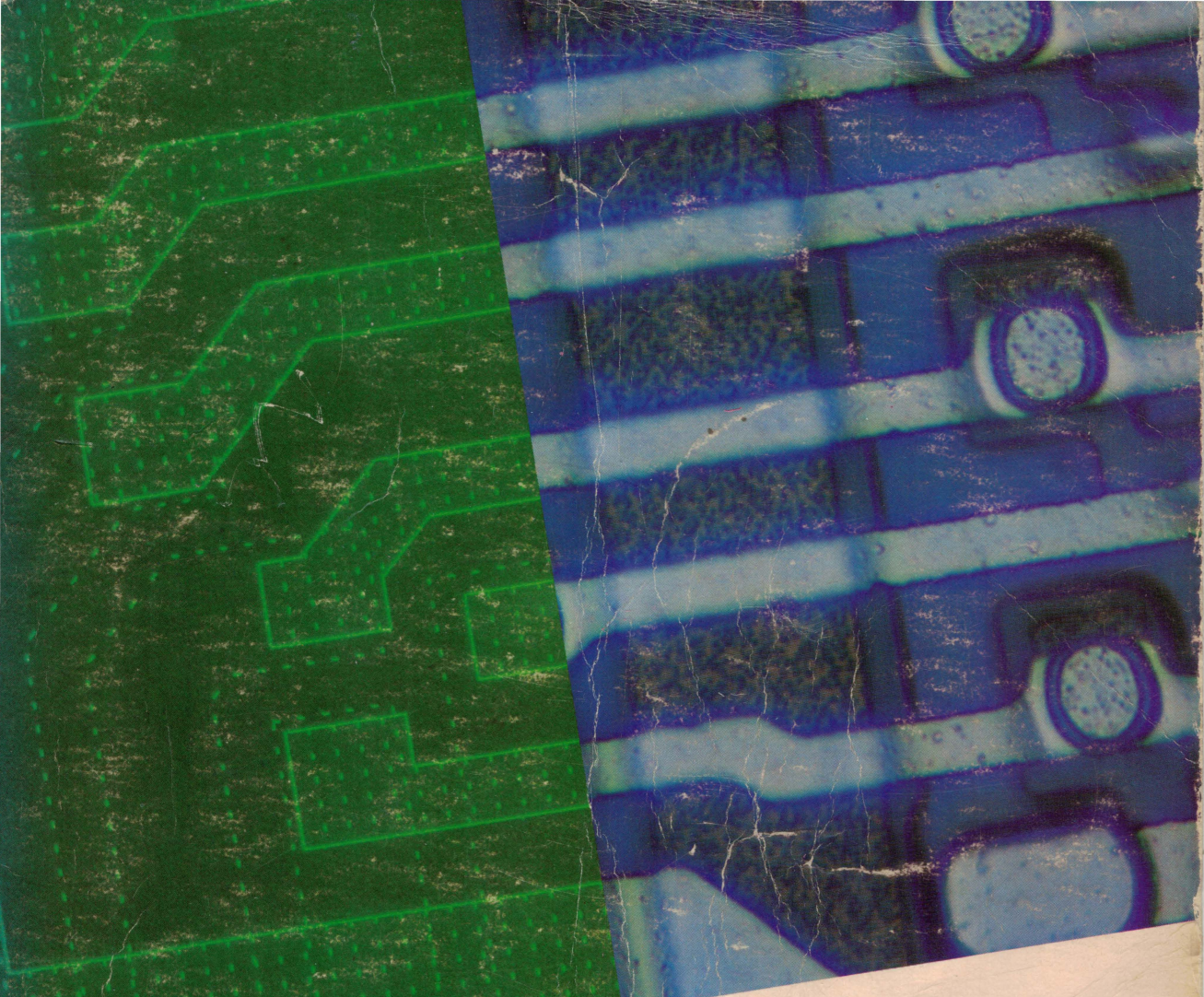

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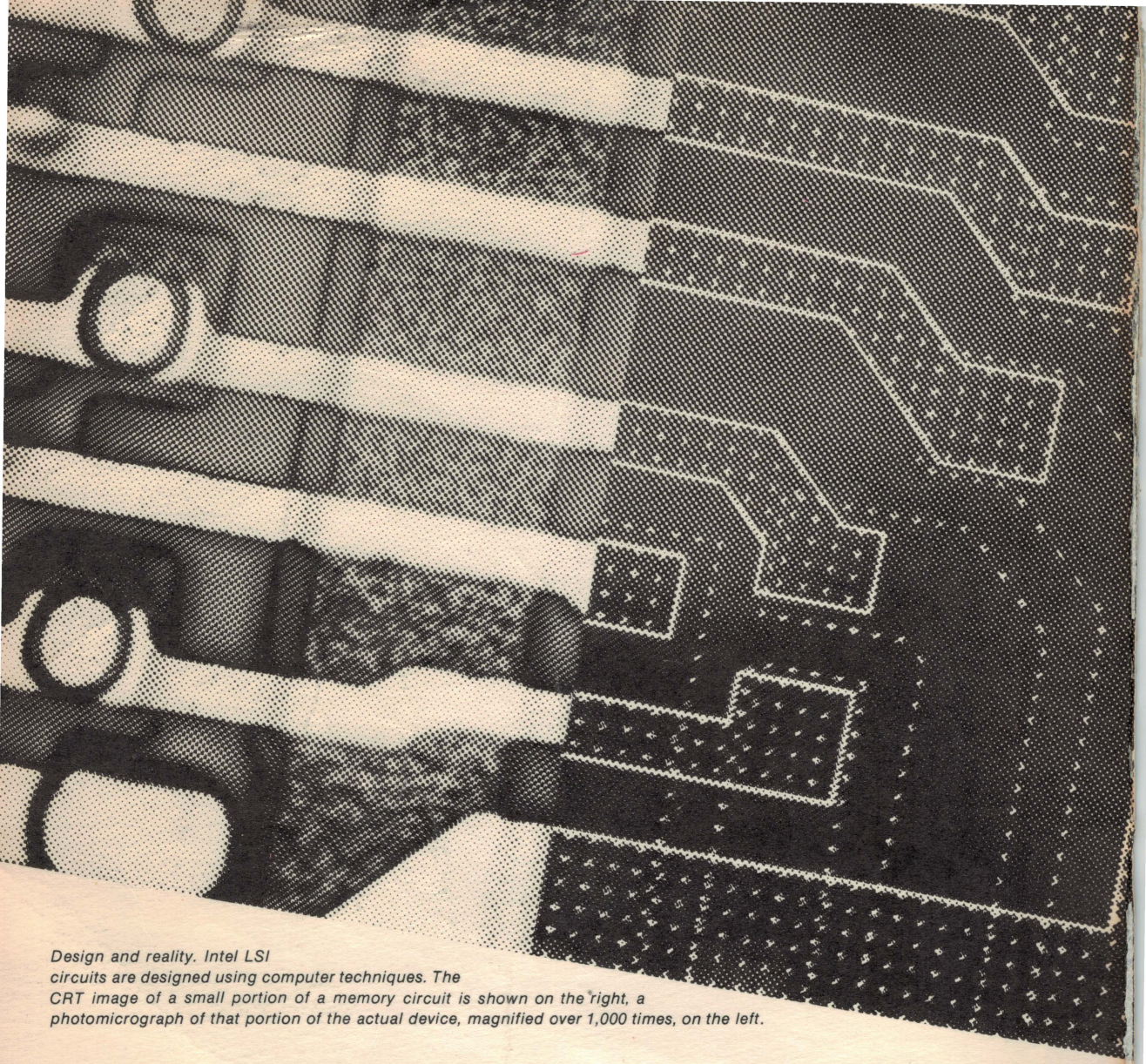

Design and reality. Intel LSI circuits are designed using computer techniques. The CRT image of a small portion of a memory circuit is shown on the right, a photomicrograph of that portion of the actual device, magnified over 1,000 times, on the left.

Intel was organized in 1968 to utilize the rapidly expanding technology of Integrated Electronics. During its brief history, Intel has become the world's largest supplier of MOS circuits, and is in the top ten of the world's producers of all semiconductor devices.

This Component Data Catalog provides complete specifications on most of Intel standard memory, microprocessor, peripheral and telecommunication components. Margin tabs provide quick guides to major product categories; indexes located in Section 1 and at the beginning of each section allow location of specific circuit types. Ordering, packaging, and product flow information may be found in Section 2.

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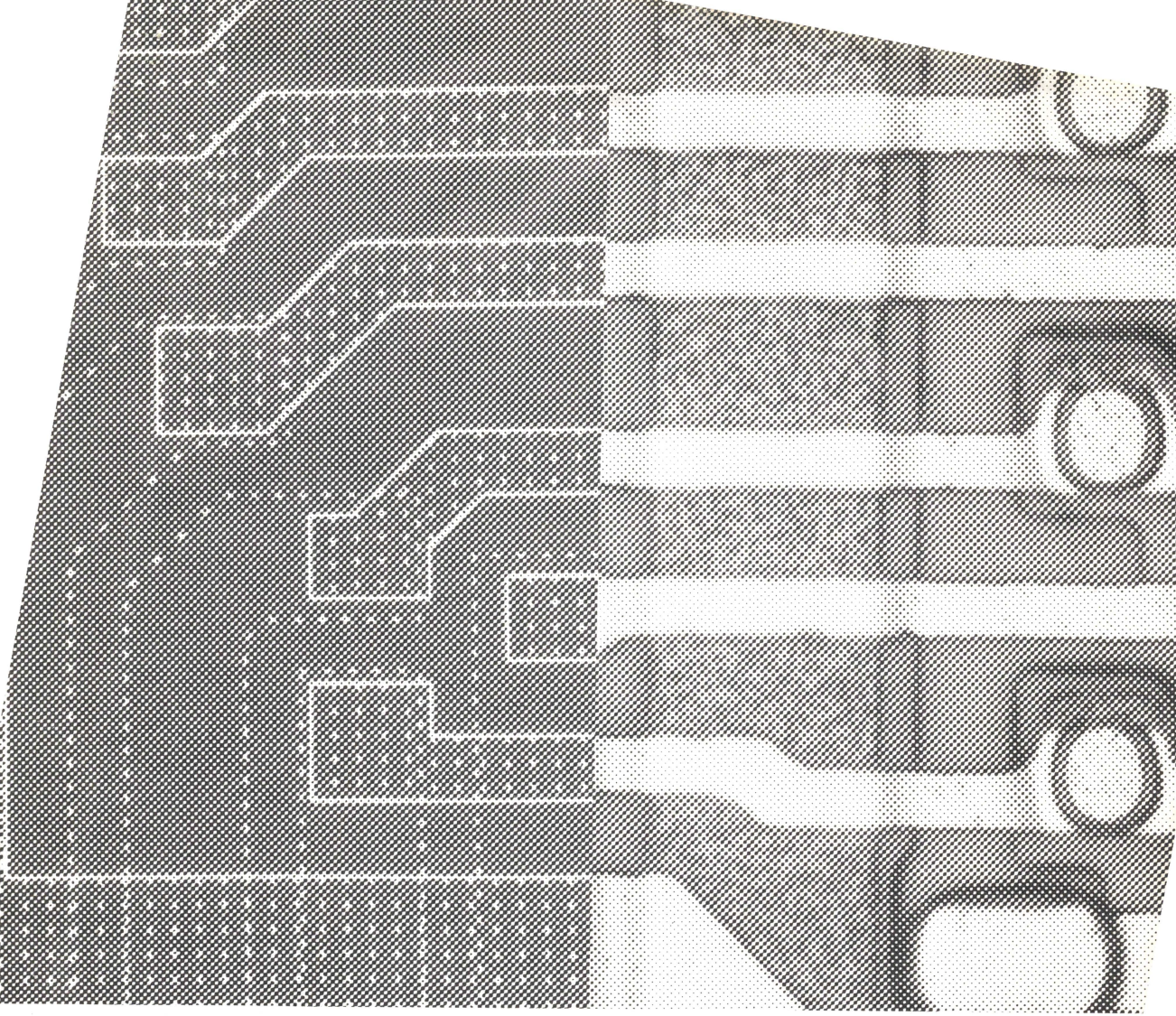

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*For specifications contact Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

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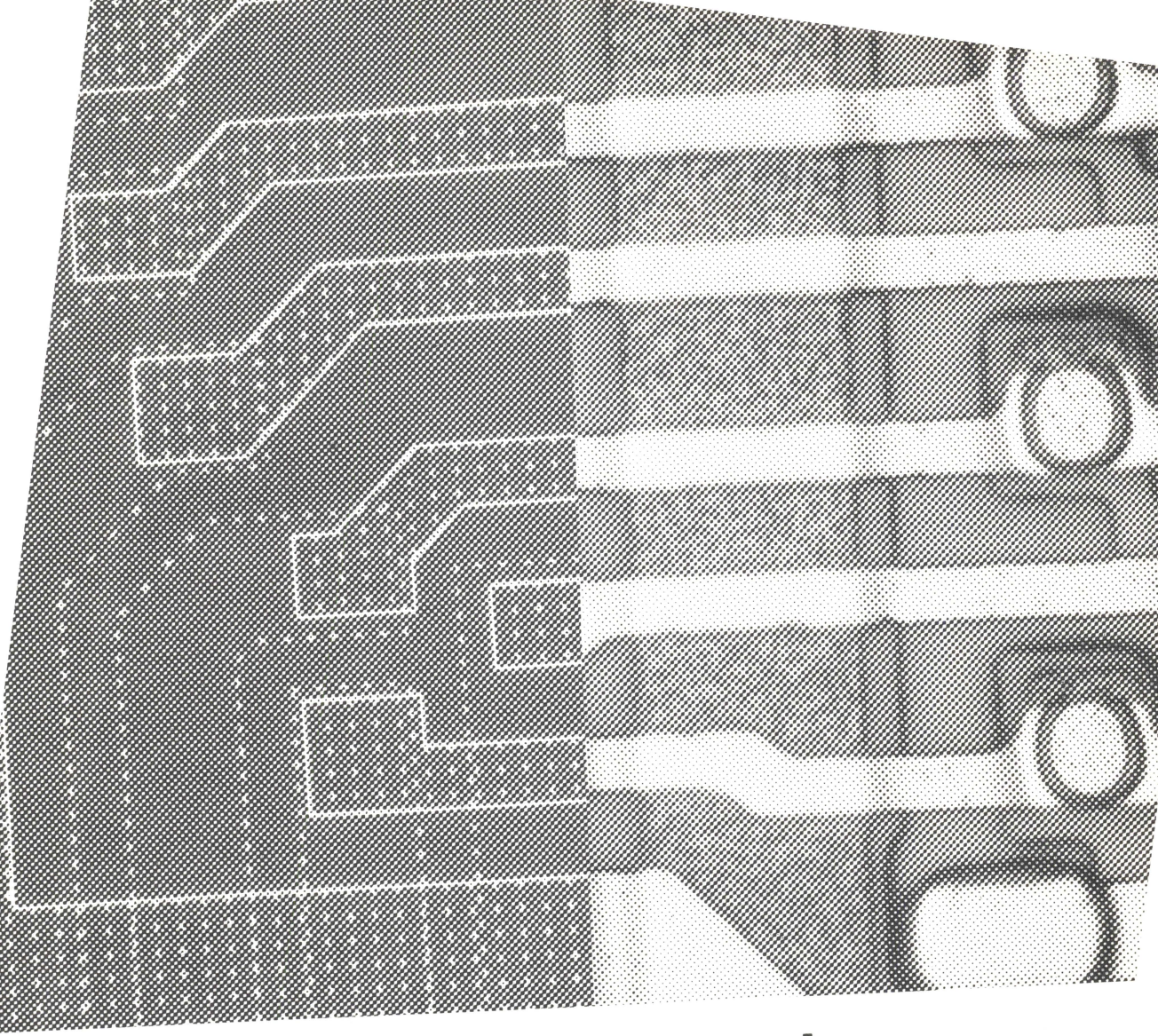

2 General Information

GENERAL INFORMATION

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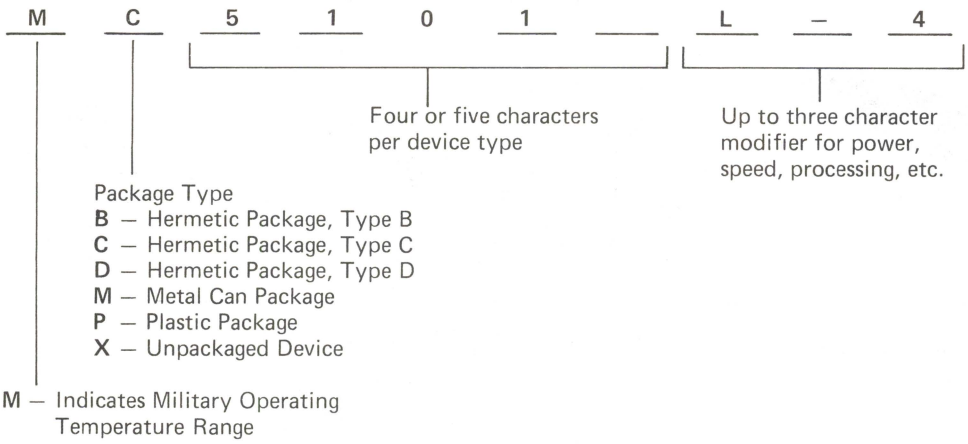
Semiconductor components are identified as follows:

Example:



Examples:

P5101L CMOS 256 X 4 RAM, low power selection, plastic package, commercial temperature range.

C8080A2 8080A Microprocessor with 1.5 μs cycle time, hermetic package Type C, commercial temperature range.

MD3604/C 512 X 8 PROM, hermetic package Type D, military temperature range, MIL-STD-883 Level C processing.*

MC8080A/B 8080A Microprocessor, hermetic package Type C, military temperature range, MIL-STD-883 Level B processing.*

Kits, boards and systems may be ordered using the part number designations in this catalog.

The latest Intel OEM price book should be consulted for availability of various options. These may be obtained from your local Intel representative or by writing directly to Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051.

**On military temperature devices, B suffix indicates MIL-STD-883 Level B processing. Suffix C indicates MIL-STD-883 Level C processing. "S" number suffixes must be specified when entering any order for military temperature devices. All orders requesting source inspection will be rejected by Intel.*

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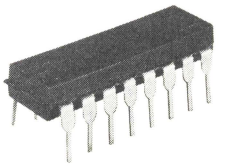

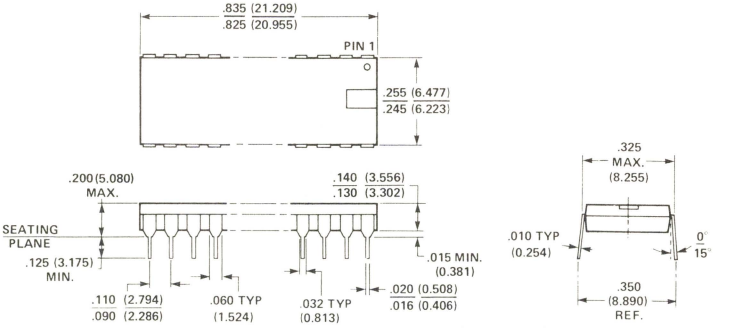

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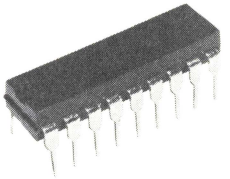

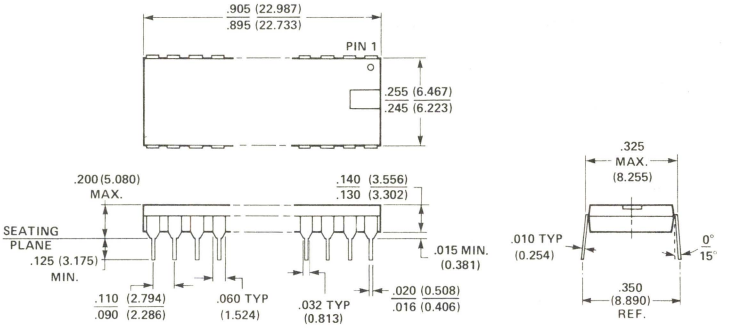

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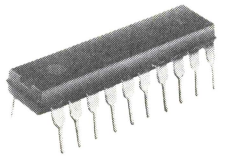

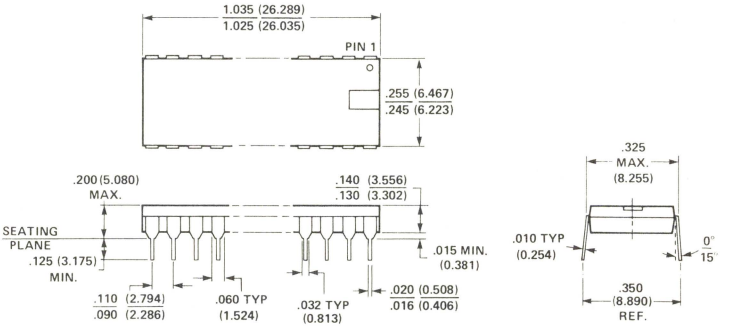

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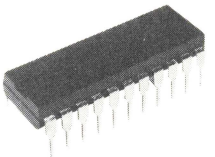

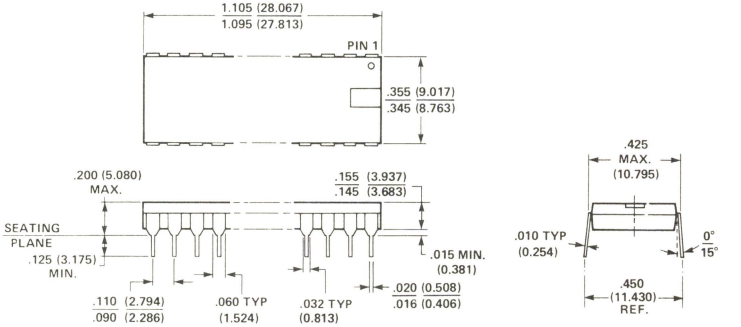

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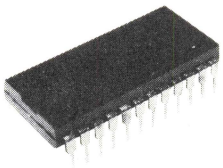

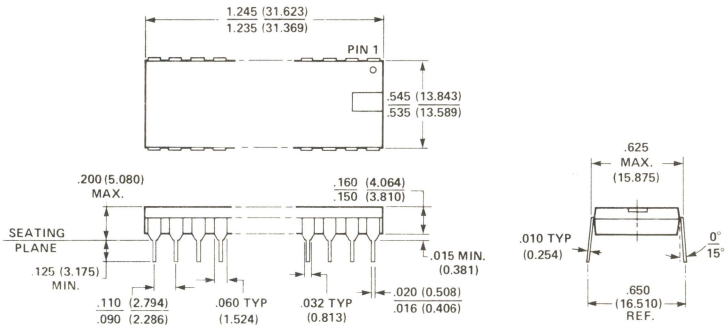

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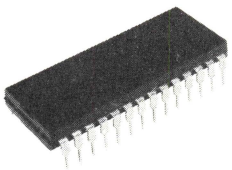

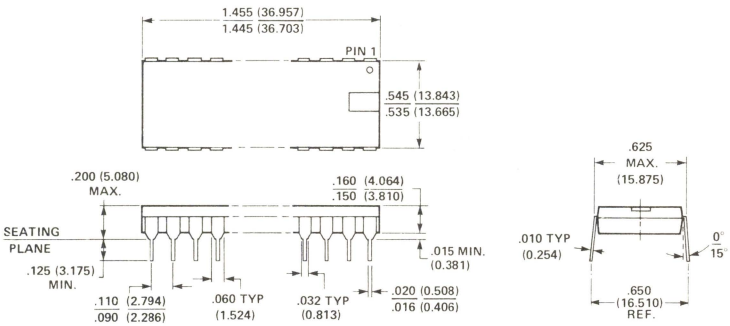

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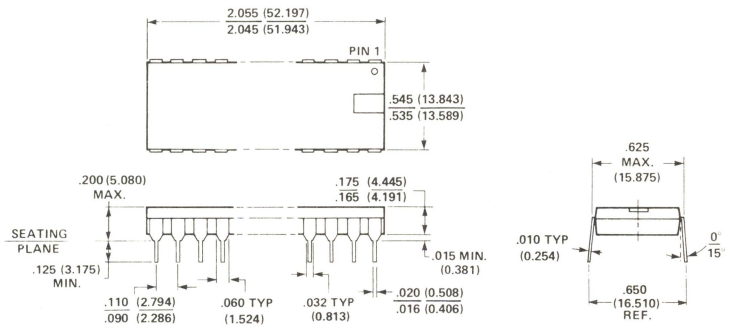

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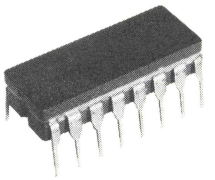

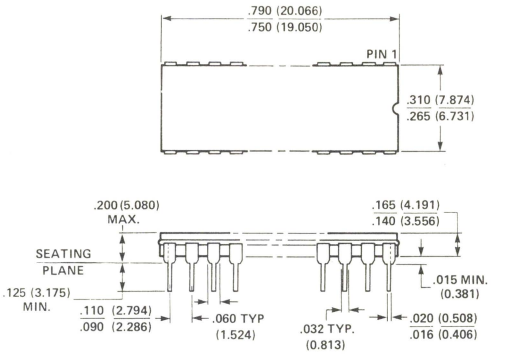

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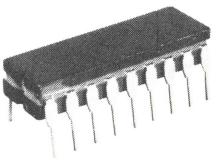

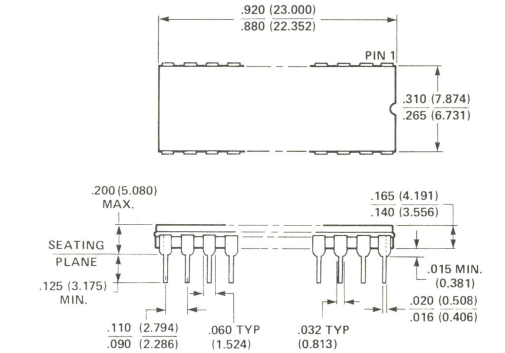

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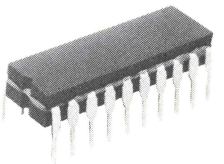

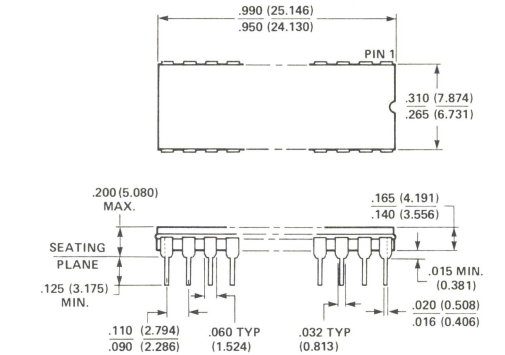

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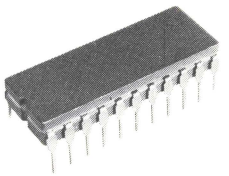

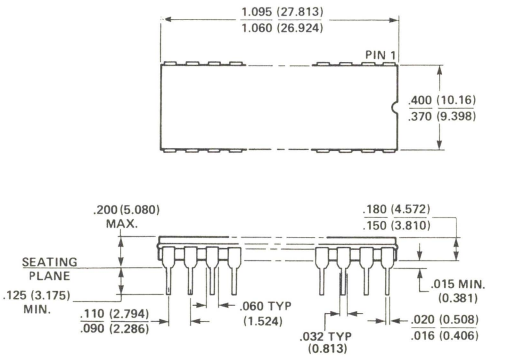

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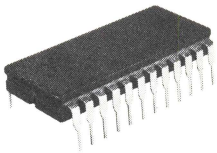

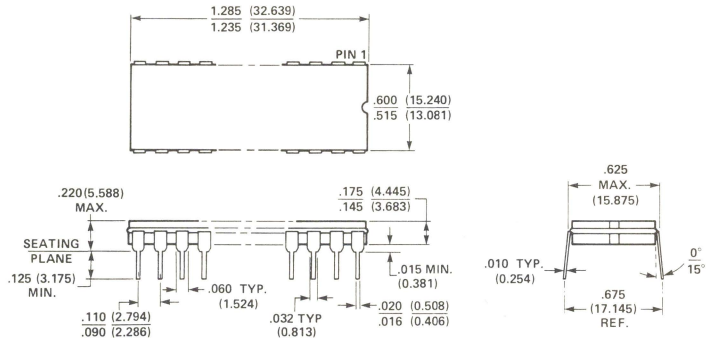

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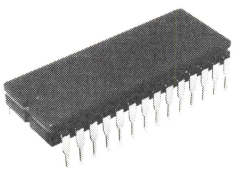

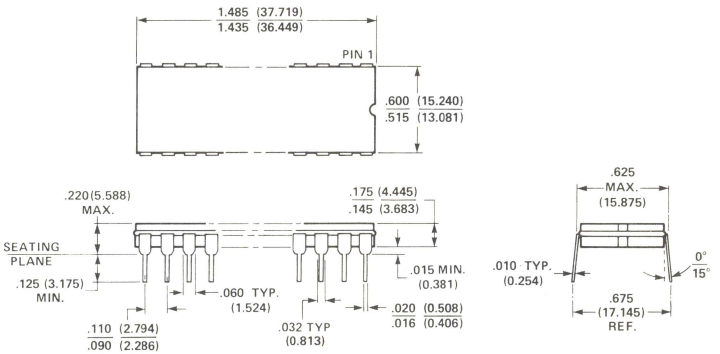

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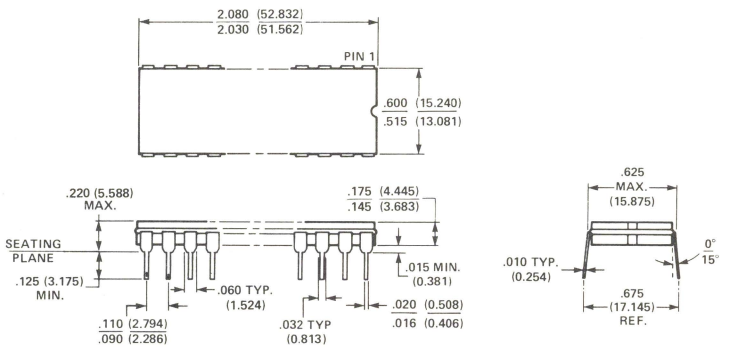

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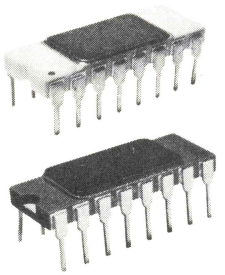

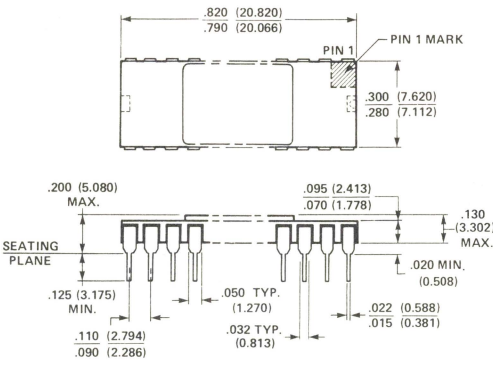

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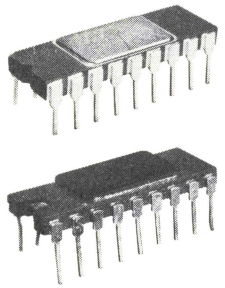

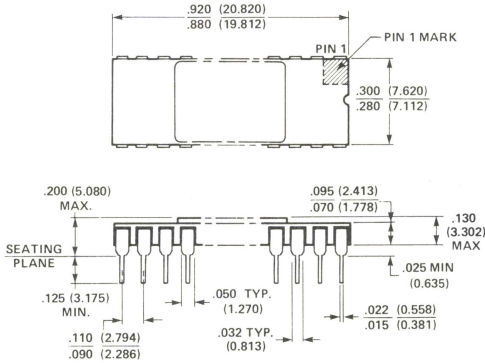

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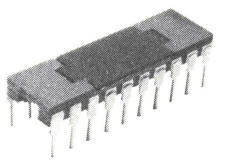

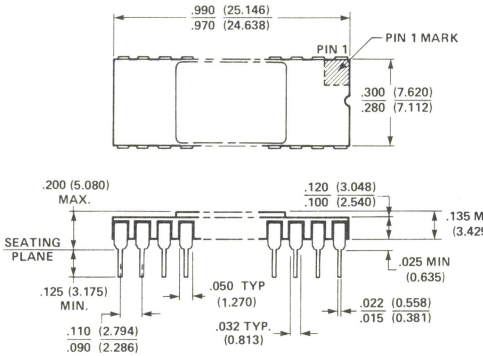

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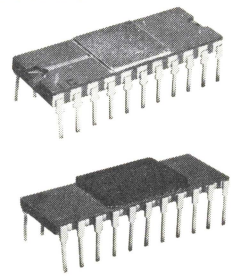

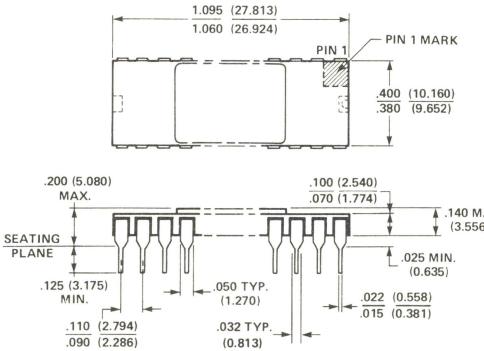

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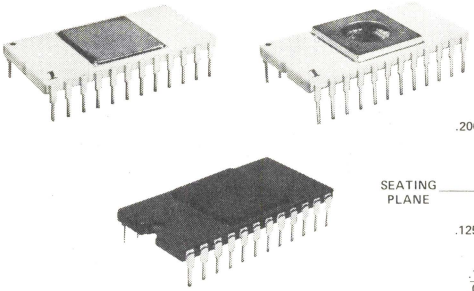

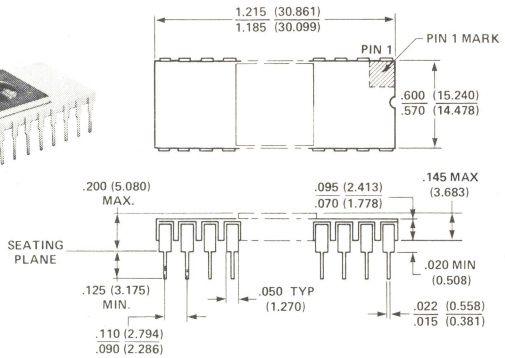

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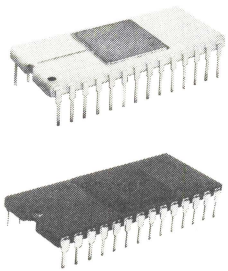

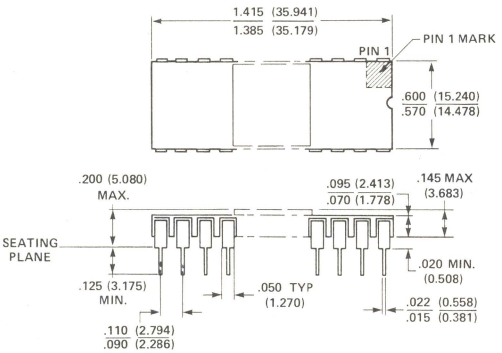

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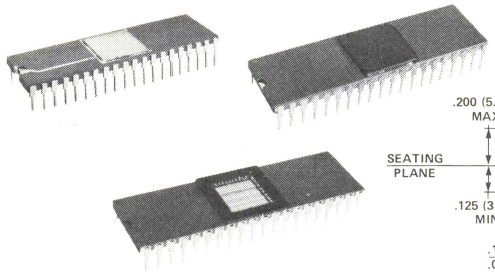

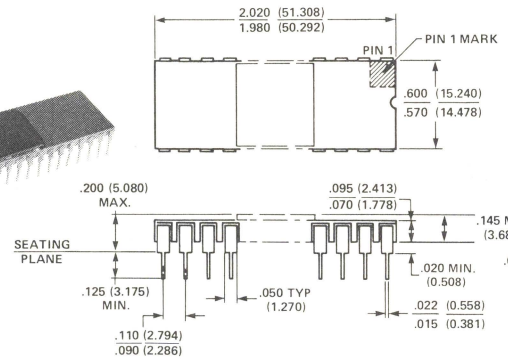

CERAMIC DUAL IN-LINE PACKAGE TYPE B

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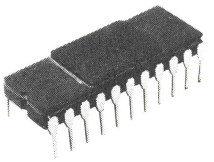

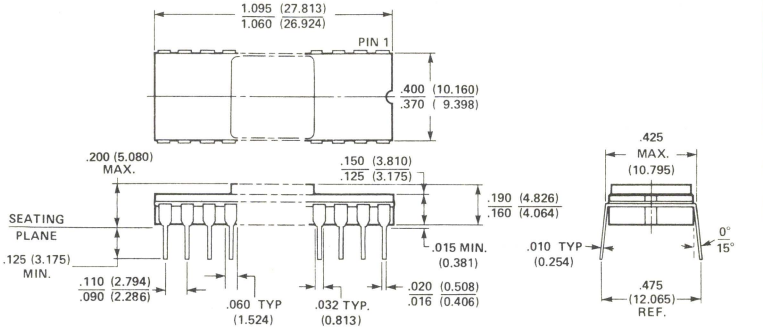

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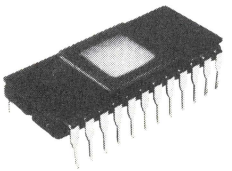

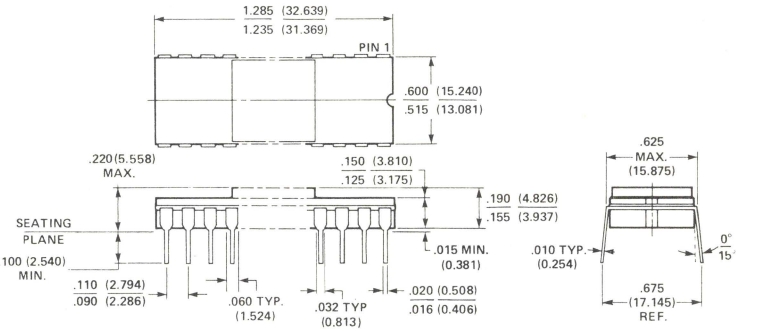

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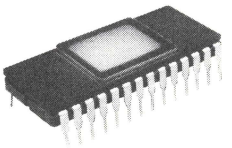

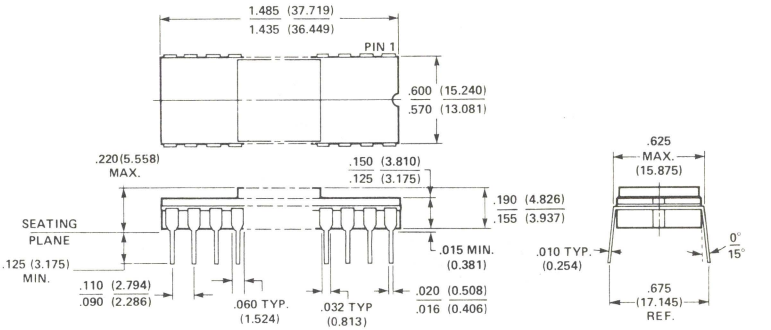

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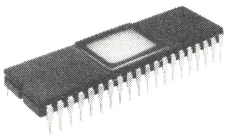
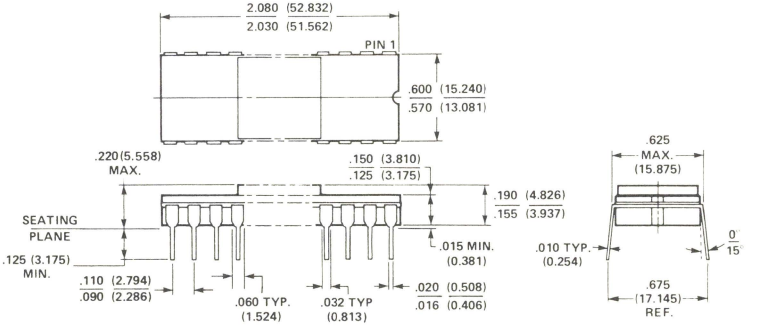
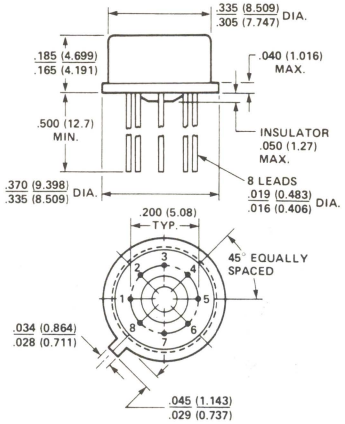


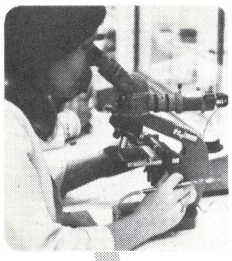


METAL CAN PACKAGE TYPE M

8-LEAD METAL CAN
PACKAGE TYPE M

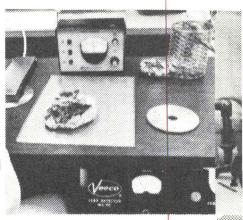


STANDARD PRODUCT FLOW



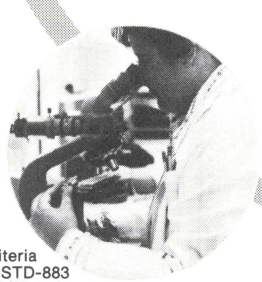
Optical inspection criteria based on MIL-STD-883 Method 2010.3B to insure that all devices are free from internal defects which could lead to failure in normal applications. (Monitored by QA)

Hermeticity Testing to eliminate devices which show insufficient hermeticity. (Monitored by QA)
Fine leak C DIPs,CERDIPs,and Metal cans (MIL-STD-883 Method 1014.2B).* **Gross Leak** C DIPs and Cerdips only (Method 1014.2C, vacuum omitted and 1 hour pressurization).



Die Attach
(Monitored by QA)

Lead Bonding (Monitored by QA per MIL-STD-883 Method 2011.2 Test Condition D.)

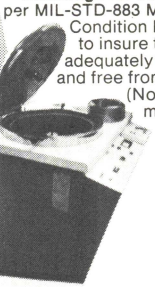


Precap Visual Inspection criteria based on MIL-STD-883 Method 2010.3B to insure that after assembly all devices are free from defects which could lead to failure in normal applications. (Each lot must pass a QA acceptance.)

Temperature Cycling per MIL-STD-883 Method 1010.2 Test Condition C (10 Cycles: −65°C to +150°C) to insure that all devices are free from metalization, bonding or packaging defects. (Monitored by QA)

***Fine leak limits:** All devices 1 x 10-7 cc•atm/sec

Ceramic DIP and Cerdip Centrifuge for constant acceleration per MIL-STD-883 Method 2001.2 Test Condition E (30,000G Y1 plane) to insure that all devices are adequately die attached, bonded and free from package defects. (Not 100% screened; monitored by QA)



Plastic Deflash, trim and form leads. (Monitored by QA)

Electrical Testing to test conditions and limits which guarantee AC, DC and functional performance over full specified temperature range.

Final QA Acceptance per MIL-STD-883 Method 2009 External Visual, and Electrical AC, DC Functional Tests to guarantee performance over full specified temperature range
Electrical 1% AQL
Mech/Vis. 7/2 LTPD

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SBC 80 and System 80 Configuration Guide	N/C
μ Scope™ 820 Brochure	N/C
PL/M Application Brochure	N/C
ICE-85™ Brochure	N/C
Microcomputer Product Line Brochure	N/C
Static RAM Brochure	N/C
2115A/2125A Brochure	N/C
Intellec® Series II Development Systems	N/C

REFERENCE CARDS

MCS-48™ Assembly Language Reference Card	N/C
UPI-41™ Assembly Language Reference Card	N/C
8085/8080 Assembly Language Reference Card	N/C

RELIABILITY REPORTS

RR 7	2107A/2107B 4K Dynamic RAM	N/C
RR 8	Polysilicon Fuse Bipolar PROM	N/C
RR 9	MOS Static RAMs	N/C
RR 10	8080/8080A Microcomputer	N/C
RR 11	2416 16K CCD Memory	N/C
RR 12	2708 8K Erasable PROM	N/C
RR 14	2115/2125 MOS Static RAMs	N/C
RR 15	2104A 4K Dynamic RAM	N/C
RR 16	2116 16K Dynamic RAM	N/C
RR 17	SBC 80/10 Single Board Computer	N/C

APPLICATION NOTES

AP 12	5101 CMOS RAM	N/C
AP 15	8255 Programmable Peripheral Interface	N/C
AP 16	8251 USART	N/C
AP 17	2708 8K Erasable PROM	N/C
AP 19	Memory Mapped PROM	N/C
AP 23	2104A 4K RAM	N/C
AP 24	MCS-48™ Family	N/C
AP 26	SBC 80/10 System 80/10	N/C
AP 27	Control with UPI-41™	N/C
AP 28	Multibus Interfacing	N/C
AP 29	Using the Intel® 8085 Serial I/O Lines	N/C
AP 31	Using the 8259	N/C
AP 32	8275 and 8279	N/C
AP 33	RMX-80™	N/C
APR 1	Simplify Dynamic RAM/Microprocessor Interface	N/C

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Middlesex
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**Note New Telephone Number

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TWX: 910-338-0255

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Tel: (415) 843-7625

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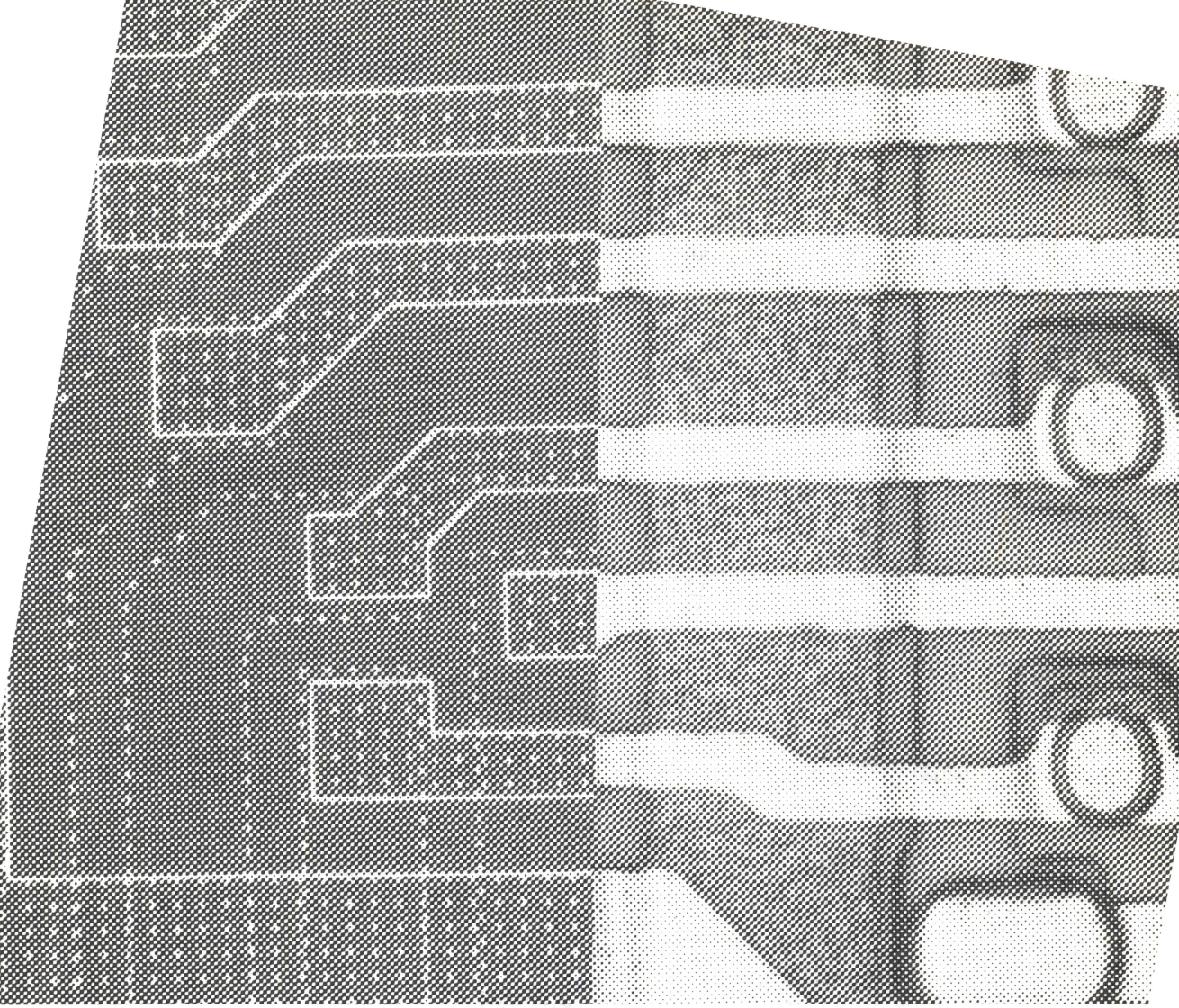
**Note New Telephone Number

***Field Application Location**



3 Random Access Memory

RANDOM ACCESS MEMORIES

SILICON GATE MOS

Type	No. of Bits	Description	Organization	No. of Pins	Electrical Characteristics Over Temperature				Page No.
					Access Time Max. (ns)	Cycle Time Min. (ns)	Power Dissipation Max.[1] Operating/ Standby (mW)	Supplies (V)	
DYNAMIC RAMS									
1103	1024	Dynamic Fully Decoded	1024x1	18	300	580	400/64	+16, +19	3-4
1103-1	1024	Dynamic Full Decoded	1024x1	18	150	340	437/76	+19, +22	
1103A	1024	Dynamic Fully Decoded	1024x1	18	205	580	400/64	+16, +19	
1003A-1	1024	Dynamic Fully Decoded	1024x1	18	145	340	627/10	+19, +22	
1103A-2	1024	Dynamic Fully Decoded	1024x1	18	145	400	570/10	+19, +22	
2104A	4096	16-Pin Dynamic	4096x1	16	350	350	441/25	+12, +5, -5	3-36
2104A-1	4096	16-Pin Dynamic	4096x1	16	150	320	462/26	+12, +5, -5	
2104A-2	4096	16-Pin Dynamic	4096x1	16	200	320	422/26	+12, +5, -5	
2104A-3	4096	16-Pin Dynamic	4096x1	16	250	375	396/26	+12, +5, -5	
2104A-4	4096	16-Pin Dynamic	4096x1	16	300	425	396/26	+12, +5, -5	
(S)2104A-1	4096	16-Pin Dynamic	4096x1	16	150	320	462/26	+12, +5, -5	
2104A-2	4096	16-Pin Dynamic	4096x1	16	200	375	422/26	+12, +5, -5	
2104A-3	4096	16-Pin Dynamic	4096x1	16	250	375	396/26	+12, +5, -5	
2104A-4	4096	16-Pin Dynamic	4096x1	16	300	425	396/26	+12, +5, -5	
2107C	4096	22-Pin Dynamic	4096x1	22	250	430	396/2.6	+12, +5, -5	3-60
2107C-1	4096	22-Pin Dynamic	4096x1	22	150	380	462/2.6	+12, +5, -5	
2107C-2	4096	22-Pin Dynamic	4096x1	22	200	400	436/2.6	+12, +5, -5	
2107C-4	4096	22-Pin Dynamic	4096x1	22	300	470	396/2.6	+12, +5, -5	
2108-2	8192	16-Pin Dynamic	8192x1	16	200	350	828/24	+12, +5, -5	3-65
2108-4	8192	16-Pin Dynamic	8192x1	16	300	425	780/24	+12, +5, -5	
2109-3	8192	16-Pin Dynamic	8192x1	16	200	375	462/20	+12, +5, -5	3-73
2109-4	8192	16-Pin Dynamic	8192x1	16	250	410	436/20	+12, +5, -5	
2116-2	16,384	16-Pin Dynamic	16,384x1	16	200	350	828/24	+12, +5, -5	3-109
2116-3	16,384	16-Pin Dynamic	16,384x1	16	250	375	816/24	+12, +5, -5	
2116-4	16,384	16-Pin Dynamic	16,384x1	16	300	425	780/24	+12, +5, -5	
2117-2	16,384	16-Pin Dynamic	16,384x1	16	150	320	462/20	+12, +5, -5	3-117
2117-3	16,384	16-Pin Dynamic	16,384x1	16	200	375	462/20	+12, +5, -5	
2117-4	16,384	16-Pin Dynamic	16,384x1	16	250	410	436/20	+12, +5, -5	
STATIC RAMS									
2101A/8101A-4	1024	Static, Separate I/O	256x4	22	350	350	300	+5	3-26
2101A-2	1024	Static, Separate I/O	256x4	22	250	250	350	+5	
2101A-4	1024	Static, Separate I/O	256x4	22	450	450	300	+5	
2102A/8102A-4	1024	Static	1024x1	16	350	350	275	+5	3-30
2102A-2	1024	Static	1024x1	16	250	250	325	+5	
2102A-4	1024	Static	1024x1	16	450	450	275	+5	
2102AL	1024	Low Standby Power Static	1024x1	16	350	350	165/35	+5	
2102AL-2	1024	Low Standby Power Static	1024x1	16	250	250	325/42	+5	
2102AL-4	1024	Low Standby Power Static	1024x1	16	450	450	165/35	+5	
M2102A-4	1024	Static, T_A = 55°C to +125°C	1024x1	16	450	450	350	+5	3-34
2111A/8111A-4	1024	Static, Common I/O with Output Deselect	256x4	18	350	350	300	+5	3-85
2111A-2	1024	Static, Common I/O	256x4	18	250	250	350	+5	
2111A-4	1024	Static, Common I/O	256x4	18	450	450	300	+5	

RANDOM ACCESS MEMORIES (Continued)

	Type	No. of Bits	Description	Organization	No. of Pins	Electrical Characteristics Over Temperature: Access Time Max. (ns)	Cycle Time Min. (ns)	Power Dissipation Max.[1] Operating/ Standby (mW)	Supplies (V)	Page No.
	STATIC RAMS (Continued)									
	2112A	1024	Static, Common I/O without Output Deselect	256x4	16	350	350	300	+5	3-89
	2112A-2	1024	Static, Common I/O without Output Deselect	256x4	16	250	250	350	+5	
	2112A-4	1024	Static, Common I/O without Output Deselect	256x4	16	450	450	300	+5	
	2114	4096	Static, Common I/O	1024x4	18	450	450	525	+5	3-94
	2114-2	4096	Static, Common I/O	1024x4	18	200	200	525	+5	
	2114-3	4096	Static, Common I/O	1024x4	18	300	300	525	+5	
	2114L	4096	Static, Common I/O	1024x4	18	450	450	370	+5	
	2114L2	4096	Static, Common I/O	1024x4	18	200	200	370	+5	
	2114L3	4096	Static, Common I/O	1024x4	18	300	300	370	+5	
	M2114	4096	Static, Common I/O T_A = 55°C to +125°C	1024x4	18	450	450	550	+5	3-98
	2115A, 2125A	1024	Static, Open Connector	1024x1	16	45	45	370	+5	3-99
	2115A-2, 2125A-2	1024	Static, Open Connector	1024x1	16	70	70	370	+5	
	2115AL, 2125AL	1024	Static, Open Connector	1024x1	16	45	45	240	+5	
	2115AL-2, 2125AL-2	1024	Static, Open Connector	1024x1	16	70	70	240	+5	
	M2115A, M2125A	1024	Static, Three State	1024x1	16	55	55	690	+5	3-104
	M2115AL, M2125AL	1024	Static, Three State	1024x1	16	75	75	415	+5	3-104
	2141-2	4096	Low Power Static	4096x1	18	120	120	385/110	+5	3-129
	2141-3	4096	Low Power Static	4096x1	18	150	150	385/110	+5	
	2141-4	4096	Low Power Static	4096x1	18	200	200	305/66	+5	
	2141-5	4096	Low Power Static	4096x1	18	250	250	305/66	+5	
	2141L-3	4096	Low Power Static	4096x1	18	150	150	220/28	+5	
	2141L-4	4096	Low Power Static	4096x1	18	200	200	220/28	+5	
	2141L-5	4096	Low Power Static	4096x1	18	250	250	220/28	+5	
	2142	4096	Static, with Output Enable	1024x1	20	450	450	525	+5	3-133
	2142-2	4096	Static, with Output Enable	1024x1	20	200	200	525	+5	
	2142-3	4096	Static, with Output Enable	1024x1	20	300	300	525	+5	
	2142L	4096	Static, with Output Enable	1024x1	20	450	450	375	+5	
	2142L-2	4096	Static, with Output Enable	1024x1	20	200	200	375	+5	
	2142L-3	4096	Static, with Output Enable	1024x1	20	300	300	375	+5	
	M2142	4096	Static, with Output Enable	1024x1	20	450	450	550	+5	3-137
	2147	4096	High Speed Static	4096x1	18	70	70	840/105	+5	3-138
	2147-3	4096	High Speed Static	4096x1	18	55	55	945/160	+5	
	2147L	4096	High Speed Static	4096x1	18	70	70	735/53	+5	
SCHOTTKY BIPOLAR	**3101**	64	Fully Decoded	16x4	16	60	60	525	+5	3-145
	3101A	64	High Speed Fully Decoded	16x4	16	35	35	525	+5	
	3104	16	Content Addressable Memory	4x4	24	30	40	625	+5	3-149
SILICON GATE CMOS	**5101**	1024	Static CMOS RAM	256x4	22	800	800	150/2.5	+5	3-153
	5101L	1024	Static CMOS RAM	256x4	22	650	650	135/20μW	+5	
	5101L-1	1024	Static CMOS RAM	256x4	22	450	450	135/20μW	+5	
	5101L-3	1024	Static CMOS RAM	256x4	22	650	650	135/1	+5	
	M5101-4	1024	Static CMOS RAM (-55°C to 125°C)	256x4	22	800	800	168/1	+5	3-157
	M5101L-4	1024	Static CMOS RAM (-55°C to 125°C)	256x4	22	800	800	168/400μW	+5	

1103
1024 x 1 BIT DYNAMIC RAM

- **Low Power Dissipation — Dissipates Power Primarily on Selected Chips**
- **Access Time — 300 nsec**
- **Cycle Time — 580 nsec**
- **Refresh Period... 2 milliseconds for 0—70° C Ambient**
- **OR-Tie Capability**
- **Simple Memory Expansion — Chip Enable Input Lead**
- **Fully Decoded—on Chip Address Decode**
- **Inputs Protected—All Inputs Have Protection Against Static Charge**
- **Ceramic and Plastic Package -- 18 Pin Dual In-Line Configuration.**

The Intel 1103 is designed primarily for main memory applications where high performance, low cost, and large bit storage are important design objectives.

It is a 1024 word by 1 bit random access memory element using normally off *P*-channel MOS devices integrated on a monolithic array. It is fully decoded, permitting the use of an 18 pin dual in-line package. It uses dynamic circuitry and primarily dissipates power only during precharge.

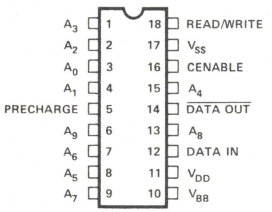
Information stored in the memory is non-destructively read. Refreshing of all 1024 bits is accomplished in 32 read cycles and is required every two milliseconds.

A separate **cenable** (chip enable) lead allows easy selection of an individual package when outputs are OR-tied.

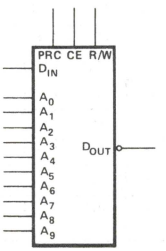
The Intel 1103 is fabricated with **silicon gate technology.** This **low threshold** technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost plastic packaging.

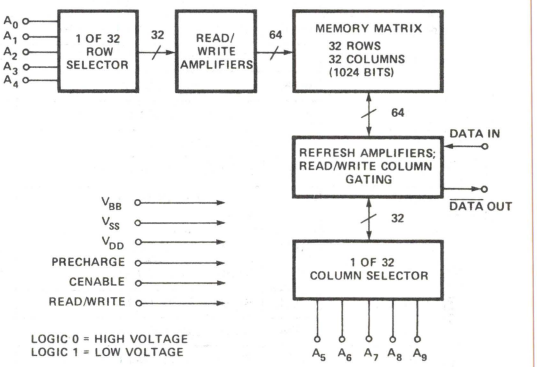
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

D_{IN}	DATA INPUT	PRC	PRECHARGE INPUT
A_0–A_9	ADDRESS INPUTS	CE	CHIP ENABLE
R/W	READ/WRITE	D_{OUT}	DATA OUTPUT

Maximum Guaranteed Ratings*

Temperature Under Bias	0°C to 70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to the Most Positive Supply Voltage, V_{BB}	−25V to 0.3V
Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB}	−25V to 0.3V
Power Dissipation	1.0 W

*COMMENT:

Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

T_A = 0°C to +70°C, $V_{SS}^{(1)}$ = 16V ± 5%, $(V_{BB} - V_{SS})^{(6)}$ = 3V to 4V, V_{DD} = 0V unless otherwise specified

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LI}	**INPUT LOAD CURRENT** (ALL INPUT PINS)			1	μA	V_{IN} = 0V
I_{LO}	OUTPUT LEAKAGE CURRENT			1	μA	V_{OUT} = 0V
I_{BB}	**V_{BB} SUPPLY CURRENT**			100	μA	
$I_{DD1}^{(2)}$	SUPPLY CURRENT DURING T_{PC}		37	56	mA	ALL ADDRESSES = 0V PRECHARGE = 0V CENABLE = V_{SS}; T_A = 25°C
$I_{DD2}^{(2)}$	SUPPLY CURRENT DURING T_{OV}		38	59	mA	ALL ADDRESSES = 0V PRECHARGE = 0V CENABLE = 0V; T_A = 25°C
$I_{DD3}^{(2)}$	SUPPLY CURRENT DURING T_{POV}		5.5	11	mA	PRECHARGE = V_{SS} CENABLE = 0V; T_A = 25°C
$I_{DD4}^{(2)}$	SUPPLY CURRENT DURING T_{CP}		3	4	mA	PRECHARGE = V_{SS} CENABLE = V_{SS}; T_A = 25°C
$I_{DDAV}^{(5)}$	**AVERAGE SUPPLY CURRENT**		**17**	**25**	**mA**	**CYCLE TIME = 580 ns; PRECHARGE WIDTH = 190 ns; T_A = 25°C**
$V_{IL1}^{(7)}$	INPUT LOW VOLTAGE (ALL ADDRESS & DATA-IN LINES)	V_{SS}−17		V_{SS}−14.2	V	T_A = 0°C
$V_{IL2}^{(7)}$	INPUT LOW VOLTAGE (ALL ADDRESS & DATA-IN LINES)	V_{SS}−17		V_{SS}−14.5	V	T_A = 70°C
$V_{IL3}^{(7,8)}$	INPUT LOW VOLTAGE (PRECHARGE CENABLE & READ/WRITE INPUTS)	V_{SS}−17		V_{SS}−14.7	V	T_A = 0°C
$V_{IL4}^{(7,8)}$	INPUT LOW VOLTAGE (PRECHARGE CENABLE& READ/WRITE INPUTS)	V_{SS}−17		V_{SS}−15.0	V	T_A = 70°C
$V_{IH1}^{(7)}$	INPUT HIGH VOLTAGE (ALL INPUTS)	V_{SS}−1		V_{SS}+1	V	T_A = 0°C
$V_{IH2}^{(7)}$	INPUT HIGH VOLTAGE (ALL INPUTS)	V_{SS}−0.7		V_{SS}+1	V	T_A = 70°C
I_{OH1}	**OUTPUT HIGH CURRENT**	**600**	**900**	**4000**	μA	T_A = 25°C
I_{OH2}	**OUTPUT HIGH CURRENT**	**500**	**800**	**4000**	μA	T_A = 70°C
I_{OL}	OUTPUT LOW CURRENT	See Note 3				R_{LOAD} = 100 Ω (4)
V_{OH1}	OUTPUT HIGH VOLTAGE	60	90	400	mV	T_A = 25°C,
V_{OH2}	OUTPUT HIGH VOLTAGE	50	80	400	mV	T_A = 70°C,
V_{OL}	OUTPUT LOW VOLTAGE	See Note 3				

Note 1: The V_{SS} current drain is equal to $(I_{DD} + I_{OH})$ or $(I_{DD} + I_{OL})$.

Note 2: See Supply Current vs. Temperature (p. 3) for guaranteed current at the temperature extremes. These values are taken from a single pulse measurement.

Note 3: The output current when reading a low output is the leakage current of the 1103 plus external noise coupled into the output line from the clocks. V_{OL} equals I_{OL} across the load resistor.

Note 4: This value of load resistance is used for measurement purposes. In applications the resistance may range from 100 Ω to 1 kΩ.

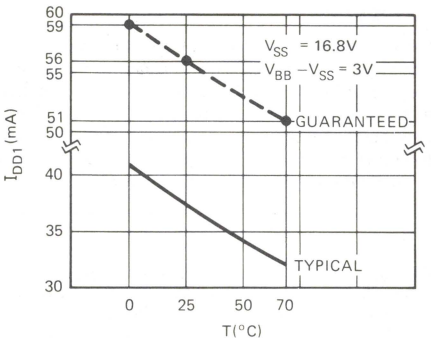
Note 5: This parameter is periodically sampled and is not 100% tested.

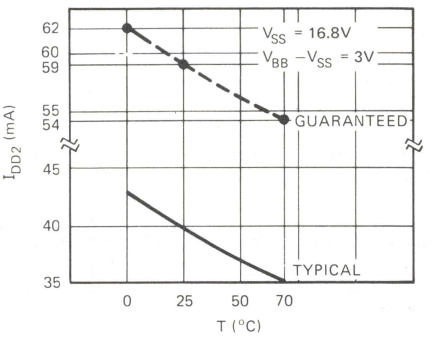
Note 6: $(V_{BB} - V_{SS})$ supply should be applied at or before V_{SS}.

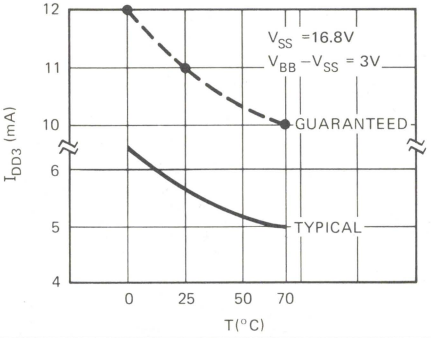
Note 7: The maximum values for V_{IL} and the minimum values for V_{IH} are linearly related to temperature between 0°C and 70°C. Thus any value in between 0°C and 70°C can be calculated by using a straight-line relationship.

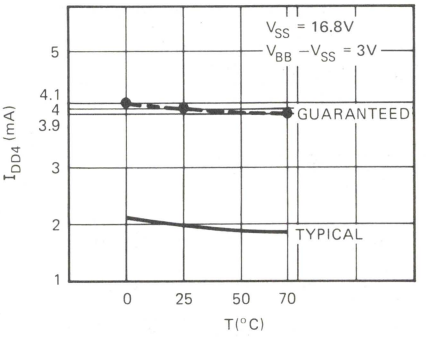
Note 8: The maximum values for V_{IL} (for precharge, cenable & read/write) may be increased to V_{SS}−14.2 @ 0°C and V_{SS}−14.5 @ 70°C (same values as those specified for the address & data-in lines) with a 40 ns degradation (worst case) in t_{AC}, t_{PC}, t_{RC}, t_{WC}, t_{RWC}, t_{ACC1} and t_{ACC2}.

Supply Current vs Temperature

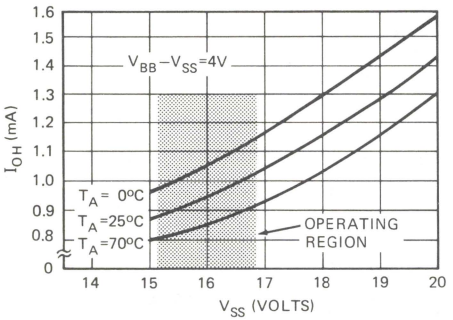


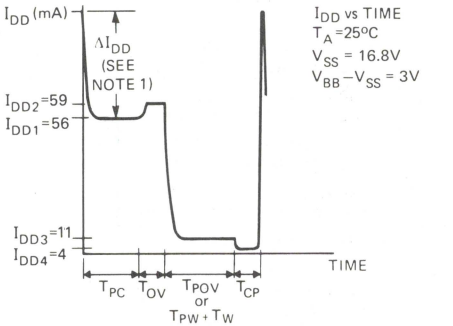






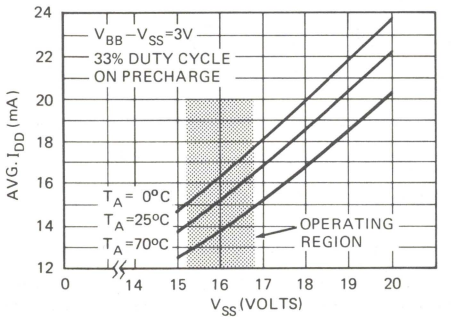
Typical Characteristics

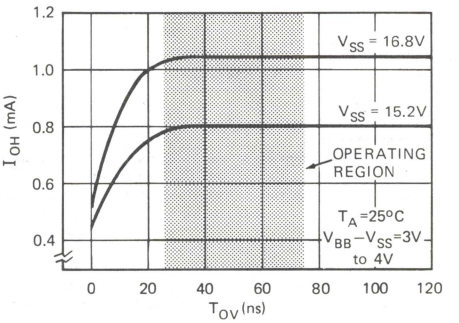




Note 1. ΔI_{DD} is due to charging of internal device node capacitance at precharge

Note 2. These values are taken from a single pulse measurement





AC Characteristics T_A = 0°C to 70°C, V_{SS} = 16 ± 5%, (V_{BB} – V_{SS}) = 3.0V to 4.0V, V_{DD} = 0V

READ, WRITE, AND READ/WRITE CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{REF}	**TIME BETWEEN REFRESH**			2	**ms**	
t_{AC} (1)	ADDRESS TO CENABLE SET UP TIME	115			ns	
t_{CA}	CENABLE TO ADDRESS HOLD TIME	20			ns	
t_{PC} (1)	PRECHARGE TO CENABLE DELAY	125			ns	
t_{CP}	CENABLE TO PRECHARGE DELAY	85			ns	
t_{OVL}	PRECHARGE & CENABLE OVERLAP, LOW	25		75	ns	t_T = 20ns
t_{OVH}	PRECHARGE & CENABLE OVERLAP, HIGH			140	ns	t_T = 20ns
t_{OVM}	PRECHARGE & CENABLE OVERLAP, 50% POINTS	45		95	ns	

READ CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{RC} (1)	**READ CYCLE**	**480**			**ns**	
t_{POV}	PRECHARGE TO END OF CENABLE	165		500	ns	
t_{PO}	END OF PRECHARGE TO OUTPUT DELAY			120	ns	
t_{ACC1} (1)	**ADDRESS TO OUTPUT ACCESS**	**300**			**ns**	$t_{ACmin} + t_{OVLmin} + t_{POmax} + 2\,t_T$; t_T = **20 ns**, C_{LOAD} = 100 pF, R_{LOAD} = 100Ω, V_{REF} = 40 mV
t_{ACC2} (1)	**PRECHARGE TO OUTPUT ACCESS**	**310**			**ns**	$t_{PCmin} + t_{OVLmin} + t_{POmax} + 2\,t_T$

WRITE OR READ/WRITE CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{WC} (1)	**WRITE CYCLE**	**580**			**ns**	t_T = **20 ns**
t_{RWC} (1)	**READ/WRITE CYCLE**	**580**			**ns**	
t_{PW}	PRECHARGE TO READ/WRITE DELAY	165		500	ns	
t_{WP}	READ/WRITE PULSE WIDTH	50			ns	
t_W	READ/WRITE SET UP TIME	80			ns	
t_{DW}	DATA SET UP TIME	105			ns	
t_{DH}	DATA HOLD TIME	10			ns	
t_{PO}	END OF PRECHARGE TO OUTPUT DELAY			120	ns	C_{LOAD} = 100 pF, R_{LOAD} = 100Ω, V_{REF} = 40 mV
t_{CW}	RELATIONSHIP BETWEEN CENABLE AND READ/WRITE			0	ns	

Note 1: These times will degrade by 40 ns (worst case) if the maximum values for V_{IL} (for precharge, cenable and read/write inputs) go to V_{SS}–14.2V @ 0°C and V_{SS}–14.5V @ 70°C as defined on page 2.

*CAPACITANCE T_A = 25°C

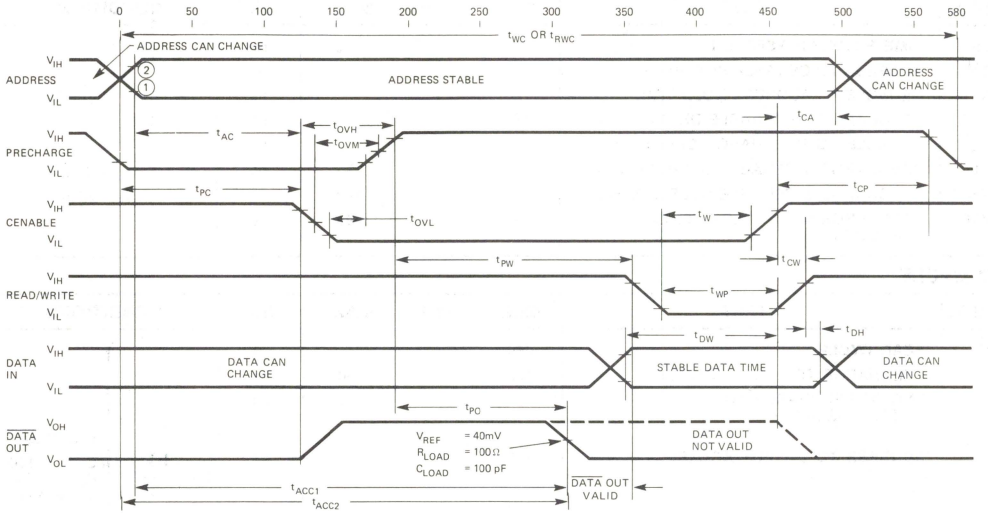
SYMBOL	TEST	TYP.	PLASTIC PKG. MAX.	CERAMIC PKG. MAX.	UNIT	CONDITIONS
C_{AD}	ADDRESS CAPACITANCE	5	7	12	pF	$V_{IN} = V_{SS}$
C_{PR}	PRECHARGE CAPACITANCE	15	18	19.5	pF	$V_{IN} = V_{SS}$
C_{CE}	CENABLE CAPACITANCE	15	18	21	pF	$V_{IN} = V_{SS}$
C_{RW}	READ/WRITE CAPACITANCE	11	15	19.5	pF	$V_{IN} = V_{SS}$
C_{IN1}	DATA INPUT CAPACITANCE	4	5	7.5	pF	CENABLE = 0V, $V_{IN} = V_{SS}$
C_{IN2}	DATA INPUT CAPACITANCE	2	4	6.5	pF	CENABLE = V_{SS}, $V_{IN} = V_{SS}$
C_{OUT}	DATA OUTPUT CAPACITANCE	2	3	7	pF	V_{OUT} = 0V

f = 1 MHz, All Unused Pins Are At A.C. Ground

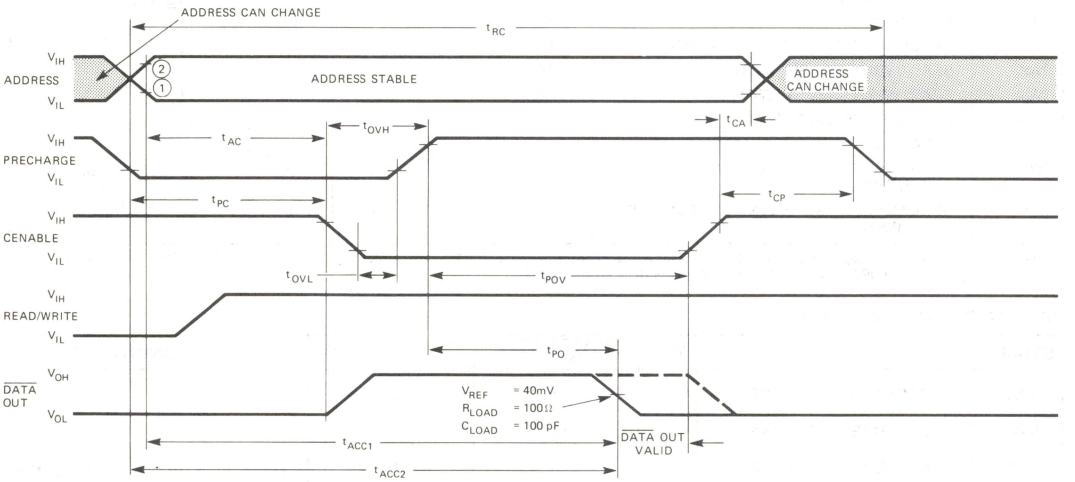
*This parameter is periodically sampled and is not 100% tested. They are measured at worst case operating conditions.

WRITE CYCLE OR READ/WRITE CYCLE

Timing illustrated for minimum cycle.



READ CYCLE



NOTE ① V_{DD} + 2V
NOTE ② V_{SS} − 2V
t_T IS DEFINED AS THE TRANSITIONS BETWEEN THESE TWO POINTS
NOTE 3 t_{DW} IS REFERENCED TO POINT ① OF THE RISING EDGE OF CENABLE OR READ/WRITE WHICHEVER OCCURS FIRST
NOTE 4 t_{DH} IS REFERENCED TO POINT ② OF THE RISING EDGE OF CENABLE OR READ/WRITE WHICHEVER OCCURS FIRST

1103-1
1024 x 1 BIT DYNAMIC RAM

The Intel® 1103-1 is a high speed 1024 bit dynamic random access memory and is the high speed version of the standard 1103. The DC and AC Characteristics for the 1103-1 are given in the following three pages. The absolute maximum ratings for the 1103-1 are the same as for the 1103 on page 3-4.

- **Access Time — 150 nsec**
- **Cycle Time — 340 nsec**

D.C. and Operating Characteristics

(T_A = 0°C to +55°C, V_{SS}[1] = 19V ±5% ($V_{BB} - V_{SS}$)[6] = 3V to 4V, V_{DD} = 0V unless otherwise specified)

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LI}	**INPUT LOAD CURRENT** (ALL INPUT PINS)			**10**	**μA**	**V_{IN} = 0V**
I_{LO}	OUTPUT LEAKAGE CURRENT			10	μA	V_{OUT} = 0V
I_{BB}	**V_{BB} SUPPLY CURRENT**			**100**	**μA**	
I_{DD1}[2]	SUPPLY CURRENT DURING T_{PC}		45	60	mA	ALL ADDRESSES = 0V PRECHARGE = 0V CENABLE = V_{SS} T_A = 25°C
I_{DD2}[2]	SUPPLY CURRENT DURING T_{OV}		50	68.5	mA	ALL ADDRESSES = 0V PRECHARGE = 0V CENABLE = 0V T_A = 25°C
I_{DD3}[2]	SUPPLY CURRENT DURING T_{POV}		8.5	11	mA	PRECHARGE = V_{SS} CENABLE = 0V T_A = 25°C
I_{DD4}[2]	SUPPLY CURRENT DURING T_{CP}		3.0	4	mA	PRECHARGE = V_{SS} CENABLE = V_{SS} T_A = 25°C
$I_{DD\,AVG}$[5]	**AVERAGE SUPPLY CURRENT**		20	**23**	**mA**	**CYCLE TIME = 340 ns PRECHARGE WIDTH @50% 105ns, T_A = 25°C**
V_{IL}	INPUT LOW VOLTAGE	V_{SS} − 20		V_{SS} − 18	V	
V_{IH}	INPUT HIGH VOLTAGE	V_{SS} − 1		V_{SS} + 1	V	
I_{OH1}	**OUTPUT HIGH CURRENT**	**1150**	**1300**	**7000**	**μA**	**T_A = 25°C**
I_{OH2}	**OUTPUT HIGH CURRENT**	**900**	**1150**	**7000**	**μA**	**T_A = 55°C**
I_{OL}[3]	OUTPUT LOW CURRENT		See Note 3			**R_{LOAD}[4] = 100 Ω**
V_{OH1}	OUTPUT HIGH VOLTAGE	115	130	700	mV	T_A = 25°C,
V_{OH2}	OUTPUT HIGH VOLTAGE	90	115	700	mV	T_A = 55°C,
V_{OL}[3]	OUTPUT LOW VOLTAGE		See Note 3			

Note 1: The V_{SS} current drain is equal to (I_{DD} + I_{OH}) or (I_{DD} + I_{OL}).

Note 2: See Supply Current vs. Temperature (p. 2-9) for guaranteed current at the temperature extremes. These values are taken from a single pulse measurement.

Note 3: The output current when reading a low output is the leakage current of the 1103 plus external noise coupled into the output line from the clocks. V_{OL} equals I_{OL} across the load resistor.

Note 4: This value of load resistance is used for measurement purposes. In applications the resistance may range from 100 Ω to 1 kΩ.

Note 5: This parameter is periodically sampled and is not 100% tested.

Note 6: ($V_{BB} - V_{SS}$) supply should be applied at or before V_{SS}.

AC Characteristics (T_A = 0°C to 55°C, V_{SS} = 19 ± 5%, $V_{BB} - V_{SS}$ = 3.0V to 4.0V, V_{DD} = 0V)

READ, WRITE, AND READ/WRITE CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{REF}	**TIME BETWEEN REFRESH**			1	ms	
t_{AC}	ADDRESS TO CENABLE SET UP TIME	30			ns	
t_{CA}	CENABLE TO ADDRESS HOLD TIME	10			ns	
t_{PC}	PRECHARGE TO CENABLE DELAY	60			ns	
t_{CP}	CENABLE TO PRECHARGE DELAY	40			ns	
t_{OVL}	PRECHARGE & CENABLE OVERLAP, LOW	5		30	ns	t_T = 20ns
t_{OVH}	PRECHARGE & CENABLE OVERLAP, HIGH			85	ns	t_T = 20ns
t_{OVM}	PRECHARGE & CENABLE OVERLAP, 50% POINTS	25		50	ns	

READ CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{RC} (1)	**READ CYCLE**	**300**			**ns**	t_T = **20 ns**
t_{POV}	PRECHARGE TO END OF CENABLE	115		500	ns	
t_{PO} (1)	END OF PRECHARGE TO OUTPUT DELAY			75	ns	C_{LOAD} = 50 pF R_{LOAD} = 100Ω V_{REF} = 80 mV
t_{ACC1} (1)	**ADDRESS TO OUTPUT ACCESS**	**150**			**ns**	$t_{ACmin} + t_{OVLmin} + t_{POmax} + 2\,t_T$ C_{LOAD} = 50 pF R_{LOAD} = 100Ω V_{REF} = 80 mV
t_{ACC2} (1)	**PRECHARGE TO OUTPUT ACCESS**	**180**			**ns**	$t_{PCmin} + t_{OVLmin} + t_{POmax} + 2\,t_T$ C_{LOAD} = 50 pF R_{LOAD} = 100Ω V_{REF} = 80 mV

WRITE OR READ/WRITE CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{WC}	**WRITE CYCLE**	**340**			**ns**	t_T = **20 ns**
t_{RWC} (1)	**READ/WRITE CYCLE**	**340**			**ns**	
t_{PW}	PRECHARGE TO READ/WRITE DELAY	115		500	ns	
t_{WP}	READ/WRITE PULSE WIDTH	20			ns	
t_W	READ/WRITE SET UP TIME	20			ns	
t_{DW}	DATA SET UP TIME	40			ns	
t_{DH}	DATA HOLD TIME	10			ns	
t_{PO} (1)	END OF PRECHARGE TO OUTPUT DELAY			75	ns	C_{LOAD} = 50 pF R_{LOAD} = 100Ω V_{REF} = 80 mV
t_{CW}	RELATIONSHIP BETWEEN CENABLE AND READ/WRITE			0	ns	

NOTE 1: These times will degrade by 35 nsec if a V_{REF} point of*40 mV is chosen instead of the 80 mV point defined in the spec.

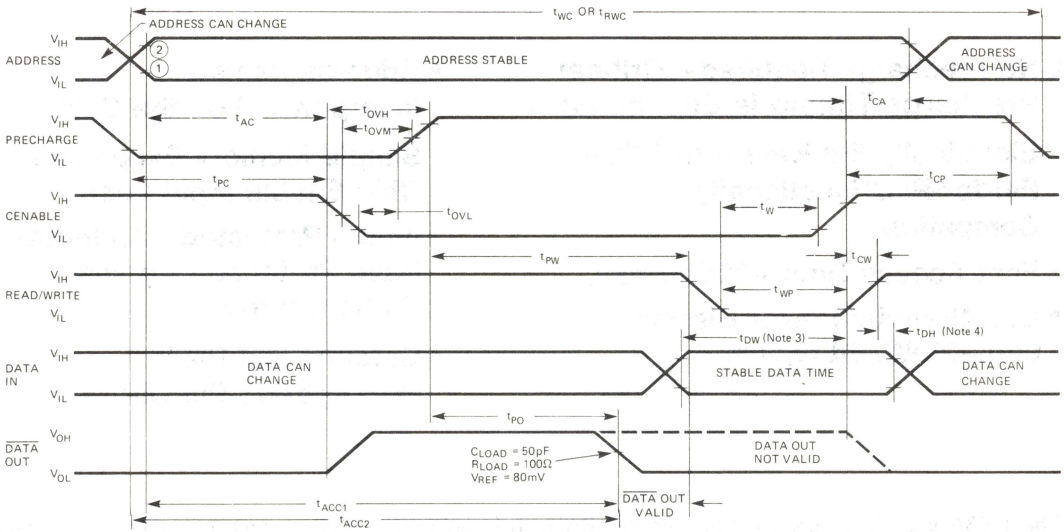
*CAPACITANCE T_A = 25°C

SYMBOL	TEST	TYP.	PLASTIC PKG. MAX.	CERAMIC PKG. MAX.	UNIT	CONDITIONS
C_{AD}	ADDRESS CAPACITANCE	5	7	12	pF	$V_{IN} = V_{SS}$
C_{PR}	PRECHARGE CAPACITANCE	15	18	19.5	pF	$V_{IN} = V_{SS}$
C_{CE}	CENABLE CAPACITANCE	15	18	21	pF	$V_{IN} = V_{SS}$
C_{RW}	READ/WRITE CAPACITANCE	11	15	19.5	pF	$V_{IN} = V_{SS}$
C_{IN1}	DATA INPUT CAPACITANCE	4	5	7.5	pF	CENABLE = 0V $V_{IN} = V_{SS}$
C_{IN2}	DATA INPUT CAPACITANCE	2	4	6.5	pF	CENABLE = V_{SS} $V_{IN} = V_{SS}$
C_{OUT}	DATA OUTPUT CAPACITANCE	2	3	7	pF	V_{OUT} = 0V

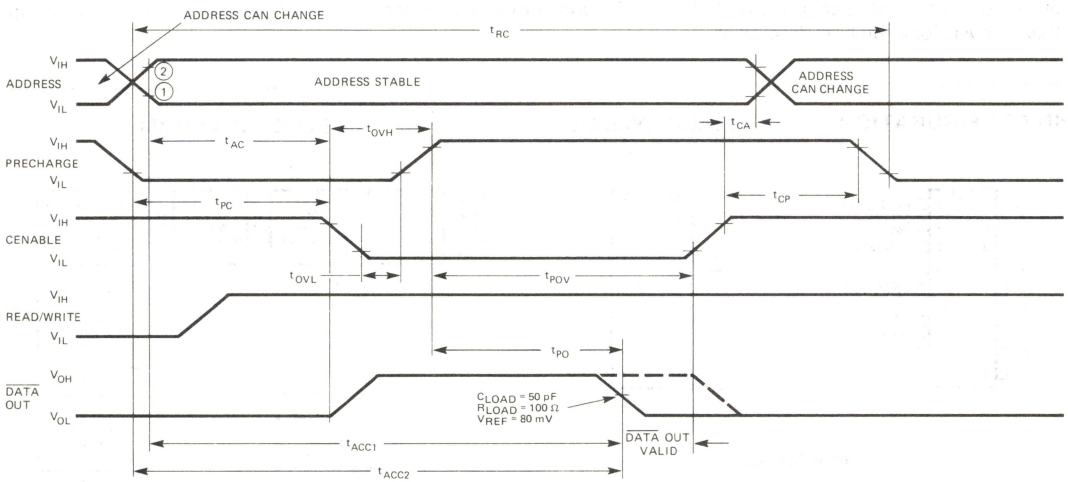
f = 1 MHz, All Unused Pins Are At A.C. Ground

*This parameter is periodically sampled and is not 100% tested. They are measured at worst case operating conditions.

WRITE OR READ/WRITE CYCLE



READ CYCLE



NOTE ① V_{DD} + 2V
NOTE ② V_{SS} − 2V
t_T IS DEFINED AS THE TRANSITIONS BETWEEN THESE TWO POINTS
NOTE 3 t_{DW} IS REFERENCED TO POINT ① OF THE RISING EDGE OF CHIP ENABLE OR READ/WRITE WHICHEVER OCCURS FIRST
NOTE 4 t_{DH} IS REFERENCED TO POINT ② OF THE RISING EDGE OF CHIP ENABLE OR READ/WRITE WHICHEVER OCCURS FIRST

1103A
1024 x 1 BIT DYNAMIC RAM

- *No Precharge Required -- Critical Precharge Timing is Eliminated
- Electrically Equivalent to 1103 -- Pin-for-Pin/Functionally Compatible
- Fast Access Time -- 205ns max.
- Low Standby Power Dissipation -- 2 µW/Bit typical
- Address Registers Incorporated on the Chip
- Simple Memory Expansion -- Chip Enable Input Lead
- Inputs Protected -- All Inputs Have Protection Against Static Charge
- Ceramic and Plastic Package -- 18-Pin DIP

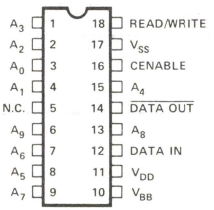
The 1103A is a 1024 word by 1 bit dynamic RAM. It is designed primarily for main memory applications where high performance, low cost, and large bit storage are important design objectives. The 1103A is electrically equivalent to the 1103.

1103A systems may be simplified due to the elimination of the precharge clock, its associated circuitry, and critical overlap timing. Only one external clock, CENABLE, is required.

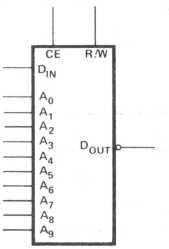
Information stored in the memory is non-destructively read. Refreshing of all 1024 bits is accomplished in 32 read cycles (addressing A_0 to A_4) and is required every two milliseconds. The memory may be used in a low power standby mode by having cenable at V_{SS} potential.

The 1103A is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

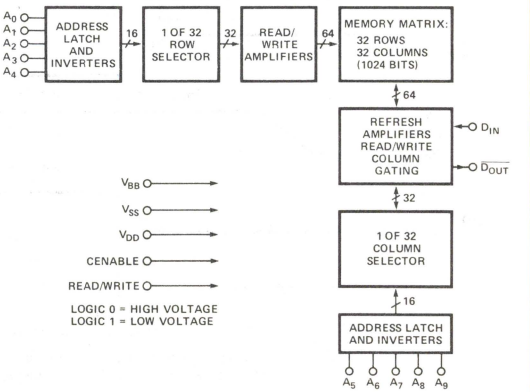
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

D_{IN}	DATA INPUT	NC	NO EXTERNAL CONNECTION REQUIRED (INTERNALLY NOT CONNECTED)
A_0-A_9	ADDRESS INPUTS	CE	CHIP ENABLE
R/W	READ/WRITE	$\overline{D_{OUT}}$	DATA OUTPUT

Absolute Maximum Ratings*

Temperature Under Bias . . . . . 0°C to 70°C

Storage Temperature . . . . . −65°C to +150°C

All Input or Output Voltages with Respect to the most Positive Supply Voltage, V_{BB} . . . . . −25V to 0.3V

Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB} . . . . . −25V to 0.3V

Power Dissipation 1.0W

**COMMENT:*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics

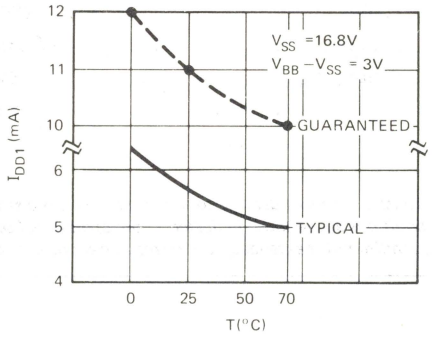
$T_A = 0°C$ to $+70°C$, V_{SS} [1] $= 16V \pm 5\%$, $(V_{BB} - V_{SS})$ [2] $= 3V$ to $4V$, $V_{DD} = 0V$ unless otherwise specified.

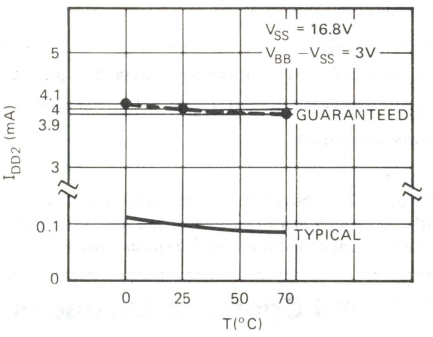
Symbol	Test	Min.	Typ.	Max.	Unit	Conditions
I_{LI}	Input Load Current (All Input Pins)			1	μA	$V_{IN} = 0V$
I_{LO}	Output Leakage Current			1	μA	$V_{OUT} = 0V$
I_{BB}	V_{BB} Supply Current			100	μA	
I_{DD1}	Supply Current During Cenable On		4	11	mA	Cenable = 0V; $T_A = 25°C$
I_{DD2}	Supply Current During Cenable Off		0.1	4	mA	Cenable = V_{SS}; $T_A = 25°C$
I_{DDAV}	Average Supply Current		17	25	mA	Cycle Time = 580ns; $T_A = 25°C$
V_{IL}	Input Low Voltage	$V_{DD} - 1$		$V_{DD} + 1$	V	
V_{IH}	Input High Voltage	$V_{SS} - 1$		$V_{SS} + 1$	V	
I_{OH1}	Output High Current	600	1800	4000	μA	$T_A = 25°C$
I_{OH2}	Output High Current	500	1500	4000	μA	$T_A = 70°C$
I_{OL}	Output Low Current	See Note Three				R_{LOAD} [4] $= 100\Omega$
V_{OH1}	Output High Voltage	60	180	400	mV	$T_A = 25°C$
V_{OH2}	Output High Voltage	50	150	400	mV	$T_A = 70°C$
V_{OL}	Output Low Voltage	See Note Three				

NOTES:

1. The V_{SS} current drain is equal to $(I_{DD} + I_{OH})$ or $(I_{DD} + I_{OL})$.
2. $(V_{BB} - V_{SS})$ supply should be applied at or before V_{SS}.
3. The output current when reading a low output is the leakage current of the 1103 plus external noise coupled into the output line from the clocks. V_{OL} equals I_{OL} across the load resistor.
4. This value of load resistance is used for measurement purposes. In applications the resistance may range from 100Ω to 1 kΩ.

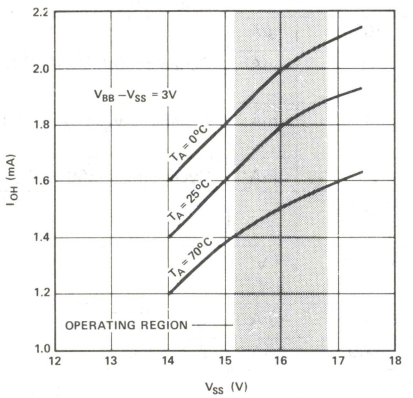
Supply Current vs Temperature



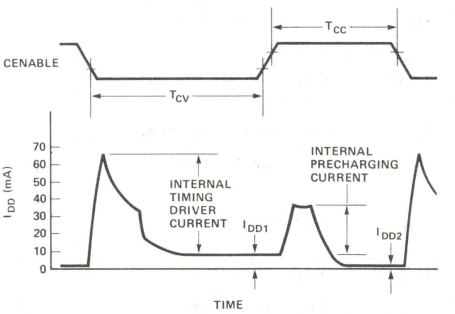


Typical Characteristics

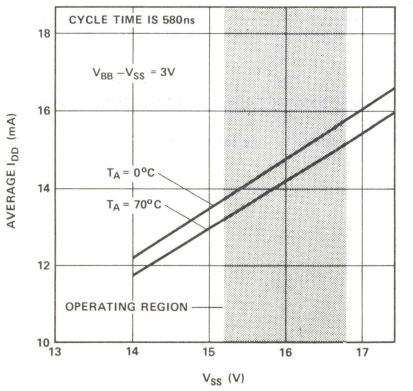
OUTPUT HIGH CURRENT VS. SUPPLY VOLTAGE



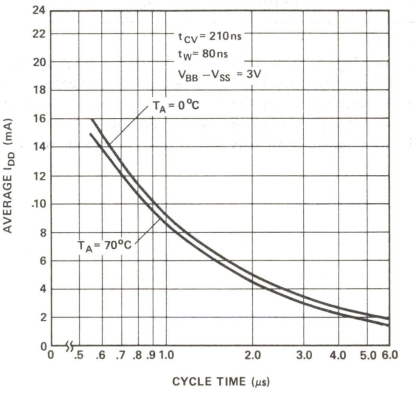
I_{DD} VS. CENABLE



AVERAGE I_{DD} VS. SUPPLY VOLTAGE



AVERAGE I_{DD} VS. 1103A CYCLE TIME



A.C. Characteristics $T_A = 0°C$ to $70°C$, $V_{SS} = 16V \pm 5\%$, $(V_{BB} - V_{SS}) = 3.0V$ to $4.0V$, $V_{DD} = 0V$

READ, WRITE, AND READ/WRITE CYCLE

Symbol	Test	Min.	Max.	Unit	Conditions
t_{REF}	Time Between Refresh		2	ms	
t_{AC}	Address to Cenable Set Up Time	0		ns	
t_{AH}	Address Hold Time	100		ns	
t_{CC}	Cenable Off Time	230		ns	

READ CYCLE

Symbol	Test	Min.	Max.	Unit	Conditions
t_{RC}	Read Cycle	480		ns	$t_T = 20ns$; $C_{LOAD} = 100pF$; $R_{LOAD} = 100\Omega$; $V_{REF} = 40mV$
t_{CV}	Cenable on Time	210	500	ns	
t_{CO}	Cenable Output Delay		185	ns	
t_{ACC}	ADDRESS TO OUTPUT ACCESS		205	ns	$t_{ACC} = t_{AC\ MIN} + t_{CO} + t_T$
t_{WH}	Read/Write Hold Time	30		ns	

WRITE OR READ/WRITE CYCLE

Symbol	Test	Min.	Max.	Unit	Conditions
t_{WCY}	Write Cycle	580		ns	$t_T = 20ns$
t_{RWC}	Read/Write Cycle	580		ns	
t_{CW}	Cenable to Read/Write Delay	210	500	ns	
t_{WP}	Read/Write Pulse Width	50		ns	
t_W	Read/Write Set Up Time	80		ns	
t_{DW}	Data Set Up Time	105		ns	
t_{DH}	Data Hold Time	10		ns	
t_{CO}	Output Delay		185	ns	$C_{LOAD} = 100pF$; $R_{LOAD} = 100\Omega$; $V_{REF} = 40mV$
t_{WC}	Read/Write to Cenable	0		ns	

CAPACITANCE[1] $T_A = 25°C$

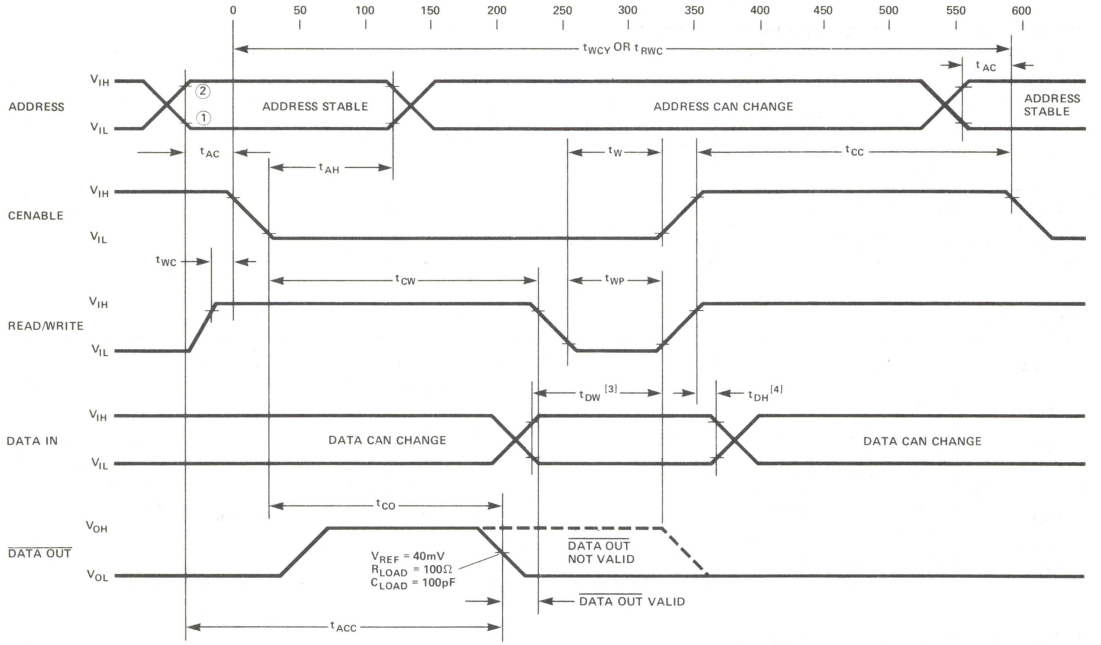
Symbol	Test	Typ. Plastic	Plastic Pkg. Max.	Ceramic Pkg. Max.	Unit	Conditions
C_{AD}	Address Capacitance	5	7	12	pF	$V_{IN} = V_{SS}$
C_{CE}	Cenable Capacitance	22	25	28	pF	$V_{IN} = V_{SS}$
C_{RW}	Read/Write Capacitance	11	15	19.5	pF	$V_{IN} = V_{SS}$
C_{IN1}	Data Input Capacitance	4	5	7.5	pF	Cenable = 0V; $V_{IN} = V_{SS}$
C_{IN2}	Data Input Capacitance	2	4	6.5	pF	Cenable = V_{SS}
C_{OUT}	Data Output Capacitance	2	3	7.0	pF	$V_{IN} = V_{SS}$; $V_{OUT} = 0V$

f = 1MHz. All unused pins are at A.C. ground.

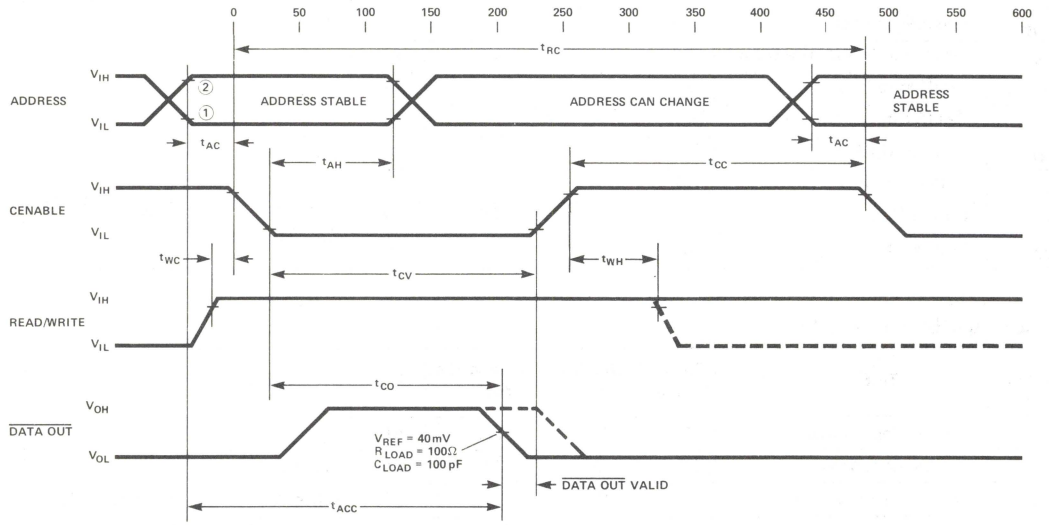
NOTES: 1. These parameters are periodically sampled and are not 100% tested. They are measured at worst case operating conditions.

WRITE CYCLE OR READ/WRITE CYCLE

Timing illustrated for minimum cycle.



READ CYCLE



NOTES:

(1.) V_{DD} + 2V
(2.) V_{SS} − 2V
t_T is defined as the transition between these two points.

3. t_{DW} is referenced to point 1 of the rising edge of cenable or Read/Write, whichever occurs first.
4. t_{DH} is referenced to point 2 of the rising edge of Read/Write.

1103-1
1024 x 1 BIT DYNAMIC RAM

- **High Speed 1103A — Access Time — 145 ns / Cycle Time — 340 ns**
- ***No Precharge Required -- Critical Precharge Timing is Eliminated**
- **Low Standby Power Dissipation -- 0.2 µW/Bit Typical**
- **Address Registers Incorporated on the Chip**
- **Simple Memory Expansion -- Chip Enable Input Lead**
- **Inputs Protected -- All Inputs Have Protection Against Static Charge**
- **Standard 18-Pin Dual In-Line Packages**

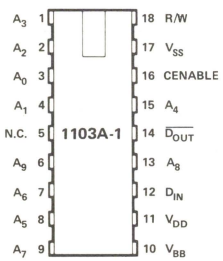
The Intel®1103A-1 is a high speed 1024 bit dynamic random access memory and is the fastest version of the standard 1103A. It is designed primarily for main memory applications where high performance, low cost, and large bit storage are important design objectives.

1103A-1 systems may be simplified due to the elimination of the precharge clock, its associated circuitry, and critical overlap timing. Only one external clock, CENABLE, is required.

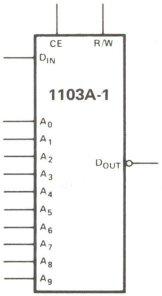
Information stored in the memory is non-destructively read. Refreshing of all 1024 bits is accomplished in 32 read cycles (addressing A_0 to A_4) and is required every one millisecond. The memory may be used in a low power standby mode by having cenable at V_{SS} potential.

The 1103A-1 is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

PIN CONFIGURATION



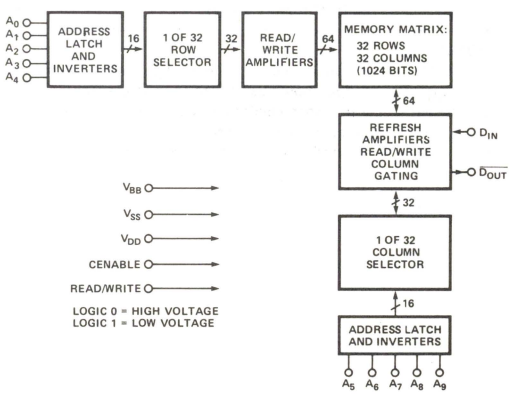
LOGIC SYMBOL



PIN NAMES

D_{IN}	DATA INPUT	NC	NO EXTERNAL CONNECTION REQUIRED (INTERNALLY NOT CONNECTED)
A_0-A_9	ADDRESS INPUTS	CE	CHIP ENABLE
R/W	READ/WRITE	$\overline{D_{OUT}}$	DATA OUTPUT

BLOCK DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias . . . . . 0°C to 70°C

Storage Temperature . . . . . −65°C to +150°C

All Input or Output Voltages with Respect to the most Positive Supply Voltage, V_{BB} . . . . . −25V to 0.3V

Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB} . . . . . −25V to 0.3V

Power Dissipation 1.0W

COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics

$T_A = 0°C$ to $+55°C$, V_{SS}[1] $= 19V \pm 5\%$, $(V_{BB} - V_{SS})$[2] $= 3V$ to $4V$, $V_{DD} = 0V$ unless otherwise specified.

Symbol	Test	Min.	Typ.	Max.	Unit	Conditions
I_{LI}	Input Load Current (All Input Pins)			10	μA	$V_{IN} = 0V$
I_{LO}	Output Leakage Current			10	μA	$V_{OUT} = 0V$
I_{BB}	V_{BB} Supply Current			100	μA	
I_{DD1}	Supply Current During Cenable On		7	11	mA	Cenable = 0V; $T_A = 25°C$
I_{DD2}	Supply Current During Cenable Off		0.01	0.5	mA	Cenable = V_{SS}; $T_A = 25°C$
I_{DDAV}	Average Supply Current		25	33	mA	Cycle Time = 340ns; $T_A = 25°C$
V_{IL}	Input Low Voltage	$V_{DD} - 1$		$V_{DD} + 1$	V	
V_{IH}	Input High Voltage	$V_{SS} - 1$		$V_{SS} + 1$	V	
I_{OH1}	Output High Current	1150	1800	7000	μA	$T_A = 25°C$
I_{OH2}	Output High Current	900	1600	7000	μA	$T_A = 55°C$
I_{OL}	Output Low Current	See Note Three				R_{LOAD}[4] $= 100\Omega$
V_{OH1}	Output High Voltage	115	180	700	mV	$T_A = 25°C$
V_{OH2}	Output High Voltage	90	160	700	mV	$T_A = 55°C$
V_{OL}	Output Low Voltage	See Note Three				

NOTES:

1. The V_{SS} current drain is equal to $(I_{DD} + I_{OH})$ or $(I_{DD} + I_{OL})$.
2. $(V_{BB} - V_{SS})$ supply should be applied at or before V_{SS}.
3. The output current when reading a low output is the leakage current of the 1103 plus external noise coupled into the output line from the clocks. V_{OL} equals I_{OL} across the load resistor.
4. This value of load resistance is used for measurement purposes. In applications the resistance may range from 100Ω to 1 kΩ.

A.C. Characteristics $T_A = 0°C$ to $55°C$, $V_{SS} = 19V \pm 5\%$, $(V_{BB} - V_{SS}) = 3.0V$ to $4.0V$, $V_{DD} = 0V$.

READ, WRITE, AND READ/WRITE CYCLE

Symbol	Test	Min.	Max.	Unit	Conditions
t_{REF}	Time Between Refresh		1	ms	
t_{AC}	Address to Cenable Set Up Time	0		ns	
t_{AH}	Address Hold Time	100		ns	
t_{CC}	Cenable Off Time	120		ns	

READ CYCLE

Symbol	Test	Min.	Max.	Unit	Conditions
t_{RC}	Read Cycle	300		ns	$t_T = 20ns$; $C_{LOAD} = 50pF$; $R_{LOAD} = 100\Omega$; $V_{REF} = 80mV$
t_{CV}	Cenable on Time	140	500	ns	
t_{CO}	Cenable Output Delay		125	ns	
t_{ACC}	ADDRESS TO OUTPUT ACCESS		145	ns	$t_{ACC} = t_{AC\ MIN} + t_{CO} + t_T$
t_{WH}	Read/Write Hold Time	30		ns	

WRITE OR READ/WRITE CYCLE

Symbol	Test	Min.	Max.	Unit	Conditions
t_{WCY}	Write Cycle	340		ns	$t_T = 20ns$
t_{RWC}	Read/Write Cycle	340		ns	
t_{CW}	Cenable to Read/Write Delay	140	500	ns	
t_{WP}	Read/Write Pulse Width	20		ns	
t_W	Read/Write Set Up Time	20		ns	
t_{DW}	Data Set Up Time	40		ns	
t_{DH}	Data Hold Time	10		ns	
t_{CO}	Output Delay		125	ns	$C_{LOAD} = 50pF$; $R_{LOAD} = 100\Omega$; $V_{REF} = 80mV$
t_{WC}	Read/Write to Cenable	0		ns	

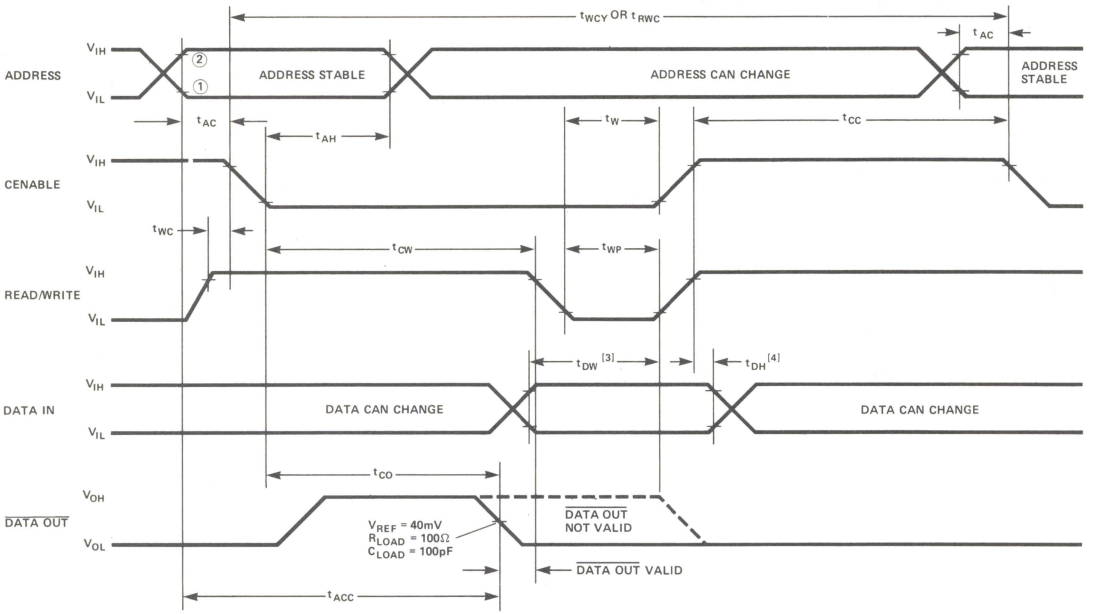
CAPACITANCE[1] $T_A = 25°C$

Symbol	Test	Typ. Plastic	Plastic Pkg. Max.	Ceramic Pkg. Max.	Unit	Conditions
C_{AD}	Address Capacitance	5	7	12	pF	$V_{IN} = V_{SS}$
C_{CE}	Cenable Capacitance	22	25	28	pF	$V_{IN} = V_{SS}$
C_{RW}	Read/Write Capacitance	11	15	19.5	pF	$V_{IN} = V_{SS}$
C_{IN1}	Data Input Capacitance	4	5	7.5	pF	Cenable = 0V; $V_{IN} = V_{SS}$
C_{IN2}	Data Input Capacitance	2	4	6.5	pF	Cenable = V_{SS}
C_{OUT}	Data Output Capacitance	2	3	7.0	pF	$V_{IN} = V_{SS}$; $V_{OUT} = 0V$

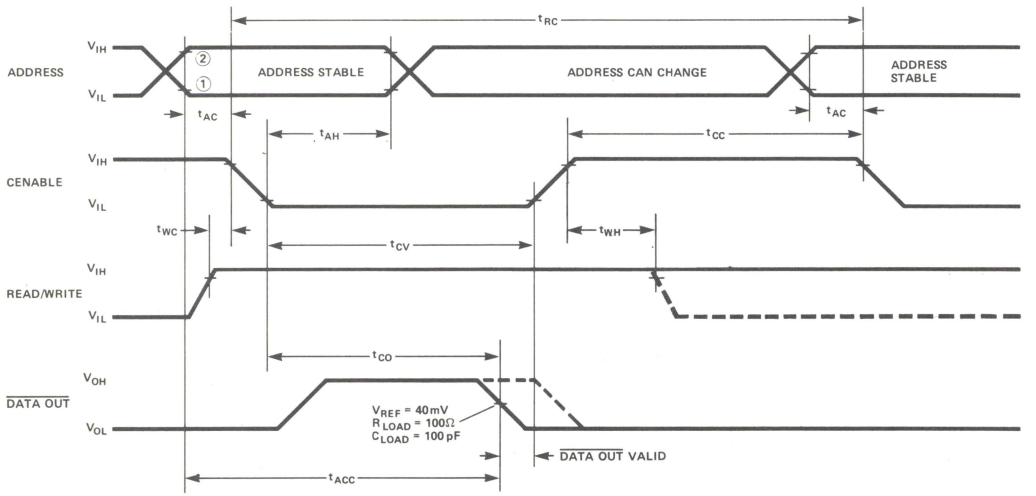
f = 1MHz. All unused pins are at A.C. ground.

NOTES: 1. These parameters are periodically sampled and are not 100% tested. They are measured at worst case operating conditions.

WRITE CYCLE OR READ/WRITE CYCLE

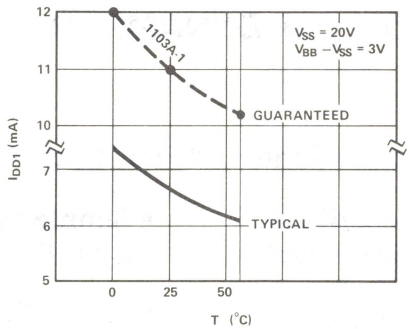


READ CYCLE



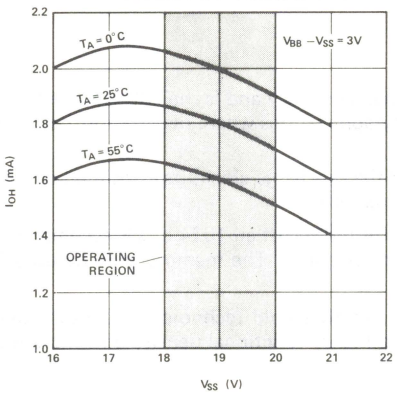
NOTES:
① V_{DD} + 2V
② V_{SS} − 2V
t_T is defined as the transition between these two points.
3. t_{DW} is referenced to point 1 of the rising edge of cenable or Read/Write, whichever occurs first.
4. t_{DH} is referenced to point 2 of the rising edge of Read/Write.

Supply Current vs Temperature

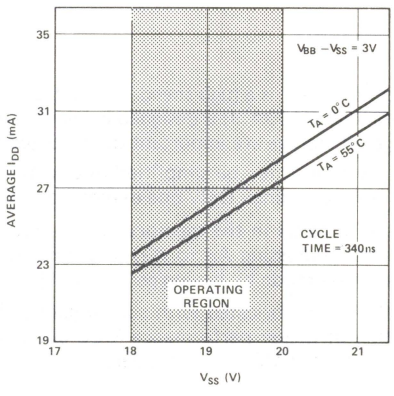


Typical Characteristics

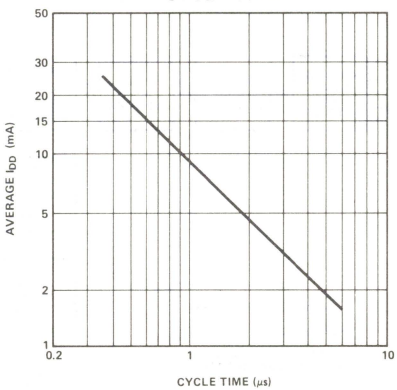
OUTPUT HIGH CURRENT VS. SUPPLY VOLTAGE



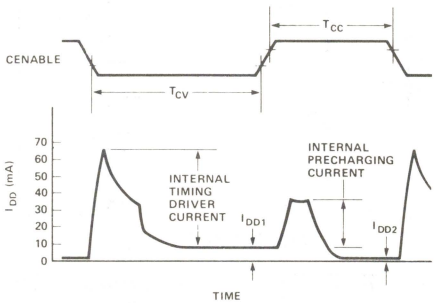
AVERAGE I_{DD} VS. SUPPLY VOLTAGE



AVERAGE I_{DD} VS. CYCLE TIME



I_{DD} VS. CENABLE



1103A-2
1024 x 1 BIT DYNAMIC RAM

- **High Speed 1103A — Access Time — 145 ns / Cycle Time — 400 ns**
- *** No Precharge Required -- Critical Precharge Timing is Eliminated**
- **Low Standby Power Dissipation -- 0.2 µW/Bit Typical**
- **Address Registers Incorporated on the Chip**
- **Simple Memory Expansion -- Chip Enable Input Lead**
- **Inputs Protected -- All Inputs Have Protection Against Static Charge**
- **Standard 18-Pin Dual In-Line Packages**

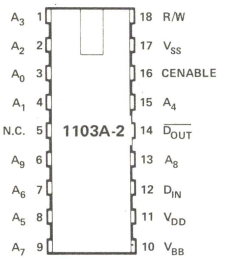
The Intel®1130A-2 is a high speed 1024 bit dynamic random access memory and is the 400 ns cycle time version of the standard 1103A. It is designed primarily for main memory applications where high performance, low cost, and large bit storage are important design objectives.

1103A-2 systems may be simplified due to the elimination of the precharge clock, its associated circuitry, and critical overlap timing. Only one external clock, CENABLE, is required.

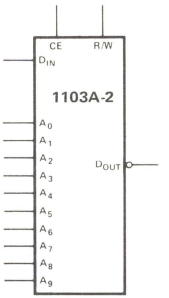
Information stored in the memory is non-destructively read. Refreshing of all 1024 bits is accomplished in 32 read cycles (addressing A_0 to A_4) and is required every one millisecond. The memory may be used in a low power standby mode by having cenable at V_{SS} potential.

The 1103A-2 is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

PIN CONFIGURATION



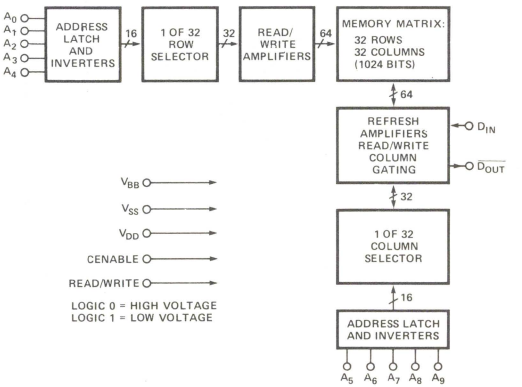
LOGIC SYMBOL



PIN NAMES

D_{IN}	DATA INPUT	NC	NO EXTERNAL CONNECTION REQUIRED (INTERNALLY NOT CONNECTED)
A_0-A_9	ADDRESS INPUTS	CE	CHIP ENABLE
R/W	READ/WRITE	$\overline{D_{OUT}}$	DATA OUTPUT

BLOCK DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias . . . . . 0°C to 70°C

Storage Temperature . . . . . −65°C to +150°C

All Input or Output Voltages with Respect to the most Positive Supply Voltage, V_{BB} . . . . . −25V to 0.3V

Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB} . . . . . −25V to 0.3V

Power Dissipation 1.0W

**COMMENT:*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics

$T_A = 0°C$ to $+55°C$, V_{SS}[1] $= 19V \pm 5\%$, $(V_{BB} - V_{SS})$[2] $= 3V$ to $4V$, $V_{DD} = 0V$ unless otherwise specified.

Symbol	Test	Min.	Typ.	Max.	Unit	Conditions
I_{LI}	Input Load Current (All Input Pins)			10	μA	$V_{IN} = 0V$
I_{LO}	Output Leakage Current			10	μA	$V_{OUT} = 0V$
I_{BB}	V_{BB} Supply Current			100	μA	
I_{DD1}	Supply Current During Cenable On		7	11	mA	Cenable = 0V; $T_A = 25°C$
I_{DD2}	Supply Current During Cenable Off		0.01	0.5	mA	Cenable = V_{SS}; $T_A = 25°C$
I_{DDAV}	Average Supply Current		22	30	mA	Cycle Time = 400ns; $T_A = 25°C$
V_{IL}	Input Low Voltage	$V_{DD} - 1$		$V_{DD} + 1$	V	
V_{IH}	Input High Voltage	$V_{SS} - 1$		$V_{SS} + 1$	V	
I_{OH1}	Output High Current	1150	1800	7000	μA	$T_A = 25°C$
I_{OH2}	Output High Current	900	1600	7000	μA	$T_A = 55°C$
I_{OL}	Output Low Current	See Note Three				R_{LOAD}[4] $= 100\Omega$
V_{OH1}	Output High Voltage	115	180	700	mV	$T_A = 25°C$
V_{OH2}	Output High Voltage	90	160	700	mV	$T_A = 55°C$
V_{OL}	Output Low Voltage	See Note Three				

NOTES:

1. The V_{SS} current drain is equal to $(I_{DD} + I_{OH})$ or $(I_{DD} + I_{OL})$.
2. $(V_{BB} - V_{SS})$ supply should be applied at or before V_{SS}.
3. The output current when reading a low output is the leakage current of the 1103 plus external noise coupled into the output line from the clocks. V_{OL} equals I_{OL} across the load resistor.
4. This value of load resistance is used for measurement purposes. In applications the resistance may range from 100Ω to 1 kΩ.

A.C. Characteristics T_A = 0°C to 55°C, V_{SS} = 19V ±5%, (V_{BB} −V_{SS})=3.0V to 4.0V, V_{DD} = 0V.

READ, WRITE, AND READ/WRITE CYCLE

Refer to page 2-23 for definitions.

Symbol	Test	Min.	Max.	Unit	Conditions
t_{REF}	Time Between Refresh		1	ms	
t_{AC}	Address to Cenable Set Up Time	0		ns	
t_{AH}	Address Hold Time	100		ns	
t_{CC}	Cenable Off Time	180		ns	

READ CYCLE

Symbol	Test	Min.	Max.	Unit	Conditions
t_{RC}	Read Cycle	360		ns	t_T= 20ns; C_{LOAD} = 50pF; R_{LOAD} = 100Ω; V_{REF} = 80mV
t_{CV}	Cenable on Time	140	500	ns	
t_{CO}	Cenable Output Delay		125	ns	
t_{ACC}	ADDRESS TO OUTPUT ACCESS		145	ns	$t_{ACC} = t_{AC\ MIN} + t_{CO} + t_T$
t_{WH}	Read/Write Hold Time	30		ns	

WRITE OR READ/WRITE CYCLE

Symbol	Test	Min.	Max.	Unit	Conditions
t_{WCY}	Write Cycle	400		ns	t_T= 20ns
t_{RWC}	Read/Write Cycle	400		ns	
t_{CW}	Cenable to Read/Write Delay	140	500	ns	
t_{WP}	Read/Write Pulse Width	20		ns	
t_W	Read/Write Set Up Time	20		ns	
t_{DW}	Data Set Up Time	40		ns	
t_{DH}	Data Hold Time	10		ns	
t_{CO}	Output Delay		125	ns	C_{LOAD} = 50pF; R_{LOAD} = 100Ω; V_{REF} = 80mV
t_{WC}	Read/Write to Cenable	0		ns	

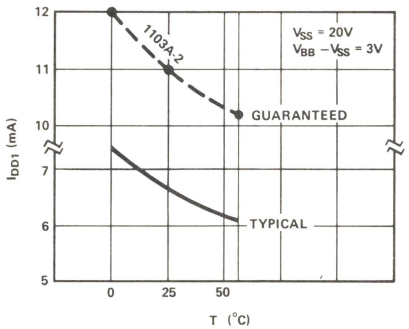
CAPACITANCE[1] T_A = 25°C

Symbol	Test	Typ. Plastic	Plastic Pkg. Max.	Ceramic Pkg. Max.	Unit	Conditions
C_{AD}	Address Capacitance	5	7	12	pF	$V_{IN} = V_{SS}$
C_{CE}	Cenable Capacitance	22	25	28	pF	$V_{IN} = V_{SS}$
C_{RW}	Read/Write Capacitance	11	15	19.5	pF	$V_{IN} = V_{SS}$
C_{IN1}	Data Input Capacitance	4	5	7.5	pF	Cenable = 0V; $V_{IN} = V_{SS}$
C_{IN2}	Data Input Capacitance	2	4	6.5	pF	Cenable = V_{SS}
C_{OUT}	Data Output Capacitance	2	3	7.0	pF	$V_{IN} = V_{SS}$; V_{OUT} = 0V

f = 1MHz. All unused pins are at A.C. ground.

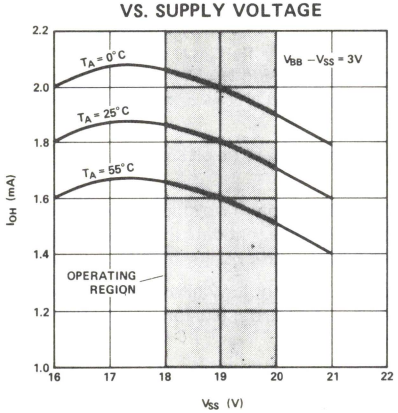
NOTES: 1. These parameters are periodically sampled and are not 100% tested. They are measured at worst case operating conditions.

Supply Current vs Temperature

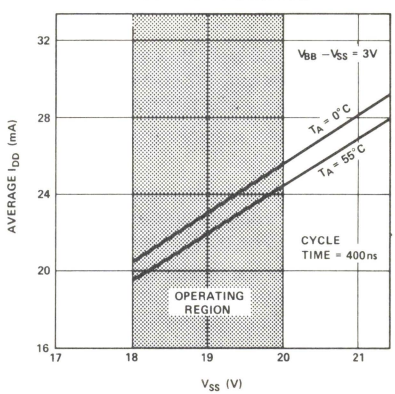


Typical Characteristics

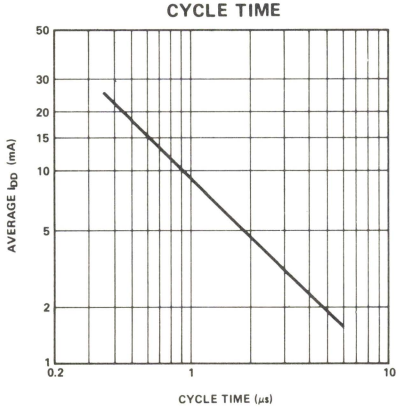
OUTPUT HIGH CURRENT VS. SUPPLY VOLTAGE



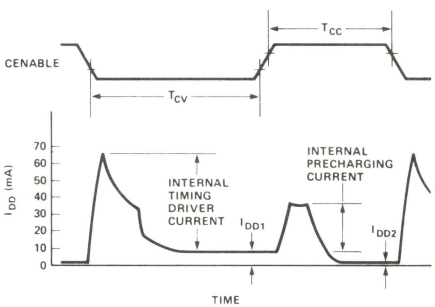
AVERAGE I_{DD} VS. SUPPLY VOLTAGE



AVERAGE I_{DD} VS. CYCLE TIME



I_{DD} VS. CENABLE



2101A/8101A-4*

256 X 4 BIT STATIC RAM

2101A-2	250 ns Max.
2101A	350 ns Max.
2101A-4	450 ns Max.

- 256 x 4 Organization to Meet Needs for Small System Memories
- Single +5V Supply Voltage
- Directly TTL Compatible: All Inputs and Output
- Statis MOS: No Clocks or Refreshing Required
- Simple Memory Expansion: Chip Enable Input
- Inputs Protected: All Inputs Have Protection Against Static Charge
- Low Cost Packaging: 22 Pin Plastic Dual In-Line Configuration
- Low Power: Typically 150 mW
- Three-State Output: OR-Tie Capability
- Output Disable Provided for Ease of Use in Common Data Bus Systems

The Intel® 2101A is a 256 word by 4-bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

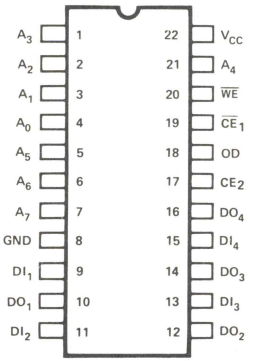
The 2101A is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Two chip-enables allow easy selection of an individual package when outputs are OR-tied. An output disable is provided so that data inputs and outputs can be tied for common I/O systems. The output disable function eliminates the need for bi-directional logic in a common I/O system.

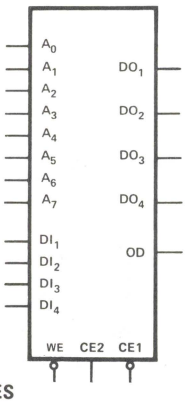
The Intel® 2101A is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost plastic packaging.

PIN CONFIGURATION



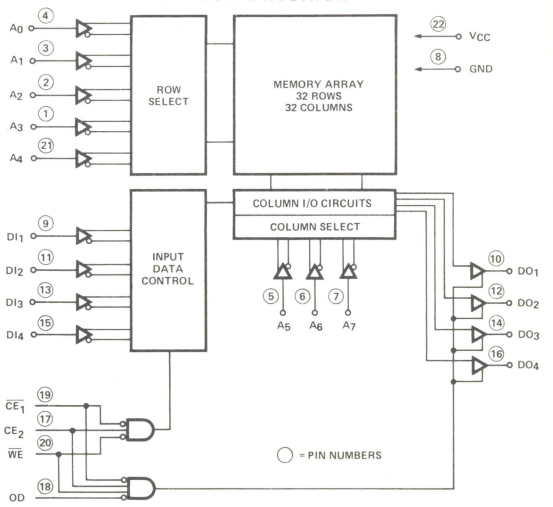
LOGIC SYMBOL



PIN NAMES

DI_1-DI_4	DATA INPUT	CE_2	CHIP ENABLE 2
A_0-A_7	ADDRESS INPUTS	OD	OUTPUT DISABLE
$\overline{WE}$	WRITE ENABLE	DO_1-DO_4	DATA OUTPUT
$\overline{CE_1}$	CHIP ENABLE 1	V_{CC}	POWER (+5V)

BLOCK DIAGRAM



*All 8101A-4 specs are identical to the 2101A-4 specs.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . -10°C to 80°C

Storage Temperature . . . . . -65°C to +150°C

Voltage On Any Pin
With Respect to Ground . . . . . -0.5V to +7V

Power Dissipation . . . . . 1 Watt

**COMMENT:*

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

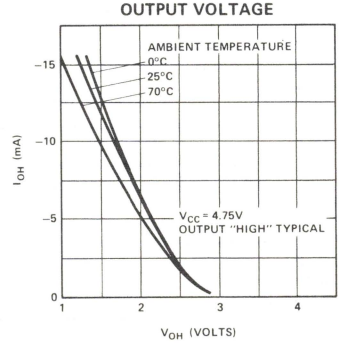
D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

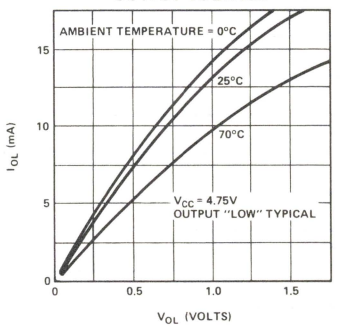
Symbol	Parameter		Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Current			1	10	µA	V_{IN} = 0 to 5.25V
I_{LOH}	Data Output Leakage Current			1	10	µA	Output Disabled, V_{OUT}=4.0V
I_{LOL}	Data Output Leakage Current			-1	-10	µA	Output Disabled, V_{OUT}=0.45V
I_{CC1}	Power Supply Current	2101A, 2101A-4		35	55	mA	V_{IN} = 5.25V, I_O = 0mA, T_A = 25°C
		2101A-2		45	65		
I_{CC2}	Power Supply Current	2101A, 2101A-4			60	mA	V_{IN} = 5.25V, I_O = 0mA, T_A = 0°C
		2101A-2			70		
V_{IL}	Input "Low" Voltage		-0.5		+0.8	V	
V_{IH}	Input "High" Voltage		2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage				+0.45	V	I_{OL} = 2.0mA
V_{OH}	Output "High" Voltage	2101A, 2101A-2	2.4			V	I_{OH} = -200µA
		2101A-4	2.4			V	I_{OH} = -150µA

TYPICAL D.C. CHARACTERISTICS

OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.

A.C. CHARACTERISTICS FOR 2101A-2 (250 ns ACCESS TIME)

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	250			ns	
t_A	Access Time			250	ns	t_r, t_f = 20ns
t_{CO}	Chip Enable To Output			180	ns	Input Levels = 0.8V or 2.0V
t_{OD}	Output Disable To Output			130	ns	Timing Reference = 1.5V
t_{DF}[3]	Data Output to High Z State	0		180	ns	Load = 1 TTL Gate
t_{OH}	Previous Read Data Valid after change of Address	40			ns	and C_L = 100pF.

WRITE CYCLE

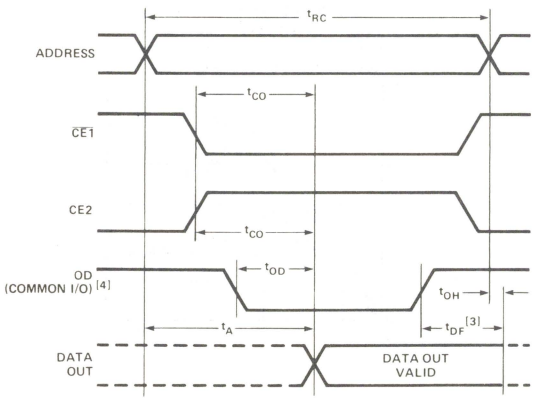
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	170			ns	
t_{AW}	Write Delay	20			ns	t_r, t_f = 20ns
t_{CW}	Chip Enable To Write	150			ns	Input Levels = 0.8V or 2.0V
t_{DW}	Data Setup	150			ns	Timing Reference = 1.5V
t_{DH}	Data Hold	0			ns	Load = 1 TTL Gate
t_{WP}	Write Pulse	150			ns	and C_L = 100pF.
t_{WR}	Write Recovery	0			ns	
t_{DS}	Output Disable Setup	20			ns	

CAPACITANCE[2] $T_A = 25°C$, f = 1MHz

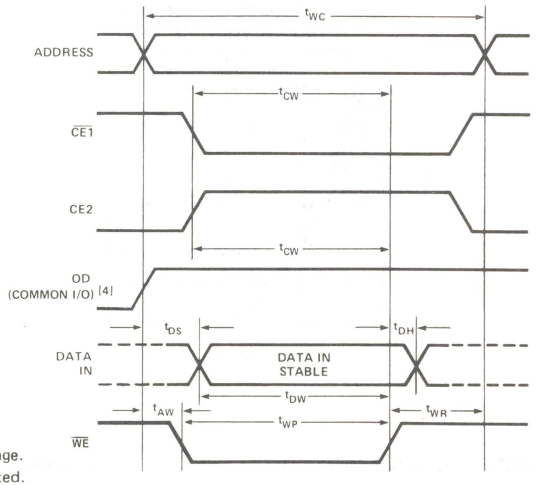
Symbol	Test	Limits (pF)	
		Typ.[1]	Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
C_{OUT}	Output Capacitance V_{OUT} = 0V	8	12

WAVEFORMS

READ CYCLE



WRITE CYCLE



NOTES:
1. Typical values are for $T_A = 25°C$ and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.
3. t_{DF} is with respect to the trailing edge of $\overline{CE_1}$, CE_2, or OD, whichever occurs first.
4. OD should be tied low for separate I/O operation.

2101A (350 ns ACCESS TIME)
A.C. CHARACTERISTICS

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	350			ns	t_r, t_f = 20ns Input Levels = 0.8V or 2.0V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_A	Access Time			350	ns	
t_{CO}	Chip Enable To Output			240	ns	
t_{OD}	Output Disable To Output			180	ns	
t_{DF} [2]	Data Output to High Z State	0		150	ns	
t_{OH}	Previous Read Data Valid after change of Address	40			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	220			ns	t_r, t_f = 20ns Input Levels = 0.8V or 2.0V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_{AW}	Write Delay	20			ns	
t_{CW}	Chip Enable To Write	200			ns	
t_{DW}	Data Setup	200			ns	
t_{DH}	Data Hold	0			ns	
t_{WP}	Write Pulse	200			ns	
t_{WR}	Write Recovery	0			ns	
t_{DS}	Output Disable Setup	20			ns	

2101A-4 (450 ns ACCESS TIME)
A.C. CHARACTERISTICS

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	450			ns	t_r, t_f = 20ns Input Levels = 0.8V or 2.0V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_A	Access Time			450	ns	
t_{CO}	Chip Enable To Output			310	ns	
t_{OD}	Output Disable To Output			250	ns	
t_{DF} [2]	Data Output to High Z State	0		200	ns	
t_{OH}	Previous Read Data Valid after change of Address	40			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	270			ns	t_r, t_f = 20ns Input Levels = 0.8V or 2.0V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_{AW}	Write Delay	20			ns	
t_{CW}	Chip Enable To Write	250			ns	
t_{DW}	Data Setup	250			ns	
t_{DH}	Data Hold	0			ns	
t_{WP}	Write Pulse	250			ns	
t_{WR}	Write Recovery	0			ns	
t_{DS}	Output Disable Setup	20			ns	

NOTES: 1. Typical values are for $T_A = 25°C$ and nominal supply voltage.
2. t_{DF} is with respect to the trailing edge of $\overline{CE_1}$, CE_2, or OD, whichever occurs first.

2102A, 2102AL/8102A-4*
1K x 1 BIT STATIC RAM

P/N	Standby Pwr. (mW)	Operating Pwr. (mW)	Access (ns)
2102AL-4	35	174	450
2102AL	35	174	350
2102AL-2	42	342	250
2102A-2	—	342	250
2102A	—	289	350
2102A-4	—	289	450

- **Single +5 Volts Supply Voltage**
- **Directly TTL Compatible: All Inputs and Output**
- **Standby Power Mode (2102AL)**
- **Three-State Output: OR-Tie Capability**
- **Inputs Protected: All Inputs Have Protection Against Static Charge**
- **Low Cost Packaging: 16 Pin Dual-In-Line Configuration**

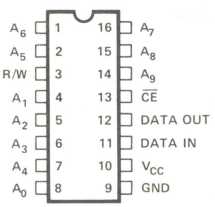
The Intel® 2102A is a high speed 1024 word by one bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

The 2102A is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. *A low standby power version (2102AL) is also available. It has all the same operating characteristics of the 2102A with the added feature of 35mW maximum power dissipation in standby and 174mW in operations.*

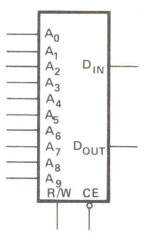
It is directly TTL compatible in all respects: inputs, output, and a single +5 volt supply. A separate chip enable ($\overline{CE}$) lead allows easy selection of an individual package when outputs are OR-tied.

The Intel® 2102A is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance easy to use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

PIN CONFIGURATION



LOGIC SYMBOL



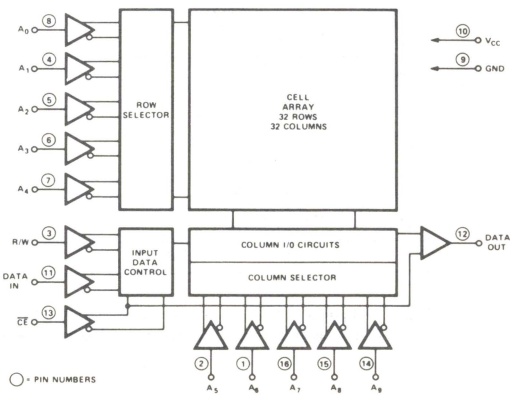
PIN NAMES

D_{IN}	DATA INPUT
A_0-A_9	ADDRESS INPUTS
R/W	READ/WRITE INPUT
$\overline{CE}$	CHIP ENABLE
D_{OUT}	DATA OUTPUT
V_{CC}	POWER (+5V)

TRUTH TABLE

$\overline{CE}$	R/W	D_{IN}	D_{OUT}	MODE
H	X	X	HIGH Z	NOT SELECTED
L	L	L	L	WRITE "0"
L	L	H	H	WRITE "1"
L	H	X	D_{OUT}	READ

BLOCK DIAGRAM



*All 8102A-4 specifications are identical to the 2102A-4 specifications.

Absolute Maximum Ratings*

Ambient Temperature Under Bias	−10°C to 80°C
Storage Temperature	−65°C to +150°C
Voltage On Any Pin With Respect To Ground	−0.5V to +7V
Power Dissipation	1 Watt

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	2102A, 2102A-4, 2102AL, 2102AL-4 Limits Min.	Typ.[1]	Max.	2102A-2, 2102AL-2 Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Load Current		1	10		1	10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	Output Leakage Current		1	5		1	5	μA	$\overline{CE}$ = 2.0V, V_{OUT} = V_{OH}
I_{LOL}	Output Leakage Current		-1	-10		-1	-10	μA	$\overline{CE}$ = 2.0V, V_{OUT} = 0.4V
I_{CC}	Power Supply Current		33	Note 2		45	65	mA	All Inputs = 5.25V, Data Out Open, T_A = 0°C
V_{IL}	Input Low Voltage	-0.5		0.8	-0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4			0.4	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.4			2.4			V	I_{OH} = -100μA

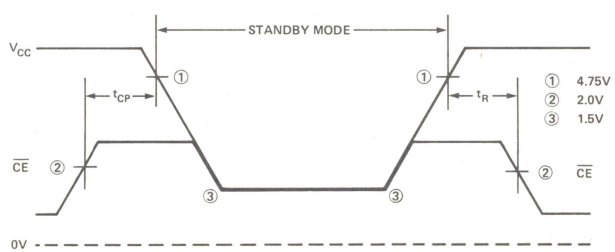
Notes: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. The maximum I_{CC} value is 55mA for the 2102A and 2102A-4, and 33mA for the 2102AL and 2102AL-4.

Standby Characteristics 2102AL, 2102AL-2, and 2102AL-4 (Available only in the Plastic Package)

T_A = 0°C to 70°C

Symbol	Parameter	2102AL, 2102AL-4 Limits Min.	Typ.[1]	Max.	2102AL-2 Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
V_{PD}	V_{CC} in Standby	1.5			1.5			V	
V_{CES}[2]	$\overline{CE}$ Bias in Standby	2.0			2.0			V	2.0V ≤ V_{PD} ≤ V_{CC} Max.
		V_{PD}			V_{PD}			V	1.5V ≤ V_{PD} < 2.0V
I_{PD1}	Standby Current		15	23		20	28	mA	All Inputs = V_{PD1} = 1.5V
I_{PD2}	Standby Current		20	30		25	38	mA	All Inputs = V_{PD2} = 2.0V
t_{CP}	Chip Deselect to Standby Time	0			0			ns	
t_R[3]	Standby Recovery Time	t_{RC}			t_{RC}			ns	

STANDBY WAVEFORMS



NOTES:
1. Typical values are for T_A = 25°C.
2. Consider the test conditions as shown: If the standby voltage (V_{PD}) is between 5.25V (V_{CC} Max.) and 2.0V, then $\overline{CE}$ must be held at 2.0V Min. (V_{IH}). If the standby voltage is less than 2.0V but greater than 1.5V (V_{PD} Min.), then $\overline{CE}$ and standby voltage must be at least the same value or, if they are different, $\overline{CE}$ must be the more positive of the two.
3. t_R = t_{RC} (READ CYCLE TIME).

A. C. Characteristics T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified

READ CYCLE

Symbol	Parameter	2102A-2, 2102AL-2 Limits (ns) Min.	Max.	2102A, 2102AL Limits (ns) Min.	Max.	2102A-4, 2102AL-4 Limits (ns) Min.	Max.
t_{RC}	Read Cycle	250		350		450	
t_A	Access Time		250		350		450
t_{CO}	Chip Enable to Output Time		130		180		230
t_{OH1}	Previous Read Data Valid with Respect to Address	40		40		40	
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0		0		0	

WRITE CYCLE

t_{WC}	Write Cycle	250	350	450
t_{AW}	Address to Write Setup Time	20	20	20
t_{WP}	Write Pulse Width	180	250	300
t_{WR}	Write Recovery Time	0	0	0
t_{DW}	Data Setup Time	180	250	300
t_{DH}	Data Hold Time	0	0	0
t_{CW}	Chip Enable to Write Setup Time	180	250	300

A. C. CONDITIONS OF TEST

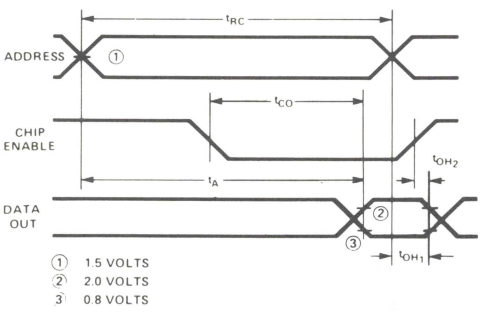
Input Pulse Levels:		0.8 Volt to 2.0 Volt
Input Rise and Fall Times:		10nsec
Timing Measurement Reference Levels	Inputs:	1.5 Volts
	Output:	0.8 and 2.0 Volts
Output Load:		1 TTL Gate and C_L = 100 pF

Capacitance[2] T_A = 25°C, f = 1 MHz

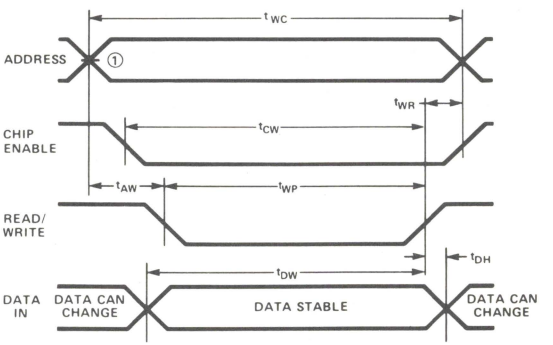
SYMBOL	TEST	LIMITS (pF) TYP.[1]	MAX.
C_{IN}	INPUT CAPACITANCE (ALL INPUT PINS) V_{IN} = 0V	3	5
C_{OUT}	OUTPUT CAPACITANCE V_{OUT} = 0V	7	10

Waveforms

READ CYCLE



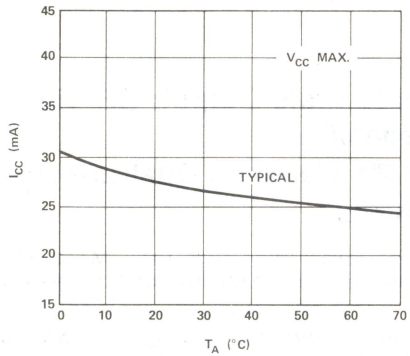
WRITE CYCLE



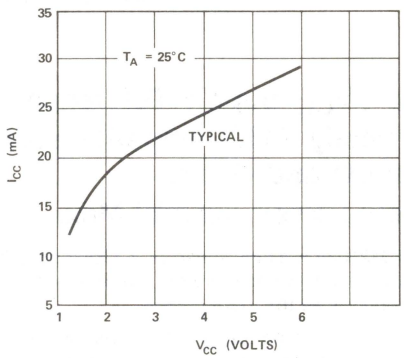
NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.

Typical D. C. and A. C. Characteristics

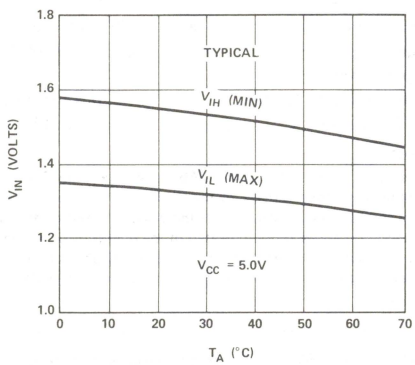
POWER SUPPLY CURRENT VS. AMBIENT TEMPERATURE



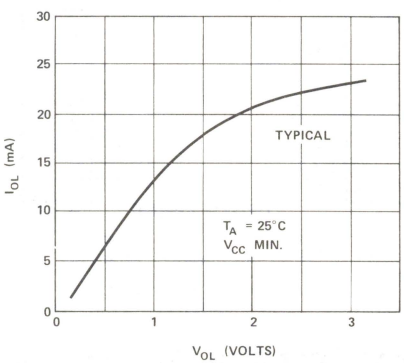
POWER SUPPLY CURRENT VS. SUPPLY VOLTAGE



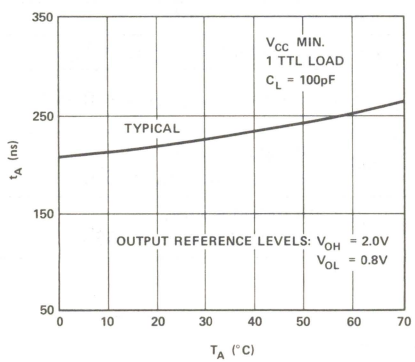
V_{IN} LIMITS VS. TEMPERATURE



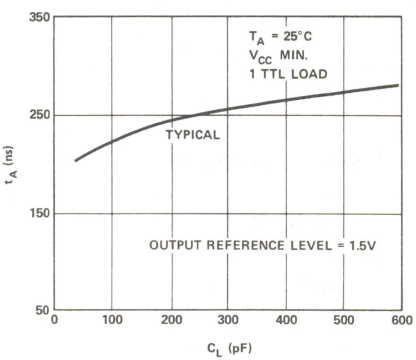
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



ACCESS TIME VS. AMBIENT TEMPERATURE



ACCESS TIME VS. LOAD CAPACITANCE



MILITARY TEMP.

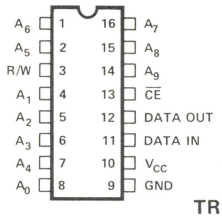
M2102A-4
1K x 1 BIT STATIC RAM

- 10% V_{CC} Supply Tolerance
- Directly TTL Compatible: All Inputs and Output
- Low Power: 385mW Max.
- Three State Output: OR-Tie Capability
- 16 Pin Hermetic Dual-In-Line Package

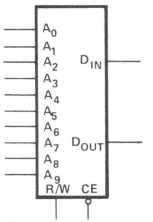
The Intel® M2102A is a high speed 1K x 1 RAM specified over the -55°C to +125°C temperature range. The RAM uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

The Intel® M2102A is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

PIN CONFIGURATION



LOGIC SYMBOL



TRUTH TABLE

$\overline{CE}$	R/W	D_{IN}	D_{OUT}	MODE
H	X	X	HIGH Z	NOT SELECTED
L	L	L	L	WRITE "0"
L	L	H	H	WRITE "1"
L	H	X	D_{OUT}	READ

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . −65°C to +135°C
Storage Temperature . . . . . −65°C to +150°C
Voltage On Any Pin
With Respect to Ground . . . . . −0.6V to +7V
Power Dissipation . . . . . 1 Watt

*COMMENT
Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics T_A = -55°C to +125°C, V_{CC} = 5V ± 10% unless otherwise specified

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[1]	Max.		
I_{LI}	Input Load Current			10	μA	V_{IN} = 0 to 5.5V
I_{LOH}	Output Leakage Current			10	μA	$\overline{CE}$ = Min. V_{IH} , V_{OUT} = V_{OH}
I_{LOL}	Output Leakage Current			−50	μA	$\overline{CE}$ = Min. V_{IH} , V_{OUT} = 0.45V
I_{CC1}	Power Supply Current		30	60	mA	All Inputs = 5.5V, Data Out Open, T_A = 25°C
I_{CC2}	Power Supply Current			70	mA	All Inputs = 5.5V, Data Out Open, T_A = -55°C
V_{IL}	Input "Low" Voltage	-0.5		0.8	V	
V_{IH}	Input "High" Voltage	2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output "High" Voltage	2.2			V	I_{OH} = −100 μA

NOTE 1. Typical values are for T_A = 25°C and nominal supply voltage.

A.C. Characteristics T_A = -55°C to +125°C, V_{CC} = 5V ± 10% unless otherwise specified

Symbol	Parameter	M2102A-4 Limits (ns) Min.	Max.
READ CYCLE			
t_{RC}	Read Cycle	450	
t_A	Access Time		450
t_{CO}	Chip Enable to Output Time		230
t_{OH1}	Previous Read Data Valid with Respect to Address	40	
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0	
WRITE CYCLE			
t_{WC}	Write Cycle	450	
t_{AW}	Address to Write Setup Time	20	
t_{WP}	Write Pulse Width	300	
t_{WR}	Write Recovery Time	0	
t_{DW}	Data Setup Time	300	
t_{DH}	Data Hold Time	0	
t_{CW}	Chip Enable to Write Setup Time	300	

A.C. CONDITIONS OF TEST

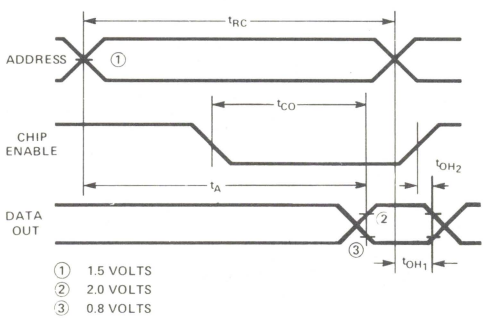
Input Pulse Levels:		0.8 Volt to 2.0 Volt
Input Rise and Fall Times:		10nsec
Timing Measurement Reference Levels	Inputs:	1.5 Volts
	Output:	0.8 and 2.0 Volts
Output Load:		1 TTL Gate and C_L = 100 pF

Capacitance[2] T_A = 25°C, f = 1MHz

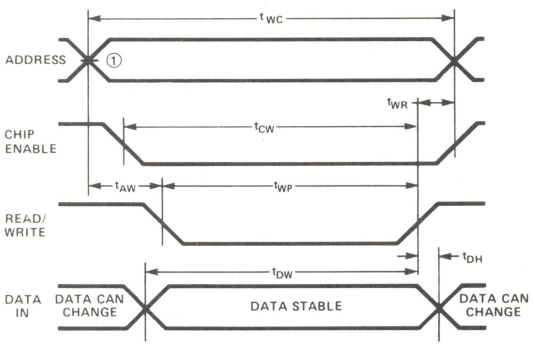
SYMBOL	TEST	LIMITS (pF) TYP.[1]	MAX.
C_{IN}	INPUT CAPACITANCE (ALL INPUT PINS) V_{IN} = 0V	3	5
C_{OUT}	OUTPUT CAPACITANCE V_{OUT} = 0V	7	10

Waveforms

READ CYCLE



WRITE CYCLE



NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.

2104A FAMILY
4096 x 1 BIT DYNAMIC RAM

	S6047	S6048	S6049	S6050
Max. Access Time (ns)	150	200	250	300
Read, Write Cycle (ns)	320	375	375	425
Max. IDD (mA)	35	32	30	30

- **Highest Density 4K RAM Industry Standard 16 Pin Package**
- **Low Power 4K RAM: 462mW Operating 27mW Standby**
- **All Inputs Including Clocks TTL Compatible**
- **±10% Tolerance on All Power Supplies +12V, +5V, -5V**
- **Refresh Period: 2 ms**
- **On-Chip Latches for Addresses, Chip Select and Data In**
- **Simple Memory Expansion: Chip Select**
- **Output is Three-State, TTL Compatible; Data is Latched and Valid into Next Cycle**
- **$\overline{RAS}$-Only Refresh Operation**

The Intel® 2104A is a 4096 word by 1 bit MOS RAM fabricated with N-channel silicon gate technology for high performance and high functional density.

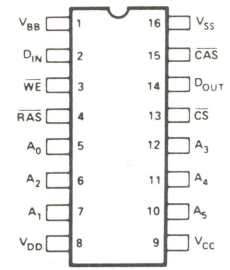
The efficient design of the 2104A allows it to be packaged in the industry standard 16 pin dual-in-line package. The 16 pin package provides the highest system bit densities and is compatible with widely available automated handling equipment.

The use of the 16 pin package is made possible by multiplexing the 12 address bits (required to address 1 of 4096 bits) into the 2104A on 6 address input pins. The two 6 bit address words are latched into the 2104A by the two TTL clocks, Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

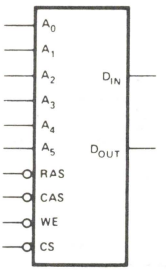
A new unique dynamic storage cell provides high speed along with low power dissipation and wide voltage margins. The memory cell requires refreshing for data retention. Refreshing is most easily accomplished by performing a $\overline{RAS}$-only refresh cycle or read cycle at each of the 64 row addresses every 2 milliseconds.

The 2104A is designed for page mode operation, $\overline{RAS}$-only refresh, and $\overline{CAS}$-only deselect.

PIN CONFIGURATION



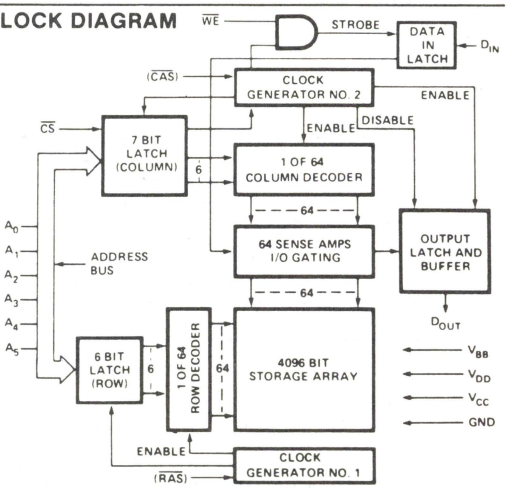
LOGIC DIAGRAM



PIN NAMES

A_0 - A_5	ADDRESS INPUTS	$\overline{WE}$	WRITE ENABLE
$\overline{CAS}$	COLUMN ADDRESS STROBE	V_{BB}	POWER (-5V)
$\overline{CS}$	CHIP SELECT	V_{CC}	POWER (+5V)
D_{IN}	DATA IN	V_{DD}	POWER (+12V)
D_{OUT}	DATA OUT	V_{SS}	GROUND
$\overline{RAS}$	ROW ADDRESS STROBE		

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . -10°C to +80°C
Storage Temperature . . . . . -65°C to +150°C
Voltage on any Pin Relative to V_{BB}
(V_{SS} - V_{BB} ≥ 4.5V) . . . . . -0.3V to +20V
Power Dissipation 1.0W
Data Out Current . . . . . 50 mA

COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS[1]

T_A = 0° to 70°C, V_{DD} = +12V ±10%, V_{CC} = +5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Limits			Unit	Conditions	
		Min.	Typ.[2]	Max.			
I_{LI}	Input Load Current (any input)			10	μA	V_{IN} = V_{SS} to $V_{IH\ MAX}$	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State			10	μA	Chip deselected: $\overline{RAS}$ and $\overline{CAS}$ at V_{IH} V_{OUT} = 0 to 5.5V	
I_{DD1}[3]	V_{DD} Standby Current		0.7	2	mA	V_{DD} = 13.2V	$\overline{CAS}$ and $\overline{RAS}$ at V_{IH}. Chip deselected prior to measurement. See Note 5.
			0.7	1.5	mA	V_{DD} = 12.6V	
I_{BB1}	V_{BB} Standby Current		5	50	μA	V_{DD} = 13.2V	
I_{DD2}[3]	Operating V_{DD} Current		24	35	mA	S6047	t_{RC} = $t_{RC\ MIN}$
			22	32	mA	S6048	t_{RC} = $t_{RC\ MIN}$
			20	30	mA	S6049, S6050	t_{RC} = $t_{RC\ MIN}$
I_{BB2}	Operating V_{BB} Current		130	325	μA	Min cycle time. T_A = 0°C	
I_{CC1}[4]	V_{CC} Supply Current when Deselected			10	μA		
I_{DD3}	Operating V_{DD} Current ($\overline{RAS}$-only cycle)		12	25	mA	S6047, S6048	t_{RC} = $t_{RC\ MIN}$
			10	22	mA	S6049, S6050	t_{RC} = $t_{RC\ MIN}$
V_{IL}	Input Low Voltage (any input)	-1.0		0.8	V		
V_{IH}	Input High Voltage (A_0-A_5, D_{IN}, $\overline{CS}$)	2.2		7.0	V		
V_{IHC}	Input High Voltage ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	2.4		7.0			
V_{OL}	Output Low Voltage	0.0		0.4	V	I_{OL} = 3.2 mA	
V_{OH}	Output High Voltage	2.4		V_{CC}	V	I_{OH} = -5 mA	

CAPACITANCE[6] T_A = 25°C

Symbol	Test	Typ.	Max.	Unit	Conditions
C_{I1}	Input Capacitance (A_0-A_5, D_{IN}, $\overline{CS}$)	3	7	pF	V_{IN} = V_{SS}
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{WRITE}$)	3	7	pF	V_{IN} = V_{SS}
C_O	Output Capacitance (D_{OUT})	4	7	pF	V_{OUT} = 0V
C_{I3}	Input Capacitance ($\overline{CAS}$)	6	7	pF	V_{IN} = V_{SS}

Notes:
1. All voltages referenced to V_{SS}. The only requirement for the sequence of applying voltages to the device is that V_{DD}, V_{CC}, and V_{SS} should never be 0.3V or more negative than V_{BB}. After the application of supply voltages or after extended periods of operation without clocks, the device must perform a minimum of one initialization cycle (any valid memory cycles containing both $\overline{RAS}$ and $\overline{CAS}$) prior to normal operation.
2. Typical values are for T_A = 25°C and nominal power supply voltages.
3. The I_{DD} current flows to V_{SS}.
4. When chip is selected V_{CC} supply current is dependent on output loading. V_{CC} is connected to output buffer only.
5. The chip is deselected; i.e., output is brought to high impedance state by $\overline{CAS}$-only cycle or by a read cycle with $\overline{CS}$ at V_{IH}.
6. Capacitance measured with Boonton Meter.

A.C.CHARACTERISTICS[1,2]

T_A=0°C to 70°C, V_{DD}=12V ±10%, V_{CC}=5V ±10%, V_{BB}=-5V ±10%, V_{SS}=0V, unless otherwise noted.

READ, WRITE, AND READ MODIFY WRITE CYCLES

Symbol	Parameter	S6047		S6048		S6049		S6050		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{REF}	Time Between Refresh		2		2		2		2	ms
t_{RP}	$\overline{RAS}$ Precharge Time	100		120		120		125		ns
t_{CP}	$\overline{CAS}$ Precharge Time	60		80		110		110		ns
t_{RCD}[3]	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	25	65	35	85	80	135	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	0		0		0		0		ns
t_{RSH}	$\overline{RAS}$ Hold Time	100		135		165		165		ns
t_{AR}	$\overline{RAS}$ to Address or $\overline{CS}$ Hold Time	95		120		160		215		ns
t_{ASR}	Row Address Set-Up Time	0		0		0		0		ns
t_{ASC}	Column Address or $\overline{CS}$ Set-Up Time	-10		-10		-10		-10		ns
t_{RAH}	Row Address Hold Time	20		25		35		80		ns
t_{CAH}	Column Address or $\overline{CS}$ Hold Time	45		55		75		80		ns
t_T	Rise or Fall Time	3	50	3	50	3	50	3	50	ns
t_{OFF}	Output Buffer Turn-Off Delay	0	50	0	60	0	60	0	80	ns
t_{CAC}[4,5]	Access Time From $\overline{CAS}$		100		135		165		165	ns
t_{RAC}[4]	Access Time From $\overline{RAS}$		150		200		250		300	ns

READ CYCLE

Symbol	Parameter	S6047		S6048		S6049		S6050		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Random Read or Write Cycle Time	320		375		375		425		ns
t_{RAS}	$\overline{RAS}$ Pulse Width	150	10000	200	10000	250	10000	300	10000	ns
t_{CAS}	$\overline{CAS}$ Pulse Width	100		135		165		165		ns
t_{RCS}	Read Command Set-Up Time	0		0		0		0		ns
t_{RCH}	Read Command Hold Time	0		0		0		0		ns
t_{DOH}	Data Out Hold Time	10		10		10		10		μs

WRITE CYCLE

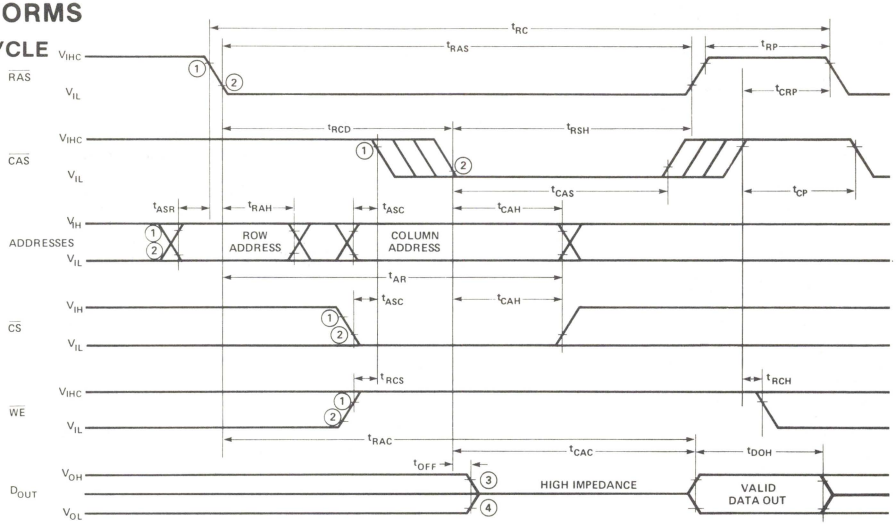
Symbol	Parameter	S6047		S6048		S6049		S6050		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Random Read or Write Cycle Time	320		375		375		425		ns
t_{RAS}	$\overline{RAS}$ Pulse Width	150	10000	200	10000	250	10000	300	10000	ns
t_{CAS}	$\overline{CAS}$ Pulse Width	100		135		165		165		ns
t_{WCS}[6]	Write Command Set-Up Time	0		0		0		0		ns
t_{WCH}	Write Command Hold Time	45		55		75		80		ns
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	95		120		160		215		ns
t_{WP}	Write Command Pulse Width	45		55		75		80		ns
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	50		70		85		130		ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	50		70		85		130		ns
t_{DS}	Data-In Set-Up Time	0		0		0		0		ns
t_{DH}	Data-In Hold Time	55		65		75		80		ns
t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	95		120		160		215		ns

NOTES:

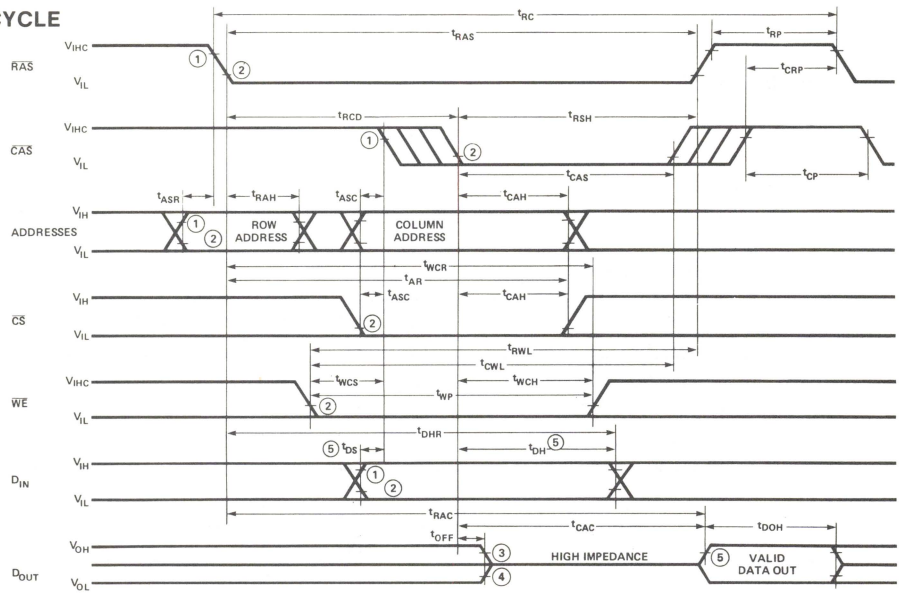
1. All voltages referenced to V_{SS}.
2. A.C. Characteristics assume t_T = 5ns.
3. $t_{RCD(MAX)}$ is specified as a reference point only; if $t_{RCD} \leq t_{RCD(MAX)}$ access time is t_{RAC}, if $t_{RCD} > t_{RCD(MAX)}$ access time is $t_{RCD} + t_{CAC}$.
4. Load = 2 TTL loads and 100pF.
5. Assumes $t_{RCD} \geq t_{RCD(MAX)}$.
6. In a write cycle with $t_{WCS} \geq t_{WCS(MIN)}$ the cycle is an early write cycle and D_{OUT} will be data written into the selected cell ($D_{OUT} = D_{IN}$). If $t_{CWD} \geq t_{CWD(MIN)}$ and $t_{RWD} \geq t_{RWD(MIN)}$ the cycle is a read-modify-write cycle and D_{OUT} will be data from the selected address read. If neither of the above conditions are satisfied, D_{OUT} is indeterminate.

WAVEFORMS

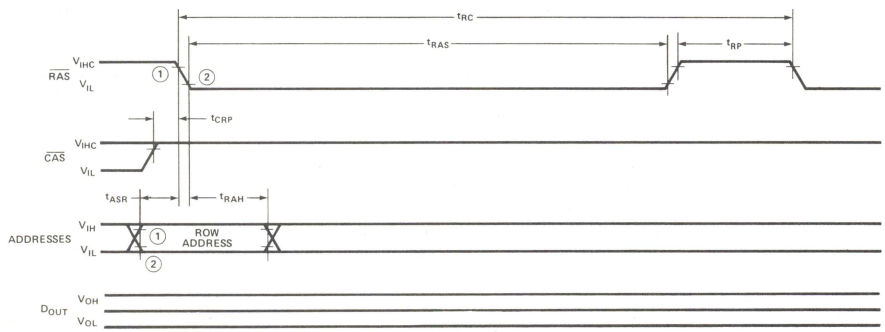
READ CYCLE



WRITE CYCLE



RAS-ONLY REFRESH CYCLE



(See next page for notes)

A.C.CHARACTERISTICS[7,8]

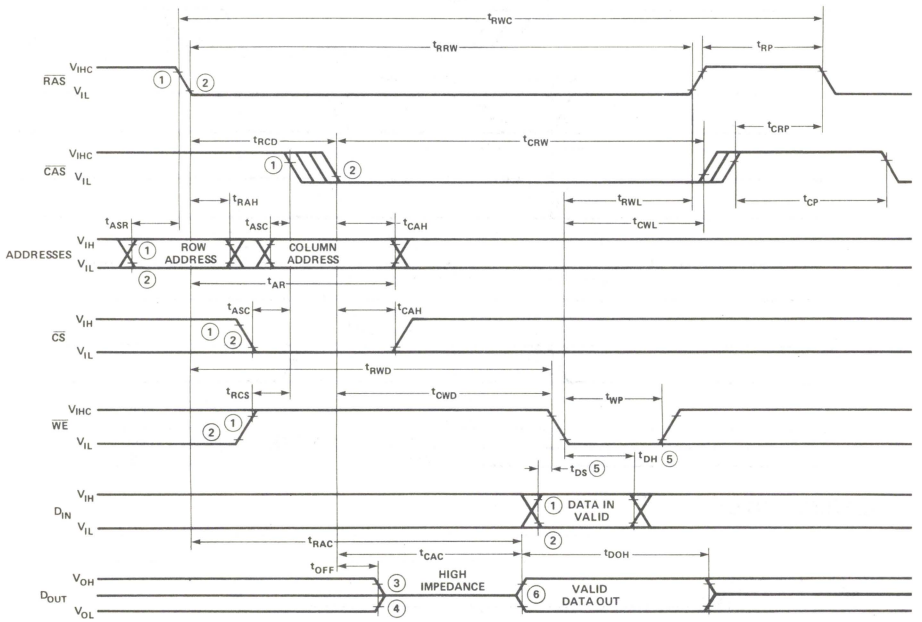
T_A = 0° to 70°C, V_{DD}=12V ±10%, V_{CC}=5V ±10%, V_{BB}=-5V ±10%, V_{SS}=0V, unless otherwise noted.

READ-MODIFY-WRITE CYCLE

Symbol	Parameter	S6047 Min.	S6047 Max.	S6048 Min.	S6048 Max.	S6049 Min.	S6049 Max.	S6050 Min.	S6050 Max.	Unit
t_{RWC}	Read Modify Write Cycle Time[2]	330		420		480		575		ns
t_{CRW}	RMW Cycle $\overline{CAS}$ Width	115		155		180		250		ns
t_{RRW}	RMW Cycle $\overline{RAS}$ Width	165	10,000	220	10,000	265	10,000	385	10,000	ns
t_{RWL}	RMW Cycle $\overline{RAS}$ Lead Time	50		70		85		130		ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	50		70		85		130		ns
t_{WP}	Write Command Pulse Width	45		55		75		80		ns
t_{RCS}	Read Command Set-Up Time	0		0		0		0		ns
t_{RWD}[6]	$\overline{RAS}$ to $\overline{WE}$ Delay	110		145		175		250		ns
t_{CWD}[6]	$\overline{CAS}$ to $\overline{WE}$ Delay	60		80		90		115		ns
t_{DS}	Data-In Set-Up Time	0		0		0		0		ns
t_{DH}	Data-In Hold Time	55		65		75		80		ns

WAVEFORMS

READ-MODIFY-WRITE CYCLE



Notes: 1,2. V_{IHMIN} or V_{IHCMIN} and V_{ILMAX} are reference levels for measuring timing of input signals.

3,4. V_{OHMIN} and V_{OLMAX} are reference levels for measuring timing of D_{OUT}.

5. Referenced to CAS or WE, whichever occurs last.

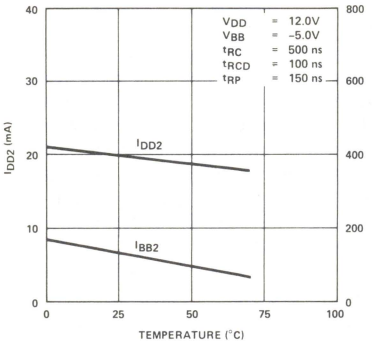
6. In a write cycle with $t_{WCS} \geq t_{WCS(MIN)}$ the cycle is an early write cycle and D_{OUT} will be data written into the selected cell ($D_{OUT} = D_{IN}$). If $t_{CWD} \geq t_{CWD(MIN)}$ and $t_{RWD} \geq t_{RWD(MIN)}$ the cycle is a read-modify-write cycle and D_{OUT} will be data from the selected address read. If neither of the above conditions are satisfied, D_{OUT} is indeterminate.

7. All voltages referenced to V_{SS}.

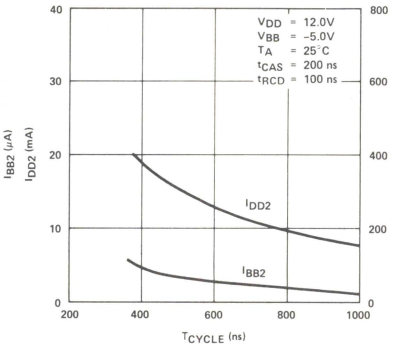
8. A.C. Characteristics assume t_T = 5ns.

TYPICAL CHARACTERISTICS

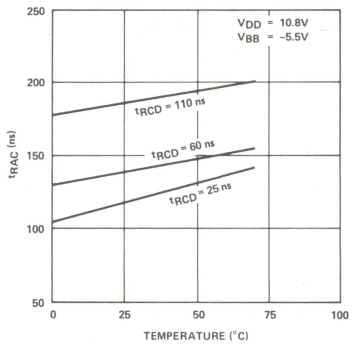
TYPICAL I_{BB2} AND I_{DD2} VS. TEMPERATURE



TYPICAL I_{BB2} AND I_{DD2} VS. CYCLE TIME



TYPICAL ACCESS TIME VS. TEMPERATURE



RAM

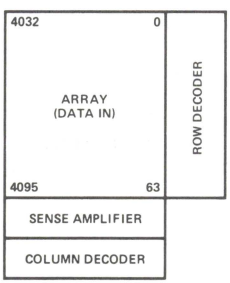
APPLICATIONS

ADDRESSING

Two externally applied negative going TTL clocks, Row Address Strobe ($\overline{RAS}$), and Column Address Strobe ($\overline{CAS}$), are used to strobe the two sets of 6 addresses into internal address buffer registers. The first clock, $\overline{RAS}$, strobes in the six low order addresses (A_0-A_5) which selects one of 64 rows and begins the timing which enables the column sense amplifiers. The second clock, $\overline{CAS}$, strobes in the six high order addresses (A_6-A_{11}) to select one of 64 column sense amplifiers and Chip Select ($\overline{CS}$) which enables the data out buffer.

An address map of the 2104A is shown below. Address "0" corresponds to all addresses at V_{IL}. All addresses are sequentially located on the chip.

2104A Address Map



DATA CYCLES/TIMING

A memory cycle begins with addresses stable and a negative transition of $\overline{RAS}$. See the waveforms on page 4. It is not necessary to know whether a Read or Write cycle is to be performed until $\overline{CAS}$ becomes valid.

Note that Chip Select ($\overline{CS}$) does not have to be valid until the second clock, $\overline{CAS}$. It is, therefore, possible to start a memory cycle before it is known which device must be selected. This can result in a significant improvement in system access time since the decode time for chip select does not enter into the calculation for access time.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks are TTL compatible and do not require level shifting and driving at high voltage MOS levels. Buffers internal to the 2104A convert the TTL level signals to MOS levels inside the device. Therefore, the delay associated with external TTL-MOS level converters is not added to the 2104A system access time.

READ CYCLE

A Read cycle is performed by maintaining Write Enable ($\overline{WE}$) high during $\overline{CAS}$. The output pin of a selected device will unconditionally go to a high impedance state immediately following the leading edge of $\overline{CAS}$ and remain in this state until valid data appears at the output at access time. The selected output data is internally latched and will remain valid for at least $t_{DOH\ MAX}$. A subsequent $\overline{CAS}$ must be given to the device either by a Read, Write, Read-Modify-Write, $\overline{CAS}$-only or $\overline{RAS}/\overline{CAS}$ refresh cycle.

Device access time, t_{ACC}, is the longer of two calculated intervals:

1. $t_{ACC} = t_{RAC}$ OR 2. $t_{ACC} = t_{RCD} + t_{CAC}$

Access time from $\overline{RAS}$, t_{RAC}, and access time from $\overline{CAS}$, t_{CAC}, are device parameters. $\overline{RAS}$ to $\overline{CAS}$ delay time, t_{RCD}, is a system dependent timing parameter. For example, substituting the device parameters to the S6050 yields:

3. $t_{ACC} = t_{RAC} = 300ns$ for $80nsec \leq t_{RCD} \leq 135nsec$

OR

4. $t_{ACC} = t_{RCD} + t_{CAC} = t_{RCD} + 165ns$ for $t_{RCD} > 135ns$.

Note that if 80nsec ≤ t_{RCD} ≤ 135nsec, device access time is determined by equation 3 and is equal to t_{RAC}. If t_{RCD} > 135ns, access time is determined by equation 4. This 55ns interval (shown in the t_{RCD} inequality in equation 3) in which the falling edge of $\overline{CAS}$ can occur without affecting access time is provided to allow for system timing skew in the generation of $\overline{CAS}$. This allowance for a t_{RCD} skew is designed in at the device level to allow minimum access times to be achieved in practical system designs.

WRITE CYCLE

A Write Cycle is generally performed by bringing Write Enable ($\overline{WE}$) low before $\overline{CAS}$. D_{OUT} will be the data written into the cell addressed. If $\overline{WE}$ goes low after $\overline{CAS}$ but t_{CWD} < $t_{CWD\ MIN}$ and t_{RWD} < $t_{RWD\ MIN}$, D_{OUT} will be indeterminate.

READ-MODIFY-WRITE CYCLE

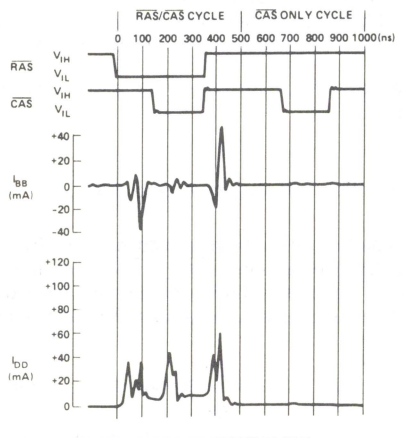
A Read-Modify-Write Cycle is performed by bringing Write Enable ($\overline{WE}$) low during a selected $\overline{RAS}$/$\overline{CAS}$ cycle with $t_{RWD} \geq t_{RWD\ MIN}$ and $t_{CWD} \geq t_{CWD\ MIN}$. Data in must be valid at or before the falling edge of $\overline{WE}$. In a read-modify-write cycle D_{OUT} is data read from the selected cell and does not change during the modify-write portion of the cycle.

$\overline{CAS}$ ONLY (DESELECT) CYCLE

In some applications, it is desirable to be able to deselect all memory devices without running a regular memory cycle. This may be accomplished with the 2104A by performing a $\overline{CAS}$-Only Cycle. Receipt of a $\overline{CAS}$ without $\overline{RAS}$ deselects the 2104A and forces the Data Output to the high-impedance state. This places the 2104A in its lowest power, standby condition. I_{DD} will be about twice I_{DD1} for the first cycle of $\overline{CAS}$-only deselection and I_{DD1} for any additional $\overline{CAS}$-only cycles. The cycle timing and $\overline{CAS}$ timing should be just as if a normal $\overline{RAS}$/$\overline{CAS}$ cycle was being performed.

CHIP SELECTION/DESELECTION

The 2104A is selected by driving $\overline{CS}$ low during a Read, Write, or Read-Modify-Write cycle. A device is deselected by 1) driving $\overline{CS}$ high during a Read, Write, or Read-Modify-Write cycle or 2) performing a $\overline{CAS}$ Only cycle independent of the state of $\overline{CS}$.



TYPICAL SUPPLY CURRENTS VS. TIME

REFRESH CYCLES

Each of the 64 rows internal to the 2104A must be refreshed every 2 msec to maintain data. Any cycle (Read, Write, Read-Modify-Write, $\overline{RAS}$-only refresh) refreshes the entire selected row (defined by the low order row addresses). The refresh operation is independent of the state of chip select. It is evident, of course, that if a Write or Read-Modify-Write cycle is used to refresh a row, the device should be deselected ($\overline{CS}$ high) if it is desired not to change the state of the selected cell.

$\overline{RAS}$/$\overline{CAS}$ TIMING

The device clocks, $\overline{RAS}$ and $\overline{CAS}$, control operation of the 2104A. The timing of each clock and the timing relationships of the two clocks must be understood by the user in order to obtain maximum performance in a memory system.

The $\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths as defined by t_{RAS} and t_{CAS} respectively. These minimum pulse widths must be maintained for proper device operation and data integrity. A cycle, once begun by driving $\overline{RAS}$ and/or $\overline{CAS}$ low must not be ended or aborted prior to fulfilling the minimum clock signal pulse width(s). A new cycle must not begin until the minimum precharge time, t_{RP}, has been met.

PAGE MODE OPERATION

The 2104A is designed for page mode operation. Product tested to page mode operating specifications are available upon request.

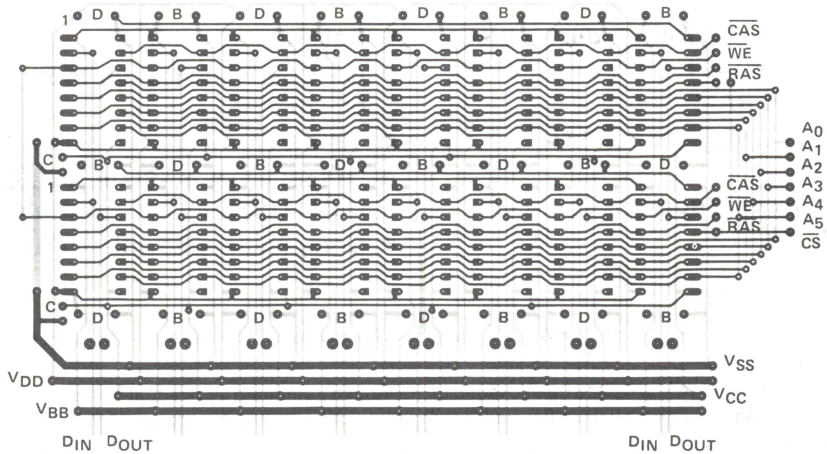
POWER SUPPLY

Typical power supply current waveforms versus time are shown below for both a $\overline{RAS}$/$\overline{CAS}$ cycle and a $\overline{CAS}$ only cycle. I_{DD} and I_{BB} current surges at $\overline{RAS}$ and $\overline{CAS}$ edges make adequate decoupling of these supplies important. Due to the high frequency noise component content of the current waveforms, the decoupling capacitors should be low inductance, ceramic units selected for their high frequency performance.

It is recommended that a 0.1 μF ceramic capacitor be connected between V_{DD} and V_{SS} at every other device in the memory array. A 0.1 μF ceramic capacitor should also be connected between V_{BB} and V_{SS} at every other device (preferably the alternate devices to the V_{DD} decoupling). For each 16 devices, a 10 μF tantalum or equivalent capacitor should be connected between V_{DD} and V_{SS} near the array. An equal or slightly smaller bulk capacitor is also recommended between V_{BB} and V_{SS} for every 32 devices.

A 0.01 μF ceramic capacitor is recommended between V_{CC} and V_{SS} at every eighth device to prevent noise coupling to the V_{CC} line which may affect the TTL peripheral logic in the system.

Due to the high frequency characteristics of the current waveforms, the inductance of the power supply distribution system on the array board should be minimized. It is recommended that the V_{DD}, V_{BB}, and V_{SS} supply lines be gridded both horizontally and vertically at each device in the array. This technique allows use of double-sided circuit boards with noise performance equal to or better than multi-layered circuit boards.



DECOUPLING CAPACITORS
D = 0.1 μF to V_{DD} TO V_{SS}
B = 0.1 μF V_{BB} TO V_{SS}
C = 0.01 μF V_{CC} TO V_{SS}

2104A FAMILY
4096 x 1 BIT DYNAMIC RAM

	2104A-1	2104A-2	2104A-3	2104A-4
Max. Access Time (ns)	150	200	250	300
Read, Write Cycle (ns)	320	320	375	425
Max. IDD (mA)	35	32	30	30

- **Highest Density 4K RAM Industry Standard 16 Pin Package**
- **Low Power 4K RAM**
- **All Inputs Including Clocks TTL Compatible**
- **Standard Power Supplies: +12V, +5V, -5V**
- **Refresh Period: 2 ms**
- **On-Chip Latches for Addresses, Chip Select and Data In**
- **Simple Memory Expansion: Chip Select**
- **Output is Three-State, TTL Compatible; Data is Latched and Valid into Next Cycle**
- **Compatible with Intel® 2116 16K RAM**

The Intel® 2104A is a 4096 word by 1 bit MOS RAM fabricated with N-channel silicon gate technology for high performance and high functional density.

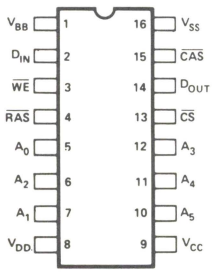
The efficient design of the 2104A allows it to be packaged in the industry standard 16 pin dual-in-line package. The 16 pin package provides the highest system bit densities and is compatible with widely available automated handling equipment.

The use of the 16 pin package is made possible by multiplexing the 12 address bits (required to address 1 of 4096 bits) into the 2104A on 6 address input pins. The two 6 bit address words are latched into the 2104A by the two TTL clocks, Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

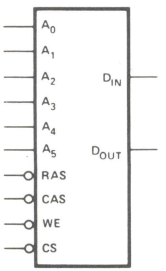
A new unique dynamic storage cell provides high speed along with low power dissipation and wide voltage margins. The memory cell requires refreshing for data retention. Refreshing is easily accomplished by performing any $\overline{RAS}/\overline{CAS}$ cycle with $\overline{CS}$ at V_{IH} for each of the 64 row addresses every 2 milliseconds.

The 2104A is designed for $\overline{CAS}$-only deselect and is compatible with Intel® 2116, 16K RAM.

PIN CONFIGURATION



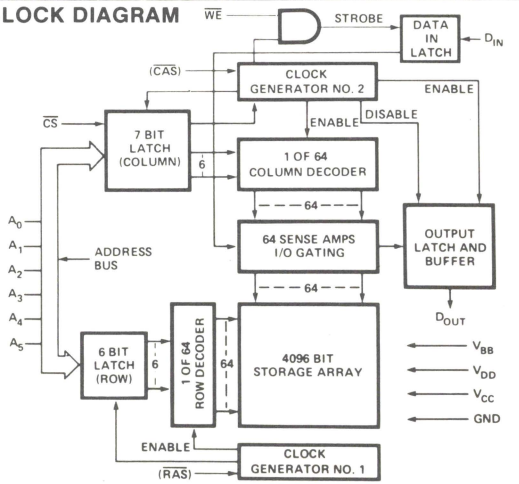
LOGIC DIAGRAM



PIN NAMES

$A_0 - A_5$	ADDRESS INPUTS	$\overline{WE}$	WRITE ENABLE
$\overline{CAS}$	COLUMN ADDRESS STROBE	V_{BB}	POWER (-5V)
$\overline{CS}$	CHIP SELECT	V_{CC}	POWER (+5V)
D_{IN}	DATA IN	V_{DD}	POWER (+12V)
D_{OUT}	DATA OUT	V_{SS}	GROUND
$\overline{RAS}$	ROW ADDRESS STROBE		

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . -10°C to +80°C
Storage Temperature . . . . . -65°C to +150°C
Voltage on any Pin Relative to V_{BB}
(V_{SS} - V_{BB} ≥ 4.5V) . . . . . -0.3V to +20V
Power Dissipation 1.0W
Data Out Current . . . . . 50 mA

COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS[1]

T_A = 0° to 70°C, V_{DD} = +12V ±10%, V_{CC} = +5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Limits			Unit	Conditions	
		Min.	Typ.(2)	Max.			
I_{LI}	Input Load Current (any input)			10	µA	V_{IN} = $V_{IL\ MIN}$ to $V_{IH\ MAX}$	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State			10	µA	Chip deselected: $\overline{RAS}$ and $\overline{CAS}$ at V_{IH} V_{OUT} = 0 to 5.5V	
I_{DD1}[3]	V_{DD} Standby Current		0.7	2	mA	V_{DD} = 13.2V	$\overline{CAS}$ and $\overline{RAS}$ at V_{IH}. Chip deselected prior to measurement. See Note 5.
			0.7	1.5	mA	V_{DD} = 12.6V	
I_{BB1}	V_{BB} Standby Current		5	50	µA	V_{DD} = 13.2V	
I_{DD2}[3]	Operating V_{DD} Current		24	35	mA	2104A-1	t_{RC} = 320 ns
			22	32	mA	2104A-2	t_{RC} = 320 ns
			20	30	mA	2104A-3, 4	t_{RC} = 375 ns
I_{BB2}	Operating V_{BB} Current		130	325	µA	Min. cycle time. T_A = 0°C	
I_{CC1}[4]	V_{CC} Supply Current when Deselected			10	µA		
V_{IL}	Input Low Voltage (any input)	-1.0		0.8	V		
V_{IH}	Input High Voltage	2.4		7.0	V		
V_{OL}	Output Low Voltage	0.0		0.4	V	I_{OL} = 3.2 mA	
V_{OH}	Output High Voltage	2.4		V_{CC}	V	I_{OH} = -5 mA	

CAPACITANCE[6] T_A = 25°C

Symbol	Test	Typ.	Max.	Unit	Conditions
C_{I1}	Input Capacitance (A_0-A_5), D_{IN}, $\overline{CS}$	3	7	pF	V_{IN} = V_{SS}
C_{I2}	Input Capacitance $\overline{RAS}$, $\overline{WRITE}$	3	7	pF	V_{IN} = V_{SS}
C_O	Output Capacitance (D_{OUT})	4	7	pF	V_{OUT} = 0V
C_{I3}	Input Capacitance $\overline{CAS}$	6	7	pF	V_{IN} = V_{SS}

Notes: 1. All voltages referenced to V_{SS}. The only requirement for the sequence of applying voltages to the device is that V_{DD}, V_{CC}, and V_{SS} should never be 0.3V or more negative than V_{BB}. After the application of supply voltages or after extended periods of operation without clocks, the device must perform a minimum of one initialization cycle (any valid memory cycles containing both $\overline{RAS}$ and $\overline{CAS}$) prior to normal operation.
2. Typical values are for T_A = 25°C and nominal power supply voltages.
3. The I_{DD} current flows to V_{SS}.
4. When chip is selected V_{CC} supply current is dependent on output loading. V_{CC} is connected to output buffer only.
5. The chip is deselected; i.e., output is brought to high impedance state by $\overline{CAS}$-only cycle or by a read cycle with $\overline{CS}$ at V_{IH}.
6. Capacitance measured with Boonton Meter.

A.C.CHARACTERISTICS[1]

T_A=0°C to 70°C, V_{DD}=12V ±10%, V_{CC}=5V ±10%, V_{BB}=-5V ±10%, V_{SS}=0V, unless otherwise noted.

READ, WRITE, AND READ MODIFY WRITE CYCLES

Symbol	Parameter	2104A-1		2104A-2		2104A-3		2104A-4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{REF}	Time Between Refresh		2		2		2		2	ms
t_{RP}	$\overline{RAS}$ Precharge Time	100		115		115		125		ns
t_{CP}	$\overline{CAS}$ Precharge Time	60		80		110		110		ns
t_{RCL}[2]	$\overline{RAS}$ to $\overline{CAS}$ Leading Edge Lead Time	20	50	25	70	35	110	80	135	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	0		0		0		0		ns
t_{RSH}	$\overline{RAS}$ Hold Time	100		130		140		165		ns
t_{CSH}	$\overline{CAS}$ Hold Time	150		200		250		300		ns
t_{AR}	$\overline{RAS}$ to Address or $\overline{CS}$ Hold Time	95		120		160		215		ns
t_{ASR}	Row Address Set-Up Time	0		0		0		0		ns
t_{ASC}	Column Address or $\overline{CS}$ Set-Up Time	-5		0		0		0		ns
t_{RAH}	Row Address Hold Time	20		25		35		80		ns
t_{CAH}	Column Address or $\overline{CS}$ Hold Time	45		50		50		80		ns
t_T	Rise or Fall Time	3	50	3	50	3	50	3	50	ns
t_{OFF}	Output Buffer Turn-Off Delay	0	50	0	60	0	60	0	80	ns
t_{CAC}[3]	Access Time From $\overline{CAS}$		100		130		140		165	ns
t_{RAC}[3]	Access Time From $\overline{RAS}$		150		200		250		300	ns

READ CYCLE

Symbol	Parameter	2104A-1		2104A-2		2104A-3		2104A-4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Random Read or Write Cycle Time	320		320		375		425		ns
t_{RAS}	$\overline{RAS}$ Pulse Width	150	32000	200	32000	250	32000	300	32000	ns
t_{CAS}	$\overline{CAS}$ Pulse Width	100		130		140		165		ns
t_{RCS}	Read Command Set-Up Time	0		0		0		0		ns
t_{RCH}	Read Command Hold Time	0		0		0		0		ns
t_{DOH}	Data Out Hold Time	32		32		32		32		μs

WRITE CYCLE[4]

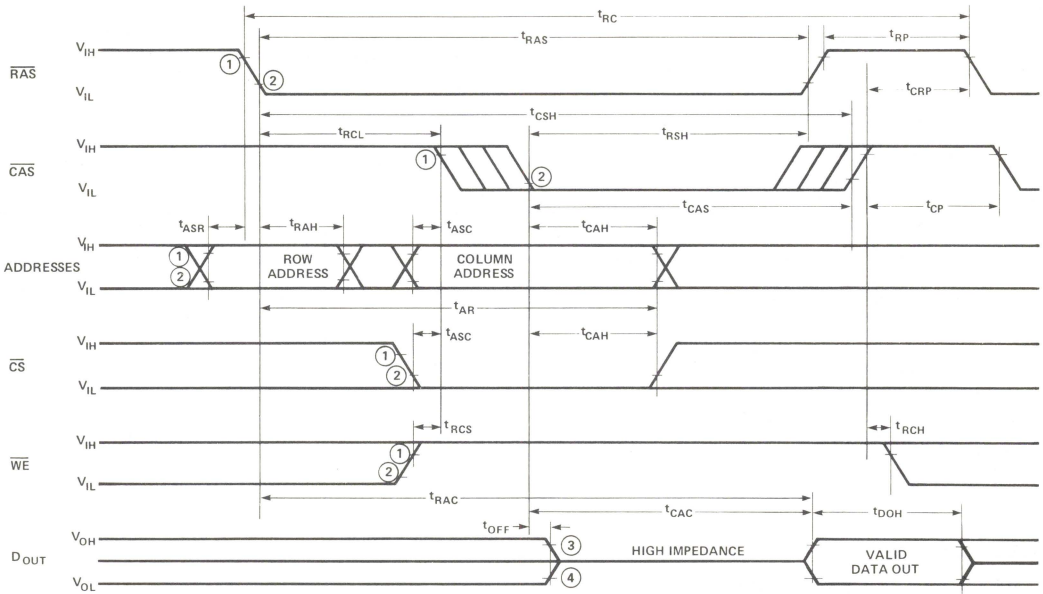
Symbol	Parameter	2104A-1		2104A-2		2104A-3		2104A-4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Random Read or Write Cycle Time	320		320		375		425		ns
t_{RAS}	$\overline{RAS}$ Pulse Width	150	32000	200	32000	250	32000	300	32000	ns
t_{CAS}	$\overline{CAS}$ Pulse Width	100		130		140		165		ns
t_{WCS}	Write Command Set-Up Time	0		0		0		0		ns
t_{WCH}	Write Command Hold Time	55		75		75		80		ns
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	105		145		185		215		ns
t_{WP}	Write Command Pulse Width	45		55		75		80		ns
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	100		130		140		150		ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	100		130		140		150		ns
t_{DS}	Data-In Set-Up Time	0		0		0		0		ns
t_{DH}	Data-In Hold Time	55		75		75		80		ns
t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	105		145		185		215		ns

Notes:

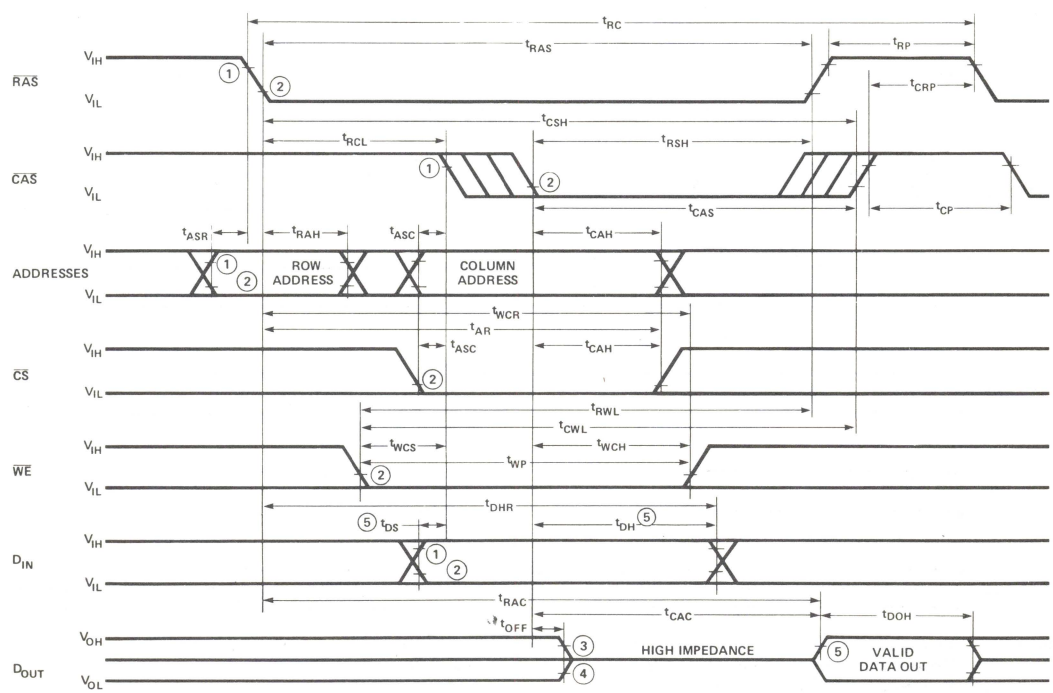
1. All voltages referenced to V_{SS}. Minimum timings do not allow for t_T or skews.
2. $\overline{CAS}$ must remain at V_{IH} a minimum of $t_{RCL\ MIN}$ after RAS switches to V_{IL}. To achieve the minimum guaranteed access time (t_{RAC}), $\overline{CAS}$ must switch to V_{IL} at or before t_{RCL} of $t_{RAC} - t_T - t_{CAC}$ as described in the Applications Information section. $t_{RCL\ MAX}$ is given for reference only as $t_{RAC} - t_{CAC}$.
3. Load = 2 TTL and 100 pF. See Applications Information.
4. In a write cycle D_{OUT} latch will contain data written into cell. In a read-modify-write cycle D_{OUT} latch will contain data read from cell. If $\overline{WE}$ goes low after $\overline{CAS}$ and prior to t_{CAC}, D_{OUT} is indeterminate.

WAVEFORMS

READ CYCLE



WRITE CYCLE



(See next page for notes)

A.C.CHARACTERISTICS[1]

T_A = 0° to 70°C, V_{DD}=12V ±10%, V_{CC}=5V ±10%, V_{BB}=-5V ±10%, V_{SS}=0V, unless otherwise noted.

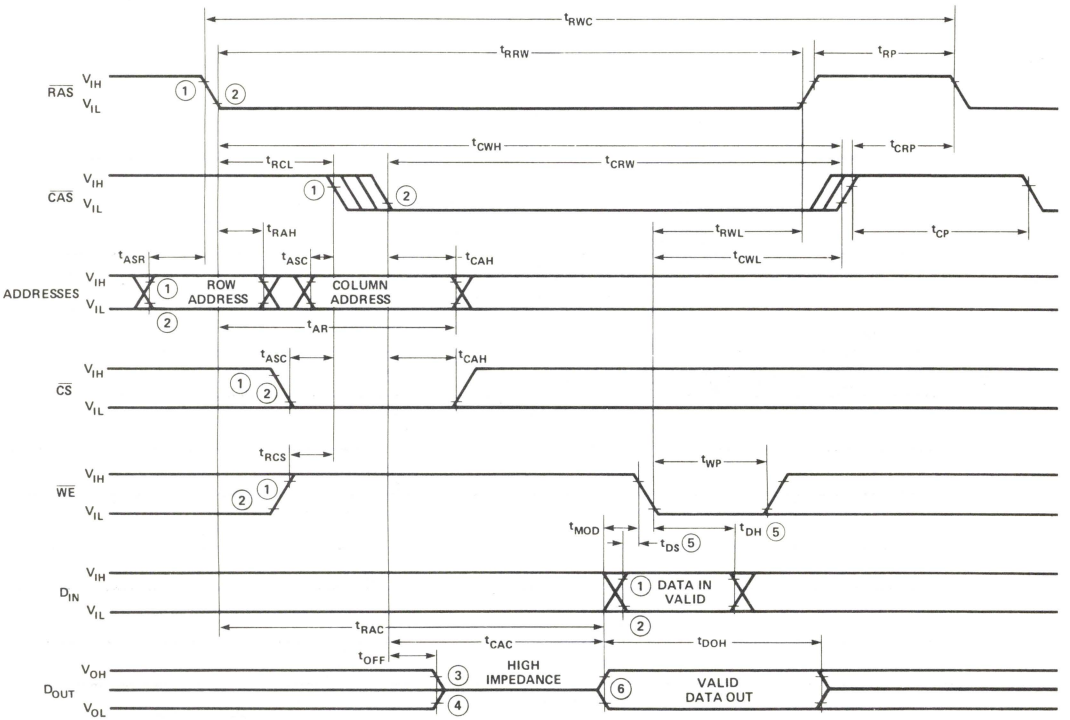
READ-MODIFY-WRITE CYCLE

Symbol	Parameter	2104A-1		2104A-2		2104A-3		2104A-4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RWC}	Read Modify Write Cycle Time[2]	350		445		505		575		ns
t_{CRW}	RMW Cycle $\overline{CAS}$ Width	200		260		280		315		ns
t_{RRW}	RMW Cycle $\overline{RAS}$ Width	250	32,000	330	32,000	390	32,000	450	32,000	ns
t_{RWL}	RMW Cycle $\overline{RAS}$ Lead Time	100		130		140		150		ns
t_{CWH}	RMW Cycle $\overline{CAS}$ Hold Time	250		330		390		450		ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	100		130		140		150		ns
t_{WP}	Write Command Pulse Width	45		55		75		80		ns
t_{RCS}	Read Command Set-Up Time	0		0		0		0		ns
t_{MOD}	Modify Time	0	10	0	10	0	10	0	10	μs
t_{DS}	Data-In Set-Up Time	0		0		0		0		ns
t_{DH}	Data-In Hold Time	55		75		75		80		ns

Notes: 1. All voltages referenced to V_{SS}.
2. The minimum cycle timing does not allow for t_T or skews.

WAVEFORMS

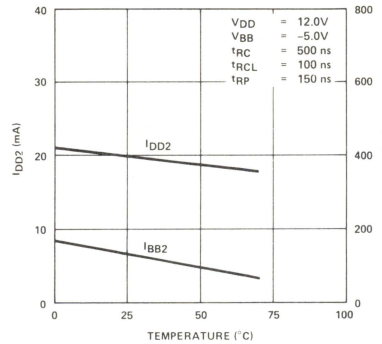
READ-MODIFY-WRITE CYCLE



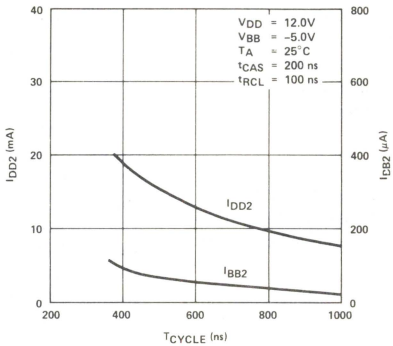
Notes: 1,2. V_{IHMIN} and V_{ILMAX} are reference levels for measuring timing of input signals.
3,4. V_{OHMIN} and V_{OLMAX} are reference levels for measuring timing of D_{OUT}.
5. Referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.
6. In a write cycle D_{OUT} latch will contain data written into cell. In a read-modify-write cycle D_{OUT} latch will contain data read from cell. If $\overline{WE}$ goes low after $\overline{CAS}$ and prior to t_{CAC}, D_{OUT} is indeterminate.

TYPICAL CHARACTERISTICS

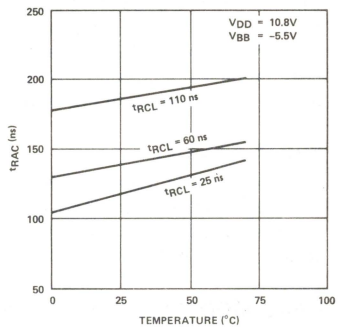
TYPICAL I_{BB2} AND I_{DD2} VS. TEMPERATURE



TYPICAL I_{BB2} AND I_{DD2} VS. CYCLE TIME



TYPICAL ACCESS TIME VS. TEMPERATURE



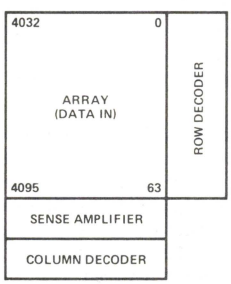
APPLICATIONS

ADDRESSING

Two externally applied negative going TTL clocks, Row Address Strobe ($\overline{RAS}$), and Column Address Strobe ($\overline{CAS}$), are used to strobe the two sets of 6 addresses into internal address buffer registers. The first clock, $\overline{RAS}$, strobes in the six low order addresses (A_0-A_5) which selects one of 64 rows and begins the timing which enables the column sense amplifiers. The second clock, $\overline{CAS}$, strobes in the six high order addresses (A_6-A_{11}) to select one of 64 column sense amplifiers and Chip Select ($\overline{CS}$) which enables the data out buffer.

An address map of the 2104A is shown below. Address "0"` corresponds to all addresses at V_{IL}. All addresses are sequentially located on the chip.

2104A Address Map



DATA CYCLES/TIMING

A memory cycle begins with addresses stable and a negative transition of $\overline{RAS}$. See the waveforms on page 4. It is not necessary to know whether a Read or Write cycle is to be performed until $\overline{CAS}$ becomes valid.

Note that Chip Select ($\overline{CS}$) does not have to be valid until the second clock, $\overline{CAS}$. It is, therefore, possible to start a memory cycle before it is known which device must be selected. This can result in a significant improvement in system access time since the decode time for chip select does not enter into the calculation for access time.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks are TTL compatible and do not require level shifting and driving at high voltage MOS levels. Buffers internal to the 2104A convert the TTL level signals to MOS levels inside the device. Therefore, the delay associated with external TTL-MOS level converters is not added to the 2104A system access time.

READ CYCLE

A Read cycle is performed by maintaining Write Enable ($\overline{WE}$) high during $\overline{CAS}$. The output pin of a selected device will unconditionally go to a high impedance state immediately following the leading edge of $\overline{CAS}$ and remain in this state until valid data appears at the output at access time. The selected output data is internally latched and will remain valid until a subsequent $\overline{CAS}$ is given to the device by a Read, Write, Read-Modify-Write, $\overline{CAS}$ only or Refresh cycle. Data-out goes to a high impedance state for all non-selected devices.

Device access time, t_{ACC}, is the longer of two calculated intervals:

1. $t_{ACC} = t_{RAC}$ OR 2. $t_{ACC} = t_{RCL} + t_T + t_{CAC}$

Access time from $\overline{RAS}$, t_{RAC}, and access time from $\overline{CAS}$, t_{CAC}, are device parameters. Row to column address strobe lead time, t_{RCL}, and transition time, t_T, are system dependent timing parameters. For example, substituting the device parameters of the 2104A-2 and assuming a TTL level transition time of 5ns yields:

3. $t_{ACC} = t_{RAC} = 200ns$ for $25nsec \leq t_{RCL} \leq 70nsec$
   OR
4. $t_{ACC} = t_{RCL} + t_T + t_{CAC} = t_{RCL} + 135ns$ for $t_{RCL} > 70ns$.

Note that if 25 nsec $\leq t_{RCL} \leq$ 70 nsec, device access time is determined by equation 3 and is equal to t_{RAC}. If $t_{RCL} >$ 70 nsec, access time is determined by equation 4. This 45ns interval (shown in the t_{RCL} inequality in equation 3) in which the failing edge of $\overline{CAS}$ can occur without affecting access time is provided to allow for system timing skew in the generation of $\overline{CAS}$. This allowance for a t_{RCL} skew is designed in at the device level to allow minimum access times to be achieved in practical designs.

WRITE CYCLE

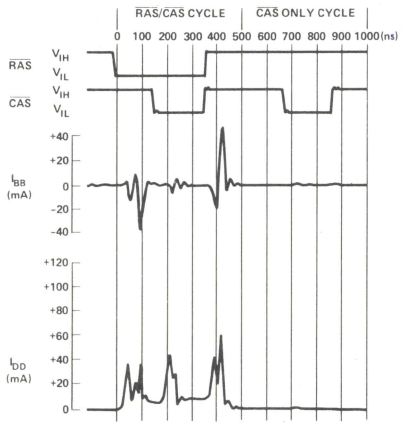
A Write Cycle is generally performed by bringing Write Enable ($\overline{WE}$) low before $\overline{CAS}$. D_{OUT} will be the data written into the cell addressed. If $\overline{WE}$ goes low after $\overline{CAS}$ and prior to t_{CAC}, D_{OUT} will be indeterminate.

READ-MODIFY-WRITE CYCLE

A Read-Modify-Write Cycle is performed by bringing Write Enable ($\overline{WE}$) low after access time, t_{RAC}, with $\overline{RAS}$ and $\overline{CAS}$ low. Data in must be valid at or before the falling edge of $\overline{WE}$. In a read-modify-write cycle D_{OUT} is data read and does not change during the modify-write portion of the cycle.

$\overline{CAS}$ ONLY (DESELECT) CYCLE

In some applications, it is desirable to be able to deselect all memory devices without running a regular memory cycle. This may be accomplished with the 2104A by performing a $\overline{CAS}$-Only Cycle. Receipt of a $\overline{CAS}$ without $\overline{RAS}$ deselects the 2104A and forces the Data Output to the high-impedance state. This places the 2104A in its lowest power, standby condition. I_{DD} will be about twice I_{DD1} for the first cycle of $\overline{CAS}$-only deselection and I_{DD1} for any additional $\overline{CAS}$-only cycles. The cycle timing and $\overline{CAS}$ timing should be just as if a normal $\overline{RAS}/\overline{CAS}$ cycle was being performed.



TYPICAL SUPPLY CURRENTS VS. TIME

CHIP SELECTION/DESELECTION

The 2104A is selected by driving $\overline{CS}$ low during a Read, Write, or Read-Modify-Write cycle. A device is deselected by 1) driving $\overline{CS}$ high during a Read, Write, or Read-Modify-Write cycle or 2) performing a $\overline{CAS}$ Only cycle independent of the state of $\overline{CS}$.

REFRESH CYCLES

Each of the 64 rows internal to the 2104A must be refreshed every 2 msec to maintain data. Any data cycle (Read, Write, Read-Modify-Write) refreshes the entire selected row (defined by the low order row addresses). The refresh operation is independent of the state of chip select. It is evident, of course, that if a Write or Read-Modify-Write cycle is used to refresh a row, the device should be deselected ($\overline{CS}$ high) if it is desired not to change the state of the selected cell.

$\overline{RAS}/\overline{CAS}$ TIMING

The device clocks, $\overline{RAS}$ and $\overline{CAS}$, control operation of the 2104A. The timing of each clock and the timing relationships of the two clocks must be understood by the user in order to obtain maximum performance in a memory system.

The $\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths as defined by t_{RAS} and t_{CAS} respectively. These minimum pulse widths must be maintained for proper device operation and data integrity. A cycle, once begun by driving $\overline{RAS}$ and/or $\overline{CAS}$ low must not be ended or aborted prior to fulfilling the minimum clock signal pulse width(s). A new cycle must not begin until the minimum precharge time, t_{RP}, has been met.

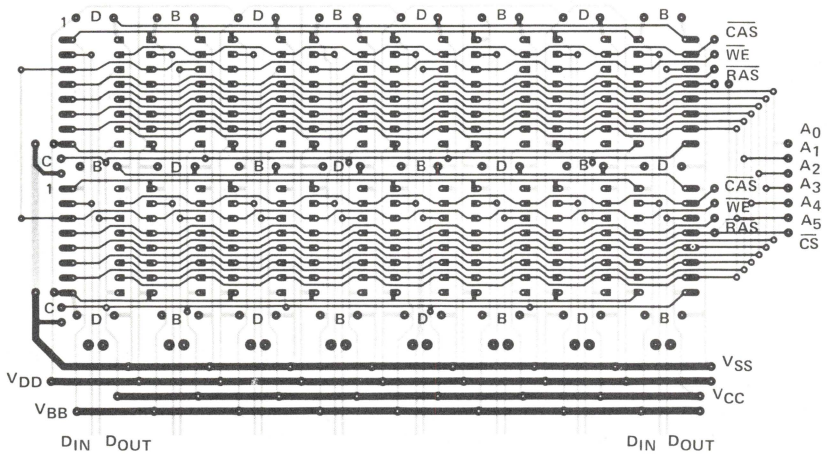
POWER SUPPLY

Typical power supply current waveforms versus time are shown below for both a $\overline{RAS}/\overline{CAS}$ cycle and a $\overline{CAS}$ only cycle. I_{DD} and I_{BB} current surges at $\overline{RAS}$ and $\overline{CAS}$ edges make adequate decoupling of these supplies important. Due to the high frequency noise component content of the current waveforms, the decoupling capacitors should be low inductance, ceramic units selected for their high frequency performance.

It is recommended that a 0.1 μF ceramic capacitor be connected between V_{DD} and V_{SS} at every other device in the memory array. A 0.1 μF ceramic capacitor should also be connected between V_{BB} and V_{SS} at every other device (preferably the alternate devices to the V_{DD} decoupling). For each 16 devices, a 10 μF tantalum or equivalent capacitor should be connected between V_{DD} and V_{SS} near the array. An equal or slightly smaller bulk capacitor is also recommended between V_{BB} and V_{SS} for every 32 devices.

A 0.01 μF ceramic capacitor is recommended between V_{CC} and V_{SS} at every eighth device to prevent noise coupling to the V_{CC} line which may affect the TTL peripheral logic in the system.

Due to the high frequency characteristics of the current waveforms, the inductance of the power supply distribution system on the array board should be minimized. It is recommended that the V_{DD}, V_{BB}, and V_{SS} supply lines be gridded both horizontally and vertically at each device in the array. This technique allows use of double-sided circuit boards with noise performance equal to or better than multi-layered circuit boards.



DECOUPLING CAPACITORS
D = 0.1 μF to V_{DD} TO V_{SS}
B = 0.1 μF V_{BB} TO V_{SS}
C = 0.01 μF V_{CC} TO V_{SS}

2104A
4096 x 1 BIT DYNAMIC RAM

	2104A
Max. Access Time (ns)	350
Read, Write Cycle (ns)	500
Max. IDD (mA)	35

- **Highest Density 4K RAM Industry Standard 16 Pin Package**
- **Low Power 4K RAM**
- **All Inputs Including Clocks TTL Compatible**
- **Standard Power Supplies: +12V, +5V, -5V**
- **Refresh Period: 2 ms**
- **On-Chip Latches for Addresses, Chip Select and Data In**
- **Simple Memory Expansion: Chip Select**
- **Output is Three-State, TTL Compatible; Data is Latched and Valid into Next Cycle**
- **Compatible with Intel® 2116 16K RAM**

The Intel® 2104A is a 4096 word by 1 bit MOS RAM fabricated with N-channel silicon gate technology for high performance and high functional density.

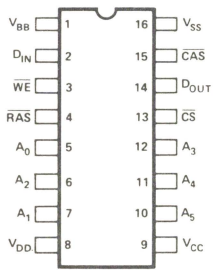
The efficient design of the 2104A allows it to be packaged in the industry standard 16 pin dual-in-line package. The 16 pin package provides the highest system bit densities and is compatible with widely available automated handling equipment.

The use of the 16 pin package is made possible by multiplexing the 12 address bits (required to address 1 of 4096 bits) into the 2104A on 6 address input pins. The two 6 bit address words are latched into the 2104A by the two TTL clocks, Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

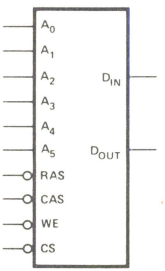
A new unique dynamic storage cell provides high speed along with low power dissipation and wide voltage margins. The memory cell requires refreshing for data retention. Refreshing is easily accomplished by performing any $\overline{RAS}/\overline{CAS}$ cycle with $\overline{CS}$ at V_{IH} for each of the 64 row addresses every 2 milliseconds.

The 2104A is designed for $\overline{CAS}$-only deselect and is compatible with Intel® 2116, 16K RAM.

PIN CONFIGURATION



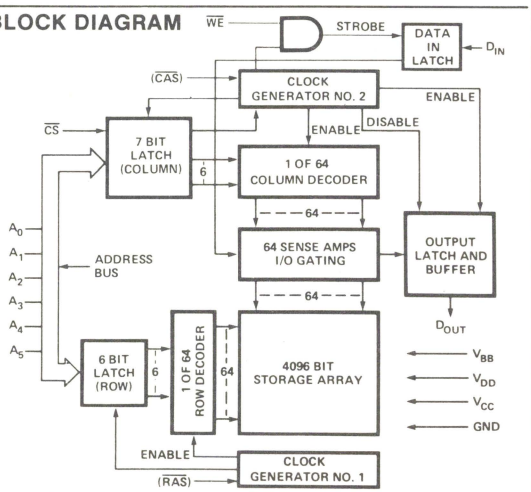
LOGIC DIAGRAM



PIN NAMES

A_0 - A_5	ADDRESS INPUTS	$\overline{WE}$	WRITE ENABLE
$\overline{CAS}$	COLUMN ADDRESS STROBE	V_{BB}	POWER (-5V)
$\overline{CS}$	CHIP SELECT	V_{CC}	POWER (+5V)
D_{IN}	DATA IN	V_{DD}	POWER (+12V)
D_{OUT}	DATA OUT	V_{SS}	GROUND
$\overline{RAS}$	ROW ADDRESS STROBE		

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... -10°C to +80°C
Storage Temperature ..... -65°C to +150°C
Voltage on any Pin Relative to V_{BB}
(V_{SS} - V_{BB} ⩾ 4.5V) ..... -0.3V to +20V
Power Dissipation 1.0W
Data Out Current ..... 50 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS[1]

T_A = 0°C to 70°C, V_{DD} = +12V ±5%, V_{CC} = +5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[2]	Max.		
I_{LI}	Input Load Current (Any Input)			10	μA	V_{IN} = $V_{IL\ MIN}$ to $V_{IH\ MAX}$
$\|I_{LO}\|$	Output Leakage Current for High Impedance State			10	μA	Chip Deselected: $\overline{RAS}$ and $\overline{CAS}$ at V_{IH} V_{OUT} = 0 to 5.5V
I_{DD1}[3]	V_{DD} Standby Current		0.7	2	mA	V_{DD} = 12.6V, $\overline{CAS}$ and $\overline{RAS}$ at V_{IH}.
I_{BB1}	V_{BB} Standby Current		5	50	μA	Chip Deselected Prior to Measurement. See Note 5.
I_{DD2}[3]	Operating V_{DD} Current		25	35	mA	t_{CYC} = 500 ns
I_{BB2}	Operating V_{BB} Current		130	400	μA	t_{RC} = 500ns, T_A = 0°C
I_{CC1}[4]	V_{CC} Supply Current When Deselected			10	μA	
V_{IL}	Input Low Voltage (Any Input)	-1.0		0.8	V	
V_{IH}	Input High Voltage	2.4		7.0	V	
V_{OL}	Output Low Voltage	0.0		0.4	V	I_{OL} = 2.0mA
V_{OH}	Output High Voltage	2.4		V_{CC}	V	I_{OH} = -5 mA

CAPACITANCE[6] T_A = 25°C

Symbol	Test	Typ.	Max.	Unit	Conditions
C_{I1}	Input Capacitance (A_0-A_5), D_{IN}, $\overline{CS}$	3	7	pF	V_{IN} = V_{SS}
C_{I2}	Input Capacitance $\overline{RAS}$, $\overline{WRITE}$	3	7	pF	V_{IN} = V_{SS}
C_O	Output Capacitance (D_{OUT})	4	7	pF	V_{OUT} = 0V
C_{I3}	Input Capacitance $\overline{CAS}$	6	7	pF	V_{IN} = V_{SS}

Notes:
1. All voltages referenced to V_{SS}. The only requirement for the sequence of applying voltages to the device is that V_{DD}, V_{CC}, and V_{SS} should never be 0.3V or more negative than V_{BB}. After the application of supply voltages or after extended periods of operation without clocks, the device must perform a minimum of one initialization cycle (any valid memory cycles containing both $\overline{RAS}$ and $\overline{CAS}$) prior to normal operation.
2. Typical values are for T_A = 25°C and nominal power supply voltages.
3. The I_{DD} current flows to V_{SS}.
4. When chip is selected V_{CC} supply current is dependent on output loading. V_{CC} is connected to output buffer only.
5. The chip is deselected; i.e., output is brought to high impedance state by $\overline{CAS}$-only cycle or by a read cycle with $\overline{CS}$ at V_{IH}.
6. Capacitance measured with Boonton Meter.

A.C.CHARACTERISTICS[1]

$T_A = 0°C$ to $70°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 10\%$, $V_{BB} = -5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

READ, WRITE, AND READ MODIFY WRITE CYCLES

Symbol	Parameter	2104A		Unit
		Min.	Max.	
t_{REF}	Time Between Refresh		2	ms
t_{RP}	$\overline{RAS}$ Precharge Time	150		ns
t_{CP}	$\overline{CAS}$ Precharge Time	150		ns
t_{RCL}[2]	$\overline{RAS}$ to $\overline{CAS}$ Leading Edge Lead Time	100	150	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	0		ns
t_{RSH}	$\overline{RAS}$ Hold Time	200		ns
t_{CSH}	$\overline{CAS}$ Hold Time	350		ns
t_{AR}	$\overline{RAS}$ to Address or $\overline{CS}$ Hold Time	250		ns
t_{ASR}	Row Address Set-Up Time	0		ns
t_{ASC}	Column Address or $\overline{CS}$ Set-Up Time	0		ns
t_{RAH}	Row Address Hold Time	100		ns
t_{CAH}	Column Address or $\overline{CS}$ Hold Time	100		ns
t_T	Rise or Fall Time	3	50	ns
t_{OFF}	Output Buffer Turn-Off Delay	0	100	ns
t_{CAC}[3]	Access Time From $\overline{CAS}$		200	ns
t_{RAC}[3]	Access Time from $\overline{RAS}$		350	ns

READ CYCLE

Symbol	Parameter	2104A		Unit
		Min.	Max.	
t_{RC}	Random Read or Write Cycle Time	500		ns
t_{RAS}	$\overline{RAS}$ Pulse Width	350	32000	ns
t_{CAS}	$\overline{CAS}$ Pulse Width	200		ns
t_{RCS}	Read Command Set-Up Time	0		ns
t_{RCH}	Read Command Time	0		ns
t_{DOH}	Data Out Hold Time	32		μs

WRITE CYCLE[4]

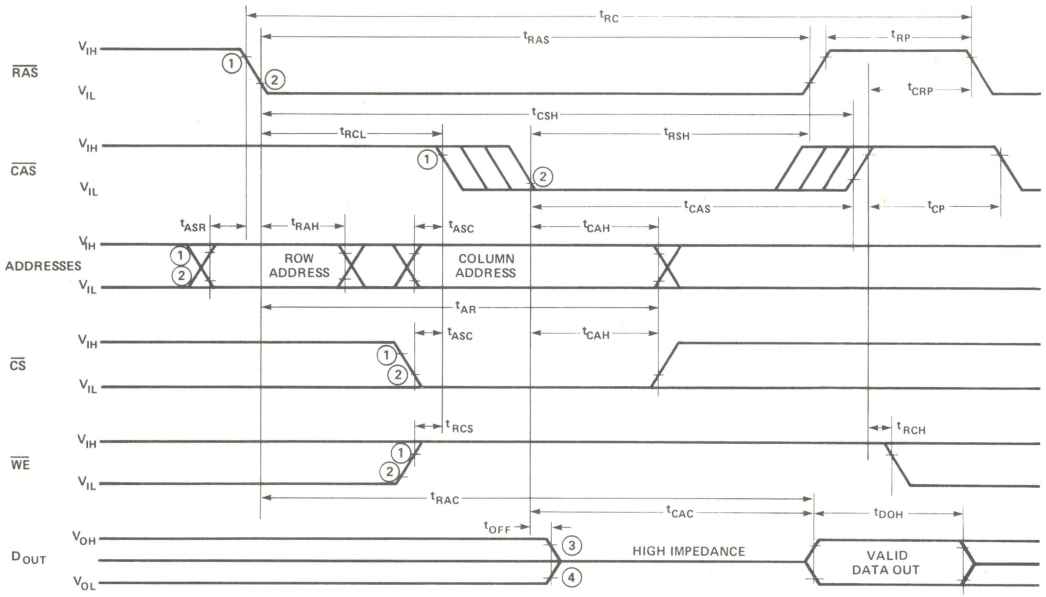
Symbol	Parameter	2104A		Unit
		Min.	Max.	
t_{RC}	Random Read or Write Cycle Time	500		ns
t_{RAS}	$\overline{RAS}$ Pulse Width	350	32000	ns
t_{CAS}	$\overline{CAS}$ Pulse Width	200		ns
t_{WCS}	Write Command Set-Up Time	0		ns
t_{WCH}	Write Command Hold Time	100		ns
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	250		ns
t_{WP}	Write Command Pulse Width	100		ns
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	200		ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	200		ns
t_{DS}	Data-In Set-Up Time	0		ns
t_{DH}	Data-In Hold Time	100		ns
t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	250		ns

Notes:

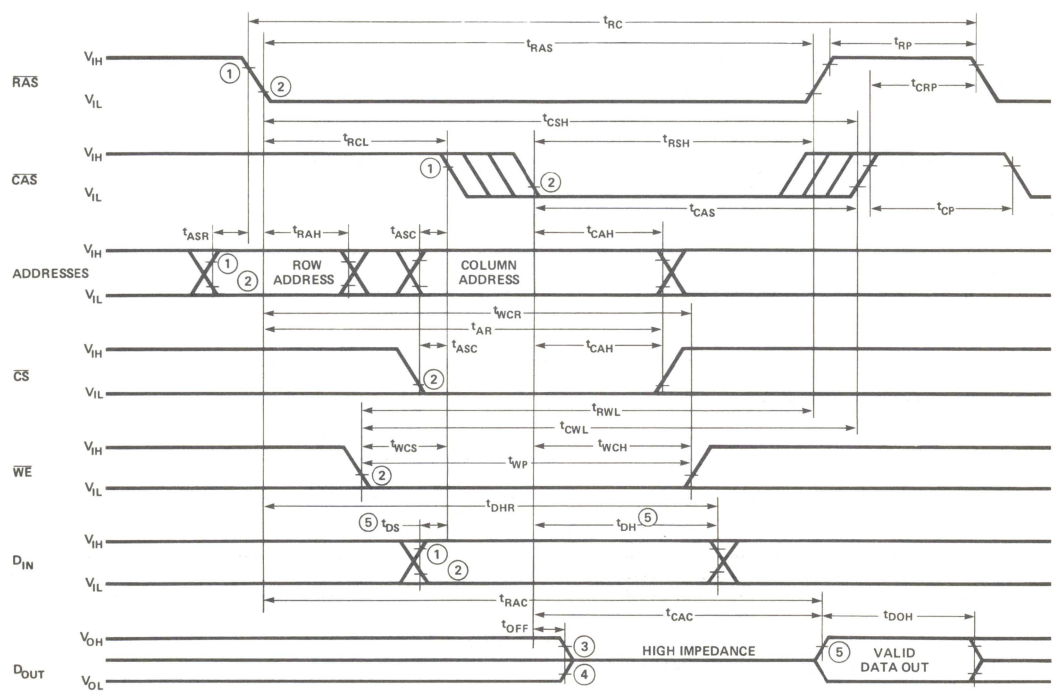
1. All voltages referenced to V_{SS}. Minimum timings do not allow for t_T or skews.
2. $\overline{CAS}$ must remain at V_{IH} a minimum of $t_{RCL\ MIN}$ after $\overline{RAS}$ switches to V_{IL}. To achieve the minimum guaranteed access time (t_{RAC}), $\overline{CAS}$ must switch to V_{IL} at or before t_{RCL} of $t_{RAC} - t_T - t_{CAC}$ as described in the Applications Information section. $t_{RCL\ MAX}$ is given for reference only as $t_{RAC} - t_{CAC}$.
3. Load = 2 TTL and 100 pF. See Applications Information.
4. In a write cycle D_{OUT} latch will contain data written into cell. In a read-modify-write cycle D_{OUT} latch will contain data read from cell. If $\overline{WE}$ goes low after $\overline{CAS}$ and prior to t_{CAC}, D_{OUT} is indeterminate.

WAVEFORMS

READ CYCLE



WRITE CYCLE



(See next page for notes)

A.C.CHARACTERISTICS[1]

T_A = 0°C to 70°C, V_{DD} = 12V ±5%, V_{CC} = 5V ±10%, V_{BB} = −5V ±10%, V_{SS} = 0V, unless otherwise noted.

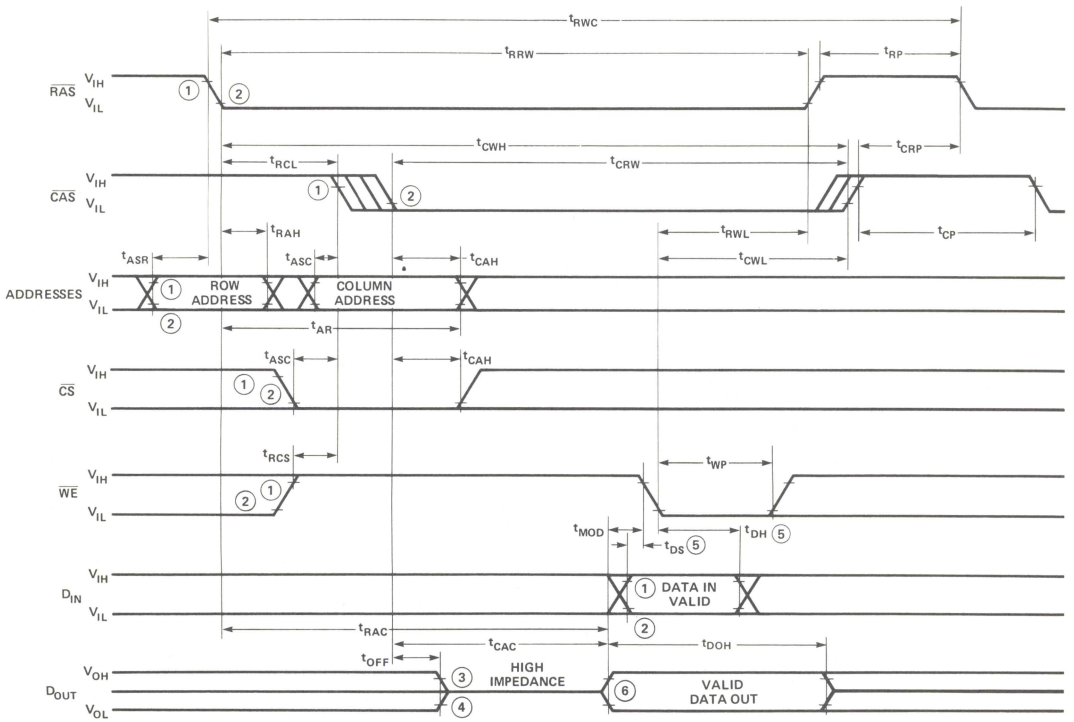
READ-MODIFY-WRITE CYCLE

Symbol	Parameter	2104A		Unit
		Min.	Max.	
t_{RWC}	Read Modify Write Cycle Time[2]	700		ns
t_{CRW}	RMW Cycle $\overline{CAS}$ Width	400		ns
t_{RRW}	RMW Cycle $\overline{RAS}$ Width	550		ns
t_{RWL}	RMW Cycle $\overline{RAS}$ Lead Time	200		ns
t_{CWH}	RMW Cycle $\overline{CAS}$ Hold Time	550		ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	200		ns
t_{WP}	Write Command Pulse Width	100		ns
t_{RCS}	Read Command Set-Up Time	0		ns
t_{MOD}	Modify Time	0	10	µs
t_{DS}	Data-In Set-Up Time	0		ns
t_{DH}	Data-In Hold Time	100		ns

Notes: 1. All voltages referenced to V_{SS}.
2. The minimum cycle timing does not allow for t_T or skews.

WAVEFORMS

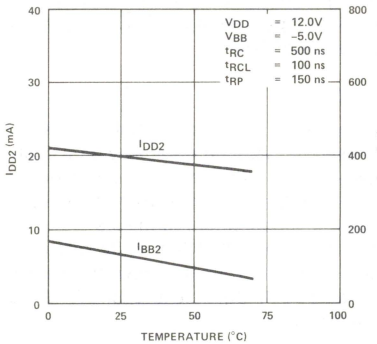
READ-MODIFY-WRITE CYCLE



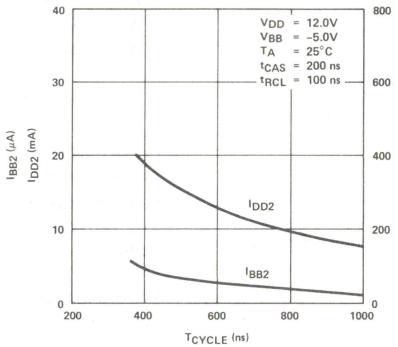
Notes: 1,2. V_{IHMIN} and V_{ILMAX} are reference levels for measuring timing of input signals.
3,4. V_{OHMIN} and V_{OLMAX} are reference levels for measuring timing of D_{OUT}.
5. Referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.
6. In a write cycle D_{OUT} latch will contain data written into cell. In a read-modify-write cycle D_{OUT} latch will contain data read from cell. If $\overline{WE}$ goes low after $\overline{CAS}$ and prior to t_{CAC}, D_{OUT} is indeterminate.

TYPICAL CHARACTERISTICS

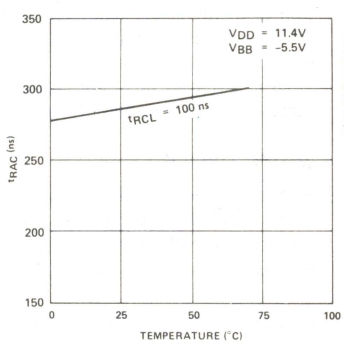
TYPICAL I_{BB2} AND I_{DD2} VS. TEMPERATURE



TYPICAL I_{BB2} AND I_{DD2} VS. CYCLE TIME



TYPICAL ACCESS TIME VS. TEMPERATURE



RAM

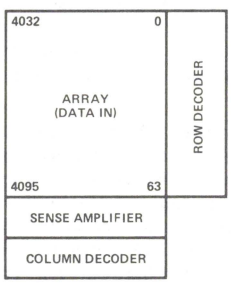
APPLICATIONS

ADDRESSING

Two externally applied negative going TTL clocks, Row Address Strobe ($\overline{RAS}$), and Column Address Strobe ($\overline{CAS}$), are used to strobe the two sets of 6 addresses into internal address buffer registers. The first clock, $\overline{RAS}$, strobes in the six low order addresses (A_0-A_5) which selects one of 64 rows and begins the timing which enables the column sense amplifiers. The second clock, $\overline{CAS}$, strobes in the six high order addresses (A_6-A_{11}) to select one of 64 column sense amplifiers and Chip Select ($\overline{CS}$) which enables the data out buffer.

An address map of the 2104A is shown below. Address "0" corresponds to all addresses at V_{IL}. All addresses are sequentially located on the chip.

2104A Address Map



DATA CYCLES/TIMING

A memory cycle begins with addresses stable and a negative transition of $\overline{RAS}$. See the waveforms on page 4. It is not necessary to know whether a Read or Write cycle is to be performed until $\overline{CAS}$ becomes valid.

Note that Chip Select ($\overline{CS}$) does not have to be valid until the second clock, $\overline{CAS}$. It is, therefore, possible to start a memory cycle before it is known which device must be selected. This can result in a significant improvement in system access time since the decode time for chip select does not enter into the calculation for access time.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks are TTL compatible and do not require level shifting and driving at high voltage MOS levels. Buffers internal to the 2104A convert the TTL level signals to MOS levels inside the device. Therefore, the delay associated with external TTL-MOS level converters is not added to the 2104A system access time.

READ CYCLE

A Read cycle is performed by maintaining Write Enable ($\overline{WE}$) high during $\overline{CAS}$. The output pin of a selected device will unconditionally go to a high impedance state immediately following the leading edge of $\overline{CAS}$ and remain in this state until valid data appears at the output at access time. The selected output data is internally latched and will remain valid until a subsequent $\overline{CAS}$ is given to the device by a Read, Write, Read-Modify-Write, $\overline{CAS}$ only or Refresh cycle. Data-out goes to a high impedance state for all non-selected devices.

Device access time, t_{ACC}, is the longer of two calculated intervals:

1. $t_{ACC} = t_{RAC}$ OR 2. $t_{ACC} = t_{RCL} + t_T + t_{CAC}$

Access time from $\overline{RAS}$, t_{RAC}, and access time from $\overline{CAS}$, t_{CAC}, are device parameters. Row to column address strobe lead time, t_{RCL}, and transition time, t_T, are system dependent timing parameters. For example, substituting the device parameters of the 2104A and assuming a TTL level transition time of 5 ns yields:

3. $t_{ACC} = t_{RAC} = 350$ ns for 100 nsec $\leqslant t_{RCL} \leqslant$ 145 nsec
   OR
4. $t_{ACC} = t_{RCL} + t_T + t_{CAC} = t_{RCL} + 205$ ns for $t_{RCL} > 145$ ns.

Note that if 100 nsec $\leqslant t_{RCL} \leqslant$ 145 nsec, device access time is determined by equation 3 and is equal to t_{RAC}. If $t_{RCL} >$ 145 nsec, access time is determined by equation 4. This 45 ns interval (shown in the t_{RCL} inequality in equation 3) in which the failing edge of $\overline{CAS}$ can occur without affecting access time is provided to allow for system timing skew in the generation of $\overline{CAS}$. This allowance for a t_{RCL} skew is designed in at the device level to allow minimum access times to be achieved in practical designs.

WRITE CYCLE

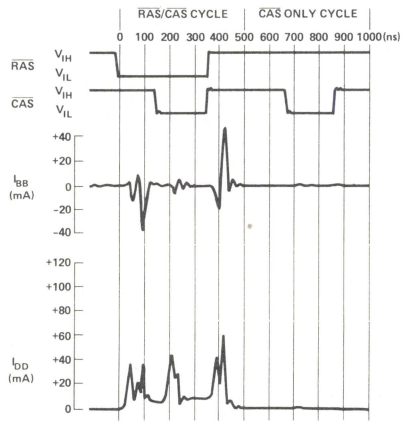
A Write Cycle is generally performed by bringing Write Enable ($\overline{WE}$) low before $\overline{CAS}$. D_{OUT} will be the data written into the cell addressed. If $\overline{WE}$ goes low after $\overline{CAS}$ and prior to t_{CAC}, D_{OUT} will be indeterminate.

READ-MODIFY-WRITE CYCLE

A Read-Modify-Write Cycle is performed by bringing Write Enable ($\overline{WE}$) low after access time, t_{RAC}, with $\overline{RAS}$ and $\overline{CAS}$ low. Data in must be valid at or before the falling edge of $\overline{WE}$. In a read-modify-write cycle D_{OUT} is data read and does not change during the modify-write portion of the cycle.

$\overline{CAS}$ ONLY (DESELECT) CYCLE

In some applications, it is desirable to be able to deselect all memory devices without running a regular memory cycle. This may be accomplished with the 2104A by performing a $\overline{CAS}$-Only Cycle. Receipt of a $\overline{CAS}$ without $\overline{RAS}$ deselects the 2104A and forces the Data Output to the high-impedance state. This places the 2104A in its lowest power, standby condition. I_{DD} will be about twice I_{DD1} for the first cycle of $\overline{CAS}$-only deselection and I_{DD1} for any additional $\overline{CAS}$-only cycles. The cycle timing and $\overline{CAS}$ timing should be just as if a normal $\overline{RAS}/\overline{CAS}$ cycle was being performed.



TYPICAL SUPPLY CURRENTS VS. TIME

CHIP SELECTION/DESELECTION

The 2104A is selected by driving $\overline{CS}$ low during a Read, Write, or Read-Modify-Write cycle. A device is deselected by 1) driving $\overline{CS}$ high during a Read, Write, or Read-Modify-Write cycle or 2) performing a $\overline{CAS}$ Only cycle independent of the state of $\overline{CS}$.

REFRESH CYCLES

Each of the 64 rows internal to the 2104A must be refreshed every 2 msec to maintain data. Any data cycle (Read, Write, Read-Modify-Write) refreshes the entire selected row (defined by the low order row addresses). The refresh operation is independent of the state of chip select. It is evident, of course, that if a Write or Read-Modify-Write cycle is used to refresh a row, the device should be deselected ($\overline{CS}$ high) if it is desired not to change the state of the selected cell.

$\overline{RAS}/\overline{CAS}$ TIMING

The device clocks, $\overline{RAS}$ and $\overline{CAS}$, control operation of the 2104A. The timing of each clock and the timing relationships of the two clocks must be understood by the user in order to obtain maximum performance in a memory system.

The $\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths as defined by t_{RAS} and t_{CAS} respectively. These minimum pulse widths must be maintained for proper device operation and data integrity. A cycle, once begun by driving $\overline{RAS}$ and/or $\overline{CAS}$ low must not be ended or aborted prior to fulfilling the minimum clock signal pulse width(s). A new cycle must not begin until the minimum precharge time, t_{RP}, has been met.

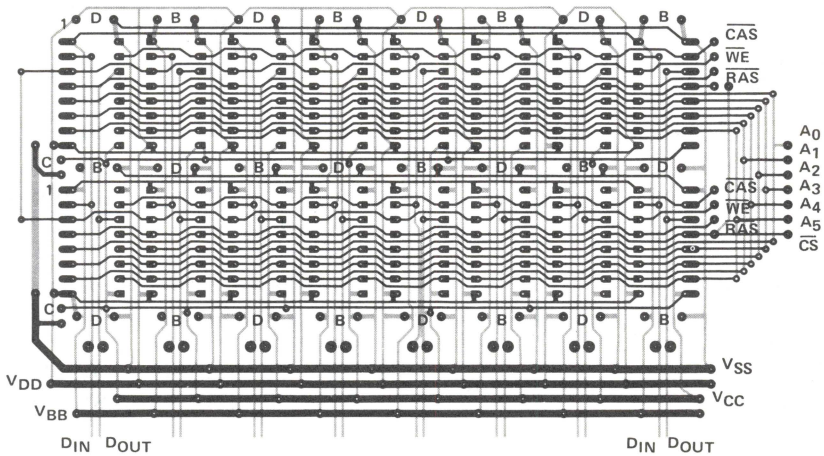
POWER SUPPLY

Typical power supply current waveforms versus time are shown below for both a $\overline{RAS}/\overline{CAS}$ cycle and a $\overline{CAS}$ only cycle. I_{DD} and I_{BB} current surges at $\overline{RAS}$ and $\overline{CAS}$ edges make adequate decoupling of these supplies important. Due to the high frequency noise component content of the current waveforms, the decoupling capacitors should be low inductance, ceramic units selected for their high frequency performance.

It is recommended that a 0.1 μF ceramic capacitor be connected between V_{DD} and V_{SS} at every other device in the memory array. A 0.1 μF ceramic capacitor should also be connected between V_{BB} and V_{SS} at every other device (preferably the alternate devices to the V_{DD} decoupling). For each 16 devices, a 10 μF tantalum or equivalent capacitor should be connected between V_{DD} and V_{SS} near the array. An equal or slightly smaller bulk capacitor is also recommended between V_{BB} and V_{SS} for every 32 devices.

A 0.01 μF ceramic capacitor is recommended between V_{CC} and V_{SS} at every eighth device to prevent noise coupling to the V_{CC} line which may affect the TTL peripheral logic in the system.

Due to the high frequency characteristics of the current waveforms, the inductance of the power supply distribution system on the array board should be minimized. It is recommended that the V_{DD}, V_{BB}, and V_{SS} supply lines be gridded both horizontally and vertically at each device in the array. This technique allows use of double-sided circuit boards with noise performance equal to or better than multi-layered circuit boards.



DECOUPLING CAPACITORS
D = 0.1 μF to V_{DD} TO V_{SS}
B = 0.1 μF V_{BB} TO V_{SS}
C = 0.01 μF V_{CC} TO V_{SS}

2107C FAMILY
4096-BIT DYNAMIC RAM

	2107C-1	2107C-2	2107C	2107C-4
Access Time (ns)	150	200	250	300
Read, Write Cycle (ns)	380	400	430	470
RMW Cycle (ns)	450	500	550	590
Max $I_{DD\ AV}$ (mA)	35	33	30	30

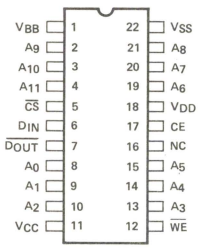
- **Direct Replacement for Industry Standard 22-Pin 4K RAMs**
- **Low Operating Power**
- **Low Standby Power**
- **Only One High Voltage Input Signal-Chip Enable**
- **150 ns Access Time**
- **±10% Tolerance on all Power Supplies**
- **Output is Three-State and TTL Compatible**
- **TTL Compatible — All Address, Data, Write Enable, Chip Select Inputs**
- **Refresh Period 2 ms**

The Intel® 2107C is a 4096-word by 1-bit dynamic n-channel MOS RAM. It was designed for memory applications where very low cost and large bit storage are important design objectives. A new unique dynamic storage cell provides high speed and wide operating margins. The 2107C uses dynamic circuitry which reduces the standby power dissipation.

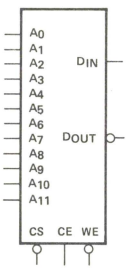
Reading information from the memory is non-destructive. Refreshing is most easily accomplished by performing one read cycle on each of the 64 row addresses. Each row address must be refreshed every two milliseconds. The memory is refreshed whether Chip Select is a logic one or a logic zero.

The 2107C is fabricated with n-channel silicon gate technology. This technology allows the design and production of high performance, easy to use MOS circuits and provides a higher functional density on a monolithic chip than other MOS technologies. The 2107C is a replacement for the 2107A, 2107B and other industry standard 22-pin 4K RAMs.

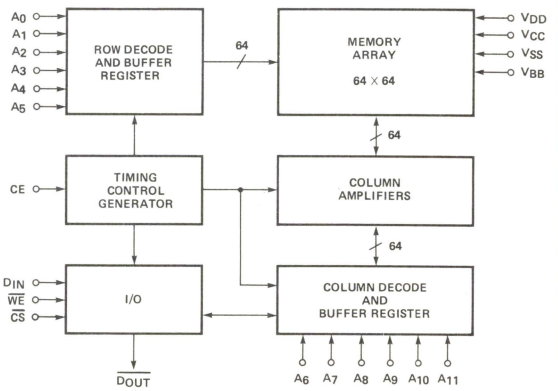
PIN CONFIGURATION
2107C



LOGIC SYMBOL
2107C



BLOCK DIAGRAM



PIN NAMES

A0–A11	ADDRESS INPUTS*	VBB	POWER (-5V)
CE	CHIP ENABLE	VCC	POWER (+5V)
CS	CHIP SELECT	VDD	POWER (+12V)
DIN	DATA INPUT	VSS	GROUND
DOUT	DATA OUTPUT	WE	WRITE ENABLE
NC	NOT CONNECTED		

*Refresh Address A0–A5.

Absolute Maximum Ratings*

Temperature Under Bias . . . . . -10°C to 80°C

Storage Temperature . . . . . -65°C to +150°C

Voltage on any Pin Relative to V_{BB} ($V_{SS} - V_{BB} \geq 4.5$) . . . . . -0.3V to +20V

Power Dissipation 1.00W

**COMMENT:*
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = +12V ±10%, V_{CC} = +5V ±10%, V_{BB}[1] = -5V ±10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[2]	Max.		
I_{LI}	Input Load Current (all inputs except CE)			10	µA	V_{IN} = 0V to $V_{IH\ MAX}$ CE = V_{ILC} or V_{IHC}
I_{LC}	Input Load Current, CE			2	µA	V_{IN} = 0V to $V_{IHC\ MAX}$
$\|I_{LO}\|$	Output Leakage Current for high impedance state			10	µA	CE = V_{ILC} or $\overline{CS}$ = V_{IH} V_O = 0V to 5.5V
I_{DD1}[3]	V_{DD} Supply Current — standby[3]		20	200	µA	CE = -1V to +0.6V
$I_{DD\ AV}$	Average V_{DD} Current — operating		24	35	mA	2107C-1, t_{CYC} = 380
			22	33	mA	2107C-2, t_{CYC} = 400
			20	30	mA	2107C, t_{CYC} = 430
			20	30	mA	2107C-4, t_{CYC} = 470
I_{CC1}[3,4]	V_{CC} Supply Current — standby			10	µA	CE = V_{ILC} or $\overline{CS}$ = V_{IH}
I_{BB1}	V_{BB} Supply Current — standby		5	50	µA	CE = -1V to +0.6V
$I_{BB\ AV}$	Average V_{BB} Current — operating		100	400	µA	Min. cycle time, Min. t_{CE}
V_{IL}	Input Low Voltage	-1.0		0.8	V	
V_{IH}	Input High Voltage	2.4		V_{CC}+1	V	
V_{ILC}	CE Input Low Voltage	-1.0		+1.0	V	
V_{IHC}	CE Input High Voltage	V_{DD}-1		V_{DD}+1	V	
V_{OL}	Output Low Voltage	0.0		0.40	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4		V_{CC}	V	I_{OH} = -2.0 mA

NOTES:

1. The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be 0.3V or more negative than V_{BB}.
2. Typical values are for T_A = 25°C and nominal power supply voltages.
3. The I_{DD} and I_{CC} currents flow to V_{SS}.
4. During CE on V_{CC} supply current is dependent on output loading. V_{CC} is connected to output buffer only.

A.C. Characteristics [1]

$T_A = 0°C$ to $70°C$, $V_{DD} = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $V_{BB} = -5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

READ, WRITE, AND READ MODIFY/WRITE CYCLE

Symbol	Parameter	2107C-1		2107C-2		2107C		2107C-4		Units	Note
		Min.	Max	Min.	Max.	Min.	Max.	Min.	Max.		
t_{REF}	Time Between Refresh		2		2		2		2	ms	
t_{AC}	Address to CE Set-Up Time	0		0		0		0		ns	2
t_{AH}	Address Hold Time	50		50		100		100		ns	
t_{CC}	CE Off Time	130		130		130		130		ns	
t_T	CE Transition Time		40		40		40		40	ns	
t_{CD}	CE Off to Output Disable Time	30		30		30		30		ns	3

READ CYCLE

Symbol	Parameter	2107C-1		2107C-2		2107C		2107C-4		Units	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{CY}	Cycle Time	380		400		430		470		ns	3
t_{CE}	CE On Time	210	4000	230	4000	260	4000	300	4000	ns	
t_{CO}	CE Output Delay		130		180		230		280	ns	4
t_{ACC}	Address to Output Access		150		200		250		300	ns	5
t_{WL}	CE to $\overline{WE}$	0		0		0		0		ns	
t_{WC}	$\overline{WE}$ to CE On	0		0		0		0		ns	

WRITE CYCLE

Symbol	Parameter	2107C-1		2107C-2		2107C		2107C-4		Units	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{CY}	Cycle Time	380		400		430		470		ns	3
t_{CE}	CE On Time	210	4000	230	4000	260	4000	300	4000	ns	
t_W	$\overline{WE}$ to CE Off	125		125		125		175		ns	
t_{CW}	CE to $\overline{WE}$	150		150		150		200		ns	
t_{DW}	D_{IN} to $\overline{WE}$ Set-Up	0		0		0		0		ns	6
t_{DH}	D_{IN} Hold Time	0		0		0		0		ns	
t_{WP}	$\overline{WE}$ Pulse Width	50		50		50		100		ns	
t_{WD}	$\overline{WE}$ to Output Disable Time	15		15		15		15			

Capacitance [7] $T_A = 25°C$

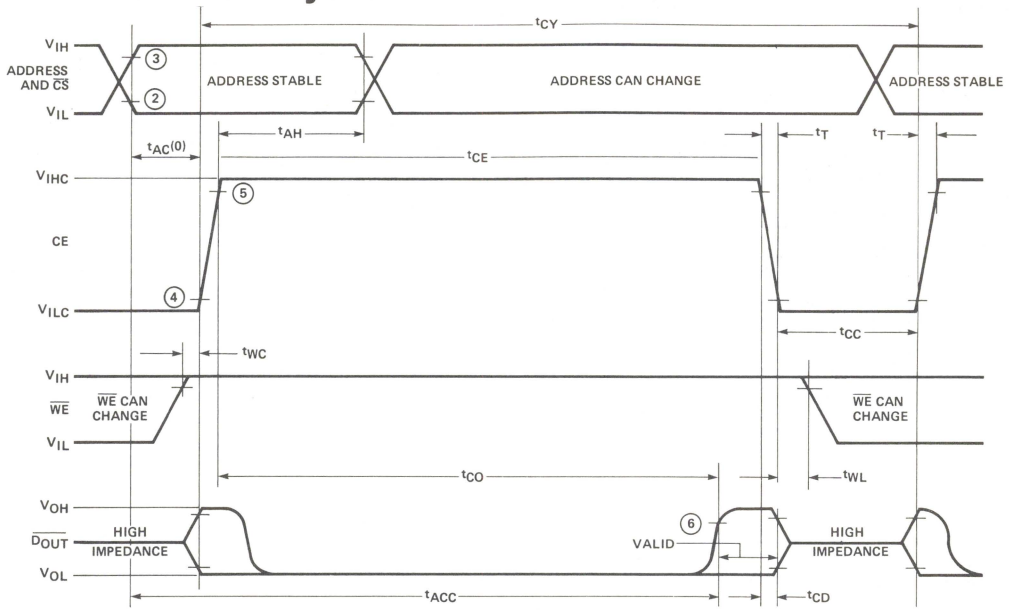
Symbol	Test	Plastic and Ceramic Package		Unit	Conditions
		Typ.	Max.		
C_{AD}	Address Capacitance, $\overline{CS}$, D_{IN}	5	7	pF	$V_{IN} = V_{SS}$
C_{CE}	CE Capacitance	10	15	pF	$V_{IN} = V_{SS}$
C_{OUT}	Data Output Capacitance	5	7	pF	$V_{OUT} = 0V$
$C_{\overline{WE}}$	$\overline{WE}$ Capacitance	6	8	pF	$V_{IN} = V_{SS}$

NOTES:

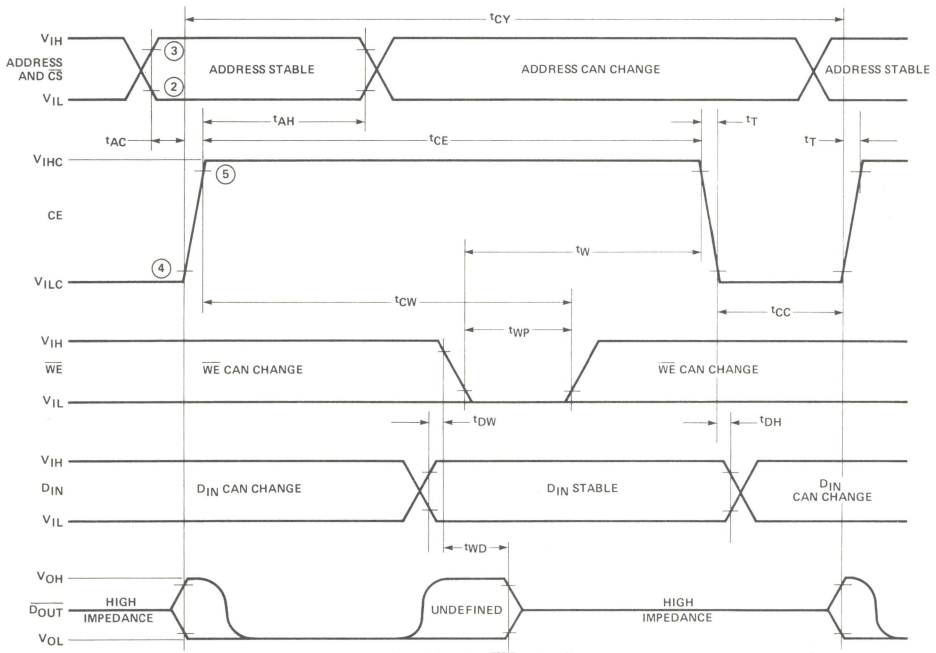
1. After the application of supply voltages or after extended periods of operation without CE, the device must perform a minimum of one initialization cycle (any valid memory cycle or refresh cycle) prior to normal operation.
2. t_{AC} is measured from end of address transition.
3. $t_T = 20$ ns.
4. $C_{LOAD} = 50$ pF, Load = One TTL Gate, Ref = 2.0V.
5. $t_{ACC} = t_{AC} + t_{CO} + 1t_T$.
6. If $\overline{WE}$ is low before CE goes high then D_{IN} must be valid when CE goes high.
7. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation:

$$C = \frac{I\Delta t}{\Delta V}$$ with the current equal to a constant 20 mA.

Read and Refresh Cycle [1]



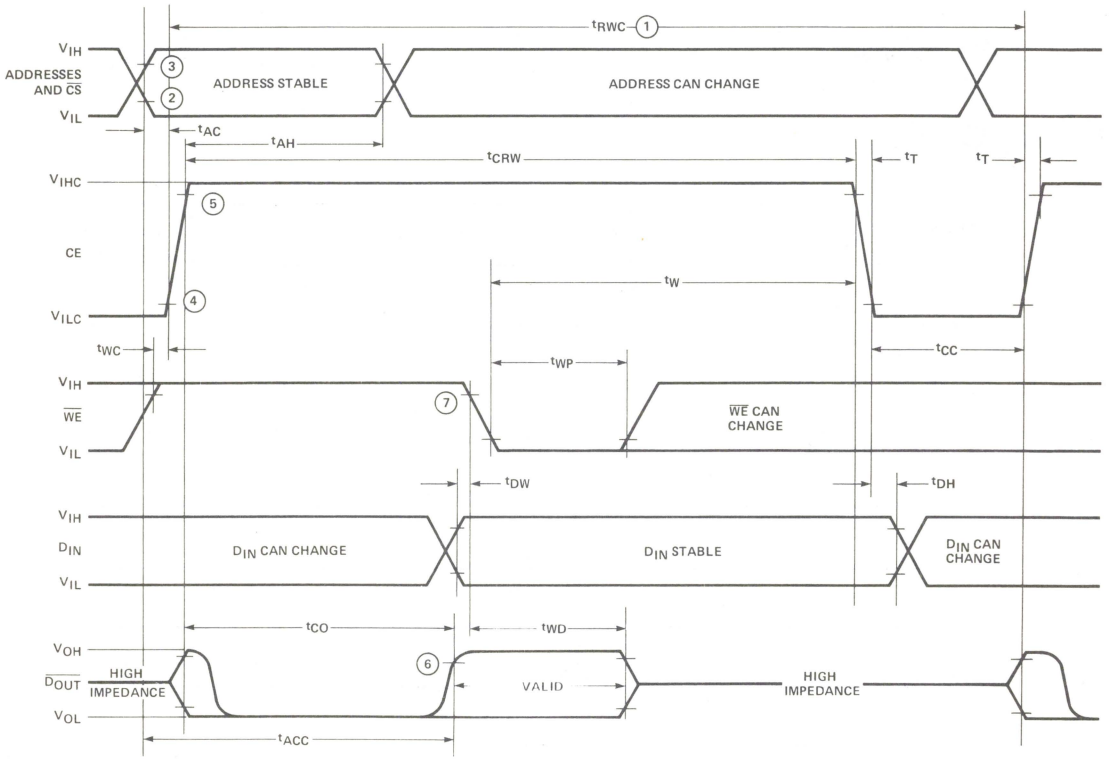
Write Cycle



NOTES:
1. For Refresh cycle, row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.
2. V_{IL} MAX is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
3. V_{IN} MIN is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
4. V_{SS} +2.0V is the reference level for measuring timing of CE.
5. V_{DD} –2V is the reference level for measuring timing of CE.
6. V_{SS} +2.0V is the reference level for measuring the timing of $\overline{D_{OUT}}$.

Read Modify Write Cycle

Symbol	Parameter	2107C-1		2107C-2		2107C		2107C-4		Units	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RWC}	Read Modify Write (RMW) Cycle	450		500		550		590		ns	1
t_{CRW}	CE Width During RMW	280	4000	330	4000	380	4000	420	4000	ns	
t_{WC}	$\overline{WE}$ to CE On	0		0		0		0		ns	
t_W	$\overline{WE}$ to CE Off	125		125		125		175		ns	
t_{WP}	$\overline{WE}$ Pulse Width	50		50		50		100		ns	
t_{DW}	D_{IN} to $\overline{WE}$ Setup	0		0		0		0		ns	
t_{DH}	D_{IN} Hold Time	0		0		0		0		ns	
t_{CO}	CE to Output Delay		130		180		230		280	ns	
t_{ACC}	Access Time		150		200		250		300	ns	
t_{WD}	$\overline{WE}$ to Output Disable Time	15		15		15		15		ns	



NOTES:
1. t_T of 20 ns.
2. V_{IL} MAX is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
3. V_{IH} MIN is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
4. V_{SS} +2.0V is the reference level for measuring timing of CE.
5. V_{DD} –2V is the reference level for measuring timing of CE.
6. V_{SS} +2.0V is the reference level for measuring the timing of $\overline{D_{OUT}}$. C_{LOAD} = 50 pF. Load = One TTL Gate.
7. $\overline{WE}$ must be at V_{IH} until end of t_{CO}.

2108-2 AND 2108-4
8192 X 1 BIT DYNAMIC RAM

	2108-2	2108-4
	S1572,S1573	S1626,S1627
Max. Access Time (ns)	200	300
Read, Write Cycle (ns)	350	425
Read-Modify-Write Cycle (ns)	400	595

- **8K RAM in Industry Standard 16 Pin Package**
- **Low Standby Power**
- **All Inputs Including Clocks TTL Compatible**
- **Standard Power Supplies +12V, +5V, -5V**
- **Only 64 Refresh Cycles Required Every 2 ms**
- **On-Chip Input Latches**
- **Output is Three-State, TTL Compatible; Data is Latched and Valid into Next Cycle**
- **Fully Compatible with 4K and 16K Dynamic RAMs**

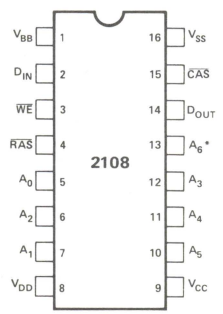
The Intel®2108 is a 8K Dynamic MOS RAM organized as 8192 words by 1 bit. The 2108 employs the same masks and highly reliable, production-proven two layer polysilicon N-MOS technology as the Intel®2116 16K RAM. As shown in the block diagram below, the 2116 is organized as two 8K RAMs on a single silicon die. Each of these 8K RAMs contains its own row decoders, sense amplifiers, and storage cells. The 2108 is fully tested to insure that one 8K RAM meets all AC and DC specifications.

The 2108 is available as either the upper or lower half of the 2116. Address A_6 selects the operating half. For S1572 or S1627, A_6 should be high (V_{IH}) during row address strobe (RAS). For S1573 or S1626, A_6 should be low (V_{IL}) during RAS. The use of the Intel® 3242 Address Multiplexer/Refresh Counter with a 2108 is described on page 3-71. The 2108 is packaged in the industry standard 16-pin DIP which is compatible with widely available automated handling equipment and facilitates easy upgrading from 2104A-type 4K RAM Systems and up to 2116-type 16K RAM Systems.

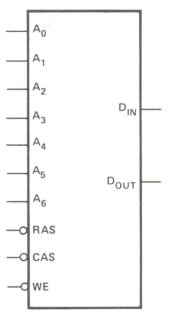
As in the 2104A-type 4K RAM and 2116-type 16K RAM, the 2108 has non-critical clock timing requirements which allow use of addressing multiplexing while maintaining high performance. Three methods of refreshing are permissable; they are described in the applications section of this data sheet.

The 2108 will provide the same reliable operation in its system usage as any Intel product. Information on the details of reliability tests performed on the 2108 and field data on the use of partial devices are available from Intel Corporation.

PIN CONFIGURATION



LOGIC SYMBOL

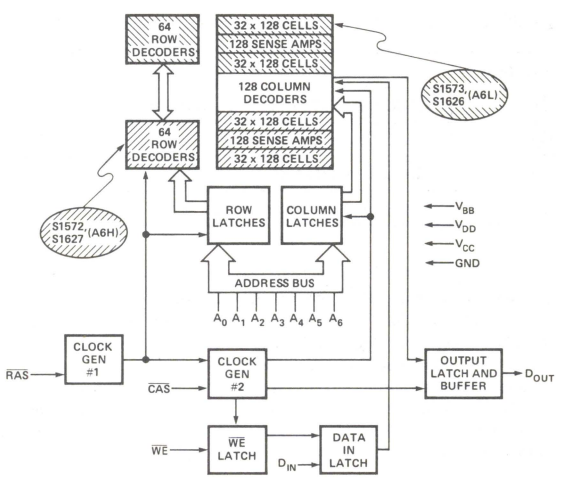


PIN NAMES

A_0 - A_6	ADDRESS INPUTS	$\overline{WE}$	WRITE ENABLE
$\overline{CAS}$	COLUMN ADDRESS STROBE	V_{BB}	POWER (-5V)
D_{IN}	DATA IN	V_{CC}	POWER (+5V)
D_{OUT}	DATA OUT	V_{DD}	POWER (+12V)
$\overline{RAS}$	ROW ADDRESS STROBE	V_{SS}	GROUND

*S1572 & S1627: A_6 SHOULD BE AT V_{IH} DURING $\overline{RAS}$
S1573 & S1626: A_6 SHOULD BE AT V_{IL} DURING $\overline{RAS}$

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... -10°C to +80°C
Storage Temperature ..... -65°C to +150°C
Voltage on any Pin Relative to V_{BB}
(V_{SS} - V_{BB} ≥ 4V) ..... -0.3V to +20V
Power Dissipation 1.25W

*COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS [1],[2]

T_A = 0°C to 70°C, V_{DD} = +12V ±10%, V_{CC} = +5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Limits			Unit	Conditions	
		Min.	Typ.[3]	Max.			
I_{LI}	Input Load Current (any input)			10	µA	V_{IN} = V_{SS} to V_{IH} MAX, V_{BB} = 5.0V	
$\|I_{LO}\|$	Output Leakage Current for high impedance state		0.1	10	µA	Chip deselected: $\overline{RAS}$ and $\overline{CAS}$ at V_{IH} V_{OUT} = 0 to 5.5V	
I_{DD1}	V_{DD} Supply Current		1.2	2	mA	$\overline{CAS}$ and $\overline{RAS}$ at V_{IH} or $\overline{CAS}$-only cycle. Chip deselected prior to measurement. See Note 5.	
I_{BB1}	V_{BB} Supply Current		1	50	µA		
I_{DD2}[4]	Operating V_{DD} Current		53	69	mA	2108-2 t_{CYC} = 350 ns	T_A = 25°C Device selected. See Note 6.
			49	65	mA	2108-4 t_{CYC} = 425 ns	
I_{BB2}	Operating V_{BB} Current		120	400	µA	Device selected	
I_{CC1}[7]	V_{CC} Supply Current when deselected			10	µA		
V_{IL}	Input Low Voltage (any input)	-1.0		0.8	V		
V_{IH}	Input High Voltage (any input)	2.4		V_{CC}+1	V		
V_{OL}	Output Low Voltage	0.0		0.4	V	I_{OL} = 4.1 mA (Read Cycle Only)	
V_{OH}	Output High Voltage	2.4		V_{CC}	V	I_{OH} = -5 mA (Read Cycle Only)	

CAPACITANCE [8]

T_A = 25°C, V_{DD} = 12V ±10%, V_{CC} = 5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{I1}	Address, Data In & $\overline{WE}$ Capacitance	4	7	pF	V_{IN} = V_{SS}
C_{I2}	$\overline{RAS}$ Capacitance	3	5	pF	V_{IN} = V_{SS}
C_{I3}	$\overline{CAS}$ Capacitance	6	10	pF	V_{IN} = V_{SS}
C_O	Data Output Capacitance	3	7	pF	V_{OUT} = 0V

Notes:
1. All voltages referenced to V_{SS}. No power supply sequencing is required but V_{DD}, V_{CC}, and V_{SS} should never be 0.3V or more negative than V_{BB}.
2. To avoid self-clocking, $\overline{RAS}$ should not be allowed to float.
3. Typical values are for T_A = 25°C and nominal power supply voltages.
4. For $\overline{RAS}$-only refresh I_{DD} = 0.78 I_{DD2}. For $\overline{CAS}$-before-$\overline{RAS}$ (64 cycle refresh) I_{DD} = 0.96 I_{DD2}.
5. The chip is deselected (i.e., output is brought to high impedance state) by $\overline{CAS}$-only cycle or by $\overline{CAS}$-before-$\overline{RAS}$ cycle. The current flowing in a selected (i.e., output on) chip with $\overline{RAS}$ and $\overline{CAS}$ at V_{IH} is approximately twice I_{DD1}.
6. See Page 3-67 for typical I_{DD} characteristics under other conditions.
7. When chip is selected V_{CC} supply current is dependent on output loading; V_{CC} is connected to output buffer only.
8. Capacitance measured with Boonton Meter.

TYPICAL CHARACTERISTICS

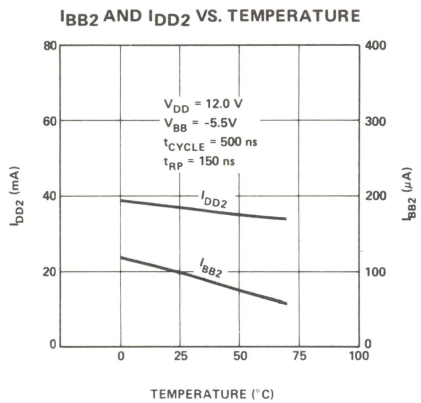


Figure 1.

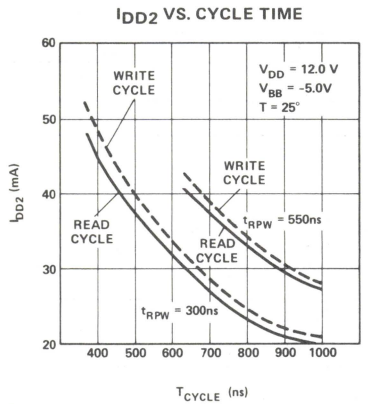


Figure 2.

Standby Power Calculations:

$$P_{REF} = P_{OP}\left(N\frac{t_{CYC}}{t_{REF}}\right) + P_{SB}\left(1 - N\frac{t_{CYC}}{t_{REF}}\right) \text{ where}$$

P_{OP} = Power dissipation — continuous operation = $V_{DD} \times I_{DD2}$.

N = Number of refresh cycles (64).

t_{CYC} = Cycle time for a refresh cycle.

t_{REF} = Time between refreshes

P_{SB} = Standby power dissipation = $V_{DD} \times I_{DD1} + |V_{BB}| \times I_{BB}$

Note that I_{DD2} depends upon refresh as follows:

1. For ($\overline{RAS}$ before $\overline{CAS}$) use I_{DD2} from Figures 1 and 2.
2. For ($\overline{CAS}$ before $\overline{RAS}$) multiply I_{DD2} determined in (1) by 0.96.
3. For ($\overline{RAS}$ only) multiply I_{DD2} determined in (1) by 0.78.

Examples of typical calculations for V_{BB} = -5.0V, V_{DD} = 12.0V, T_A = 25°C, t_{CYC} = 0.425 μs, t_{RAS} = 0.3 μs. t_{REF} = 2000 μs:

1. 128 cycle ($\overline{RAS}$ before $\overline{CAS}$): P_{OP} = 12.0V x 43 mA = 516 mW

$$P_{REF} = 516\left(128\ \frac{0.425}{2000}\right) + (12x1.2+5x0.001)\left(1-128\ \frac{0.425}{2000}\right)$$

P_{REF} = 28.0 mW

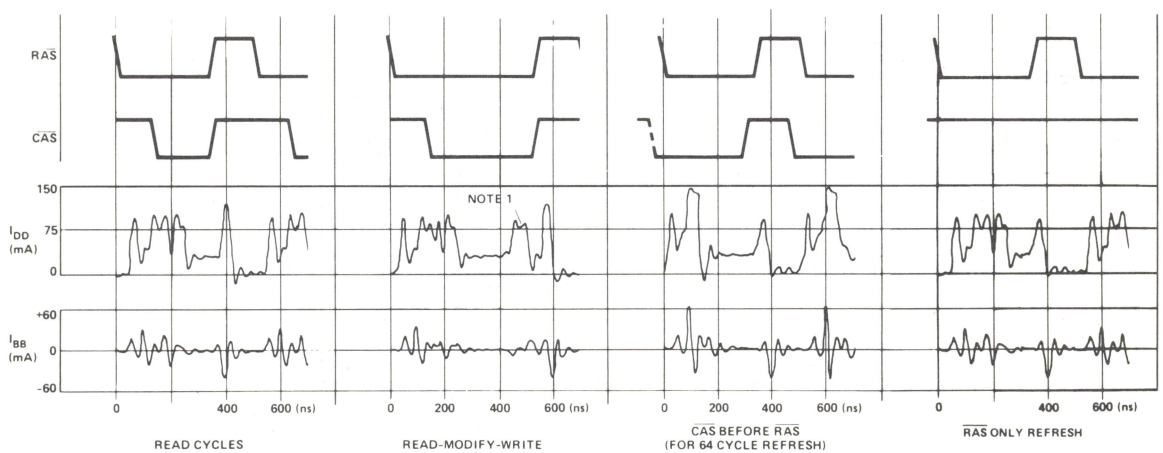
2. 64 cycle ($\overline{CAS}$ before $\overline{RAS}$); P_{OP} = 12.0V x 43 (0.96) mA = 495 mW.

$$P_{REF} = 495\left(64\ \frac{0.425}{2000}\right) + (12x1.2+5x0.001)\left(1-64\ \frac{0.425}{2000}\right) =$$

P_{REF} = 20.9 mW

3. 128 cycle ($\overline{RAS}$ only): P_{OP} = 12.0V x 43 (0.78) mA = 402 mW

P_{REF} = 25.0 mW



Note 1: Increase in current due to $\overline{WE}$ going low. Width of this current pulse is independent of $\overline{WE}$ pulse width.

Figure 3. Supply Current Waveforms.

A.C. CHARACTERISTICS[1]

T_A=0°C to 70°C, V_{DD}=12V ±10%, V_{CC}=5V ±10%, V_{BB}=−5V ±10%, V_{SS}=0V, unless otherwise noted.

READ, WRITE, READ-MODIFY-WRITE AND REFRESH CYCLES

Symbol	Parameter	2108-2 Min.	2108-2 Max.	2108-4 Min.	2108-4 Max.	Unit
t_{REF}	Time Between Refresh		2		2	ms
t_{RP}	$\overline{RAS}$ Precharge Time	75		95		ns
t_{CP}	$\overline{CAS}$ Precharge Time	100		125		ns
t_{RCL}[2]	$\overline{RAS}$ to $\overline{CAS}$ Leading Edge Lead Time	45	75	60	110	ns
t_{CRP}[3]	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	0		0		ns
t_{RSH}	$\overline{RAS}$ Hold Time	160		220		ns
t_{CSH}	$\overline{CAS}$ Hold Time	200		300		ns
t_{ASR}	Row Address Set-Up Time	0		0		ns
t_{ASC}	Column Address Set-Up Time	−10		−10		ns
t_{AH}	Address Hold Time	45		60		ns
t_T	Transition Time (Rise and Fall)		50		50	ns
t_{OFF}	Output Buffer Turn Off Delay	0	60	0	80	ns
t_{CAC}[4]	Access Time From $\overline{CAS}$		125		190	ns
t_{RAC}[4]	Access Time From $\overline{RAS}$		200		300	ns

READ AND REFRESH CYCLES

Symbol	Parameter	2108-2 Min.	2108-2 Max.	2108-4 Min.	2108-4 Max.	Unit
t_{CYC}[5]	Random Read Cycle Time	350		425		ns
t_{RAS}	$\overline{RAS}$ Pulse Width	275	32000	330	32000	ns
t_{CAS}	$\overline{CAS}$ Pulse Width	125	3000	190	3000	ns
t_{CH}	$\overline{CAS}$ Hold Time for $\overline{RAS}$-Only Refresh	30		30		ns
t_{CPR}	$\overline{CAS}$ Precharge for 64 Cycle Refresh	30		30		ns
t_{RCH}	Read Command Hold Time	20		20		ns
t_{RCS}	Read Command Set-Up Time	0		0		ns
t_{DOH}	Data-Out Hold Time	32		32		μs

WRITE CYCLE

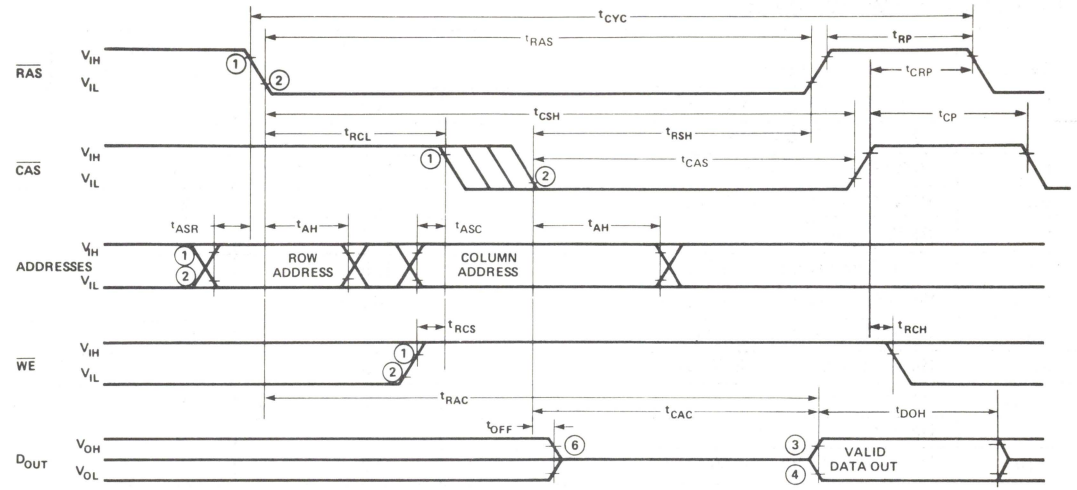
Symbol	Parameter	2108-2 Min.	2108-2 Max.	2108-4 Min.	2108-4 Max.	Unit
t_{CYC}[5]	Random Write Cycle Time	350		425		ns
t_{RAS}	$\overline{RAS}$ Pulse Width	275	32000	330	32000	ns
t_{CAS}	$\overline{CAS}$ Pulse Width	125	10000	190	10000	ns
t_{WCH}	Write Command Hold Time	75		100		ns
t_{WP}	Write Command Pulse Width	50		100		ns
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	125		200		ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	100		160		ns
t_{DS}[6]	Data-In Set-Up Time	0		0		ns
t_{DH}[6]	Data-In Hold Time	100		125		ns

Notes: 1. All voltages referenced to V_{SS}.

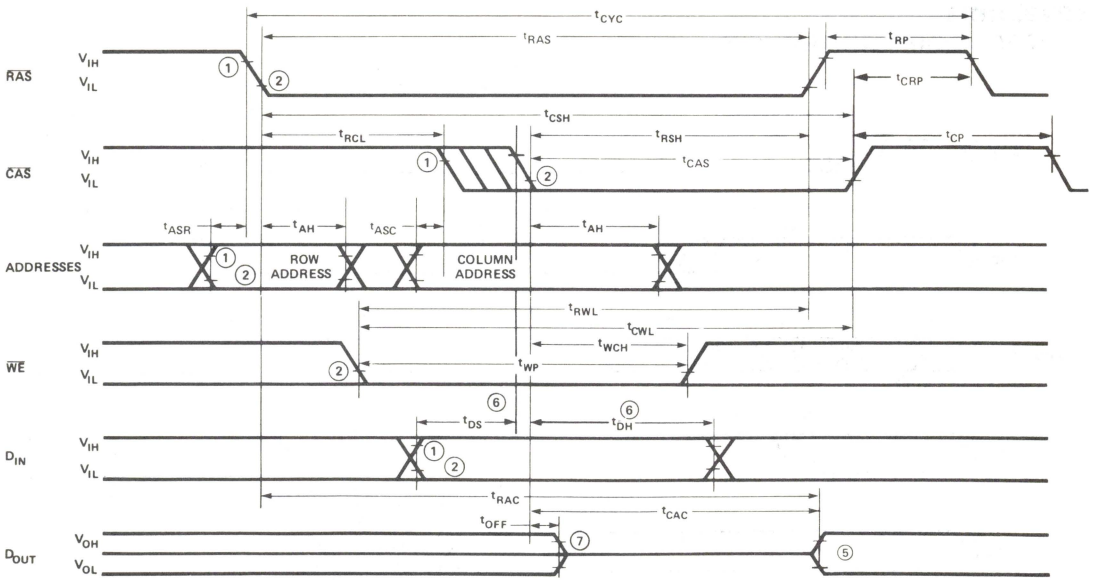
2. $\overline{CAS}$ must remain at V_{IH} a minimum of $t_{RCL\ MIN}$ after $\overline{RAS}$ switches to V_{IL}. To achieve the minimum guaranteed access time (t_{RAC}), $\overline{CAS}$ must switch to V_{IL} at or before $t_{RCL\ (MAX)} = t_{RAC} - t_{CAC}$. Device operation is not guaranteed for $t_{RCL} > 2$ μs.
3. The t_{CRP} specification is less restrictive than the t_{CRL} range which was specified in the 2108 preliminary data sheet.
4. Load = 1 TTL and 50 pF.
5. The minimum cycle timing does not allow for t_T or skews.
6. Referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.

WAVEFORMS

READ CYCLE



WRITE CYCLE



Notes:
1,2. $V_{IH\ MIN}$ and $V_{IL\ MAX}$ are reference levels for measuring timing of input signals.
3,4. $V_{OH\ MIN}$ and $V_{OL\ MAX}$ are reference levels for measuring timing of D_{OUT}.
5. D_{OUT} follows D_{IN} when writing, with $\overline{WE}$ before $\overline{CAS}$.
6. Referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.
7. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.

A.C. Characteristics

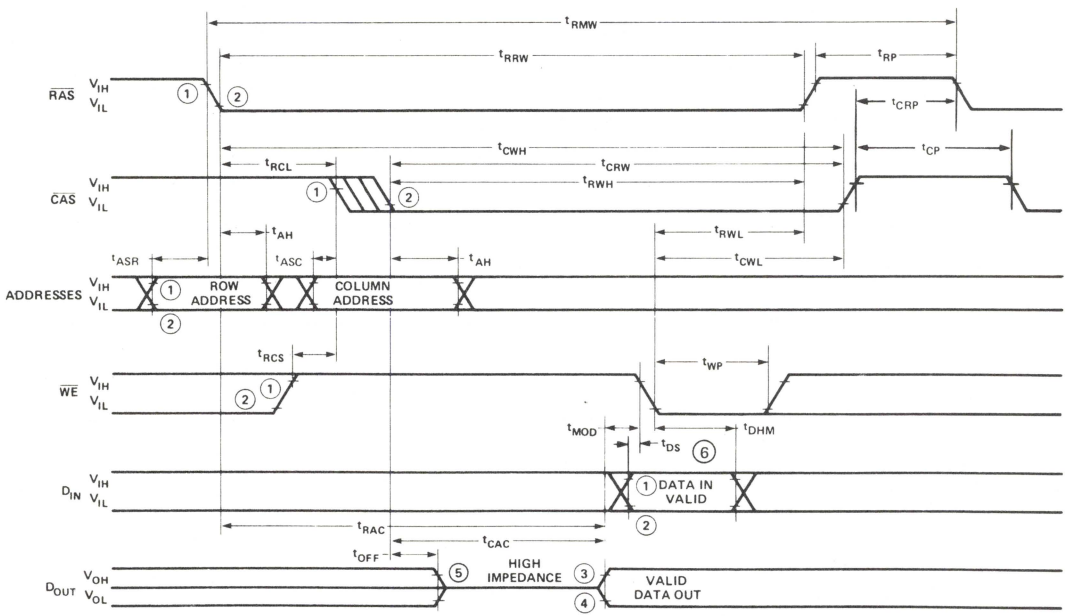
T_A = 0°C to 70°C, V_{DD} = 12V ±10%, V_{CC} = 5V ±10%, V_{BB} = −5V ±10%, V_{SS} = 0V, unless otherwise noted.

READ-MODIFY-WRITE CYCLE

Symbol	Parameter	2108-2 Min.	2108-2 Max.	2108-4 Min.	2108-4 Max.	Unit
t_{RMW}	Read-Modify-Write Cycle Time	400		595		ns
t_{CRW}	RMW Cycle $\overline{CAS}$ Width	225	3000	350	3000	ns
t_{RRW}	RMW Cycle $\overline{RAS}$ Width	325	32000	500	32000	ns
t_{RWH}	RMW Cycle $\overline{RAS}$ Hold Time	250		390		ns
t_{CWH}	RMW Cycle $\overline{CAS}$ Hold Time	300		460		ns
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	125		200		ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	100		160		ns
t_{WP}	Write Command Pulse Width	50		100		ns
t_{RCS}	Read Command Set-Up Time	0		0		ns
t_{MOD}	Modify Time	0	10	0	10	μs
t_{DS}	Data-In Set-Up Time	0		0		ns
t_{DHM}	Data-In Hold Time (RMW Cycle)	50		125		ns

Waveforms

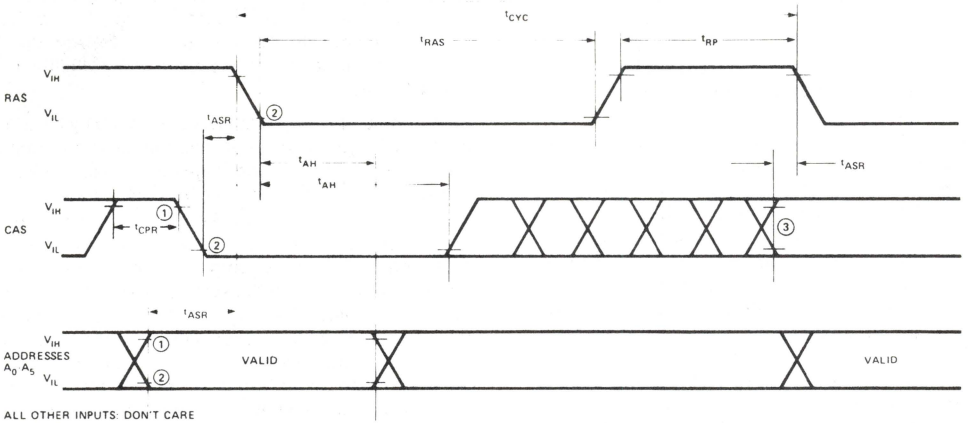
READ MODIFY WRITE CYCLE



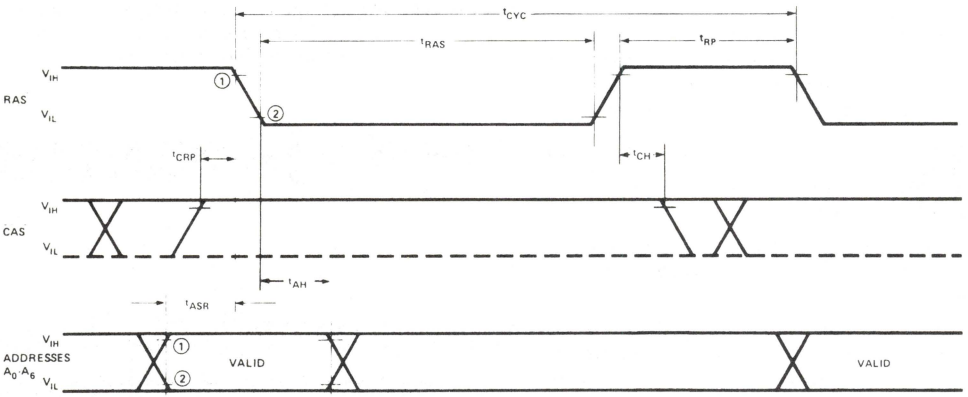
Notes 1.2. V_{IHMIN} and V_{ILMAX} are reference levels for measuring timing of input signals.
3.4. V_{OHMIN} and V_{OLMAX} are reference levels for measuring timing of D_{OUT}.
5. t_{OFF} is measured to I_{OUT}· I_{LO} .
6. Referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.

Refresh Cycle Waveforms

$\overline{CAS}$ BEFORE $\overline{RAS}$ CYCLES. (64 CYCLE REFRESH)



$\overline{RAS}$ ONLY CYCLES (128 CYCLE REFRESH)



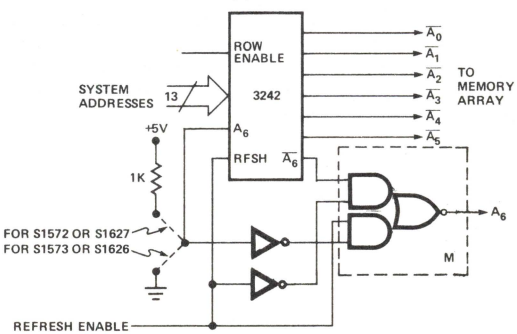
Notes: 1,2. V_{IHMIN} and V_{ILMAX} are reference levels for measuring timing of input signals.
3. $\overline{CAS}$ must be high or low as appropriate for the next cycle.

Applications Information

The 2108 may be refreshed in any of three modes: read cycles with $\overline{RAS}$ before $\overline{CAS}$ timing as shown on page 5, $\overline{RAS}$ only cycles (page 7), or $\overline{CAS}$ before $\overline{RAS}$ cycles (page 7). In all three modes A_6 must be held high for the S1572 and S1627 or low for the S1573 and S1626. The row addressed by A_0 through A_5 is refreshed. Therefore, 64 cycles are required to refresh the stored data.

The $\overline{CAS}$-before-$\overline{RAS}$ mode is useful in the 2116 as a technique for increasing memory availability and minimizing standby power dissipation by requiring only 64 refresh cycles every 2 ms. Systems employing the 2108 in a $\overline{CAS}$-before-$\overline{RAS}$ refresh mode can be easily upgraded to the most efficient 16K RAM capability.

Since the 2108 input pin A_6 supplies two system addresses (A_6 and A_{13}) to the internal memory array, it is not possible to simply tie this input high or low. The 2108 input A_6 must be tied to the appropriate level only during row address strobe ($\overline{RAS}$) and then used to supply the high order system address A_{13} during column address strobe ($\overline{CAS}$). Control of A_6 in a system may be implemented. as shown at right. In this circuit the output A_6 of multiplexer M supplies the appropriate high or low level (determined by S1572, S1627, S1573, or S1626) during $\overline{RAS}$ for both a memory cycle and refresh cycle. During $\overline{CAS}$, system address A_{13} is multiplexed on A_6 as shown. See the 2116 section for additional applications information.



POWER SUPPLY DECOUPLING/ DISTRIBUTION

Power supply current waveforms for the 2108 are shown in Figure 3. The V_{DD} supply provides virtually all of the operating current for the 2108. The V_{DD} supply current, I_{DD}, has two components: transient current peaks when the clocks change state and a DC component while the clocks are active (low). When selecting the decoupling capacitors for the V_{DD} supply, the characteristics of capacitors as well as the current waveform must be considered. Suppression of transient or pulse currents require capacitors with small physical size and low inherent inductance. Monolithic and other ceramic capacitors exhibit these desirable characteristics. When the current waveform indicates a DC component, bulk capacity must be located near the current load to supply the load power. Inductive effects of PC board traces and bus bars preclude supplying the DC component from bulk capacitors at the periphery of a memory matrix without voltage droop during the active portion of a memory cycle. This means that some bulk capacity in the form of electrolytic or large ceramic capacitors should be distributed around or within the memory matrix.

The V_{BB} supply current, I_{BB}, has high transient current peaks, with essentially no DC component (less than 400 microamperes). The V_{BB} capacitors should be selected for transient suppression characteristics. The following capacitance values and locations are recommended for the 2108:

1. A 0.33 μF ceramic capacitor between V_{DD} and V_{SS} (ground) at every other device.
2. A 0.1 μF ceramic capacitor between V_{BB} and V_{SS} at every other device (preferably alternate devices to the V_{DD} decoupling above).
3. A 4.7 μF electrolytic capacitor between V_{DD} and V_{SS} for each eight devices and located adjacent to the devices.

The V_{CC} supply is connected only to the 2108 output buffer and is not used internally. The load current from the V_{CC} supply is dependent only upon the output loading and is usually only the input high level current to a TTL gate and the output leakage currents of any OR-tied 2108 (typically 100 μA or less total). Intel recommends that a 0.1 or 0.01 μF ceramic capacitor be connected between V_{CC} and V_{SS} for every eight devices to preclude coupled noise from affecting the TTL devices in the system.

Intel recommends a power supply distribution system such that each power supply is grided both horizontally and vertically at each memory device. This technique minimizes the power distribution system impedance and enhances the effect of the decoupling capacitors.

OUTPUT DATA LATCH

The 2108 contains an output data latch eliminating the need for an external system data latch and the timing circuitry required to strobe an external latch. The output latch operates identically to the 16-pin 4K RAM (Intel 2104) output latch enhancing the system compatibility of the 16K and 4K devices.

Operation of the output latch is controlled by $\overline{CAS}$. The data output will go to the high-impedance state immediately following the $\overline{CAS}$ leading edge during each data cycle and will either go to valid data at access time on selected devices (devices receiving both $\overline{RAS}$ and $\overline{CAS}$) or will remain in the high impedance state on unselected devices (devices receiving only $\overline{CAS}$). During $\overline{RAS}$-only refresh cycles, the data output remains in the state it was prior to the $\overline{RAS}$-only cycle. This unique feature of latched output RAMs allows a refresh cycle to be hidden among data cycles without impacting data availability. For instance, a $\overline{RAS}$-only refresh cycle could follow each data cycle in a microprocessor system but the accessed data would remain at the device output and the microprocessor could take the data at any time within the cycle. Non-latched output devices do not provide this type of hidden refresh capability since their data output would go to the high impedance state at the end of the data cycle.

2109 FAMILY
8,192 x 1 BIT DYNAMIC RAM

	2109-3 S6000,S6001	2109-4 S6002,S6003
Maximum Access Time (ns)	200	250
Read, Write Cycle (ns)	375	410
Read-Modify-Write Cycle (ns)	375	475

- **8K RAM, Industry Std. 16-Pin Package**
- **±10% Tolerance on All Power Supplies: +12V, +5V, -5V**
- **Low Power: 462mW Max. Operating, 20mW Max. Standby**
- **Low I_{DD} Current Transients**
- **All Inputs, Including Clocks, TTL Compatible**
- **Non-Latched Output is Three-State, TTL Compatible**
- **$\overline{RAS}$ Only Refresh**
- **64 Refresh Cycles Required Every 2ms**
- **Page Mode Capability**
- **$\overline{CAS}$ Controlled Output Allows Hidden Refresh**

The Intel® 2109 is a 8,192 word by 1-bit Dynamic MOS RAM which is pin compatible with the industry standard 16K dynamic RAMs. The 2109 is manufactured with the same masks as the Intel® 2117 and is fabricated with Intel's standard two layer polysilicon NMOS technology — a production proven process for high reliability, high performance, and high storage density. As is shown in the block diagram below, the device is organized as two 8K arrays separated by sense amplifiers and column decoders. The selected 8K array is tested for all of the A.C. and D.C. characteristics necessary to permit the 2109 to be considered a functionally compatible 8K version of the 16K device.

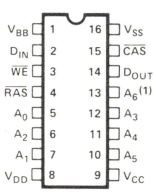
The 2109 uses a single transistor dynamic storage cell and advanced dynamic circuitry to achieve high speed with low power dissipation. The circuit design minimizes the current transients typical of dynamic RAM operation. These low current transients and ±10% tolerance on all power supplies contribute to the high noise immunity of the 2109 in a system environment.

The 2109 is available as either an "upper" or "lower" half of the 2117. Row Address 6 (A_6) selects the operating half, and is V_{IH} for S6000, S6002, S6064 and S6066 specifications and A_6 is V_{IL} for S6001, S6003, S6065 and S6067 specifications.

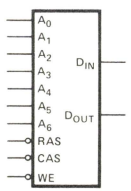
The 2109 three-state output is controlled by Column Address Strobe ($\overline{CAS}$) independent of Row Address Strobe ($\overline{RAS}$). After a valid read or read-modify-write cycle, data is latched on the output by holding $\overline{CAS}$ low. The data out pin is returned to the high impedance state by returning $\overline{CAS}$ to a high state. The 2109 hidden refresh feature allows $\overline{CAS}$ to be held low to maintain latched data while $\overline{RAS}$ is used to execute $\overline{RAS}$-Only refresh cycles.

The single transistor storage cell requires refreshing for data retention. Refreshing is accomplished by performing $\overline{RAS}$-Only refresh cycles, hidden refresh cycles, or normal read or write cycles on the 64 row address combinations of A_0 through A_5. A_6 must be at its proper state (V_{IH} or V_{IL} depending on the device specification) for 64 cycle refresh. A write cycle will refresh stored data on all bits of the selected row except the bit which is addressed.

PIN CONFIGURATION



LOGIC SYMBOL

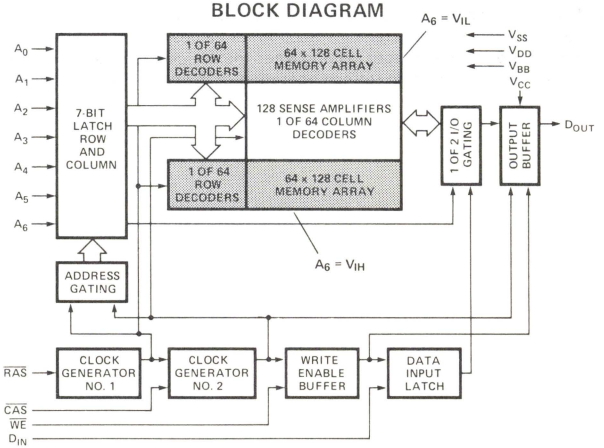


NOTE 1: S6000, S6002: A_6 AT V_{IH} DURING ROW ADDRESS VALID
S6001, S6003: A_6 AT V_{IL} DURING ROW ADDRESS VALID

PIN NAMES

A_0-A_6	ADDRESS INPUTS	$\overline{WE}$	WRITE ENABLE
$\overline{CAS}$	COLUMN ADDRESS STROBE	V_{BB}	POWER (-5V)
D_{IN}	DATA IN	V_{CC}	POWER (+5V)
D_{OUT}	DATA OUT	V_{DD}	POWER (+12V)
$\overline{RAS}$	ROW ADDRESS STROBE	V_{SS}	GROUND

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ... -10°C to +80°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin Relative to V_{BB}
($V_{SS} - V_{BB} \geq 4V$) ..... -0.3V to +20V
Data Out Current 50mA
Power Dissipation 1.0W

COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

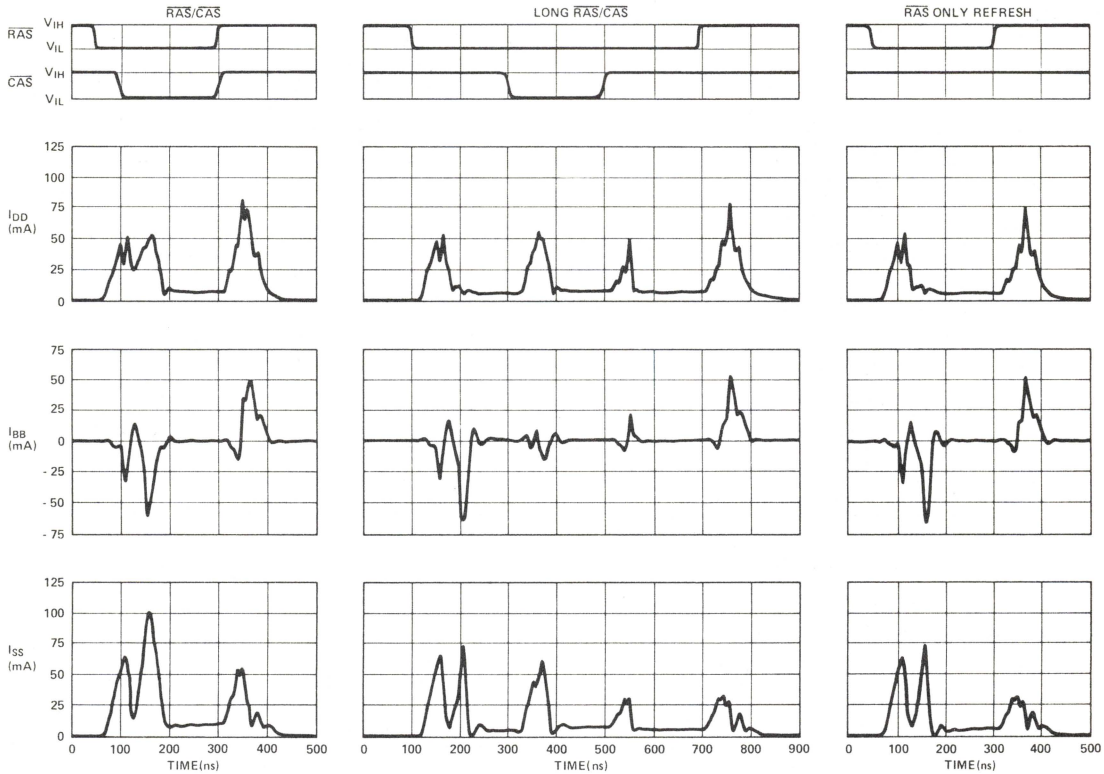
D.C. AND OPERATING CHARACTERISTICS[1,2]

T_A = 0°C to 70°C, V_{DD} = 12V ±10%, V_{CC} = 5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Limits Min.	Typ.[3]	Max.	Unit	Test Conditions	Notes
$\|I_{LI}\|$	Input Load Current (any input)		0.1	10	µA	V_{IN}=V_{SS} to 7.0V, V_{BB}=-5.0V	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State		0.1	10	µA	Chip Deselected: $\overline{CAS}$ at V_{IH}, V_{OUT} = 0 to 5.5V	
I_{DD1}	V_{DD} Supply Current, Standby			1.5	mA	$\overline{CAS}$ and $\overline{RAS}$ at V_{IH}	4
I_{BB1}	V_{BB} Supply Current, Standby		1.0	50	µA		
I_{CC1}	V_{CC} Supply Current, Output Deselected		0.1	10	µA	$\overline{CAS}$ at V_{IH}	5
I_{DD2}	V_{DD} Supply Current, Operating			35	mA	2109-3, t_{RC} = 375ns, t_{RAS} = 200ns	4
				33	mA	2109-4, t_{RC} = 410ns, t_{RAS} = 250ns	4
I_{BB2}	V_{BB} Supply Current, Operating, $\overline{RAS}$-Only Refresh, Page Mode		150	300	µA	T_A = 0°C	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh			27	mA	2109-3, t_{RC} = 375ns, t_{RAS} = 200ns	4
				26	mA	2109-4, t_{RC} = 410ns, t_{RAS} = 250ns	4
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled		1.5	3	mA	$\overline{CAS}$ at V_{IL}, $\overline{RAS}$ at V_{IH}	
V_{IL}	Input Low Voltage (all inputs)	-1.0		0.8	V		
V_{IH}	Input High Voltage (all inputs)	2.4		6.0	V		
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.2mA	4
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -5mA	4

NOTES:
1. All voltages referenced to V_{SS}.
2. No power supply sequencing is required. However, V_{DD}, V_{CC} and V_{SS} should never be more negative than -0.3V with respect to V_{BB} as required by the absolute maximum ratings.
3. Typical values are for T_A = 25°C and nominal supply voltages.
4. See the Typical Characteristics Section for values of this parameter under alternate conditions.
5. I_{CC} is dependent on output loading when the device output is selected. V_{CC} is connected to the output buffer only. V_{CC} may be reduced to V_{SS} without affecting refresh operation or maintenance of internal device data.

TYPICAL SUPPLY CURRENT WAVEFORMS



Typical power supply current waveforms vs. time are shown for the $\overline{RAS}/\overline{CAS}$ timings of Read/Write, Read/Write (Long $\overline{RAS}/\overline{CAS}$), and $\overline{RAS}$-only refresh cycles. I_{DD} and I_{BB} current transients at the $\overline{RAS}$ and $\overline{CAS}$ edges require adequate decoupling of these supplies. Decoupling recommendations are provided in the Applications section.

The effects of cycle time, V_{DD} supply voltage and ambient temperature on the I_{DD} current are shown in graphs included in the Typical Characteristics Section. Each family of curves for I_{DD1}, I_{DD2}, and I_{DD3} is related by a common point at $V_{DD} = 12.0V$ and $T_A = 25°C$ for two given t_{RAS} pulse widths. The typical I_{DD} current for a given condition of cycle time, V_{DD} and T_A can be determined by combining the effects of the appropriate family of curves.

CAPACITANCE [1]

$T_A = 25°C$, $V_{DD} = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $V_{BB} = -5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise specified.

Symbol	Parameter	Typ.	Max.	Unit
C_{I1}	Address, Data In	3	5	pF
C_{I2}	$\overline{RAS}$ Capacitance, $\overline{WE}$ Capacitance	4	7	pF
C_{I3}	$\overline{CAS}$ Capacitance	6	10	pF
C_O	Data Output Capacitance	4	7	pF

NOTES:
1. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation:
   $C = \frac{I \Delta t}{\Delta V}$ with ΔV equal to 3 volts and power supplies at nominal levels.

A.C. CHARACTERISTICS[1,2,3]

T_A = 0°C to 70°C, V_{DD} = 12V ±10%, V_{CC} = 5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, unless otherwise noted.

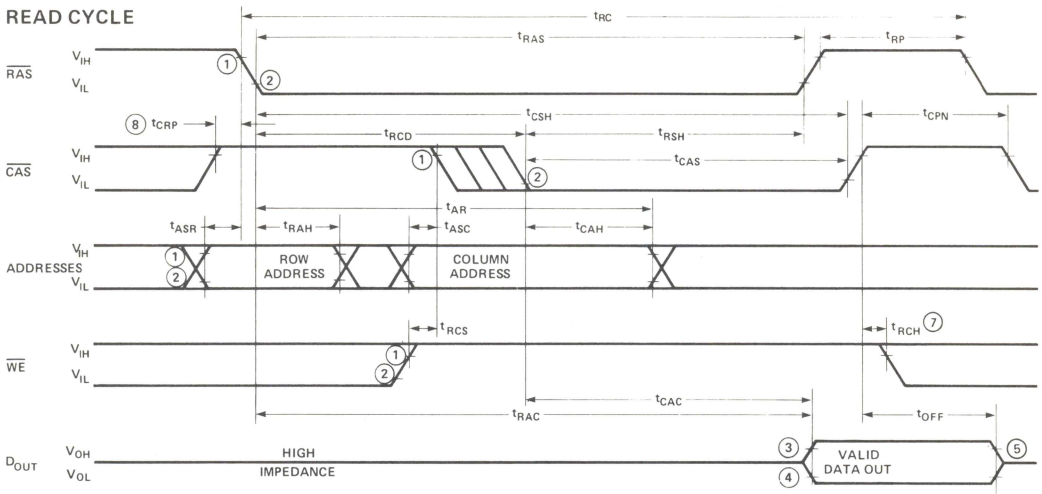
READ, WRITE, READ-MODIFY-WRITE AND REFRESH CYCLES

Symbol	Parameter	2109-3 S6000,S6001 Min.	2109-3 S6000,S6001 Max.	2109-4 S6002,S6003 Min.	2109-4 S6002,S6003 Max.	Unit	Notes
t_{RAC}	Access Time From $\overline{RAS}$		200		250	ns	4,5
t_{CAC}	Access Time From $\overline{CAS}$		135		165	ns	4,5,6
t_{REF}	Time Between Refresh		2		2	ms	
t_{RP}	$\overline{RAS}$ Precharge Time	120		150		ns	
t_{CPN}	$\overline{CAS}$ Precharge Time(non-page cycles)	25		25		ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	-20		-20		ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	65	35	85	ns	7
t_{RSH}	$\overline{RAS}$ Hold Time	135		165		ns	
t_{CSH}	$\overline{CAS}$ Hold Time	200		250		ns	
t_{ASR}	Row Address Set-Up Time	0		0		ns	
t_{RAH}	Row Address Hold Time	25		35		ns	
t_{ASC}	Column Address Set-Up Time	-10		-10		ns	
t_{CAH}	Column Address Hold Time	55		75		ns	
t_{AR}	Column Address Hold Time, to $\overline{RAS}$	120		160		ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	8
t_{OFF}	Output Buffer Turn Off Delay	0	60	0	70	ns	
READ AND REFRESH CYCLES							
t_{RC}	Random Read Cycle Time	375		410		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	200	10000	250	10000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	135	10000	165	10000	ns	
t_{RCS}	Read Command Set-Up Time	0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		ns	
WRITE CYCLE							
t_{RC}	Random Write Cycle Time	375		410		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	200	10000	250	10000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	135	10000	165	10000	ns	
t_{WCS}	Write Command Set-Up Time	-20		-20		ns	9
t_{WCH}	Write Command Hold Time	55		75		ns	
t_{WCR}	Write Command Hold Time, to $\overline{RAS}$	120		160		ns	
t_{WP}	Write Command Pulse Width	55		75		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	80		100		ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	80		100		ns	
t_{DS}	Data-In Set-Up Time	0		0		ns	
t_{DH}	Data-In Hold Time	55		75		ns	
t_{DHR}	Data-In Hold Time, to $\overline{RAS}$	120		160		ns	
READ-MODIFY-WRITE CYCLE							
t_{RWC}	Read-Modify-Write Cycle Time	375		475		ns	
t_{RRW}	RMW Cycle $\overline{RAS}$ Pulse Width	245	10000	305	10000	ns	
t_{CRW}	RMW Cycle $\overline{CAS}$ Pulse Width	180	10000	230	10000	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	160		200		ns	9
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	95		125		ns	9

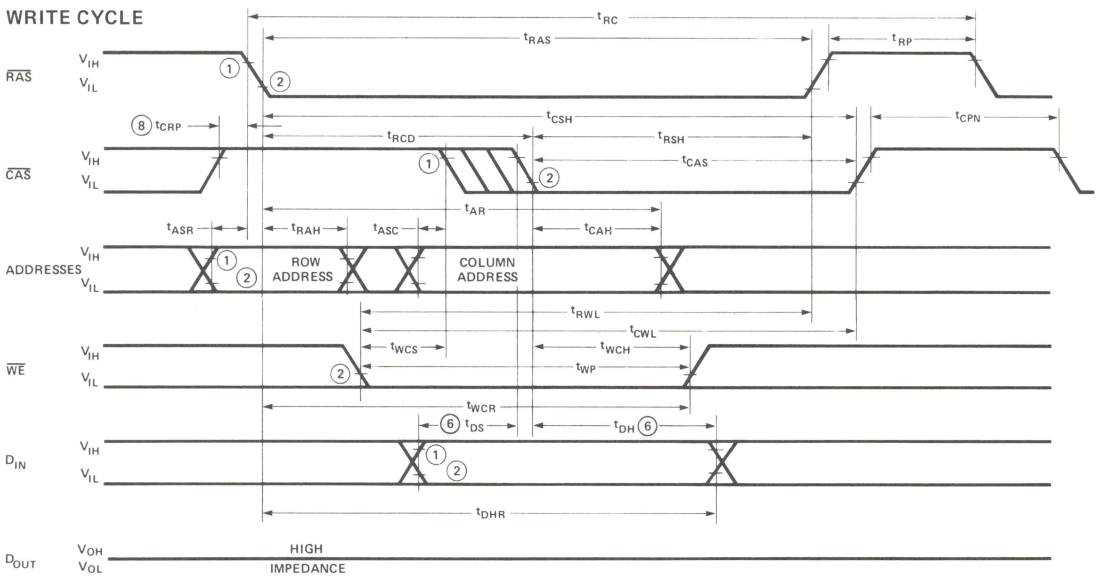
Notes: See following page for A.C. Characteristics Notes.

WAVEFORMS

READ CYCLE



WRITE CYCLE



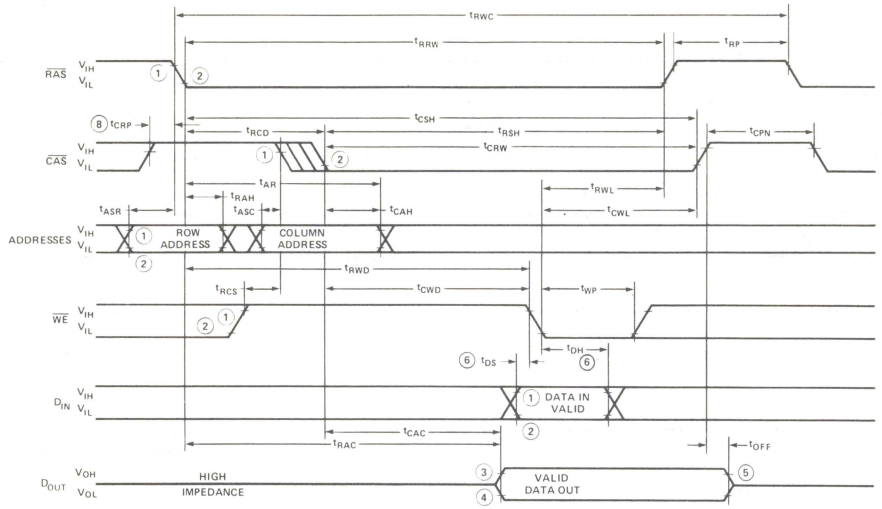
NOTES: 1,2. $V_{IH\ MIN}$ AND $V_{IL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF INPUT SIGNALS.
3,4. $V_{OH\ MIN}$ AND $V_{OL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF D_{OUT}.
5. t_{OFF} IS MEASURED TO $I_{OUT} \leq |I_{LO}|$.
6. t_{DS} AND t_{DH} ARE REFERENCED TO $\overline{CAS}$ OR $\overline{WE}$, WHICHEVER OCCURS LAST.
7. t_{RCH} IS REFERENCED TO THE TRAILING EDGE OF $\overline{CAS}$ OR $\overline{RAS}$, WHICHEVER OCCURS FIRST.
8. t_{CRP} REQUIREMENT IS ONLY APPLICABLE FOR $\overline{RAS}$/$\overline{CAS}$ CYCLES PRECEEDED BY A $\overline{CAS}$-ONLY CYCLE (i.e., FOR SYSTEMS WHERE $\overline{CAS}$ HAS NOT BEEN DECODED WITH $\overline{RAS}$).

A.C. CHARACTERISTICS NOTES (From Previous Page)

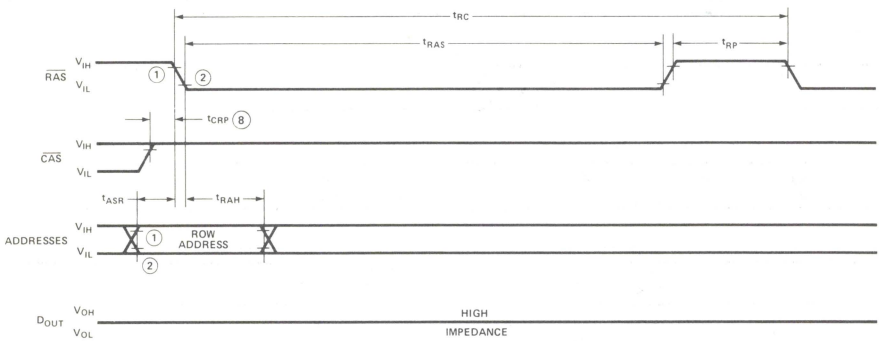
1. All voltages referenced to V_{SS}.
2. Eight cycles are required after power-up or prolonged periods (greater than 2ms) of $\overline{RAS}$ inactivity before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
3. A.C. Characteristics assume t_T = 5ns.
4. Assume that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.) then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
5. Load = 2 TTL loads and 100pF.
6. Assumes $t_{RCD} \geq t_{RCD}$ (max.).
7. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is less than t_{RCD} (max.) access time is t_{RAC}, if t_{RCD} is greater than t_{RCD} (max.) access time is $t_{RCD} + t_{CAC}$.
8. t_T is measured between V_{IH} (min.) and V_{IL} (max.).
9. t_{WCS}, t_{CWD} and t_{RWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}$ (min.) the cycle is an early write cycle and the data out pin will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} \geq t_{RWD}$ (min.), the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.

WAVEFORMS

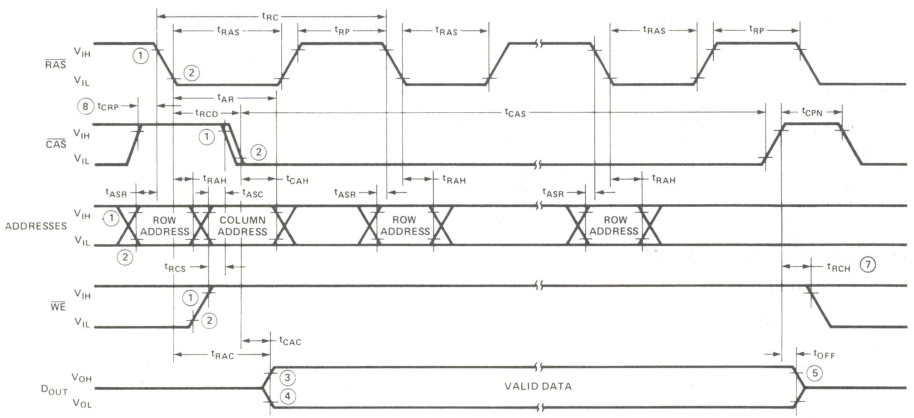
READ-MODIFY-WRITE CYCLE



RAS-ONLY REFRESH CYCLE



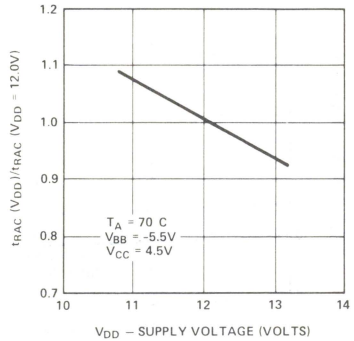
HIDDEN REFRESH CYCLE



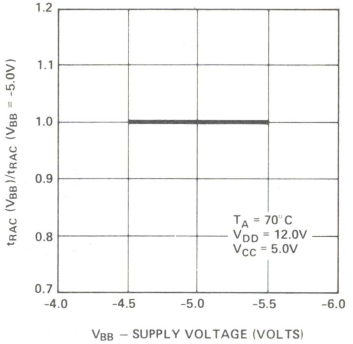
NOTES:
1,2. $V_{IH\ MIN}$ AND $V_{IL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF INPUT SIGNALS.
3,4. $V_{OH\ MIN}$ AND $V_{OL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF D_{OUT}.
5. t_{OFF} IS MEASURED TO $|I_{OUT}| \leq |I_{LO}|$.
6. t_{DS} AND t_{DH} ARE REFERENCED TO $\overline{CAS}$ OR $\overline{WE}$, WHICHEVER OCCURS LAST.
7. t_{RCH} IS REFERENCED TO THE TRAILING EDGE OF $\overline{CAS}$ OR $\overline{RAS}$, WHICHEVER OCCURS FIRST.
8. t_{CRP} REQUIREMENT IS ONLY APPLICABLE FOR $\overline{RAS}$/$\overline{CAS}$ CYCLES PRECEEDED BY A $\overline{CAS}$-ONLY CYCLE (i.e., FOR SYSTEMS WHERE $\overline{CAS}$ HAS NOT BEEN DECODED WITH $\overline{RAS}$).

TYPICAL CHARACTERISTICS[1]

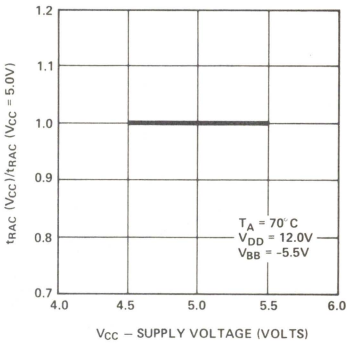
GRAPH 1
TYPICAL ACCESS TIME
t_{RAC} (NORMALIZED) VS. V_{DD}



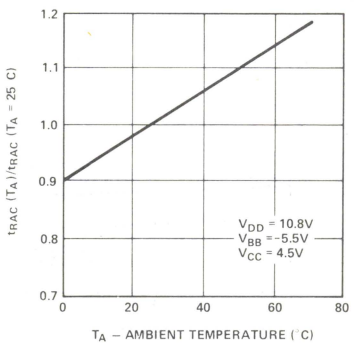
GRAPH 2
TYPICAL ACCESS TIME
t_{RAC} (NORMALIZED) VS. V_{BB}



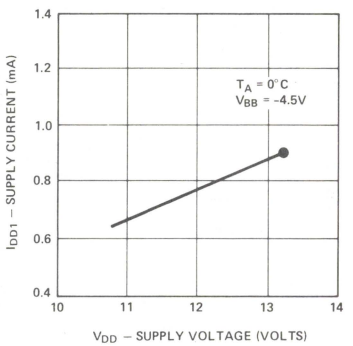
GRAPH 3
TYPICAL ACCESS TIME
t_{RAC} (NORMALIZED) VS. V_{CC}



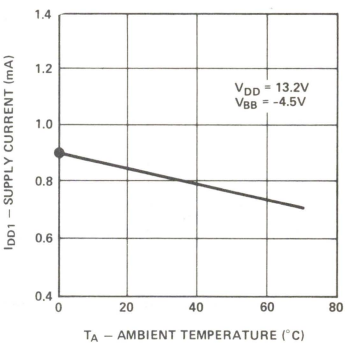
GRAPH 4
TYPICAL ACCESS TIME
t_{RAC} (NORMALIZED) VS.
AMBIENT TEMPERATURE



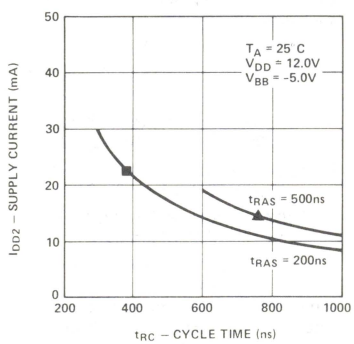
GRAPH 5
TYPICAL STANDBY CURRENT
I_{DD1} VS. V_{DD}



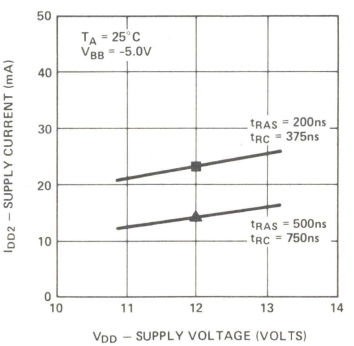
GRAPH 6
TYPICAL STANDBY CURRENT
I_{DD1} VS. AMBIENT TEMPERATURE



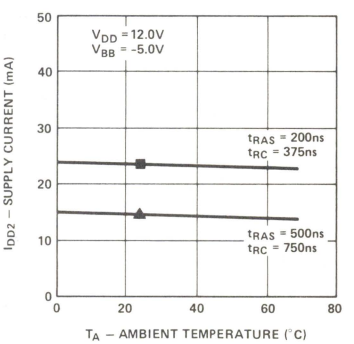
GRAPH 7
TYPICAL OPERATING CURRENT
I_{DD2} VS. t_{RC}



GRAPH 8
TYPICAL OPERATING CURRENT
I_{DD2} VS. V_{DD}



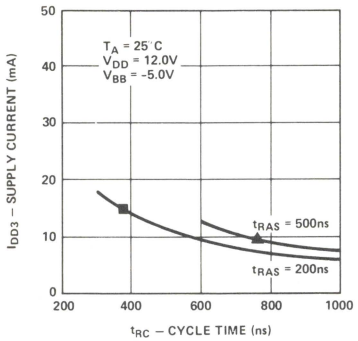
GRAPH 9
TYPICAL OPERATING CURRENT
I_{DD2} VS. AMBIENT TEMPERATURE



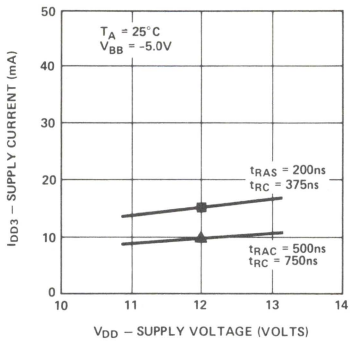
NOTES: See following page for Typical Characteristics Notes.

TYPICAL CHARACTERISTICS [1]

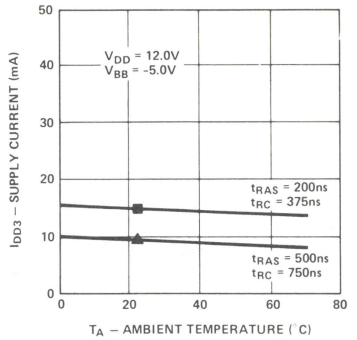
GRAPH 10
TYPICAL $\overline{RAS}$ ONLY
REFRESH CURRENT
I_{DD3} VS. t_{RC}



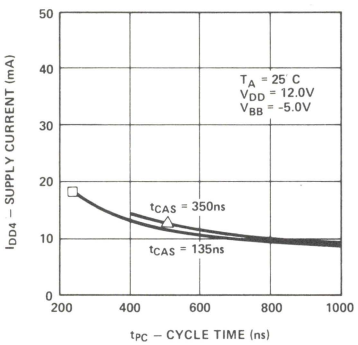
GRAPH 11
TYPICAL $\overline{RAS}$ ONLY
REFRESH CURRENT
I_{DD3} VS. V_{DD}



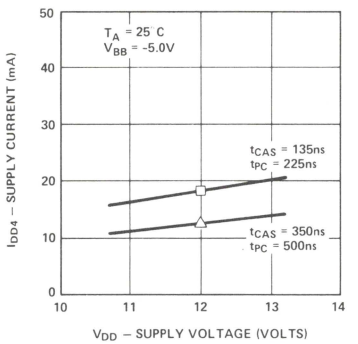
GRAPH 12
TYPICAL $\overline{RAS}$ ONLY
REFRESH CURRENT
I_{DD3} VS. AMBIENT TEMPERATURE



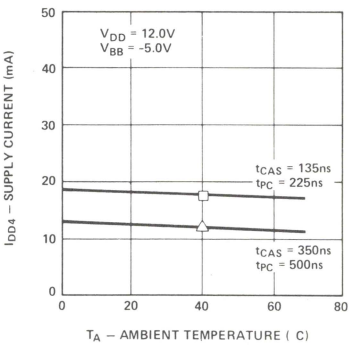
GRAPH 13
TYPICAL PAGE MODE CURRENT
I_{DD4} VS. t_{PC}



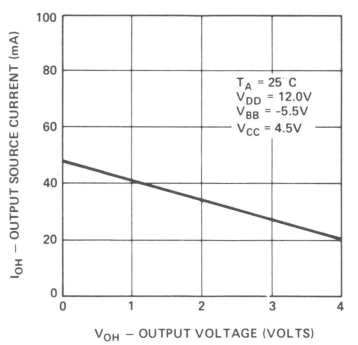
GRAPH 14
TYPICAL PAGE MODE CURRENT
I_{DD4} VS. V_{DD}



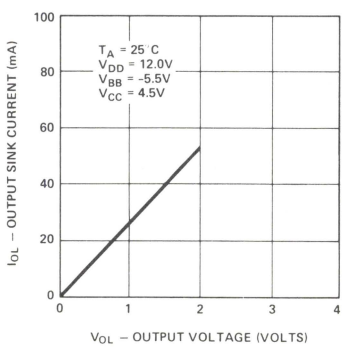
GRAPH 15
TYPICAL PAGE MODE CURRENT
I_{DD4} VS. AMBIENT TEMPERATURE



GRAPH 16
TYPICAL OUTPUT SOURCE CURRENT
I_{OH} VS. OUTPUT VOLTAGE V_{OH}



GRAPH 17
TYPICAL OUTPUT SINK CURRENT
I_{OL} VS. OUTPUT VOLTAGE V_{OL}



NOTES:

1. The cycle time, V_{DD}, supply voltage, and ambient temperature dependence of I_{DD1}, I_{DD2}, I_{DD3} and I_{DD4} is shown in related graphs. Common points of related curves are indicated:
   - ● I_{DD1} @ V_{DD} = 13.2V, T_A = 0°C
   - ■ I_{DD2} or I_{DD3} @ t_{RAS} = 200ns, t_{RC} = 375ns, V_{DD} = 12.0V, T_A = 25°C
   - ▲ I_{DD2} or I_{DD3} @ t_{RAS} = 500ns, t_{RC} = 750ns, V_{DD} = 12.0V, T_A = 25°C
   - □ I_{DD4} @ t_{CAS} = 135ns, t_{PC} = 225ns, V_{DD} = 12.0V, T_A = 25°C
   - △ I_{DD4} @ t_{CAS} = 350ns, t_{PC} = 500ns, V_{DD} = 12.0V, T_A = 25°C

   The typical I_{DD} current for a given combination of cycle time, V_{DD} supply voltage and ambient temperature may be determined by combining the effects of the appropriate family of curves.

D.C. AND A.C. CHARACTERISTICS, PAGE MODE [7,8,11]

T_A = 0°C to 70°C, V_{DD} = 12V±10%, V_{CC} = 5V±10%, V_{BB} = -5V±10%, V_{SS} = 0V, unless otherwise noted.

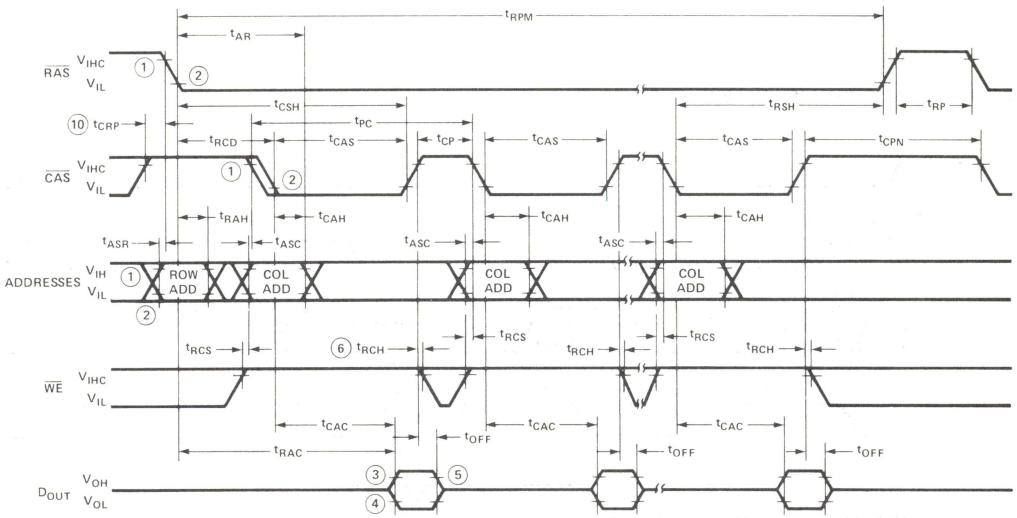
For Page Mode Operation order: 2109-3* S6064, S6065 or 2109-4* S6066, S6067.

Symbol	Parameter	2109-3 S6064,S6065		2109-4 S6066,S6067		Unit	Notes
		Min.	Max.	Min.	Max.		
t_{PC}	Page Mode Read or Write Cycle	225		275		ns	
t_{PCM}	Page Mode Read Modify Write	270		340		ns	
t_{CP}	$\overline{CAS}$ Precharge Time, Page Cycle	80		100		ns	
t_{RPM}	$\overline{RAS}$ Pulse Width, Page Mode	200	10,000	250	10,000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	135	10,000	165	10,000	ns	
I_{DD4}	V_{DD} Supply Current Page Mode, Minimum t_{PC}, Minimum t_{CAS}		30		26	mA	9

***S6064, S6066: A6 at VIH during Row Address Valid.**
S6065, S6067: A6 at VIL during Row Address Valid.

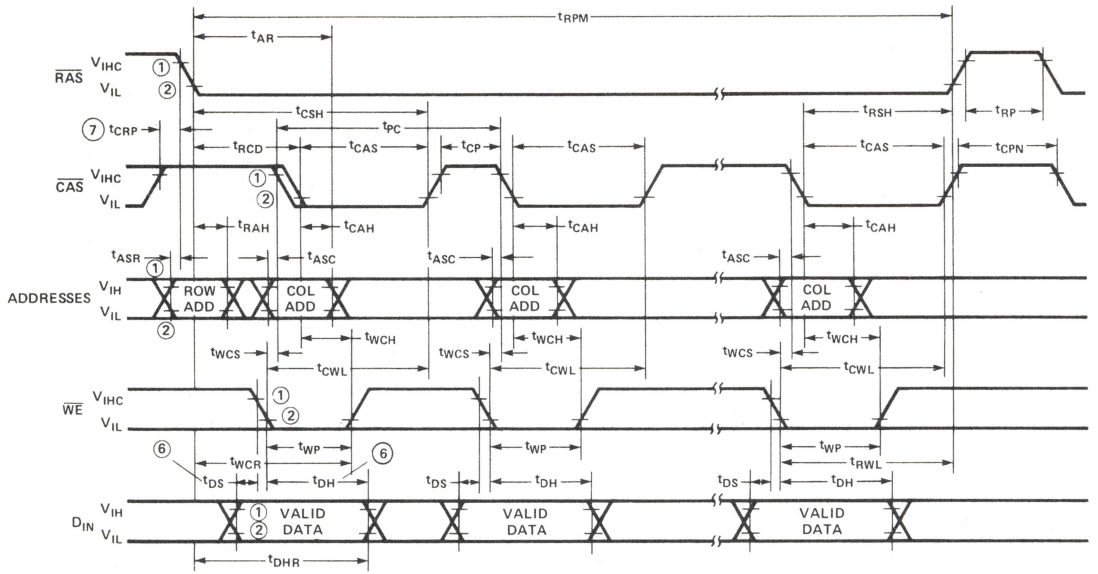
WAVEFORMS

PAGE MODE READ CYCLE

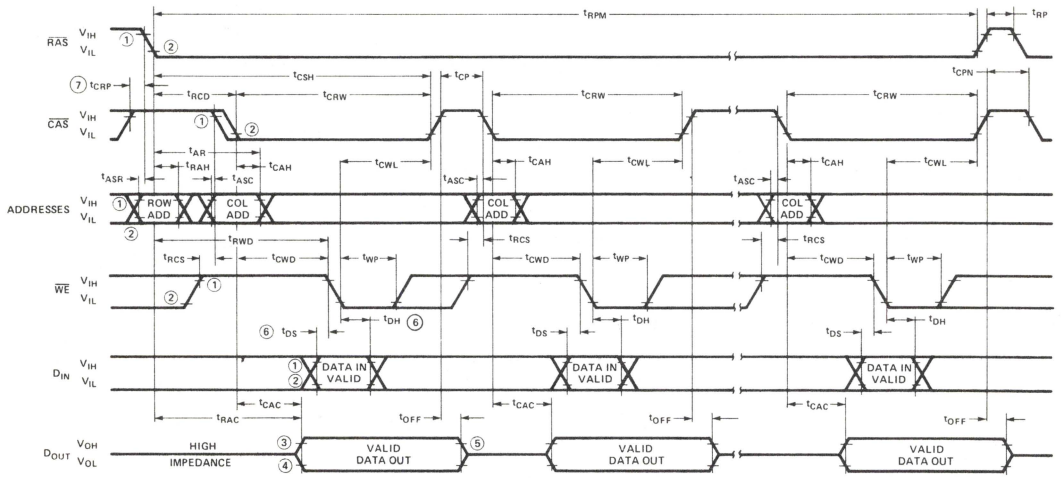


NOTES:
1,2. $V_{IH\ MIN}$ AND $V_{IL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF INPUT SIGNALS.
3,4. $V_{OH\ MIN}$ AND $V_{OL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF D_{OUT}.
5. t_{OFF} IS MEASURED TO $|I_{OUT}| = |I_{LO}|$.
6. t_{RCH} IS REFERENCED TO THE TRAILING EDGE OF $\overline{CAS}$ OR $\overline{RAS}$, WHICHEVER OCCURS FIRST.
7. ALL VOLTAGES REFERENCED TO V_{SS}.
8. AC CHARACTERISTIC ASSUME t_T = 5ns.
9. SEE THE TYPICAL CHARACTERISTICS SECTION FOR VALUES OF THIS PARAMETER UNDER ALTERNATE CONDITIONS.
10. t_{CRP} REQUIREMENT IS ONLY APPLICABLE FOR $\overline{RAS}$/$\overline{CAS}$ CYCLES PRECEEDED BY A $\overline{CAS}$-ONLY CYCLE (i.e., FOR SYSTEMS WHERE $\overline{CAS}$ HAS NOT BEEN DECODED WITH $\overline{RAS}$).
11. ALL PREVIOUSLY SPECIFIED A.C. AND D.C. CHARACTERISTICS ARE APPLICABLE TO THEIR RESPECTIVE PAGE MODE DEVICE (i.e., 2109-3, S6064 OR S6065 WILL OPERATE AS A 2109-3).

PAGE MODE WRITE CYCLE



PAGE MODE READ-MODIFY-WRITE CYCLE



NOTES: 1,2. $V_{IH\ MIN}$ AND $V_{IL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF INPUT SIGNALS.
3,4. $V_{OH\ MIN}$ AND $V_{OL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF D_{OUT}.
5. t_{OFF} IS MEASURED TO $I_{OUT} \leq |I_{LO}|$.
6. t_{DS} AND t_{DH} ARE REFERENCED TO $\overline{CAS}$ OR $\overline{WE}$, WHICHEVER OCCURS LAST.
7. t_{CRP} REQUIREMENT IS ONLY APPLICABLE FOR $\overline{RAS}$/$\overline{CAS}$ CYCLES PRECEEDED BY A $\overline{CAS}$-ONLY CYCLE (i.e., FOR SYSTEMS WHERE $\overline{CAS}$ HAS NOT BEEN DECODED WITH $\overline{RAS}$).

APPLICATIONS

The 2109 is packaged in a standard 16-pin DIP by multiplexing 14 address bits onto 7 input pins (A_0-A_6). The 7 bit address words are latched into the 2109 by two TTL clocks, Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). Since the 2109 is an 8K memory device, only 13 of the 14 address bits are required and the 14th address bit must be at V_{IH} (for S6000, S6002, S6064 or S6066) or V_{IL} (for S6001, S6003, S6065 or S6067) during Row Address Valid. This means it is not possible to simply tie input pin A_6 high or low, since it supplies two system addresses to the memory array. Input pin A_6 must be at the appropriate level (determined by the "S"-specification) during the row address valid period and then changed to the proper high order address during the column address valid period.

READ CYCLE

A Read cycle is performed by maintaining Write Enable ($\overline{WE}$) high during a $\overline{RAS}/\overline{CAS}$ operation. The output pin of a selected device will remain in a high impedance state until valid data appears at the output at access time.

Device access time, t_{ACC}, is the longer of the two calculated intervals:

1. $t_{ACC} = t_{RAC}$ OR 2. $t_{ACC} = t_{RCD} + t_{CAC}$

Access time from $\overline{RAS}$, t_{RAC}, and access time from $\overline{CAS}$, t_{CAC}, are device parameters. Row to column address strobe delay time, t_{RCD}, are system dependent timing parameters. For example, substituting the device parameters of the 2109-3 yields:

3. $t_{ACC} = t_{RAC} = 200\text{nsec}$ for $25\text{nsec} \leq t_{RCL} \leq 65$ nsec

OR

4. $t_{ACC} = t_{RCD} + t_{CAC} = t_{RCD} + 135$ for $t_{RCD} > 65\text{nsec}$

Note that if $25\text{nsec} \leq t_{RCD} \leq 65\text{nsec}$ device access time is determined by equation 3 and is equal to t_{RAC}. If $t_{RCL} > 65\text{nsec}$, access time is determined by equation 4. This 40nsec interval (shown in the t_{RCD} inequality in equation 3) in which the falling edge of $\overline{CAS}$ can occur without affecting access time is provided to allow for system timing skew in the generation of $\overline{CAS}$.

REFRESH CYCLES

Each of the 64 rows of the 2109 must be refreshed every 2 milliseconds to maintain data. Any memory cycle:

1. Read Cycle
2. Write Cycle (Early Write, Delayed Write or Read-Modify-Write)
3. $\overline{RAS}$-only Cycle

refreshes the selected row as defined by the low order ($\overline{RAS}$) addresses. A_6 must be held at the proper level (V_{IH} or V_{IL} depending on specification) to perform 64 cycle refresh operation, but may be driven high and low for 128 cycle $\overline{RAS}$-only refresh without affecting device data retention. Any Write cycle, of course, may change the state of the selected cell. Using a Read, Write, or Read-Modify-Write cycle for refresh is not recommended for systems which utilize "wire-OR" outputs since output bus contention will occur.

A $\overline{RAS}$-only refresh cycle is the recommended technique for most applications to provide for data retention. A $\overline{RAS}$-only refresh cycle maintains the D_{OUT} in the high impedance state with a typical power reduction of 20% over a Read or Write cycle.

$\overline{RAS}/\overline{CAS}$ TIMING

$\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths as defined by t_{RAS} and t_{CAS} respectively. These minimum pulse widths must be maintained for proper device operation and data integrity. A cycle, once begun by driving $\overline{RAS}$ and/or $\overline{CAS}$ low must not be ended or aborted prior to fulfilling the minimum clock signal pulse width(s). A new cycle can not begin until the minimum precharge time, t_{RP}, has been met.

DATA OUTPUT OPERATION

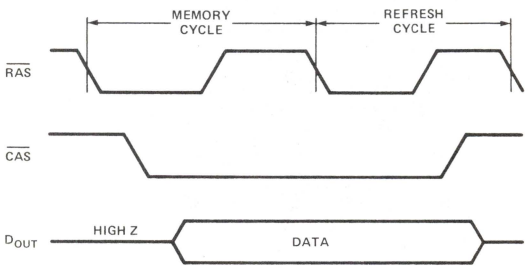
The 2109 Data Output (D_{OUT}), which has three-state capability, is controlled by $\overline{CAS}$. During $\overline{CAS}$ high state ($\overline{CAS}$ at V_{IH}) the output is in the high impedance state. The following table summarizes the D_{OUT} state for various types of cycles.

Intel 2109 Data Output Operation for Various Types of Cycles

Type of Cycle	D_{OUT} State
Read Cycle	Data From Addressed Memory Cell
Fast Write Cycle	HI-Z
$\overline{RAS}$-Only Refresh Cycle	HI-Z
$\overline{CAS}$-Only Cycle	HI-Z
Read/Modify/Write Cycle	Data From Addressed Memory Cell
Delayed Write Cycle	Indeterminate

HIDDEN REFRESH

A feature of the 2109 is that refresh cycles may be performed while maintaining valid data at the output pin. This feature is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a "$\overline{RAS}$-Only" refresh cycle, but with $\overline{CAS}$ held low (see Figure below).



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

POWER ON

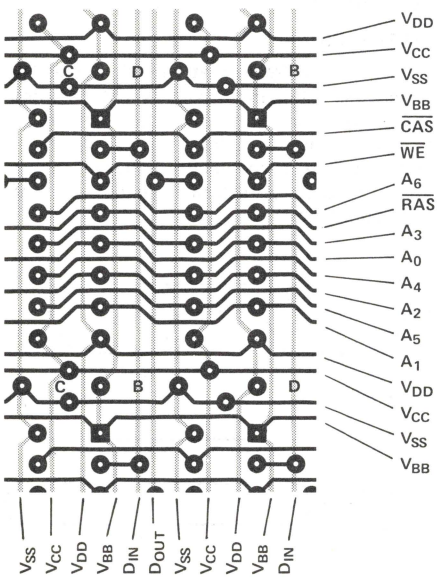
The 2109 requires no power on sequence providing absolute maximum ratings are not exceeded. After the application of supply voltages or after extended periods of bias (greater than 2 milliseconds) without clocks, the device must perform a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock, such as $\overline{RAS}$-Only refresh) prior to normal operation.

POWER SUPPLY DECOUPLING/DISTRIBUTION

It is recommended that a 0.1μF ceramic capacitor be connected between V_{DD} and V_{SS} at every other device in the memory array. A 0.1μF ceramic capacitor should also be connected between V_{BB} and V_{SS} at every other device (preferably the alternate devices to the V_{DD} decoupling). For each 16 devices, a 10μF tantalum or equivalent capacitor should be connected between V_{DD} and V_{SS} near the array. An equal or slightly smaller bulk capacitor is also recommended between V_{BB} and V_{SS} for every 32 devices.

The V_{CC} supply is connected only to the 2109 output buffer and is not used internally. The load current from the V_{CC} supply is dependent only upon the output loading and is associated with the input high level current to a TTL gate and the output leakage currents of any OR-tied 2109's (typically 100μA or less total). Intel recommends that a 0.1 or 0.01μF ceramic capacitor be connected between V_{CC} and V_{SS} for every eight memory devices.

Due to the high frequency characteristics of the current waveforms, the inductance of the power supply distribution system on the array board should be minimized. It is recommended that the V_{DD}, V_{BB}, and V_{SS} supply lines be gridded both horizontally and vertically at each device in the array. This technique allows use of double sided circuit boards with noise performance equal to or better than multi-layered circuit boards.



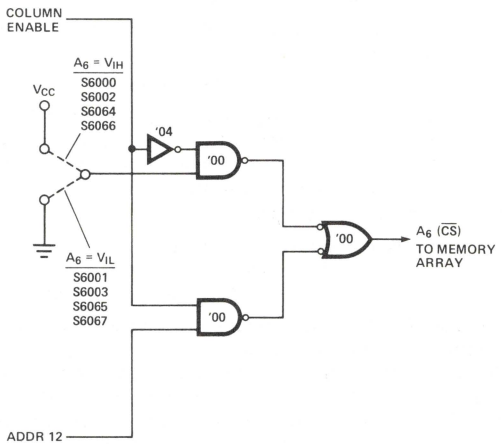
DECOUPLING CAPACITORS
D = 0.1μF TO V_{DD} TO V_{SS}
B = 0.1μF V_{BB} TO V_{SS}
C = 0.01μF V_{CC} TO V_{SS}

SAMPLE P.C. BOARD LAYOUT EMPLOYING VERTICAL AND HORIZONTAL GRIDDING ON ALL POWER SUPPLIES.

8K UPGRADE FOR 4K SYSTEMS

The 2109 can be used to upgrade existing 4K (Intel 2104A) memory systems with minimal redesign. The 2109 maintains many of the features of the 4K RAMs. For example, the latched data output of the 4Ks can be emulated by holding $\overline{CAS}$ low to maintain data out valid. Hidden refresh capability for the 4Ks is also maintained with the 2109. The 64 cycle refresh operation of the 2109 makes it compatible with 4K systems.

To upgrade a 4K system to accept the 2109, an extra memory address multiplexer must be implemented to replace the Chip Select ($\overline{CS}$) input of the 4Ks. The replacement circuitry is shown in the figure below, and involves some gating to control the output of the multiplexer during row and column address valid periods and also some control to handle the multiplexer during refresh operation.



2111A/8111A-4*
256 x 4 BIT STATIC RAM

2111A-2	250 ns Max.
2111A	350 ns Max.
2111A-4	450 ns Max.

- **Common Data Input and Output**
- **Single +5V Supply Voltage**
- **Directly TTL Compatible: All Inputs and Output**
- **Static MOS: No Clocks or Refreshing Required**
- **Simple Memory Expansion: Chip Enable Input**
- **Fully Decoded: On Chip Address Decode**
- **Inputs Protected: All Inputs Have Protection Against Static Charge**
- **Low Cost Packaging: 18 Pin Plastic Dual In-Line Configuration**
- **Low Power: Typically 150 mW**
- **Three-State Output: OR-Tie Capability**

The Intel® 2111A is a 256 word by 4-bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

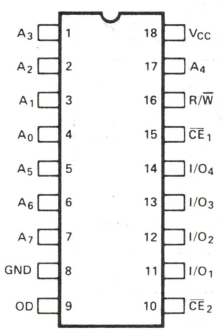
The 2111A is designed for memory applications in small systems where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Separate chip enable ($\overline{CE}$) leads allow easy selection of an individual package when outputs are OR-tied.

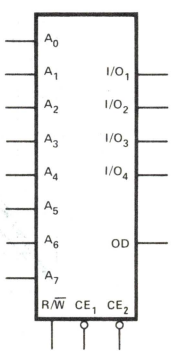
The Intel® 2111A is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost plastic packaging.

PIN CONFIGURATION



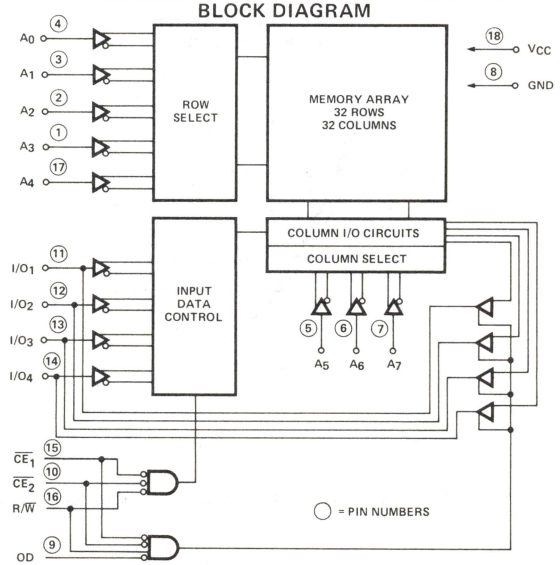
LOGIC SYMBOL



PIN NAMES

A_0-A_7	ADDRESS INPUTS
OD	OUTPUT DISABLE
$R/\overline{W}$	READ/WRITE INPUT
$\overline{CE}_1$	CHIP ENABLE 1
$\overline{CE}_2$	CHIP ENABLE 2
I/O_1- I/O_4	DATA INPUT/OUTPUT

BLOCK DIAGRAM



*All 8111A-4 specifications are identical to the 2111A-4 specifications.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . -10°C to 80°C

Storage Temperature . . . . . -65°C to +150°C

Voltage On Any Pin
With Respect to Ground . . . . . -0.5V to +7V

Power Dissipation . . . . . 1 Watt

*COMMENT:

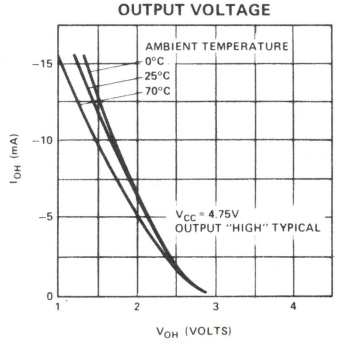
Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

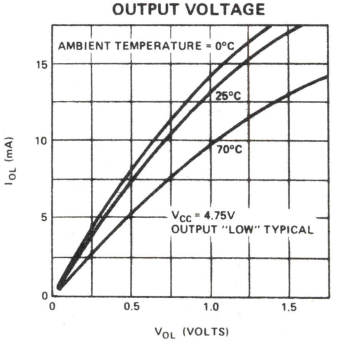
T_A = 0°C to 70°C, V_{CC} = 5V ±5% , unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Load Current		1	10	µA	V_{IN} = 0 to 5.25V
I_{LOH}	I/O Leakage Current		1	10	µA	Output Disabled, $V_{I/O}$ = 4.0V
I_{LOL}	I/O Leakage Current		-1	-10	µA	Output Disabled, $V_{I/O}$=0.45V
I_{CC1}	Power Supply Current 2111A, 2111A-4		35	55	mA	V_{IN} = 5.25V
	Power Supply Current 2111A-2		45	65	mA	$I_{I/O}$ = 0mA, T_A = 25°C
I_{CC2}	Power Supply Current 2111A, 2111A-4			60	mA	V_{IN} = 5.25V
	Power Supply Current 2111A-2			70	mA	$I_{I/O}$ = 0mA, T_A = 0°C
V_{IL}	Input Low Voltage	-0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.0mA
V_{OH}	Output High Voltage 2111A, 2111A-2	2.4			V	I_{OH} = -200µA
	Output High Voltage 2111A-4	2.4			V	I_{OH} = -150µA

OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

A.C. CHARACTERISTICS FOR 2111A-2 (250 ns ACCESS TIME)

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	250			ns	t_r, t_f = 20ns Input Levels = 0.8V or 2.0V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_A	Access Time			250	ns	
t_{CO}	Chip Enable To Output			180	ns	
t_{OD}	Output Disable To Output			130	ns	
t_{DF}[3]	Data Output to High Z State	0		180	ns	
t_{OH}	Previous Read Data Valid after change of Address	40			ns	

WRITE CYCLE

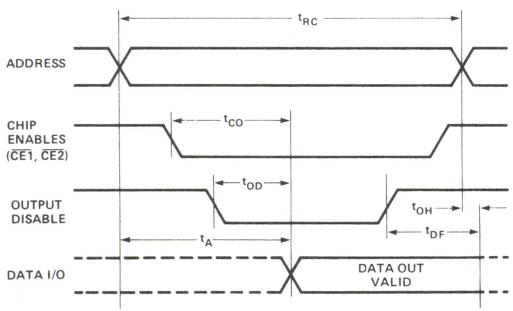
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	170			ns	t_r, t_f = 20ns Input Levels = 0.8V or 2.0V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_{AW}	Write Delay	20			ns	
t_{CW}	Chip Enable To Write	150			ns	
t_{DW}	Data Setup	150			ns	
t_{DH}	Data Hold	0			ns	
t_{WP}	Write Pulse	150			ns	
t_{WR}	Write Recovery	0			ns	
t_{DS}	Output Disable Setup	20			ns	

CAPACITANCE[2] $T_A = 25°C$, f = 1MHz

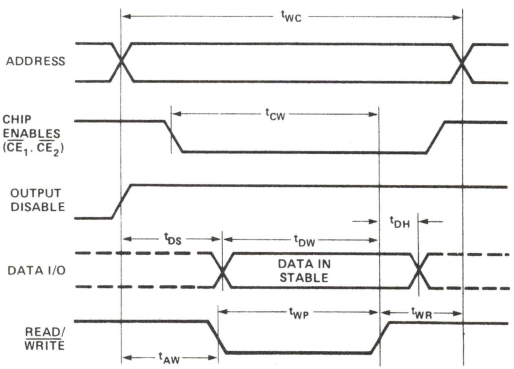
Symbol	Test	Limits (pF)	
		Typ.[1]	Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
$C_{I/O}$	I/O Capacitance $V_{I/O}$ = 0V	10	15

WAVEFORMS

READ CYCLE



WRITE CYCLE



NOTES: 1. Typical values are for $T_A = 25°C$ and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.
3. t_{DF} is with respect to the trailing edge of $\overline{CE_1}$, $\overline{CE_2}$, or OD, whichever occurs first.

2111A (350 ns ACCESS TIME)

A.C. CHARACTERISTICS

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	350			ns	t_r, t_f = 20ns Input Levels = 0.8V or 2.0V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_A	Access Time			350	ns	
t_{CO}	Chip Enable To Output			240	ns	
t_{OD}	Output Disable To Output			180	ns	
t_{DF} [2]	Data Output to High Z State	0		150	ns	
t_{OH}	Previous Read Data Valid after change of Address	40			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	220			ns	t_r, t_f = 20ns Input Levels = 0.8V or 2.0V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_{AW}	Write Delay	20			ns	
t_{CW}	Chip Enable To Write	200			ns	
t_{DW}	Data Setup	200			ns	
t_{DH}	Data Hold	0			ns	
t_{WP}	Write Pulse	200			ns	
t_{WR}	Write Recovery	0			ns	
t_{DS}	Output Disable Setup	20			ns	

2111A-4 (450 ns ACCESS TIME)

A.C. CHARACTERISTICS

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	450			ns	t_r, t_f = 20ns Input Levels = 0.8V or 2.0V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_A	Access Time			450	ns	
t_{CO}	Chip Enable To Output			310	ns	
t_{OD}	Output Disable To Output			250	ns	
t_{DF} [2]	Data Output to High Z State	0		200	ns	
t_{OH}	Previous Read Data Valid after change of Address	40			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	270			ns	t_r, t_f = 20ns Input Levels = 0.8V or 2.0V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_{AW}	Write Delay	20			ns	
t_{CW}	Chip Enable To Write	250			ns	
t_{DW}	Data Setup	250			ns	
t_{DH}	Data Hold	0			ns	
t_{WP}	Write Pulse	250			ns	
t_{WR}	Write Recovery	0			ns	
t_{DS}	Output Disable Setup	20			ns	

NOTES: 1. Typical values are for $T_A = 25°C$ and nominal supply voltage.
2. t_{DF} is with respect to the trailing edge of $\overline{CE}_1$, $\overline{CE}_2$, or OD, whichever occurs first.

2112A
256 X 4 BIT STATIC RAM

2112A-2	250 ns Max.
2112A	350 ns Max.
2112A-4	450 ns Max.

- **Single +5V Supply Voltage**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Static MOS: No Clocks or Refreshing Required**
- **Simple Memory Expansion: Chip Enable Input**
- **Fully Decoded: On Chip Address Decode**
- **Inputs Protected: All Inputs Have Protection Against Static Charge**
- **Low Cost Packaging: 16 Pin Plastic Dual In-Line Configuration**
- **Low Power: Typically 150 mW**
- **Three-State Output: OR-Tie Capability**

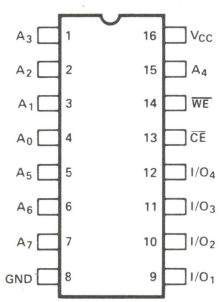
The Intel® 2112A is a 256 word by 4-bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

The 2112A is designed for memory applications in small systems where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

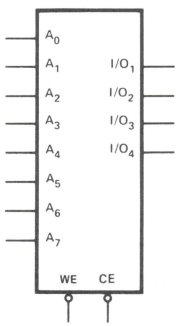
It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate chip enable ($\overline{CE}$) lead allows easy selection of an individual package when outputs are OR-tied.

The Intel® 2112A is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

PIN CONFIGURATION



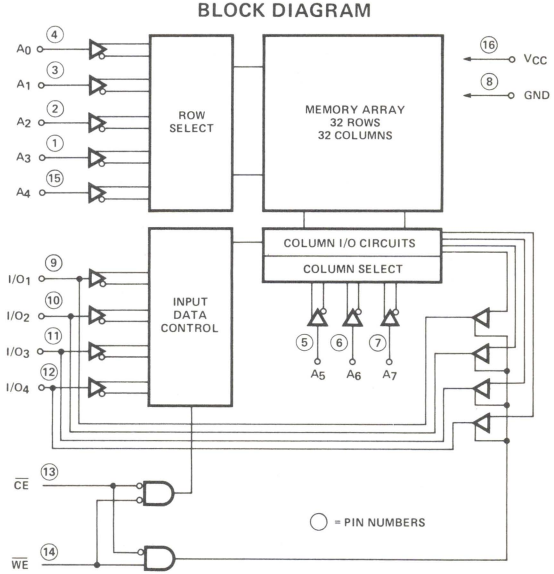
LOGIC SYMBOL



PIN NAMES

A_0-A_7	ADDRESS INPUTS
$\overline{WE}$	WRITE ENABLE
$\overline{CE}$	CHIP ENABLE INPUT
I/O_1-I/O_4	DATA INPUT/OUTPUT
V_{CC}	POWER (+5V)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . -10°C to 80°C

Storage Temperature . . . . . -65°C to +150°C

Voltage On Any Pin
With Respect to Ground . . . . . -0.5V to +7V

Power Dissipation . . . . . 1 Watt

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

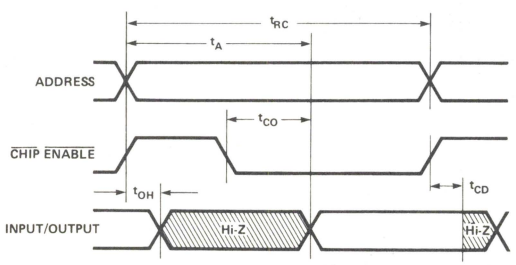
Symbol	Parameter		Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Current			1	10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	I/O Leakage Current			1	10	μA	Output Disabled, $V_{I/O}$=4.0V
I_{LOL}	I/O Leakage Current			-1	-10	μA	Output Disabled, $V_{I/O}$=0.45V
I_{CC1}	Power Supply Current	2112A, 2112A-4		35	55	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0mA, T_A = 25°C
		2112A-2		45	65		
I_{CC2}	Power Supply Current	2112A, 2112A-4			60	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0mA, T_A = 0°C
		2112A-2			70		
V_{IL}	Input "Low" Voltage		-0.5		0.8	V	
V_{IH}	Input "High" Voltage		2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage				+0.45	V	I_{OL} = 2.0 mA
V_{OH}	Output "High" Voltage	2112A, 2112A-2	2.4			V	I_{OH} = -200μA
		2112A-4	2.4			V	I_{OH} = -150μA

A.C. CHARACTERISTICS FOR 2112A-2

READ CYCLE T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	250			ns	t_r, t_f = 20ns
t_A	Access Time			250	ns	
t_{CO}	Chip Enable To Output Time			180	ns	Timing Reference = 1.5V
t_{CD}	Chip Enable To Output Disable Time	0		120	ns	Load = 1 TTL Gate
t_{OH}	Previous Read Data Valid After Change of Address	40			ns	and C_L = 100pF.

READ CYCLE WAVEFORMS



CAPACITANCE[2] T_A = 25°C, f = 1 MHz

Symbol	Test	Limits (pF)	
		Typ.[1]	Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
$C_{I/O}$	I/O Capacitance $V_{I/O}$ = 0V	10	15

NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS FOR 2112A-2 (Continued)

WRITE CYCLE #1 $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

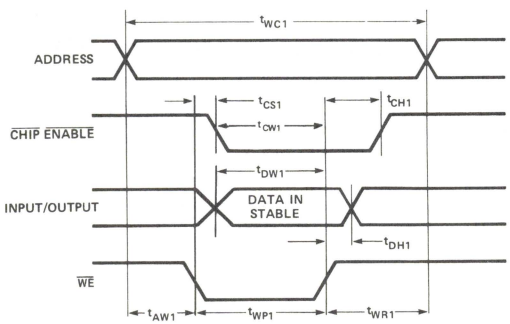
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC1}	Write Cycle	200			ns	t_r, t_f = 20ns
t_{AW1}	Address To Write Setup Time	20			ns	Input Levels = 0.8V or 2.0V
t_{DW1}	Write Setup Time	180			ns	Timing Reference = 1.5V
t_{WP1}	Write Pulse Width	180			ns	Load = 1 TTL Gate
t_{CS1}	Chip Enable Setup Time	0			ns	and C_L = 100pF.
t_{CH1}	Chip Enable Hold Time	0			ns	
t_{WR1}	Write Recovery Time	0			ns	
t_{DH1}	Data Hold Time	0			ns	
t_{CW1}	Chip Enable To Write Setup Time	180			ns	

WRITE CYCLE #2 $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

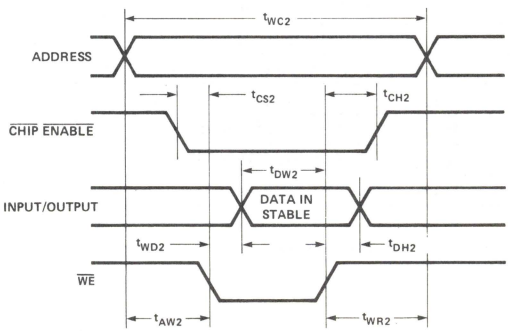
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC2}	Write Cycle	320			ns	t_r, t_f = 20ns
t_{AW2}	Address To Write Setup Time	20			ns	Input Levels = 0.8V or 2.0V
t_{DW2}	Write Setup Time	180			ns	Timing Reference = 1.5V
t_{WD2}	Write To Output Disable Time	120			ns	Load = 1 TTL Gate
t_{CS2}	Chip Enable Setup Time	0			ns	and C_L = 100pF.
t_{CH2}	Chip Enable Hold Time	0			ns	
t_{WR2}	Write Recovery Time	0			ns	
t_{DH2}	Data Hold Time	0			ns	

WRITE CYCLE WAVEFORMS

WRITE CYCLE #1



WRITE CYCLE #2



NOTE: 1. Typical values are for $T_A = 25°C$ and nominal supply voltage.

A.C. CHARACTERISTICS FOR 2112A

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	350			ns	t_r, t_f = 20ns
t_A	Access Time			350	ns	Input Levels = 0.8V or 2.0V
t_{CO}	Chip Enable To Output Time			240	ns	Timing Reference = 1.5V
t_{CD}	Chip Enable To Output Disable Time	0		200	ns	Load = 1 TTL Gate
t_{OH}	Previous Read Data Valid After Change of Address	40			ns	and C_L = 100pF.

WRITE CYCLE #1 $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC1}	Write Cycle	270			ns	t_r, t_f = 20ns
t_{AW1}	Address To Write Setup Time	20			ns	Input Levels = 0.8V or 2.0V
t_{DW1}	Write Setup Time	250			ns	Timing Reference = 1.5V
t_{WP1}	Write Pulse Width	250			ns	Load = 1 TTL Gate
t_{CS1}	Chip Enable Setup Time	0			ns	and C_L = 100pF.
t_{CH1}	Chip Enable Hold Time	0			ns	
t_{WR1}	Write Recovery Time	0			ns	
t_{DH1}	Data Hold Time	0			ns	
t_{CW1}	Chip Enable to Write Setup Time	250			ns	

WRITE CYCLE #2 $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC2}	Write Cycle	470			ns	t_r, t_f = 20ns
t_{AW2}	Address To Write Setup Time	20			ns	Input Levels = 0.8V or 2.0V
t_{DW2}	Write Setup Time	250			ns	Timing Reference = 1.5V
t_{WD2}	Write To Output Disable Time	200			ns	Load = 1 TTL Gate
t_{CS2}	Chip Enable Setup Time	0			ns	and C_L = 100pF.
t_{CH2}	Chip Enable Hold Time	0			ns	
t_{WR2}	Write Recovery Time	0			ns	
t_{DH2}	Data Hold Time	0			ns	

NOTE: 1. Typical values are for $T_A = 25°C$ and nominal supply voltage.

A.C. CHARACTERISTICS FOR 2112A-4

READ CYCLE T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	450			ns	t_r, t_f = 20ns
t_A	Access Time			450	ns	Input Levels = 0.8V or 2.0V
t_{CO}	Chip Enable To Output Time			310	ns	Timing Reference = 1.5V
t_{CD}	Chip Enable To Output Disable Time	0		260	ns	Load = 1 TTL Gate
t_{OH}	Previous Read Data Valid After Change of Address	40			ns	and C_L = 100pF.

WRITE CYCLE #1 T_A = 0°C to 70°C, V_{CC} = 5V ±5%

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC1}	Write Cycle	320			ns	t_r, t_f = 20ns
t_{AW1}	Address To Write Setup Time	20			ns	Input Levels = 0.8V or 2.0V
t_{DW1}	Write Setup Time	300			ns	Timing Reference = 1.5V
t_{WP1}	Write Pulse Width	300			ns	Load = 1 TTL Gate
t_{CS1}	Chip Enable Setup Time	0			ns	and C_L = 100pF.
t_{CH1}	Chip Enable Hold Time	0			ns	
t_{WR1}	Write Recovery Time	0			ns	
t_{DH1}	Data Hold Time	0			ns	
t_{CW1}	Chip Enable to Write Setup Time	300			ns	

WRITE CYCLE #2 T_A = 0°C to 70°C, V_{CC} = 5V ±5%

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC2}	Write Cycle	580			ns	t_r, t_f = 20ns
t_{AW2}	Address To Write Setup Time	20			ns	Input Levels = 0.8V or 2.0V
t_{DW2}	Write Setup Time	300			ns	Timing Reference = 1.5V
t_{WD2}	Write To Output Disable Time	260			ns	Load = 1 TTL Gate
t_{CS2}	Chip Enable Setup Time	0			ns	and C_L = 100pF.
t_{CH2}	Chip Enable Hold Time	0			ns	
t_{WR2}	Write Recovery Time	0			ns	
t_{DH2}	Data Hold Time	0			ns	

NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

2114
1024 X 4 BIT STATIC RAM

	2114-2	2114-3	2114	2114L2	2114L3	2114L
Max. Access Time (ns)	200	300	450	200	300	450
Max. Power Dissipation (mw)	525	525	525	370	370	370

- **High Density 18 Pin Package**
- **Identical Cycle and Access Times**
- **Single +5V Supply**
- **No Clock or Timing Strobe Required**
- **Completely Static Memory**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Common Data Input and Output Using Three-State Outputs**
- **Pin-Out Compatible with 3605 and 3625 Bipolar PROMs**

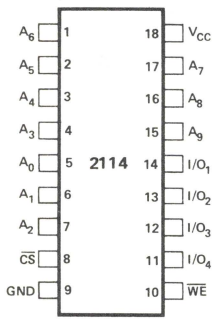
The Intel® 2114 is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits using N-channel Silicon-Gate MOS technology. It uses fully DC stable (static) circuitry throughout — in both the array and the decoding — and therefore requires no clocks or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

The 2114 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. The 2114 is placed in an 18-pin package for the highest possible density.

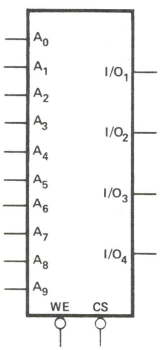
It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate Chip Select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are or-tied.

The 2114 is fabricated with Intel's N-channel Silicon-Gate technology — a technology providing excellent protection against contamination permitting the use of low cost plastic packaging.

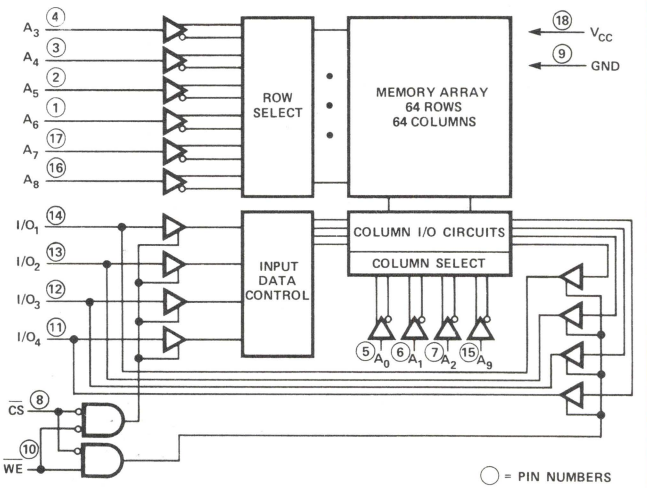
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0–A_9	ADDRESS INPUTS	V_{CC} POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND GROUND
$\overline{CS}$	CHIP SELECT	
I/O_1–I/O_4	DATA INPUT/OUTPUT	

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . -10°C to 80°C
Storage Temperature . . . . . -65°C to +150°C
Voltage on Any Pin
With Respect to Ground . . . . . -0.5V to +7V
Power Dissipation 1.0W
D.C. Output Current 5mA

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise noted.

SYMBOL	PARAMETER	2114-2, 2114-3, 2114 Min.	Typ.[1]	Max.	2114L2, 2114L3, 2114L Min.	Typ.[1]	Max.	UNIT	CONDITIONS
I_{LI}	Input Load Current (All Input Pins)			10			10	μA	V_{IN} = 0 to 5.25V
$\|I_{LO}\|$	I/O Leakage Current			10			10	μA	$\overline{CS}$ = 2.4V, $V_{I/O}$ = 0.4V to V_{CC}
I_{CC1}	Power Supply Current		80	95			65	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0 mA, T_A = 25°C
I_{CC2}	Power Supply Current			100			70	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0 mA, T_A = 0°C
V_{IL}	Input Low Voltage	-0.5		0.8	-0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		6.0	2.0		6.0	V	
I_{OL}	Output Low Current	2.1	6.0		2.1	6.0		mA	V_{OL} = 0.4V
I_{OH}	Output High Current	-1.0	-1.4		-1.0	-1.4		mA	V_{OH} = 2.4V
I_{OS}[2]	Output Short Circuit Current			40			40	mA	

NOTE: 1. Typical values are for T_A = 25°C and V_{CC} = 5.0V.
2. Duration not to exceed 30 seconds.

CAPACITANCE

T_A = 25°C, f = 1.0 MHz

SYMBOL	TEST	MAX	UNIT	CONDITIONS
$C_{I/O}$	Input/Output Capacitance	5	pF	$V_{I/O}$ = OV
C_{IN}	Input Capacitance	5	pF	V_{IN} = OV

NOTE: This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels . . . . . 0.8 Volt to 2.4 Volt
Input Rise and Fall Times . . . . . 10 nsec
Input and Output Timing Levels . . . . . 1.5 Volts
Output Load . . . . . 1 TTL Gate and C_L = 100 pF

A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise noted.

READ CYCLE [1]

SYMBOL	PARAMETER	2114-2, 2114L2 Min.	2114-2, 2114L2 Max.	2114-3, 2114L3 Min.	2114-3, 2114L3 Max.	2114, 2114L Min.	2114, 2114L Max.	UNIT
t_{RC}	Read Cycle Time	200		300		450		ns
t_A	Access Time		200		300		450	ns
t_{CO}	Chip Selection to Output Valid		70		100		120	ns
t_{CX}	Chip Selection to Output Active	20		20		20		ns
t_{OTD}	Output 3-state from Deselection		60		80		100	ns
t_{OHA}	Output Hold from Address Change	50		50		50		ns

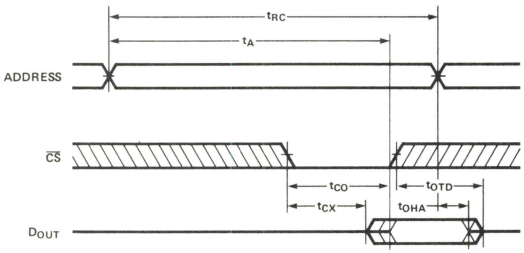
WRITE CYCLE [2]

SYMBOL	PARAMETER	2114-2, 2114L2 Min.	2114-2, 2114L2 Max.	2114-3, 2114L3 Min.	2114-3, 2114L3 Max.	2114, 2114L Min.	2114, 2114L Max.	UNIT
t_{WC}	Write Cycle Time	200		300		450		ns
t_W	Write Time	120		150		200		ns
t_{WR}	Write Release Time	0		0		0		ns
t_{OTW}	Output 3-state from Write		60		80		100	ns
t_{DW}	Data to Write Time Overlap	120		150		200		ns
t_{DH}	Data Hold From Write Time	0		0		0		ns

NOTES:
1. A Read occurs during the overlap of a low $\overline{CS}$ and a high $\overline{WE}$.
2. A Write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

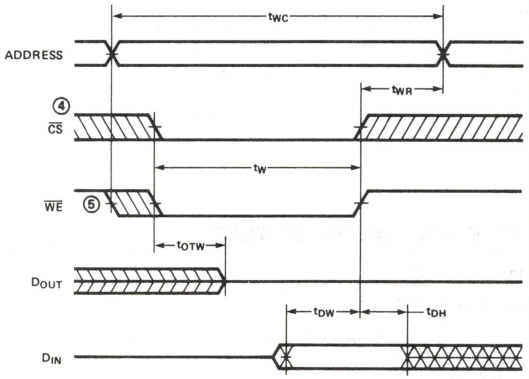
WAVEFORMS

READ CYCLE ③



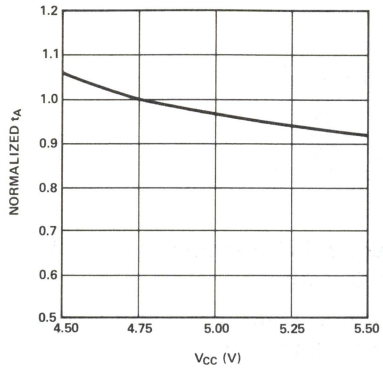
NOTES:
③ $\overline{WE}$ is high for a Read Cycle.
④ If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition, the output buffers remain in a high impedance state.
⑤ $\overline{WE}$ must be high during all address transitions.

WRITE CYCLE

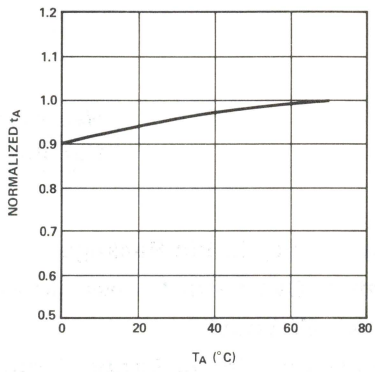


TYPICAL D.C. AND A.C. CHARACTERISTICS

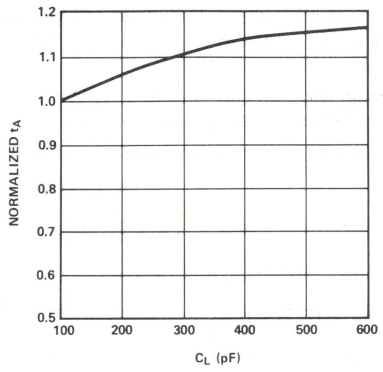
NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE



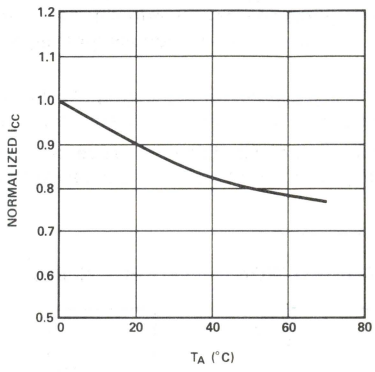
NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE



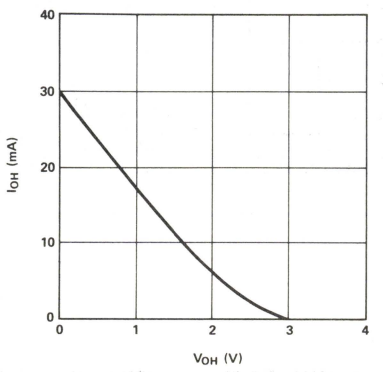
NORMALIZED ACCESS TIME VS. OUTPUT LOAD CAPACITANCE



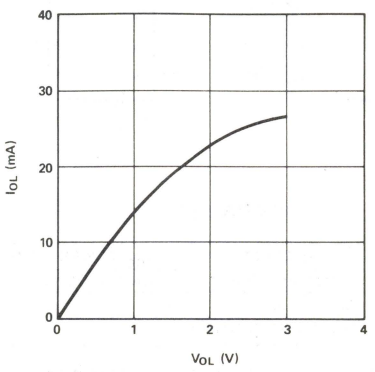
NORMALIZED POWER SUPPLY CURRENT VS. AMBIENT TEMPERATURE



OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



MILITARY TEMP.
ADVANCE
INFORMATION
Characteristics are subject to change without notice.

M2114
1024 X 4 BIT STATIC RAM

	M2114
Max. Access Time (ns)	450
Max. Power Dissipation (mW)	550

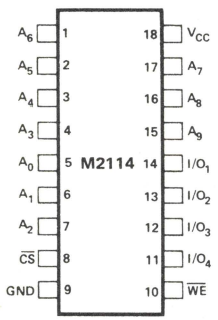
- **High Density 18 Pin Package**
- **Identical Cycle and Access Times**
- **Single +5V Supply**
- **No Clock or Timing Strobe Required**
- **Completely Static Memory**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Common Data Input and Output Using Three-State Outputs**
- **Military Temperature Range -55° C to +125° C**

The Intel® M2114 is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits using N-channel Silicon-Gate MOS technology. It uses fully DC stable (static) circuitry throughout — in both the array and the decoding — and therefore requires no clocks or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

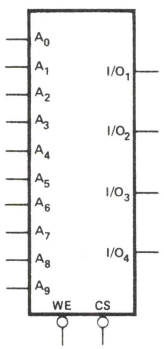
The M2114 is designed for memory applications where high performance, large bit storage, and simple interfacing are important design objectives. The M2114 is placed in an 18-pin package for the highest possible density.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate Chip Select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are OR-tied.

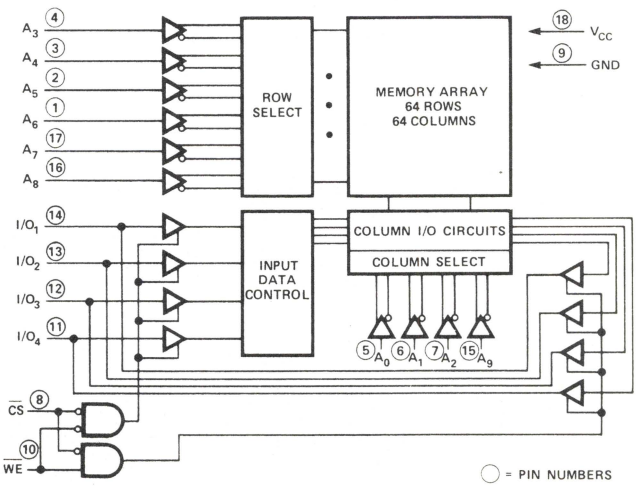
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0–A_9	ADDRESS INPUTS	V_{CC} POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND GROUND
$\overline{CS}$	CHIP SELECT	
I/O_1–I/O_4	DATA INPUT/OUTPUT	

2115A, 2125A FAMILY
HIGH SPEED 1K X 1 BIT STATIC RAM

	2115AL 2125AL	2115A 2125A	2115AL-2 2125AL-2	2115A-2 2125A-2
Max. T_{AA}(ns)	45	45	70	70
Max. I_{CC}(mA)	75	125	75	125

- **Pin Compatible To 93415A (2115A) And 93425A (2125A)**
- **Fan-Out Of 10 TTL (2115A Family) -- 16mA Output Sink Current**
- **Low Operating Power Dissipation --Max. 0.39mW/Bit (2115AL, 2125AL)**
- **TTL Inputs And Outputs**
- **Single +5V Supply**
- **Uncommitted Collector (2115A) And Three-State (2125A) Output**
- **Standard 16-Pin Dual In-Line Package**

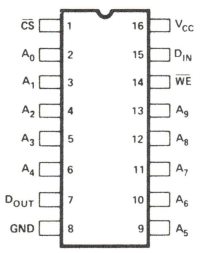
The Intel® 2115A and 2125A families are high-speed, 1024 words by 1 bit random access memories. Both open collector (2115A) and three-state output (2125A) are available. The 2115A and 2125A use fully DC stable (static) circuitry throughout – in both the array and the decoding and, therefore, require no clocks or refreshing to operate. The data is read out non-destructively and has the same polarity as the input data.

The 2115AL/2125AL at 45 ns maximum access time and the 2115AL-2/2125AL-2 at 70 ns maximum access time are fully compatible with the industry-produced 1K bipolar RAMs, yet offer a 50% reduction in power of their bipolar equivalents. The power dissipation of the 2115AL/2125AL and 2115AL-2/2125AL-2 is 394 mW maximum as compared to 814 mW maximum of their bipolar equivalents. For systems already designed for 1K bipolar RAMs, the 2115A/2125A and the 2115A-2/2125A-2 at 45 ns and 70 ns maximum access times, respectively, offer complete compatibility with a 20% reduction in maximum power dissipation.

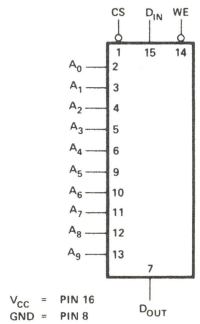
The devices are directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are OR-tied.

The 2115A and 2125A families are fabricated with Intel's N-channel MOS Silicon Gate Technology.

PIN CONFIGURATION



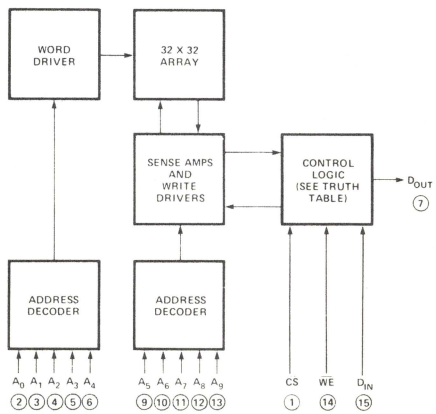
LOGIC SYMBOL



PIN NAMES

$\overline{CS}$	CHIP SELECT
A_0 TO A_9	ADDRESS INPUTS
$\overline{WE}$	WRITE ENABLE
D_{IN}	DATA INPUT
D_{OUT}	DATA OUTPUT

BLOCK DIAGRAM



TRUTH TABLE

INPUTS			OUTPUT 2115A FAMILY	OUTPUT 2125A FAMILY	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	D_{OUT}	
H	X	X	H	HIGH Z	NOT SELECTED
L	L	L	H	HIGH Z	WRITE "0"
L	L	H	H	HIGH Z	WRITE "1"
L	H	X	D_{OUT}	D_{OUT}	READ

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . –10°C to +85°C
Storage Temperature . . . . . –65°C to +150°C
All Output or Supply Voltages . . . . . –0.5V to +7V
All Input Voltages . . . . . –0.5V to +5.5V
D.C. Output Current . . . . . 20 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS[1,2]

V_{CC} = 5V ±5%, T_A = 0°C to 75°C

Symbol	Test	Min.	Typ.	Max.	Unit	Conditions
V_{OL1}	2115A Family Output Low Voltage			0.45	V	I_{OL} = 16 mA
V_{OL2}	2125A Family Output Low Voltage			0.45	V	I_{OL} = 7 mA
V_{IH}	Input High Voltage	2.1			V	
V_{IL}	Input Low Voltage			0.8	V	
I_{IL}	Input Low Current		–0.1	–40	μA	V_{CC} = Max., V_{IN} = 0.4V
I_{IH}	Input High Current		0.1	40	μA	V_{CC} = Max., V_{IN} = 4.5V
I_{CEX}	2115A Family Output Leakage Current		0.1	100	μA	V_{CC} = Max., V_{OUT} = 4.5V
$\|I_{OFF}\|$	2125A Family Output Current (High Z)		0.1	50	μA	V_{CC} = Max., V_{OUT} = 0.5V/2.4V
I_{OS}[3]	2125A Family Current Short Circuit to Ground			–100	mA	V_{CC} = Max.
V_{OH}	Family Output High Voltage	2.4			V	I_{OH} = –3.2 mA
I_{CC}	Power Supply Current: I_{CC1}: 2115AL, 2115AL-2, 2125AL, 2125AL-2		60	75	mA	All Inputs Grounded, Output Open
	I_{CC2}: 2115A, 2115A-2, 2125A, 2125A-2		100	125	mA	

NOTES:

1. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up. Typical thermal resistance values of the package at maximum temperature are:

   θ_{JA} (@ 400 f_{PM} air flow) = 45°C/W
   θ_{JA} (still air) = 60°C/W
   θ_{JC} = 25°C/W

2. Typical limits are at V_{CC} = 5V, T_A = +25°C, and maximum loading.
3. Duration of short circuit current should not exceed 1 second.

2115A FAMILY A.C. CHARACTERISTICS[1,2] V_{CC} = 5V ±5%, T_A = 0°C to 75°C

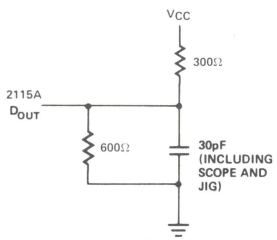
READ CYCLE

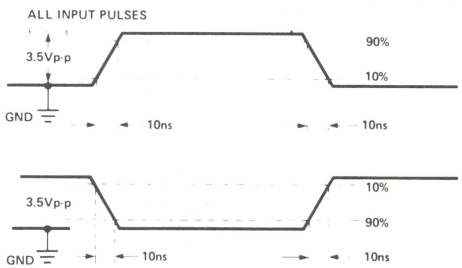
Symbol	Test	2115AL Limits Min.	Typ.	Max.	2115A Limits Min.	Typ.	Max.	2115AL-2 Limits Min.	Typ.	Max.	2115A-2 Limits Min.	Typ.	Max.	Units
t_{ACS}	Chip Select Time	5	15	30	5	15	30	5	15	30	5	15	40	ns
t_{RCS}	Chip Select Recovery Time		10	30		10	30		10	30		10	40	ns
t_{AA}	**Address Access Time**		**30**	**45**		**30**	**45**		**40**	**70**		**40**	**70**	**ns**
t_{OH}	Previous Read Data Valid After Change of Address	10			10			10			10			ns

WRITE CYCLE

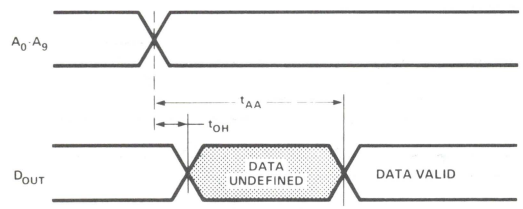
Symbol	Test	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
t_{WS}	Write Enable Time		10	25		10	30		10	25		10	40	
t_{WR}	Write Recovery Time	0		25	0		30	0		25	0		45	ns
t_W	Write Pulse Width	30	20		30	10		30	15		50	15		ns
t_{WSD}	Data Set-Up Time Prior to Write	0	–5		5	–5		0	–5		5	–5		ns
t_{WHD}	Data Hold Time After Write	5	0		5	0		5	0		5	0		ns
t_{WSA}	Address Set-Up Time	5	0		5	0		5	0		15	0		ns
t_{WHA}	Address Hold Time	5	0		5	0		5	0		5	0		ns
t_{WSCS}	Chip Select Set-Up Time	5	0		5	0		5	0		5	0		ns
t_{WHCS}	Chip Select Hold Time	5	0		5	0		5	0		5	0		ns

A.C. TEST CONDITIONS

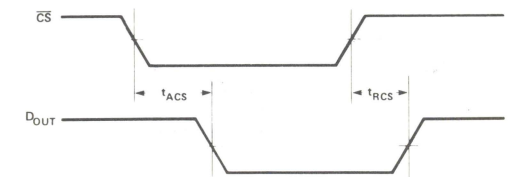




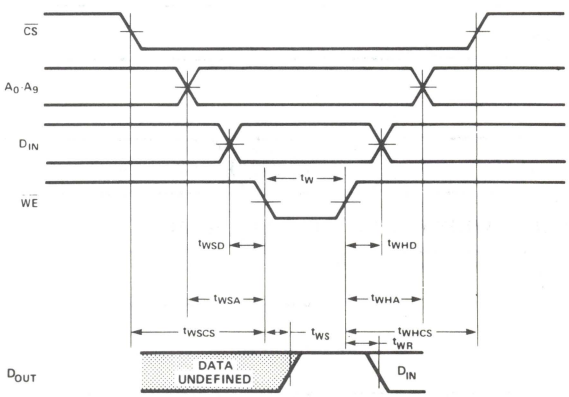
READ CYCLE



PROPAGATION DELAY FROM CHIP SELECT



WRITE CYCLE



(ALL ABOVE MEASUREMENTS REFERENCED TO 1.5V)

2125 FAMILY A.C. CHARACTERISTICS[1,2] V_{CC} = 5V ±5%, T_A = 0°C to 75°C

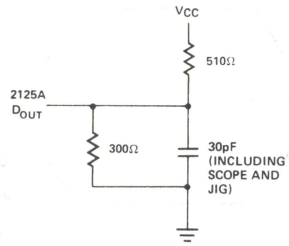
READ CYCLE

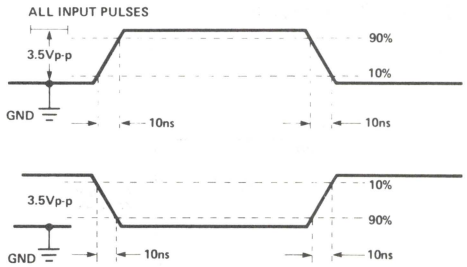
Symbol	Test	2125AL Limits Min.	Typ.	Max.	2125A Limits Min.	Typ.	Max.	2125AL-2 Limits Min.	Typ.	Max.	2125A-2 Limits Min.	Typ.	Max.	Units
t_{ACS}	Chip Select Time	5	15	30	5	15	30	5	15	30	5	15	40	ns
t_{ZRCS}	Chip Select to HIGH Z		10	30		10	30		10	30		10	40	ns
t_{AA}	**Address Access Time**		**30**	**45**		**30**	**45**		**40**	**70**		**40**	**70**	**ns**
t_{OH}	Previous Read Data Valid After Change of Address	10			10			10			10			ns

WRITE CYCLE

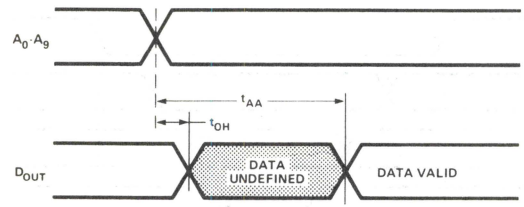
Symbol	Test	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
t_{ZWS}	Write Enable to HIGH Z		10	25		10	30		10	25		10	40	ns
t_{WR}	Write Recovery Time	0		25	0		30	0		25	0		45	ns
t_W	Write Pulse Width	30	20		30	10		30	10		50	15		ns
t_{WSD}	Data Set-Up Time Prior to Write	0	−5		5	−5		0	−5		5	−5		ns
t_{WHD}	Data Hold Time After Write	5	0		5	0		5	0		5	0		ns
t_{WSA}	Address Set-Up Time	5	0		5	0		5	0		15	0		ns
t_{WHA}	Address Hold Time	5	0		5	0		5	0		5	0		ns
t_{WSCS}	Chip Select Set-Up Time	5	0		5	0		5	0		5	0		ns
t_{WHCS}	Chip Select Hold Time	5	0		5	0		5	0		5	0		ns

A.C. TEST CONDITIONS

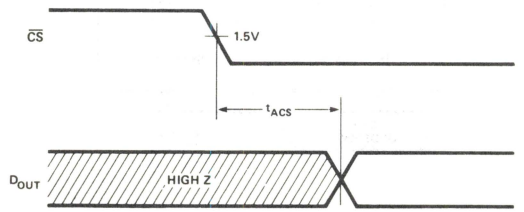




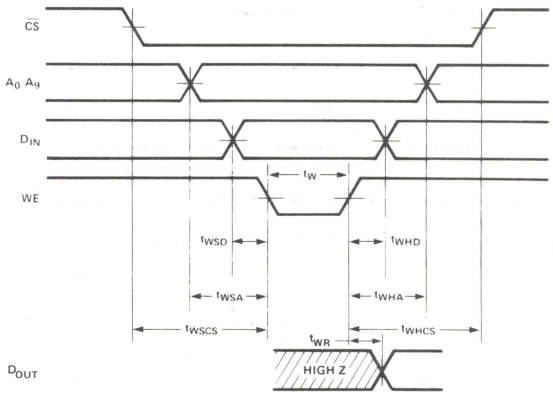
READ CYCLE



PROPAGATION DELAY FROM CHIP SELECT

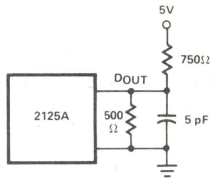


WRITE CYCLE

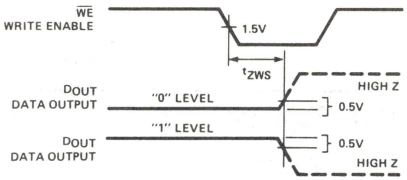


(ALL ABOVE MEASUREMENTS REFERENCED TO 1.5V)

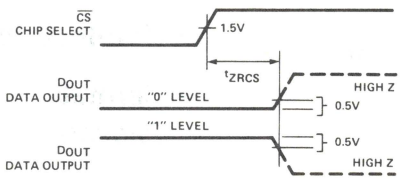
2125A FAMILY WRITE ENABLE TO HIGH Z DELAY



LOAD 1



2125A FAMILY PROPAGATION DELAY FROM CHIP SELECT TO HIGH Z



(ALL t_{ZXXX} PARAMETERS ARE MEASURED AT A DELTA OF 0.5V FROM THE LOGIC LEVEL AND USING LOAD 1.)

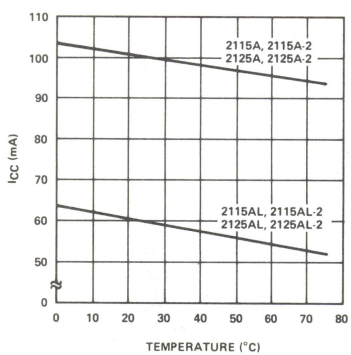
2115A/2125A FAMILY CAPACITANCE* V_{CC}= 5V, f = 1 MHz, T_A = 25°C

SYMBOL	TEST	2115A Family LIMITS		2125A Family LIMITS		UNITS	TEST CONDITIONS
		TYP.	MAX.	TYP.	MAX.		
C_I	Input Capacitance	3	5	3	5	pF	All Inputs = 0V, Output Open
C_O	Output Capacitance	5	8	5	8	pF	$\overline{CS}$ = 5V, All Other Inputs = 0V, Output Open

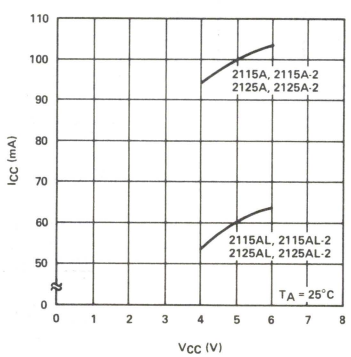
*This parameter is periodically sampled and is not 100% tested.

TYPICAL CHARACTERISTICS

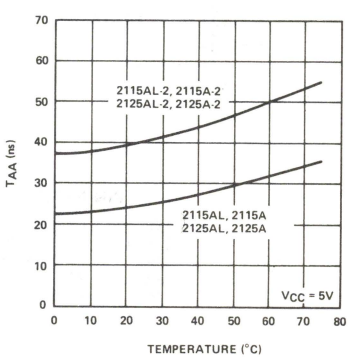
I_{CC} VS. TEMPERATURE



I_{CC} VS. V_{CC}



ACCESS TIME VS. TEMPERATURE



MILITARY TEMP.

M2115A, M2125A, FAMILY
HIGH SPEED 1K X 1 BIT STATIC RAM

	M2115AL, M2125AL	M2115A, M2125A
Max. T_{AA} (ns)	75	55
Max. I_{CC} (mA)	75	125

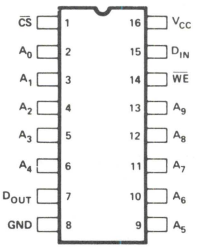
- **Low Operating Power Dissipation 413mW (M2115AL, M2125AL)**
- **Fast Access Time Over −55°C to 125°C --55ns Maximum (M2115A, M2125A)**
- **Single 5V Supply With ±10% Tolerance**
- **TTL Inputs and Output**
- **Uncommitted Collector (M2115A, M2115AL) and Three State (M2125A, M2125AL) Output**
- **Non-Inverting Data Output**
- **Hermetic 16 Pin Dual In-Line Package**

The Intel® M2115A and M2125A families are fully static, random access memories (RAMs) organized as 1024 words by 1 bit, which operate over a −55°C to +125°C ambient temperature range. Both open collector (M2115A) and three-state (M2125A) outputs are available. The M2115A and M2125A use fully DC stable (static) circuitry throughout in both the array and the decoding, and, therefore, require no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

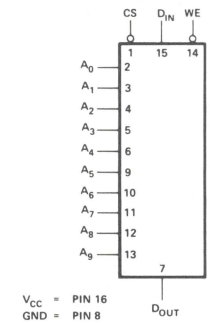
The M2125AL/M2125AL is ideal for high-performance systems where speed and power dissipation are significant design considerations. They have a maximum access time of 75 ns, while power dissipation is only 413 mW maximum. The M2115A/M2125A at 55 ns maximum should be considered for applications in which speed is a primary design objective.

The devices are directly TTL compatible in all respects: inputs, outputs and a single +5V supply. A separate chip select lead allows easy selection of an individual package when outputs are OR-tied.

PIN CONFIGURATION



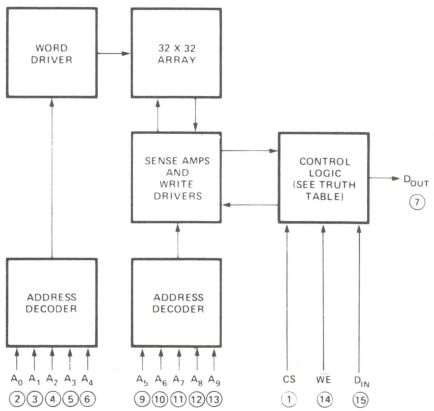
LOGIC SYMBOL



PIN NAMES

$\overline{CS}$	CHIP SELECT
A_0 TO A_9	ADDRESS INPUTS
$\overline{WE}$	WRITE ENABLE
D_{IN}	DATA INPUT
D_{OUT}	DATA OUTPUT

BLOCK DIAGRAM



TRUTH TABLE

INPUTS			OUTPUT 2115A FAMILY	OUTPUT 2125A FAMILY	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	D_{OUT}	
H	X	X	H	HIGH Z	NOT SELECTED
L	L	L	H	HIGH Z	WRITE "0"
L	L	H	H	HIGH Z	WRITE "1"
L	H	X	D_{OUT}	D_{OUT}	READ

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . −65°C to +135°C
Storage Temperature . . . . . −65°C to +150°C
All Output or Supply Voltages. . . . . −0.5V to +7V
All Input Voltages . . . . . −0.5V to +6V
D.C. Output Current . . . . . 20 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS[1,2]

V_{CC} = 5V ±10%, T_A = −55°C to +125°C

Symbol	Test	Min.	Typ.	Max.	Unit	Conditions
V_{OL1}	M2115A, M2115AL Output Low Voltage			0.45	V	I_{OL} = 10 mA
V_{OL2}	M2125A, M2125AL Output Low Voltage			0.45	V	I_{OL} = 5 mA
V_{IH}	Input High Voltage	2.1			V	
V_{IL}	Input Low Voltage			0.8	V	
I_{IL}	Input Low Current		−0.1	−40	μA	V_{CC} = Max., V_{IN} = 0.4V
I_{IH}	Input High Current		0.1	40	μA	V_{CC} = Max., V_{IN} = 4.5V
I_{CEX}	M2115A, M2115AL Output Leakage Current		0.1	100	μA	V_{CC} = Max., V_{OUT} = 4.5V
$\|I_{OFF}\|$	M2125A, M2125AL Output Leakage Current (High Z)		0.1	50	μA	V_{CC} = Max., V_{OUT} = 0.5V/2.4V
I_{OS}[3]	M2125A, M2125AL Current Short Circuit to Ground			−100	mA	V_{CC} = Max.
V_{OH}	M2115A, M2115AL Output High Voltage	2.4			V	I_{OH} = −3.2 mA
I_{CC1}	M2115AL, M2125AL Power Supply Current		60	75	mA	All Inputs Grounded, Output Open
I_{CC2}	M2115A, M2125A Power Supply Current		100	125	mA	All Inputs Grounded, Output Open

NOTES:

1. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warmup. Typical thermal resistance values of the package at maximum temperature are:

   θ_{JA} (@ 400 f_{PM} air flow) = 45°C/W
   θ_{JA} (still air) = 60°C/W
   θ_{JC} = 25°C/W

2. Typical limits are at V_{CC} = 5V, T_A = +25°C and maximum loading.
3. Duration of short circuit current should not exceed 1 second.

M2115AL, M2115A A.C. CHARACTERISTICS[1,2] V_{CC} = 5V ±10%, T_A = −55°C to +125°C

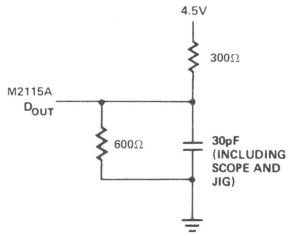
READ CYCLE

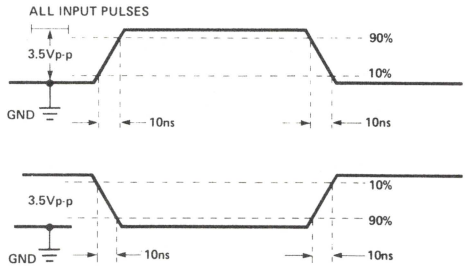
Symbol	Test	M2115AL Limits Min.	Typ.	Max.	M2115A Limits Min.	Typ.	Max.	Units
t_{ACS}	Chip Select Time	5		45	5		45	ns
t_{RCS}	Chip Select Recovery Time			50			35	ns
t_{AA}	**Address Access Time**		**40**	**75**		**35**	**55**	**ns**
t_{OH}	Previous Read Data Valid After Change of Address	10			10			ns

WRITE CYCLE

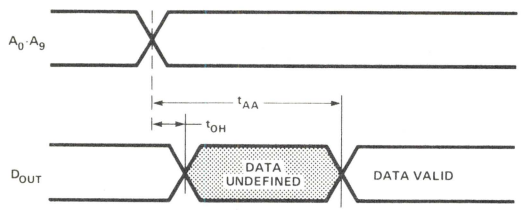
Symbol	Test	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
t_{WS}	Write Enable Time			45			35	ns
t_{WR}	Write Recovery Time	0		50	0		35	ns
t_W	Write Pulse Width	55	10		40	10		ns
t_{WSD}	Data Setup Time Prior to Write	5	−5		5	−5		ns
t_{WHD}	Data Hold Time After Write	5	0		5	0		ns
t_{WSA}	Address Setup Time	15	0		5	0		ns
t_{WHA}	Address Hold Time	5	0		5	0		ns
t_{WSCS}	Chip Select Setup Time	5	0		5	0		ns
t_{WHCS}	Chip Select Hold Time	5	0		5	0		ns

A.C. TEST CONDITIONS

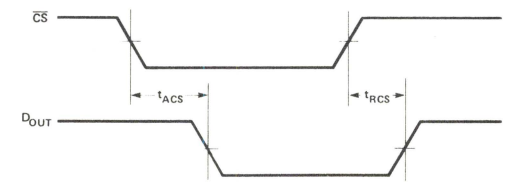




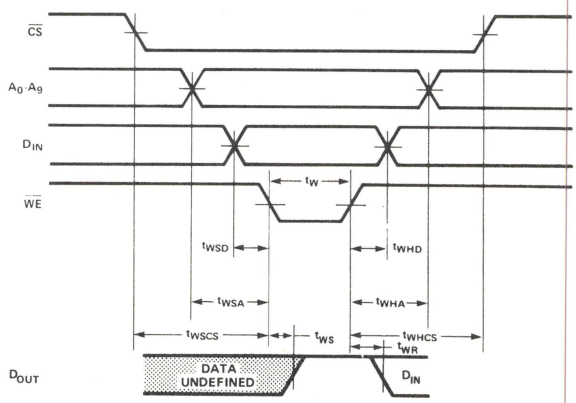
READ CYCLE



PROPAGATION DELAY FROM CHIP SELECT



WRITE CYCLE



(ALL ABOVE MEASUREMENTS REFERENCED TO 1.5V)

M2125AL, M2125A A.C. CHARACTERISTICS[1,2] V_{CC} = 5V ±10%, T_A = −55°C to +125°C

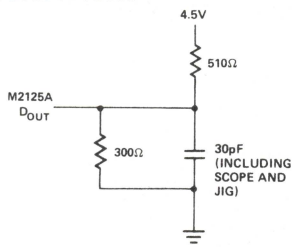
READ CYCLE

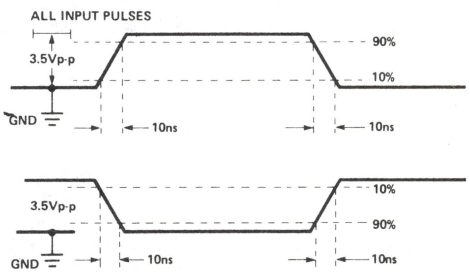
Symbol	Test	M2125AL Limits			M2125A Limits			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{ACS}	Chip Select Time	5		45	5		45	ns
t_{ZRCS}	Chip Select to HIGH Z			50			35	ns
t_{AA}	**Address Access Time**		**40**	**75**		**25**	**55**	**ns**
t_{OH}	Previous Read Data Valid After Change of Address	10			10			ns

WRITE CYCLE

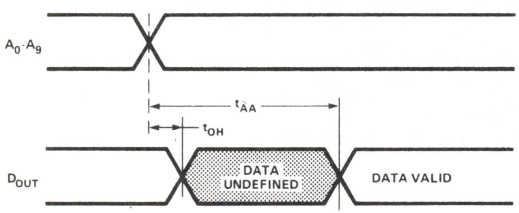
Symbol	Test	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
t_{ZWS}	Write Enable to HIGH Z			45			35	ns
t_{WR}	Write Recovery Time	0		50	0		35	ns
t_W	Write Pulse Width	55	10		40	10		ns
t_{WSD}	Data Setup Time Prior to Write	5	−5		5	−5		ns
t_{WHD}	Data Hold Time After Write	5	0		5	0		ns
t_{WSA}	Address Setup Time	15	0		5	0		ns
t_{WHA}	Address Hold Time	5	0		5	0		ns
t_{WSCS}	Chip Select Setup Time	5	0		5	0		ns
t_{WHCS}	Chip Select Hold Time	5	0		5	0		ns

A.C. TEST CONDITIONS

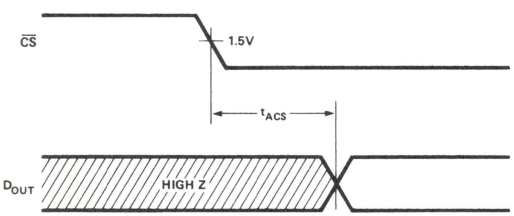




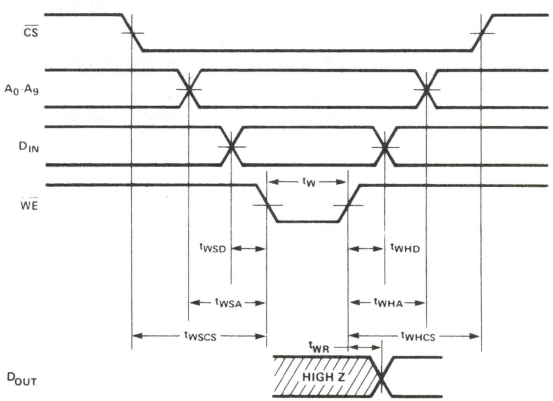
READ CYCLE



PROPAGATION DELAY FROM CHIP SELECT

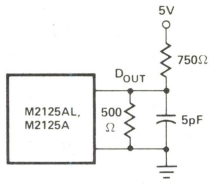


WRITE CYCLE

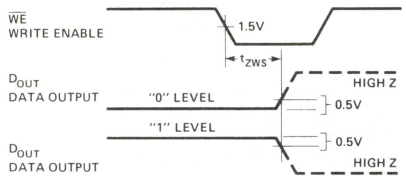


(ALL ABOVE MEASUREMENTS REFERENCED TO 1.5V)

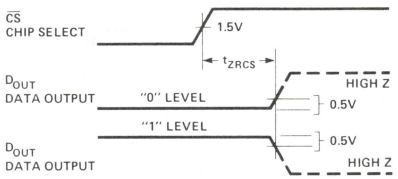
M2125AL, M2125A WRITE ENABLE TO HIGH Z DELAY



LOAD 1



M2125AL, M2125A PROPAGATION DELAY FROM CHIP SELECT TO HIGH Z



(All t_{ZXXX} parameters are measured at a delta of 0.5V from the logic level and using Load 1.)

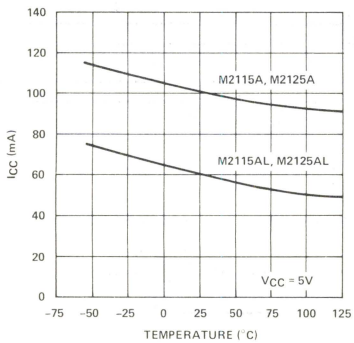
CAPACITANCE* V_{CC} = 5V, f = 1 MHz, T_A = 25°C

Symbol	Test	M2115AL, M2115A Limits		M2125AL, M2125A Limits		Units	Test Conditions
		Typ.	Max.	Typ.	Max.		
C_I	Input Capacitance	3	5	3	5	pF	All Inputs = 0V, Output Open
C_O	Output Capacitance	5	8	5	8	pF	CS = 5V, All other inputs = 0V, Output Open

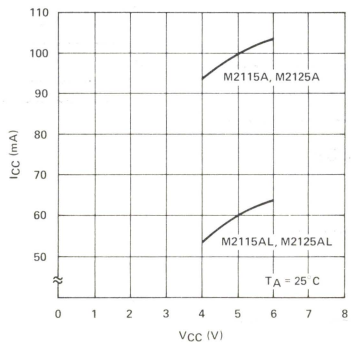
*This parameter is periodically sampled and is not 100% tested.

TYPICAL CHARACTERISTICS

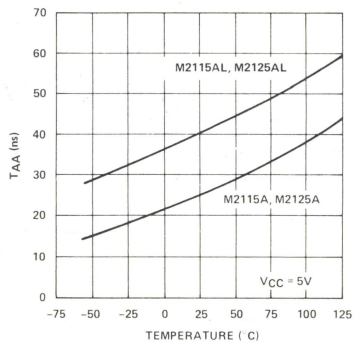
I_{CC} vs. TEMPERATURE



I_{CC} vs. V_{CC}



ACCESS TIME vs. TEMPERATURE



2116 FAMILY
16,384 X 1 BIT DYNAMIC RAM

	2116-2	2116-3	2116-4
Max. Access Time (ns)	200	250	300
Read, Write Cycle (ns)	350	375	425
Read-Modify-Write Cycle (ns)	400	525	595

- **Highest Density 16K RAM: Industry Standard 16 Pin Package**
- **Low Standby Power**
- **All Inputs Including Clocks TTL Compatible**
- **±10% Tolerance on all Power Supplies +12V, +5V, −5V**
- **On-Chip Latches for Address and Data In**
- **Only 64 Refresh Cycles Required Every 2 ms**
- **Output is Three-State, TTL Compatible; Data is Latched and Valid into Next Cycle**

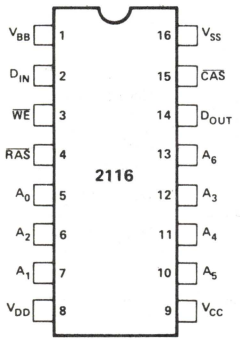
The Intel® 2116 is a 16,384 word by 1 bit MOS RAM fabricated with two layer polysilicon N-MOS technology — a production-proven process for high performance, high reliability, and high functional density. The 2116 uses a single transistor dynamic storage cell and dynamic circuitry to achieve high speed and low power dissipation.

The unique design of the 2116 allows it to be packaged in the industry standard 16 pin dual-in-line package. The 16 pin package provides the highest system bit densities and is compatible with widely available automated handling equipment. The 2116 is designed to facilitate upgrading of 2104A-type 4K RAM systems to 16K capabilities.

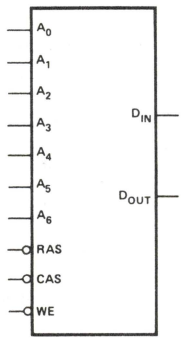
The use of the 16 pin package is made possible by multiplexing the 14 address bits (required to address 1 of 16,384 bits) into the 2116 on 7 address input pins. The two 7 bit address words are latched into the 2116 by the two TTL clocks, Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

The single transistor dynamic storage cell provides high speed along with low power dissipation. The memory cell requires refreshing for data retention. Refreshing can be accomplished every 2 ms by any one of the three following methods: (1) $\overline{CAS}$ before $\overline{RAS}$ cycles on 64 addresses, A_0–A_5, (2) $\overline{RAS}$-only cycles on 128 address, A_0–A_6, or (3) normal read or write cycles on 128 addresses, A_0–A_6. A write cycle will refresh stored data on all bits of the selected row except the bit which is addressed. The output is brought to a high impedance state by a $\overline{CAS}$-only cycle or by a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

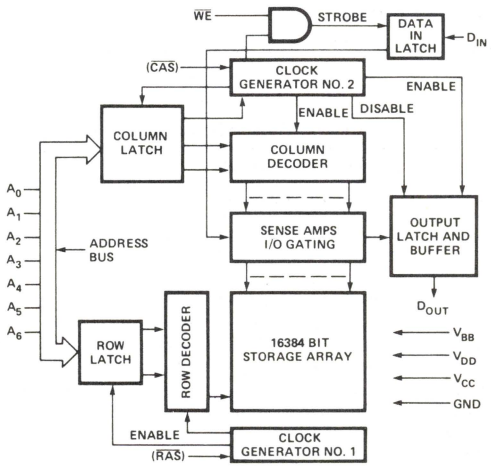
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_6	ADDRESS INPUTS	$\overline{WE}$	WRITE ENABLE
$\overline{CAS}$	COLUMN ADDRESS STROBE	V_{BB}	POWER (-5V)
D_{IN}	DATA IN	V_{CC}	POWER (+5V)
D_{OUT}	DATA OUT	V_{DD}	POWER (+12V)
$\overline{RAS}$	ROW ADDRESS STROBE	V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . -10°C to +80°C
Storage Temperature . . . . . -65°C to +150°C
Voltage on any Pin Relative to V_{BB}
(V_{SS} - V_{BB} ≥ 4V) . . . . . -0.3V to +20V
Power Dissipation 1.25W

*COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS [1],[2]

T_A = 0°C to 70°C, V_{DD} = +12V ±10%, V_{CC} = +5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Limits			Unit	Conditions	
		Min.	Typ.[3]	Max.			
I_{LI}	Input Load Current (any input)			10	µA	V_{IN} = V_{SS} to $V_{IH\,MAX}$, V_{BB} = -5.0V	
$\|I_{LO}\|$	Output Leakage Current for high impedance state		0.1	10	µA	Chip deselected: $\overline{RAS}$ and $\overline{CAS}$ at V_{IH} V_{OUT} = 0 to 5.5V	
I_{DD1}	V_{DD} Supply Current		1.2	2	mA	$\overline{CAS}$ and $\overline{RAS}$ at V_{IH} or $\overline{CAS}$-only cycle. Chip deselected prior to measurement. See Note 5.	
I_{BB1}	V_{BB} Supply Current		1	50	µA		
I_{DD2}[4]	Operating V_{DD} Current		53	69	mA	2116-2 t_{CYC} = 350 ns	T_A = 25°C Device selected. See Note 6.
			51	68	mA	2116-3 t_{CYC} = 375 ns	
			49	65	mA	2116-4 t_{CYC} = 425 ns	
I_{BB2}	Operating V_{BB} Current		120	400	µA	Device selected	
I_{CC1}[7]	V_{CC} Supply Current when deselected			10	µA		
V_{IL}	Input Low Voltage (any input)	-1.0		0.8	V		
V_{IH}	Input High Voltage (any input)	2.4		V_{CC}+1	V		
V_{OL}	Output Low Voltage	0.0		0.4	V	I_{OL} = 4.1 mA (Read Cycle Only)	
V_{OH}	Output High Voltage	2.4		V_{CC}	V	I_{OH} = -5 mA (Read Cycle Only)	

CAPACITANCE [8]

T_A = 25°C, V_{DD} = 12V ±10%, V_{CC} = 5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{I1}	Address, Data In & $\overline{WE}$ Capacitance	4	7	pF	V_{IN} = V_{SS}
C_{I2}	$\overline{RAS}$ Capacitance	3	5	pF	V_{IN} = V_{SS}
C_{I3}	$\overline{CAS}$ Capacitance	6	10	pF	V_{IN} = V_{SS}
C_O	Data Output Capacitance	3	7	pF	V_{OUT} = 0V

Notes:
1. All voltages referenced to V_{SS}. No power supply sequencing is required but V_{DD}, V_{CC}, and V_{SS} should never be 0.3V or more negative than V_{BB}.
2. To avoid self-clocking, $\overline{RAS}$ should not be allowed to float.
3. Typical values are for T_A = 25°C and nominal power supply voltages.
4. For $\overline{RAS}$-only refresh I_{DD} = 0.78 I_{DD2}. For $\overline{CAS}$-before-$\overline{RAS}$ (64 cycle refresh) I_{DD} = 0.96 I_{DD2}.
5. The chip is deselected (i.e., output is brought to high impedance state) by $\overline{CAS}$-only cycle or by $\overline{CAS}$-before-$\overline{RAS}$ cycle. The current flowing in a selected (i.e., output on) chip with $\overline{RAS}$ and $\overline{CAS}$ at V_{IH} is approximately twice I_{DD1}.
6. For typical I_{DD} characteristics under other conditions see following page.
7. When chip is selected V_{CC} supply current is dependent on output loading; V_{CC} is connected to output buffer only.
8. Capacitance measured with Boonton Meter.

TYPICAL CHARACTERISTICS

I_{BB2} AND I_{DD2} VS. TEMPERATURE

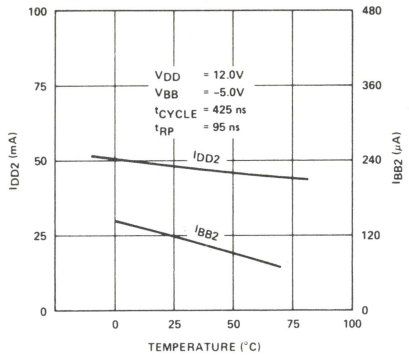


Figure 1.

I_{DD2} VS. CYCLE TIME

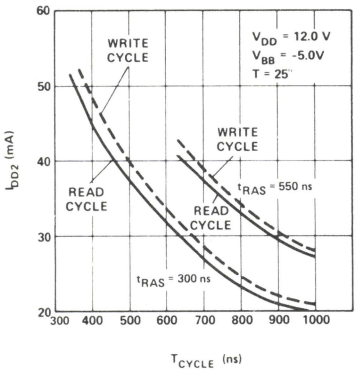


Figure 2.

Standby Power Calculations:

$$P_{REF} = P_{OP}\left(N\frac{t_{CYC}}{t_{REF}}\right) + P_{SB}\left(1 - N\frac{t_{CYC}}{t_{REF}}\right) \text{ where}$$

P_{OP} = Power dissipation (continuous operation) $\cong V_{DD} \times I_{DD2}$.

N = Number of refresh cycles (64 or 128)

t_{CYC} = Cycle time for a refresh cycle.

t_{REF} = Time between refreshes

P_{SB} = Standby power dissipation = $V_{DD} \times I_{DD1} + |V_{BB}| \times I_{BB}$

Note that I_{DD2} depends upon refresh as follows:

1. For 128 cycle ($\overline{RAS}$ before $\overline{CAS}$) use I_{DD2} from Figures 1 and 2.
2. For 64 cycle ($\overline{CAS}$ before $\overline{RAS}$) multiply I_{DD2} determined in (1) by 0.96.
3. For 128 cycle ($\overline{RAS}$ only) multiply I_{DD2} determined in (1) by 0.78.

Examples of typical calculations for V_{BB} = -5.0V, V_{DD} = 12.0V, $T_A = 25°C$, t_{CYC} = 0.425 μs, t_{RAS} = 0.3 μs. t_{REF} = 2000 μs:

1. 128 cycle ($\overline{RAS}$ before $\overline{CAS}$): P_{OP} = 12.0V x 43 mA = 516 mW

$$P_{REF} = 516\left(128\ \frac{0.425}{2000}\right) + (12x1.2+5x0.001)\left(1-128\ \frac{0.425}{2000}\right)$$

P_{REF} = 28.0 mW

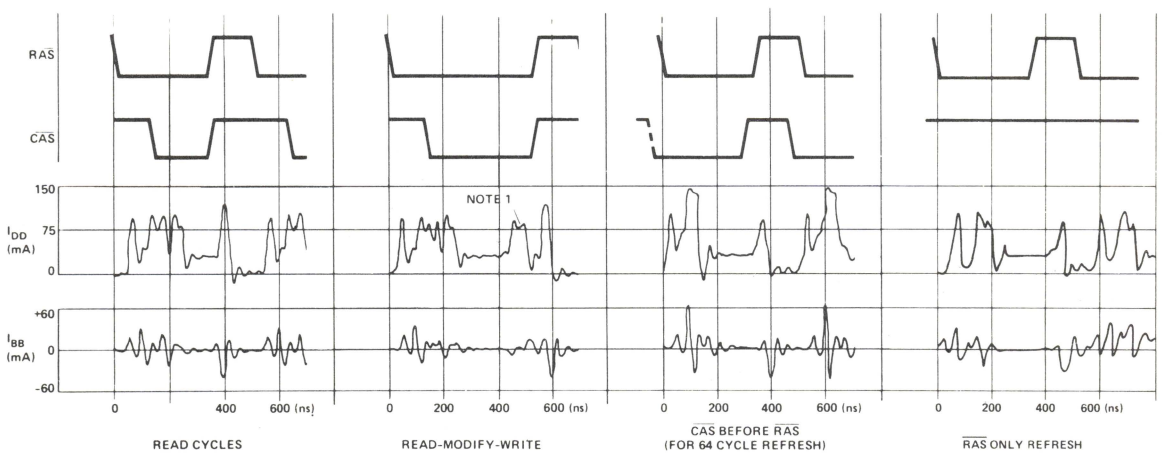
2. 64 cycle ($\overline{CAS}$ before $\overline{RAS}$); P_{OP} = 12.0V x 43 (0.96) mA = 495 mW.

$$P_{REF} = 495\ (64\ \frac{0.425}{2000}) + (12x1.2+5x0.001)\ (1-64\ \frac{0.425}{2000}) =$$

P_{REF} = 20.9 mW

3. 128 cycle ($\overline{RAS}$ only): P_{OP} = 12.0V x 43 (0.78) mA = 402 mW

P_{REF} = 25.0 mW



Note 1: Increase in current due to $\overline{WE}$ going low. Width of this current pulse is independent of $\overline{WE}$ pulse width.

Figure 3. Supply Current Waveforms.

A.C. CHARACTERISTICS[1]

T_A=0°C to 70°C, V_{DD}=12V ±10%, V_{CC}=5V ±10%, V_{BB}=−5V ±10%, V_{SS}=0V, unless otherwise noted.

READ, WRITE, READ-MODIFY-WRITE AND REFRESH CYCLES

Symbol	Parameter	2116-2 Min.	2116-2 Max.	2116-3 Min.	2116-3 Max.	2116-4 Min.	2116-4 Max.	Unit
t_{REF}	Time Between Refresh		2		2		2	ms
t_{RP}	$\overline{RAS}$ Precharge Time	75		75		95		ns
t_{CP}	$\overline{CAS}$ Precharge Time	100		125		125		ns
t_{RCL}[2]	$\overline{RAS}$ to $\overline{CAS}$ Leading Edge Lead Time	45	75	50	110	60	110	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	0		0		0		ns
t_{RSH}	$\overline{RAS}$ Hold Time	160		200		220		ns
t_{CSH}	$\overline{CAS}$ Hold Time	200		250		300		ns
t_{ASR}	Row Address Set-Up Time	0		0		0		ns
t_{ASC}	Column Address Set-Up Time	−10		−10		−10		ns
t_{AH}	Address Hold Time	45		50		60		ns
t_T	Transition Time (Rise and Fall)		50		50		50	ns
t_{OFF}	Output Buffer Turn Off Delay	0	60	0	60	0	80	ns
t_{CAC}[3]	Access Time From $\overline{CAS}$		125		150		190	ns
t_{RAC}[3]	Access Time From $\overline{RAS}$		200		250		300	ns

READ AND REFRESH CYCLES

Symbol	Parameter	2116-2 Min.	2116-2 Max.	2116-3 Min.	2116-3 Max.	2116-4 Min.	2116-4 Max.	Unit
t_{CYC}[4]	Random Read Cycle Time	350		375		425		ns
t_{RAS}	$\overline{RAS}$ Pulse Width	275	32000	300	32000	330	32000	ns
t_{CAS}	$\overline{CAS}$ Pulse Width	125	10000	150	10000	190	10000	ns
t_{CH}	$\overline{CAS}$ Hold Time for $\overline{RAS}$-Only Refresh	30		30		30		ns
t_{CPR}	$\overline{CAS}$ Precharge for 64 Cycle Refresh	30		30		30		ns
t_{RCH}	Read Command Hold Time	20		20		20		ns
t_{RCS}	Read Command Set-Up Time	0		0		0		ns
t_{DOH}	Data-Out Hold Time	32		32		32		μs

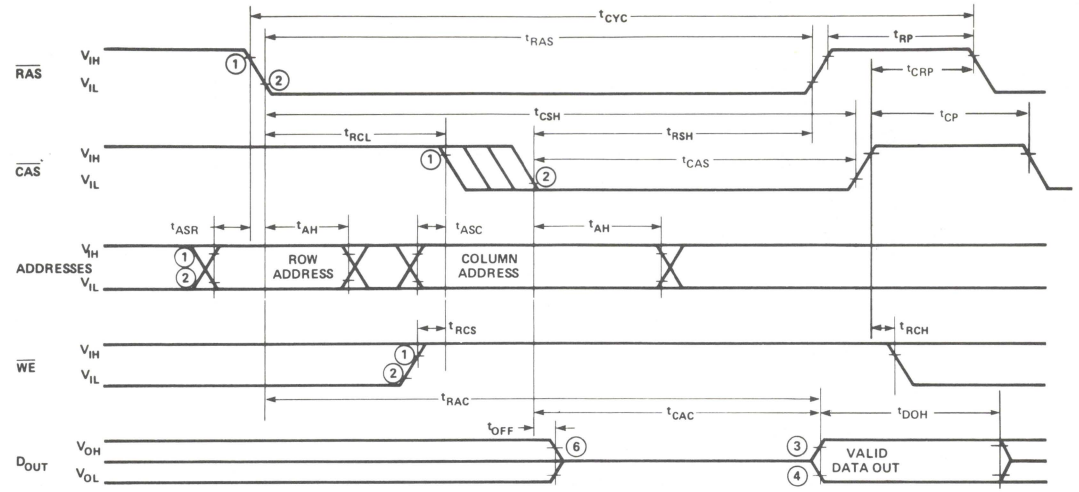
WRITE CYCLE

Symbol	Parameter	2116-2 Min.	2116-2 Max.	2116-3 Min.	2116-3 Max.	2116-4 Min.	2116-4 Max.	Unit
t_{CYC}[4]	Random Write Cycle Time	350		375		425		ns
t_{RAS}	$\overline{RAS}$ Pulse Width	275	32000	300	32000	330	32000	ns
t_{CAS}	$\overline{CAS}$ Pulse Width	125	10000	150	10000	190	10000	ns
t_{WCH}	Write Command Hold Time	75		100		100		ns
t_{WP}	Write Command Pulse Width	50		100		100		ns
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	125		200		200		ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	100		150		160		ns
t_{DS}[5]	Data-In Set-Up Time	0		0		0		ns
t_{DH}[5]	Data-In Hold Time	100		100		125		ns

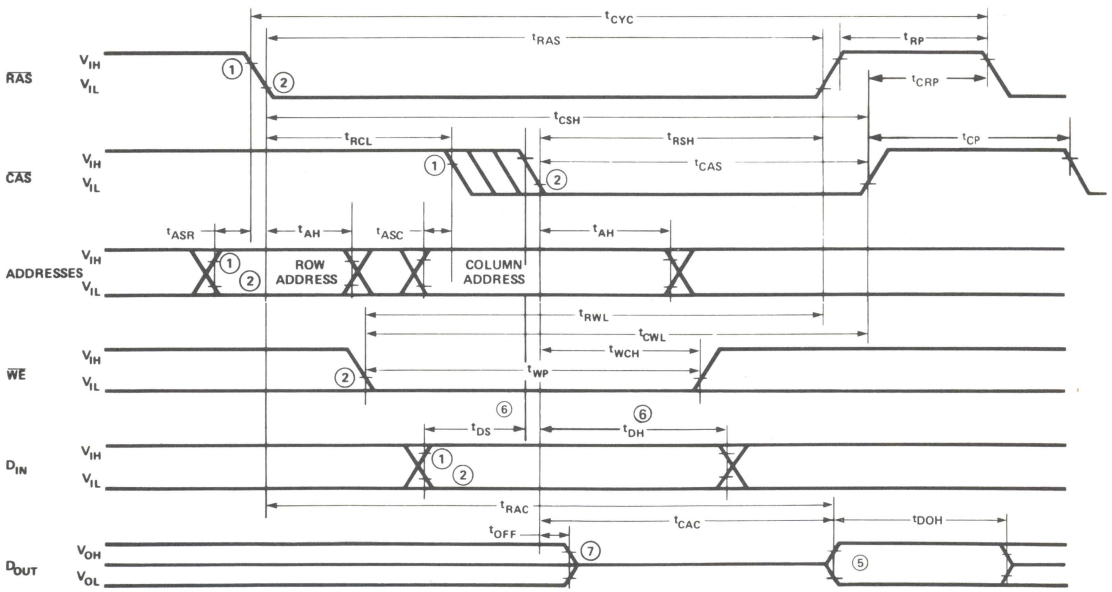
Notes:
1. All voltages referenced to V_{SS}.
2. $\overline{CAS}$ must remain at V_{IH} a minimum of $t_{RCL\ MIN}$ after $\overline{RAS}$ switches to V_{IL}. To achieve the minimum guaranteed access time (t_{RAC}), $\overline{CAS}$ must switch to V_{IL} at or before $t_{RCL\ (MAX)} = t_{RAC} - t_{CAC}$. Device operation is not guaranteed for $t_{RCL} > 2$ μs.
3. Load = 1 TTL and 50 pF.
4. The minimum cycle timing does not allow for t_T or skews.
5. Referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.

WAVEFORMS

READ CYCLE



WRITE CYCLE



Notes:
1,2. $V_{IH\ MIN}$ and $V_{IL\ MAX}$ are reference levels for measuring timing of input signals.
3,4. $V_{OH\ MIN}$ and $V_{OL\ MAX}$ are reference levels for measuring timing of D_{OUT}.
5. D_{OUT} follows D_{IN} when writing, with $\overline{WE}$ before $\overline{CAS}$.
6. Referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.
7. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.

A.C. CHARACTERISTICS

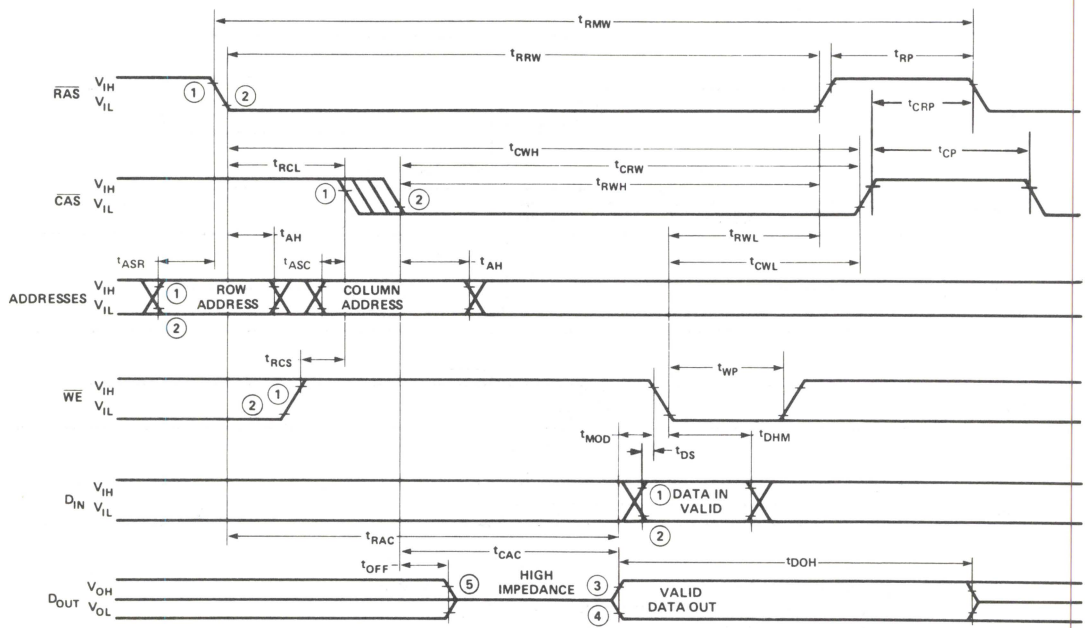
T_A = 0°C to 70°C, V_{DD} = 12V ±10%, V_{CC} = 5V ±10%, V_{BB} = −5V ±10%, V_{SS} = 0V, unless otherwise noted.

READ-MODIFY-WRITE CYCLE

Symbol	Parameter	2116-2 Min.	2116-2 Max.	2116-3 Min.	2116-3 Max.	2116-4 Min.	2116-4 Max.	Unit
t_{RMW}	Read-Modify-Write Cycle Time	400		525		595		ns
t_{CRW}	RMW Cycle $\overline{CAS}$ Width	225	10000	310	10000	350	10000	ns
t_{RRW}	RMW Cycle $\overline{RAS}$ Width	325	32000	450	32000	500	32000	ns
t_{RWH}	RMW Cycle $\overline{RAS}$ Hold Time	250		350		390		ns
t_{CWH}	RMW Cycle $\overline{CAS}$ Hold Time	300		410		460		ns
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	125		200		200		ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	100		160		160		ns
t_{WP}	Write Command Pulse Width	50		100		100		ns
t_{RCS}	Read Command Set-Up Time	0		0		0		ns
t_{MOD}	Modify Time	0	10	0	10	0	10	µs
t_{DS}	Data-In Set-Up Time	0		0		0		ns
t_{DHM}	Data-In Hold Time (RMW Cycle)	50		100		125		ns

WAVEFORMS

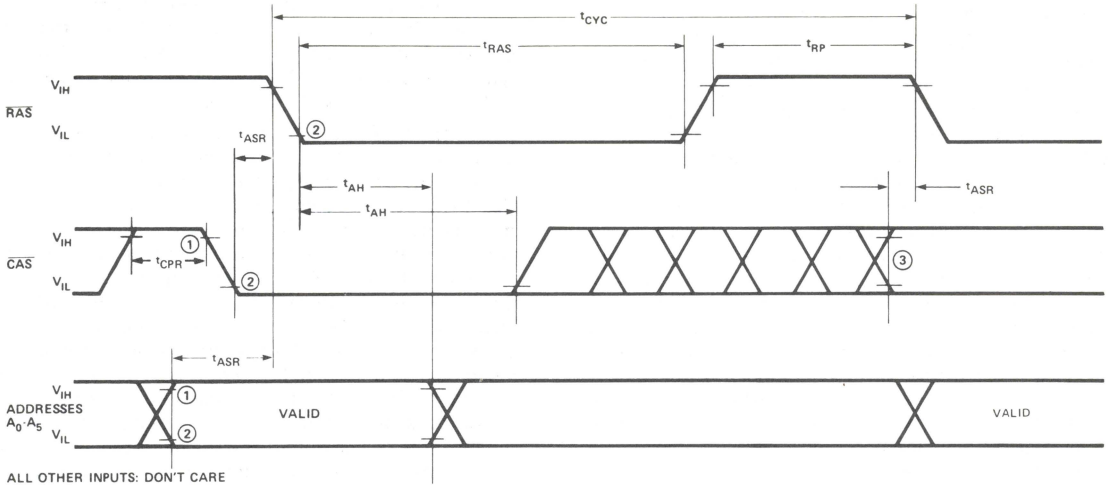
READ MODIFY WRITE CYCLE



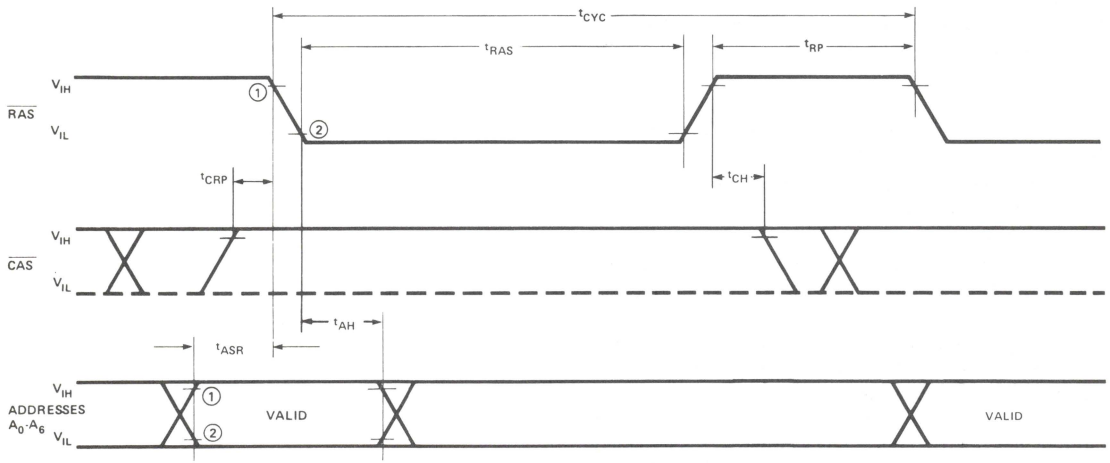
Notes: 1,2. V_{IHMIN} and V_{ILMAX} are reference levels for measuring timing of input signals.
3,4. V_{OHMIN} and V_{OLMAX} are reference levels for measuring timing of D_{OUT}.
5. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.

REFRESH CYCLE WAVEFORMS

$\overline{CAS}$ BEFORE $\overline{RAS}$ CYCLES. (64 CYCLE REFRESH)



$\overline{RAS}$ ONLY CYCLES (128 CYCLE REFRESH)



Notes: 1,2. V_{IHMIN} and V_{ILMAX} are reference levels for measuring timing of input signals.
3. $\overline{CAS}$ must be high or low as appropriate for the next cycle.

APPLICATIONS INFORMATION

REFRESH MODES

The 2116 may be refreshed in any of three modes. Read/Refresh cycles and $\overline{RAS}$-only cycles refresh the row addressed by A_0 through A_6 and therefore require 128 cycles to refresh the stored data. Assuming a 500 nsec system cycle time, the refresh operations require 64 μsec out of each 2.0 msec refresh period or 3.2% of the available memory time. The third 2116 refresh mode, $\overline{CAS}$-before-$\overline{RAS}$, allows refresh of the stored data in only 64 cycles and requires only 32 μsec or 1.6% of the available memory time (equal to the 64-cycle refresh 4K RAMs). While some 2116 aplications would not be impacted by the 3.2% memory lockout time using 128 cycle refresh, most large mainframe memory applications would suffer throughput degradation in that refresh mode. Intel designed the 2116 to allow either 128-cycle or 64-cycle refresh, allowing the system designer to choose the refresh mode which fits his system needs. In addition to allowing higher memory throughput, the $\overline{CAS}$-before-RAS 64-cycle refresh mode dissipates approximately 14% less power than the 128-cycle $\overline{RAS}$-only mode and 23% less power than the 128-cycle Read/Refresh mode (refer to the Standby Power Calculation section).

POWER SUPPLY DECOUPLING/ DISTRIBUTION

Power supply current waveforms for the 2116 are shown in Figure 3. The V_{DD} supply provides virtually all of the operating current for the 2116. The V_{DD} supply current, I_{DD}, has two components: transient current peaks when the clocks change state and a DC component while the clocks are active (low). When selecting the decoupling capacitors for the V_{DD} supply, the characteristics of capacitors as well as the current waveform must be considered. Suppression of transient or pulse currents require capacitors with small physical size and low inherent inductance. Monolithic and other ceramic capacitors exhibit these desirable characteristics. When the current waveform indicates a DC component, bulk capacity must be located near the current load to supply the load power. Inductive effects of PC board traces and bus bars preclude supplying the DC component from bulk capacitors at the periphery of a memory matrix without voltage droop during the active portion of a memory cycle. This means that some bulk capacity in the form of electrolytic or large ceramic capacitors should be distributed around or within the memory matrix.

The V_{BB} supply current, I_{BB}, has high transient current peaks, with essentially no DC component (less than 400 microamperes). The V_{BB} capacitors should be selected for transient suppression characteristics. The following capacitance values and locations are recommended for the 2116:

1. A 0.33 μF ceramic capacitor between V_{DD} and V_{SS} (ground) at every other device.
2. A 0.1 μF ceramic capacitor between V_{BB} and V_{SS} at every other device (preferably alternate devices to the V_{DD} decoupling above).
3. A 4.7 μF electrolytic capacitor between V_{DD} and V_{SS} for each eight devices and located adjacent to the devices.

The V_{CC} supply is connected only to the 2116 output buffer and is not used internally. The load current from the V_{CC} supply is dependent only upon the output loading and is usually only the input high level current to a TTL gate and the output leakage currents of any OR-tied 2116s (typically 100 μA or less total). Intel recommends that a 0.1 or 0.01 μF ceramic capacitor be connected between V_{CC} and V_{SS} for every eight devices to preclude coupled noise from affecting the TTL devices in the system.

Intel recommends a power supply distribution system such that each power supply is grided both horizontally and vertically at each memory device. This technique minimizes the power distribution system impedance and enhances the effect of the decoupling capacitors.

OUTPUT DATA LATCH

The 2116 contains an output data latch eliminating the need for an external system data latch and the timing circuitry required to strobe an external latch. The 2116 output latch operates identically to the output latch found on all industry standard 16-pin, 4K RAMs and enhances the system compatibility of the 16K and 4K devices.

Operation of the output latch is controlled by $\overline{CAS}$. The data output will go to the high-impedance state immediately following the $\overline{CAS}$ leading edge during each data cycle and will either go to valid data at access time on selected devices (devices receiving both $\overline{RAS}$ and $\overline{CAS}$) or will remain in the high impedance state on unselected devices (devices receiving only $\overline{CAS}$). During $\overline{RAS}$-only refresh cycles, the data output remains in the state it was prior to the $\overline{RAS}$-only cycle. This unique feature of latched output RAMs allows a refresh cycle to be hidden among data cycles without impacting data availability. For instance, a $\overline{RAS}$-only refresh cycle could follow each data cycle in a microprocessor system but the accessed data would remain at the device output and the microprocessor could take the data at any time within the cycle. Non-latched output devices do not provide this type of hidden refresh capability since their data output would go to the high impedance state at the end of the data cycle.

2117 FAMILY
16,384 x 1 BIT DYNAMIC RAM

	2117-2	2117-3	2117-4
Maximum Access Time (ns)	150	200	250
Read, Write Cycle (ns)	320	375	410
Read-Modify-Write Cycle (ns)	330	375	475

- **Industry Standard 16-Pin Configuration**
- **±10% Tolerance on All Power Supplies: +12V, +5V, -5V**
- **Low Power: 462mW Max. Operating, 20mW Max. Standby**
- **Low I_{DD} Current Transients**
- **All Inputs, Including Clocks, TTL Compatible**
- **Non-Latched Output is Three-State, TTL Compatible**
- **$\overline{RAS}$ Only Refresh**
- **128 Refresh Cycles Required Every 2ms**
- **Page Mode Capability**
- **$\overline{CAS}$ Controlled Output Allows Hidden Refresh**

The Intel® 2117 is a 16,384 word by 1-bit Dynamic MOS RAM fabricated with Intel's standard two layer polysilicon NMOS technology — a production proven process for high performance, high reliability, and high storage density.

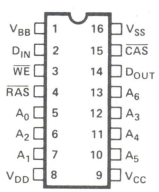
The 2117 uses a single transistor dynamic storage cell and advanced dynamic circuitry to achieve high speed with low power dissipation. The circuit design minimizes the current transients typical of dynamic RAM operation. These low current transients and ±10% tolerance on all power supplies contribute to the high noise immunity of the 2117 in a system environment.

Multiplexing the 14 address bits into the 7 address input pins allows the 2117 to be packaged in the industry standard 16-pin DIP. The two 7-bit address words are latched into the 2117 by the two TTL clocks, Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). Non-critical timing requirements for $\overline{RAS}$ and $\overline{CAS}$ allow use of the address multiplexing technique while maintaining high performance.

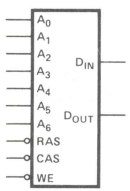
The 2117 three-state output is controlled by $\overline{CAS}$, independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is latched on the output by holding $\overline{CAS}$ low. The data out pin is returned to the high impedance state by returning $\overline{CAS}$ to a high state. The 2117 hidden refresh feature allows $\overline{CAS}$ to be held low to maintain latched data while $\overline{RAS}$ is used to execute $\overline{RAS}$-only refresh cycles.

The single transistor storage cell requires refreshing for data retention. Refreshing is accomplished by performing $\overline{RAS}$-only refresh cycles, hidden refresh cycles, or normal read or write cycles on the 128 address combinations of A_0 through A_6 during a 2ms period. A write cycle will refresh stored data on all bits of the selected row except the bit which is addressed.

PIN CONFIGURATION



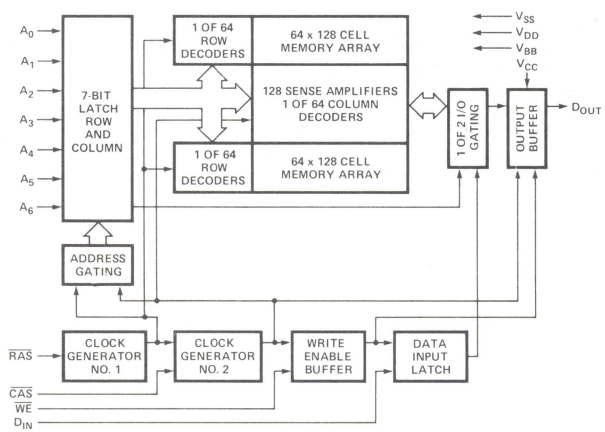
LOGIC SYMBOL



PIN NAMES

A_0-A_6	ADDRESS INPUTS	$\overline{WE}$	WRITE ENABLE
$\overline{CAS}$	COLUMN ADDRESS STROBE	V_{BB}	POWER (-5V)
D_{IN}	DATA IN	V_{CC}	POWER (+5V)
D_{OUT}	DATA OUT	V_{DD}	POWER (+12V)
$\overline{RAS}$	ROW ADDRESS STROBE	V_{SS}	GROUND

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ... -10°C to +80°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin Relative to V_{BB}
(V_{SS} - $V_{BB} \geq 4V$) ..... -0.3V to +20V
Data Out Current 50mA
Power Dissipation 1.0W

COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

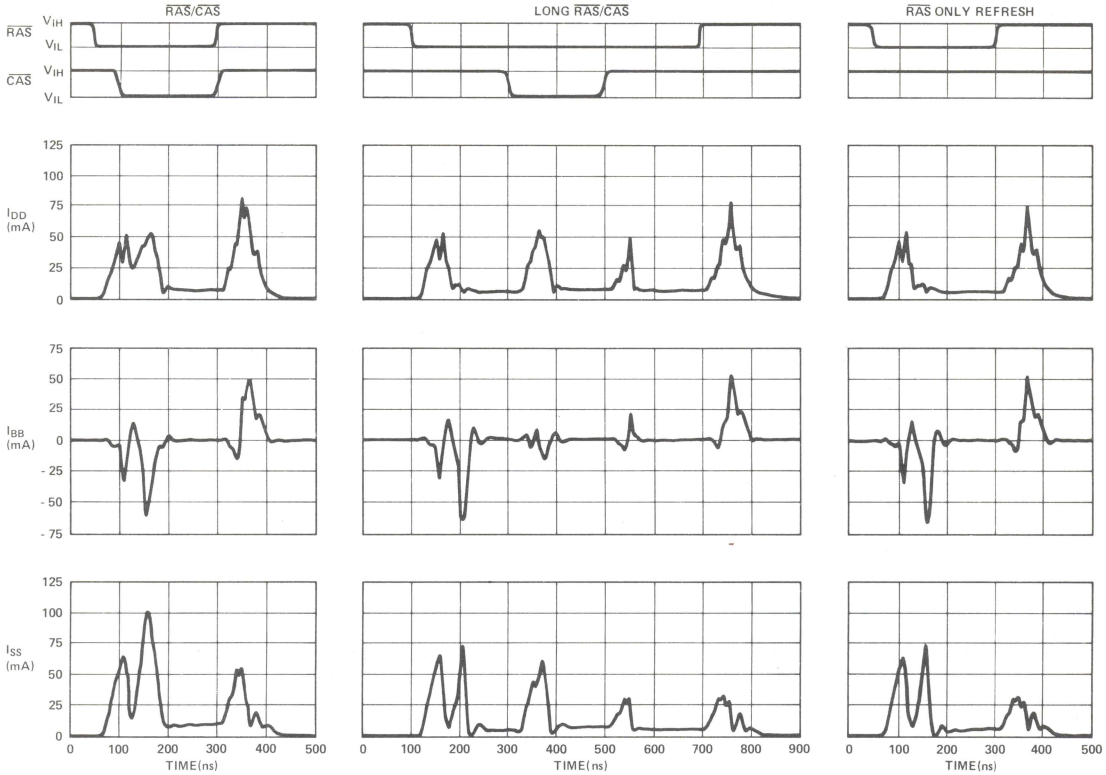
D.C. AND OPERATING CHARACTERISTICS[1,2]

T_A = 0°C to 70°C, V_{DD} = 12V ±10%, V_{CC} = 5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Limits Min.	Typ.[3]	Max.	Unit	Test Conditions	Notes
$\|I_{LI}\|$	Input Load Current (any input)		0.1	10	µA	V_{IN}=V_{SS} to 7.0V, V_{BB}=-5.0V	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State		0.1	10	µA	Chip Deselected: $\overline{CAS}$ at V_{IH}, V_{OUT} = 0 to 5.5V	
I_{DD1}	V_{DD} Supply Current, Standby			1.5	mA	$\overline{CAS}$ and $\overline{RAS}$ at V_{IH}	4
I_{BB1}	V_{BB} Supply Current, Standby		1.0	50	µA		
I_{CC1}	V_{CC} Supply Current, Output Deselected		0.1	10	µA	$\overline{CAS}$ at V_{IH}	5
I_{DD2}	V_{DD} Supply Current, Operating			35	mA	2117-2, t_{RC} = 375ns, t_{RAS} = 150ns	4,6
				35	mA	2117-3, t_{RC} = 375ns, t_{RAS} = 200ns	4
				33	mA	2117-4, t_{RC} = 410ns, t_{RAS} = 250ns	4
I_{BB2}	V_{BB} Supply Current, Operating, $\overline{RAS}$-Only Refresh, Page Mode		150	300	µA	T_A = 0°C	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh			27	mA	2117-2, t_{RC} = 375ns, t_{RAS} = 150ns	4,6
				27	mA	2117-3, t_{RC} = 375ns, t_{RAS} = 200ns	4
				26	mA	2117-4, t_{RC} = 410ns, t_{RAS} = 250ns	4
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled		1.5	3	mA	$\overline{CAS}$ at V_{IL}, $\overline{RAS}$ at V_{IH}	
V_{IL}	Input Low Voltage (all inputs)	-1.0		0.8	V		
V_{IH}	Input High Voltage (all inputs)	2.4		6.0	V		
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.2mA	4
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -5mA	4

NOTES:
1. All voltages referenced to V_{SS}.
2. No power supply sequencing is required. However, V_{DD}, V_{CC} and V_{SS} should never be more negative than -0.3V with respect to V_{BB} as required by the absolute maximum ratings.
3. Typical values are for T_A = 25°C and nominal supply voltages.
4. See the Typical Characteristics Section for values of this parameter under alternate conditions.
5. I_{CC} is dependent on output loading when the device output is selected. V_{CC} is connected to the output buffer only. V_{CC} may be reduced to V_{SS} without affecting refresh operation or maintenance of internal device data.
6. For the 2117-2 at t_{RC} = 320ns, t_{RAS} = 150ns, I_{DD2} max. is 45mA and I_{DD3} max. is 31mA.

TYPICAL SUPPLY CURRENT WAVEFORMS



Typical power supply current waveforms vs. time are shown for the $\overline{RAS}/\overline{CAS}$ timings of Read/Write, Read/Write (Long $\overline{RAS}/\overline{CAS}$), and $\overline{RAS}$-only refresh cycles. I_{DD} and I_{BB} current transients at the $\overline{RAS}$ and $\overline{CAS}$ edges require adequate decoupling of these supplies. Decoupling recommendations are provided in the Applications section.

The effects of cycle time, V_{DD} supply voltage and ambient temperature on the I_{DD} current are shown in graphs included in the Typical Characteristics Section. Each family of curves for I_{DD1}, I_{DD2}, and I_{DD3} is related by a common point at $V_{DD} = 12.0V$ and $T_A = 25°C$ for two given t_{RAS} pulse widths. The typical I_{DD} current for a given condition of cycle time, V_{DD} and T_A can be determined by combining the effects of the appropriate family of curves.

CAPACITANCE [1]

$T_A = 25°C$, $V_{DD} = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $V_{BB} = -5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise specified.

Symbol	Parameter	Typ.	Max.	Unit
C_{I1}	Address, Data In	3	5	pF
C_{I2}	$\overline{RAS}$ Capacitance, $\overline{WE}$ Capacitance	4	7	pF
C_{I3}	$\overline{CAS}$ Capacitance	6	10	pF
C_O	Data Output Capacitance	4	7	pF

NOTES:
1. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation: $C = \frac{I\Delta t}{\Delta V}$ with ΔV equal to 3 volts and power supplies at nominal levels.

A.C. CHARACTERISTICS[1,2,3]

T_A = 0°C to 70°C, V_{DD} = 12V ±10%, V_{CC} = 5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, unless otherwise noted.

READ, WRITE, READ-MODIFY-WRITE AND REFRESH CYCLES

Symbol	Parameter	2117-2		2117-3		2117-4		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RAC}	Access Time From $\overline{RAS}$		150		200		250	ns	4,5
t_{CAC}	Access Time From $\overline{CAS}$		100		135		165	ns	4,5,6
t_{REF}	Time Between Refresh		2		2		2	ms	
t_{RP}	$\overline{RAS}$ Precharge Time	100		120		150		ns	
t_{CPN}	$\overline{CAS}$ Precharge Time(non-page cycles)	25		25		25		ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	-20		-20		-20		ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	25	65	35	85	ns	7
t_{RSH}	$\overline{RAS}$ Hold Time	100		135		165		ns	
t_{CSH}	$\overline{CAS}$ Hold Time	150		200		250		ns	
t_{ASR}	Row Address Set-Up Time	0		0		0		ns	
t_{RAH}	Row Address Hold Time	20		25		35		ns	
t_{ASC}	Column Address Set-Up Time	-10		-10		-10		ns	
t_{CAH}	Column Address Hold Time	45		55		75		ns	
t_{AR}	Column Address Hold Time, to $\overline{RAS}$	95		120		160		ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	8
t_{OFF}	Output Buffer Turn Off Delay	0	50	0	60	0	70	ns	

READ AND REFRESH CYCLES

t_{RC}	Random Read Cycle Time	320		375		410		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	150	10000	200	10000	250	10000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	100	10000	135	10000	165	10000	ns	
t_{RCS}	Read Command Set-Up Time	0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		ns	

WRITE CYCLE

t_{RC}	Random Write Cycle Time	320		375		410		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	150	10000	200	10000	250	10000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	100	10000	135	10000	165	10000	ns	
t_{WCS}	Write Command Set-Up Time	-20		-20		-20		ns	9
t_{WCH}	Write Command Hold Time	45		55		75		ns	
t_{WCR}	Write Command Hold Time, to $\overline{RAS}$	95		120		160		ns	
t_{WP}	Write Command Pulse Width	45		55		75		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	60		80		100		ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	60		80		100		ns	
t_{DS}	Data-In Set-Up Time	0		0		0		ns	
t_{DH}	Data-In Hold Time	45		55		75		ns	
t_{DHR}	Data-In Hold Time, to $\overline{RAS}$	95		120		160		ns	

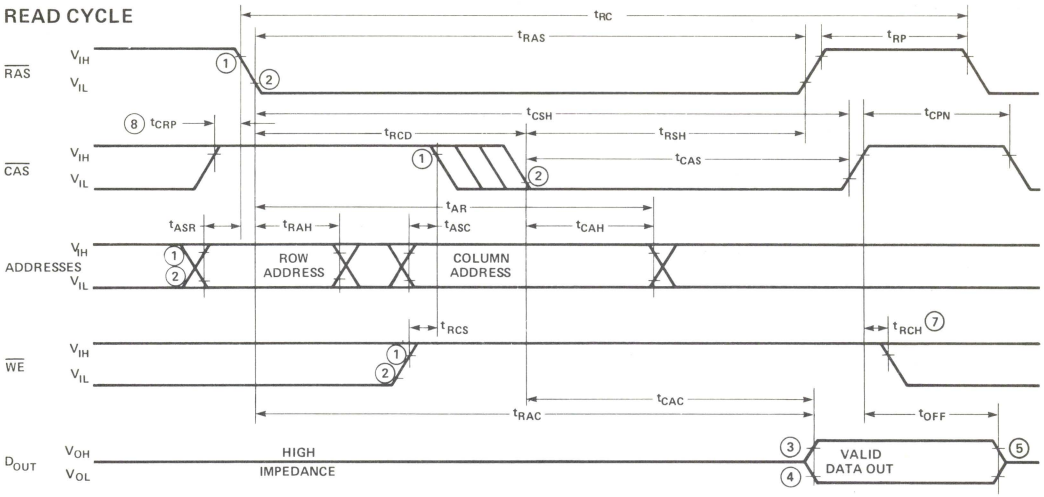
READ-MODIFY-WRITE CYCLE

t_{RWC}	Read-Modify-Write Cycle Time	330		375		475		ns	
t_{RRW}	RMW Cycle $\overline{RAS}$ Pulse Width	185	10000	245	10000	305	10000	ns	
t_{CRW}	RMW Cycle $\overline{CAS}$ Pulse Width	135	10000	180	10000	230	10000	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	120		160		200		ns	9
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	70		95		125		ns	9

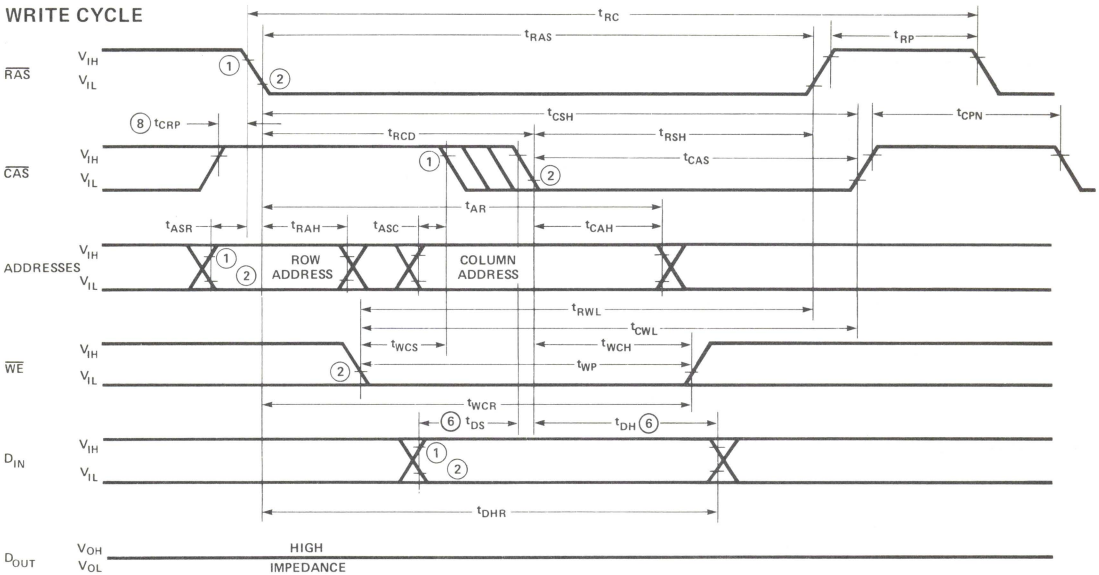
Notes: See following page for A.C. Characteristics Notes.

WAVEFORMS

READ CYCLE



WRITE CYCLE



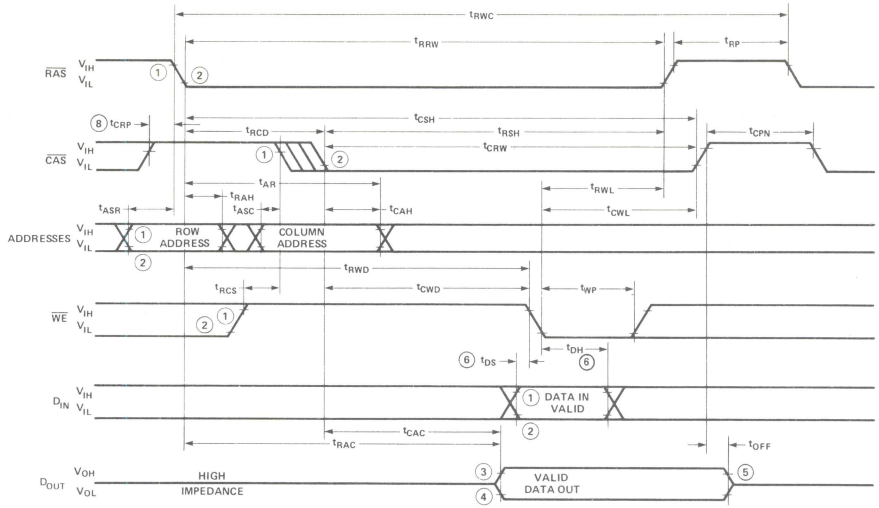
NOTES:
1,2. $V_{IH\ MIN}$ AND $V_{IL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF INPUT SIGNALS.
3,4. $V_{OH\ MIN}$ AND $V_{OL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF D_{OUT}.
5. t_{OFF} IS MEASURED TO $|I_{OUT}| \leq |I_{LO}|$.
6. t_{DS} AND t_{DH} ARE REFERENCED TO $\overline{CAS}$ OR $\overline{WE}$, WHICHEVER OCCURS LAST.
7. t_{RCH} IS REFERENCED TO THE TRAILING EDGE OF $\overline{CAS}$ OR $\overline{RAS}$, WHICHEVER OCCURS FIRST.
8. t_{CRP} REQUIREMENT IS ONLY APPLICABLE FOR $\overline{RAS}$/$\overline{CAS}$ CYCLES PRECEEDED BY A $\overline{CAS}$-ONLY CYCLE (i.e., FOR SYSTEMS WHERE $\overline{CAS}$ HAS NOT BEEN DECODED WITH $\overline{RAS}$).

A.C. CHARACTERISTICS NOTES (From Previous Page)

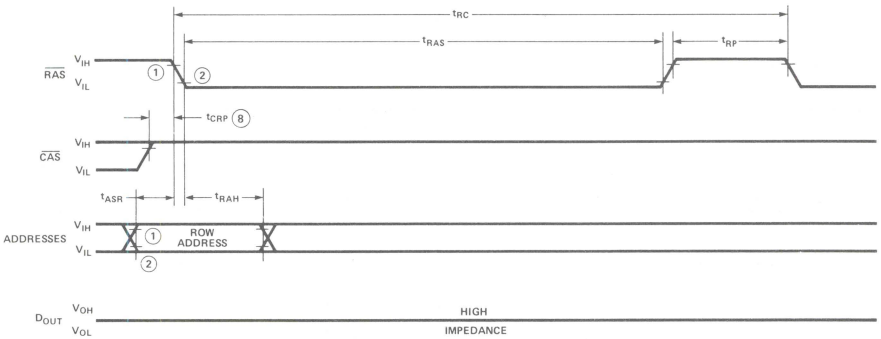
1. All voltages referenced to V_{SS}.
2. Eight cycles are required after power-up or prolonged periods (greater than 2ms) of $\overline{RAS}$ inactivity before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
3. A.C. Characteristics assume $t_T = 5ns$.
4. Assume that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.) then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
5. Load = 2 TTL loads and 100pF.
6. Assumes $t_{RCD} \geq t_{RCD}$ (max.).
7. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is less than t_{RCD} (max.) access time is t_{RAC}, if t_{RCD} is greater than t_{RCD} (max.) access time is $t_{RCD} + t_{CAC}$.
8. t_T is measured between V_{IH} (min.) and V_{IL} (max.).
9. t_{WCS}, t_{CWD} and t_{RWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}$ (min.) the cycle is an early write cycle and the data out pin will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} \geq t_{RWD}$ (min.), the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.

WAVEFORMS

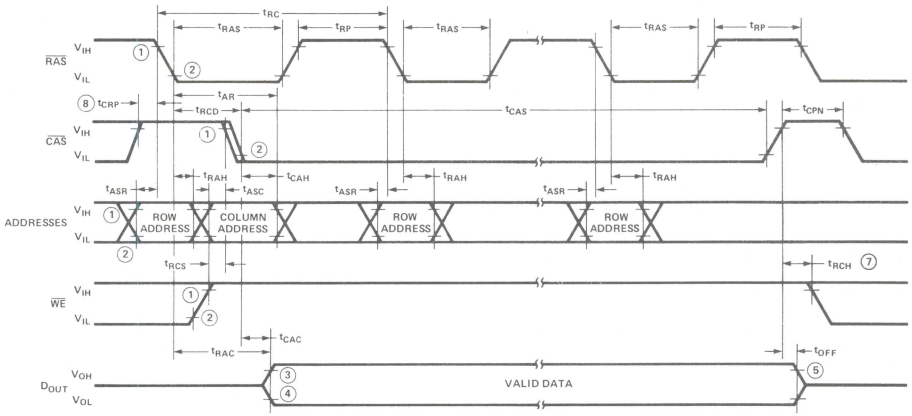
READ-MODIFY-WRITE CYCLE



RAS-ONLY REFRESH CYCLE



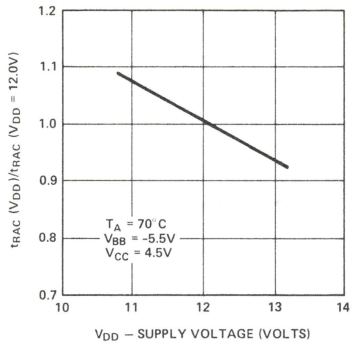
HIDDEN REFRESH CYCLE



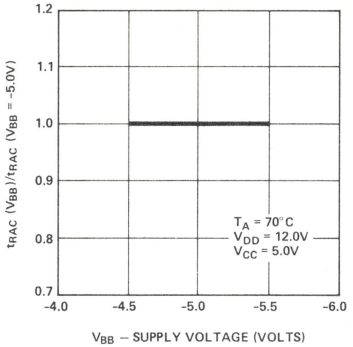
NOTES: 1,2. $V_{IH\ MIN}$ AND $V_{IL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF INPUT SIGNALS.
3,4. $V_{OH\ MIN}$ AND $V_{OL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF D_{OUT}.
5. t_{OFF} IS MEASURED TO $I_{OUT} \leq |I_{LO}|$.
6. t_{DS} AND t_{DH} ARE REFERENCED TO $\overline{CAS}$ OR $\overline{WE}$, WHICHEVER OCCURS LAST.
7. t_{RCH} IS REFERENCED TO THE TRAILING EDGE OF $\overline{CAS}$ OR $\overline{RAS}$, WHICHEVER OCCURS FIRST.
8. t_{CRP} REQUIREMENT IS ONLY APPLICABLE FOR $\overline{RAS}$/$\overline{CAS}$ CYCLES PRECEEDED BY A $\overline{CAS}$-ONLY CYCLE (i.e., FOR SYSTEMS WHERE $\overline{CAS}$ HAS NOT BEEN DECODED WITH $\overline{RAS}$).

TYPICAL CHARACTERISTICS[1]

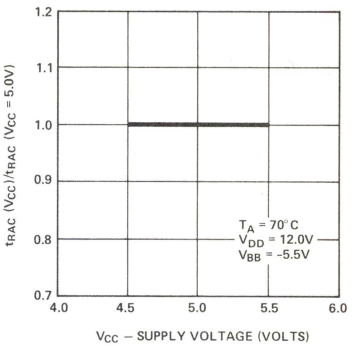
GRAPH 1
TYPICAL ACCESS TIME
t_{RAC} (NORMALIZED) VS. V_{DD}



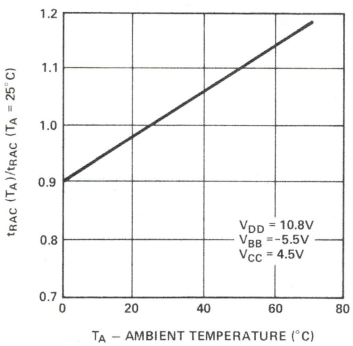
GRAPH 2
TYPICAL ACCESS TIME
t_{RAC} (NORMALIZED) VS. V_{BB}



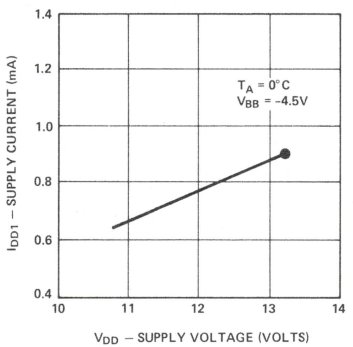
GRAPH 3
TYPICAL ACCESS TIME
t_{RAC} (NORMALIZED) VS. V_{CC}



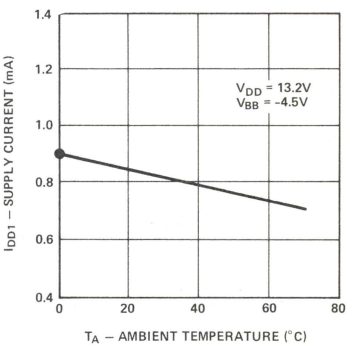
GRAPH 4
TYPICAL ACCESS TIME
t_{RAC} (NORMALIZED) VS.
AMBIENT TEMPERATURE



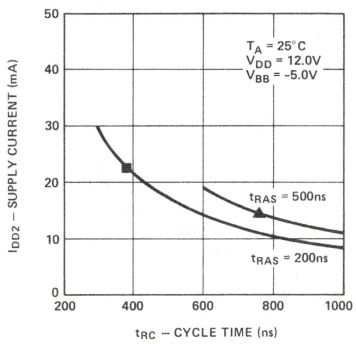
GRAPH 5
TYPICAL STANDBY CURRENT
I_{DD1} VS. V_{DD}



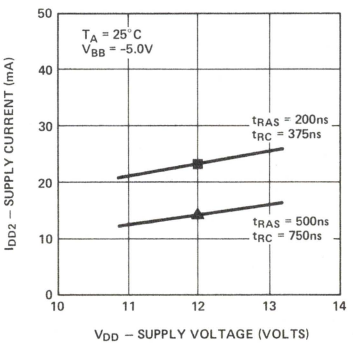
GRAPH 6
TYPICAL STANDBY CURRENT
I_{DD1} VS. AMBIENT TEMPERATURE



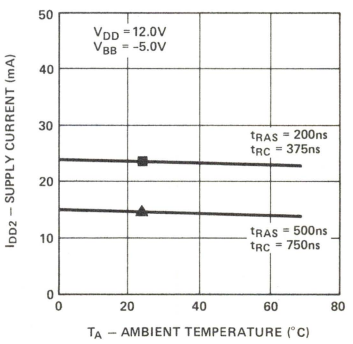
GRAPH 7
TYPICAL OPERATING CURRENT
I_{DD2} VS. t_{RC}



GRAPH 8
TYPICAL OPERATING CURRENT
I_{DD2} VS. V_{DD}



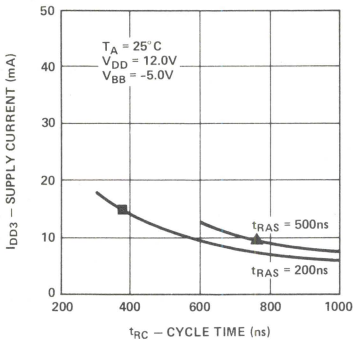
GRAPH 9
TYPICAL OPERATING CURRENT
I_{DD2} VS. AMBIENT TEMPERATURE



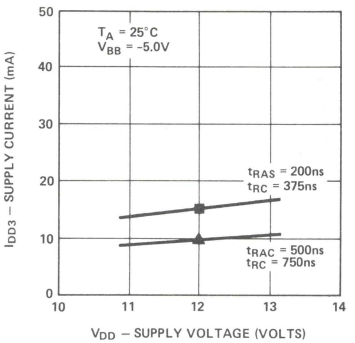
NOTES: See following page for Typical Characteristics Notes.

TYPICAL CHARACTERISTICS [1]

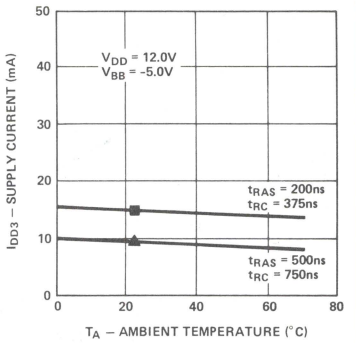
GRAPH 10
TYPICAL $\overline{RAS}$ ONLY
REFRESH CURRENT
I_{DD3} VS. t_{RC}



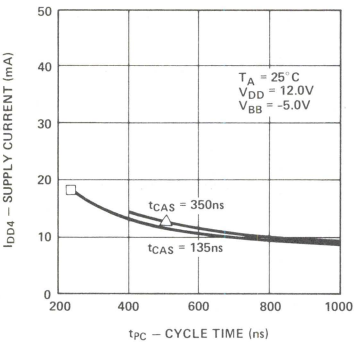
GRAPH 11
TYPICAL $\overline{RAS}$ ONLY
REFRESH CURRENT
I_{DD3} VS. V_{DD}



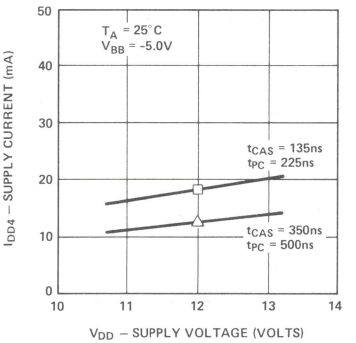
GRAPH 12
TYPICAL $\overline{RAS}$ ONLY
REFRESH CURRENT
I_{DD3} VS. AMBIENT TEMPERATURE



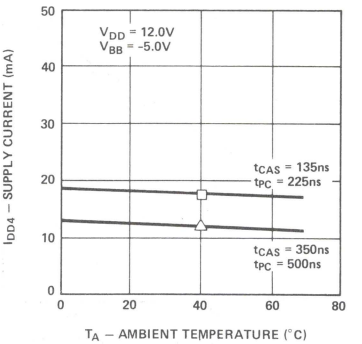
GRAPH 13
TYPICAL PAGE MODE CURRENT
I_{DD4} VS. t_{PC}



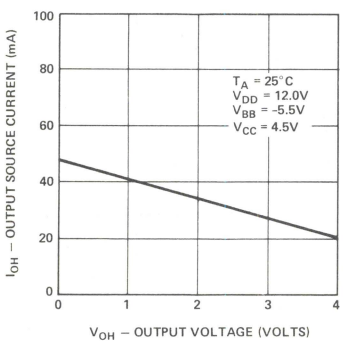
GRAPH 14
TYPICAL PAGE MODE CURRENT
I_{DD4} VS. V_{DD}



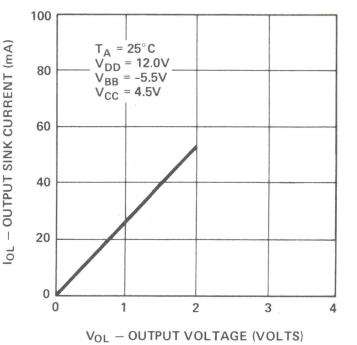
GRAPH 15
TYPICAL PAGE MODE CURRENT
I_{DD4} VS. AMBIENT TEMPERATURE



GRAPH 16
TYPICAL OUTPUT SOURCE CURRENT
I_{OH} VS. OUTPUT VOLTAGE V_{OH}



GRAPH 17
TYPICAL OUTPUT SINK CURRENT
I_{OL} VS. OUTPUT VOLTAGE V_{OL}



NOTES:

1. The cycle time, V_{DD} supply voltage, and ambient temperature dependence of I_{DD1}, I_{DD2}, I_{DD3} and I_{DD4} is shown in related graphs. Common points of related curves are indicated:
   - ● I_{DD1} @ V_{DD} = 13.2V, T_A = 0°C
   - ■ I_{DD2} or I_{DD3} @ t_{RAS} = 200ns, t_{RC} = 375ns, V_{DD} = 12.0V, T_A = 25°C
   - ▲ I_{DD2} or I_{DD3} @ t_{RAS} = 500ns, t_{RC} = 750ns, V_{DD} = 12.0V, T_A = 25°C
   - □ I_{DD4} @ t_{CAS} = 135ns, t_{PC} = 225ns, V_{DD} = 12.0V, T_A = 25°C
   - △ I_{DD4} @ t_{CAS} = 350ns, t_{PC} = 500ns, V_{DD} = 12.0V, T_A = 25°C

   The typical I_{DD} current for a given combination of cycle time, V_{DD} supply voltage and ambient temperature may be determined by combining the effects of the appropriate family of curves.

D.C. AND A.C. CHARACTERISTICS, PAGE MODE [7,8,11]

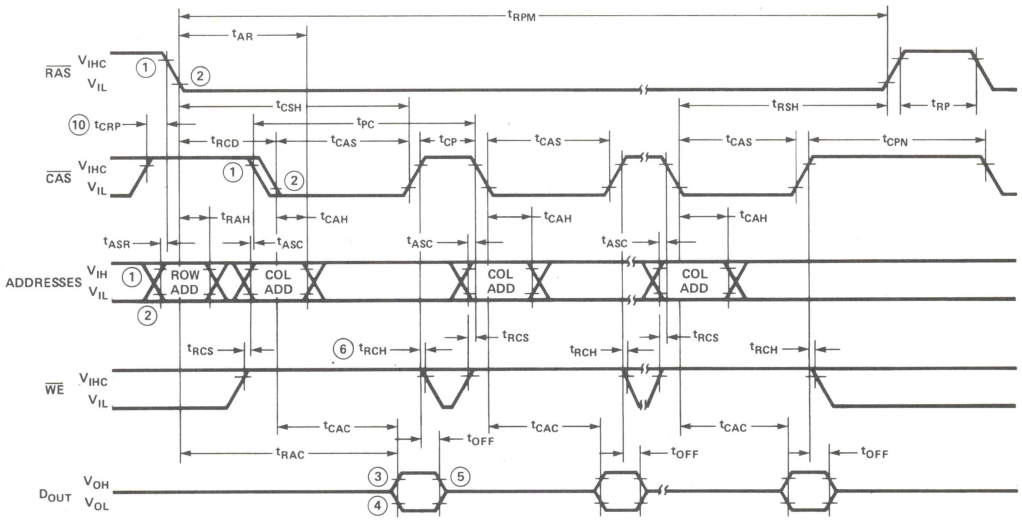
T_A = 0°C to 70°C, V_{DD} = 12V±10%, V_{CC} = 5V±10%, V_{BB} = -5V±10%, V_{SS} = 0V, unless otherwise noted.

For Page Mode Operation order 2117-2 S6053, 2117-3 S6054, or 2117-4 S6055.

Symbol	Parameter	2117-2 S6053		2117-3 S6054		2117-4 S6055		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PC}	Page Mode Read or Write Cycle	170		225		275		ns	
t_{PCM}	Page Mode Read Modify Write	205		270		340		ns	
t_{CP}	$\overline{CAS}$ Precharge Time, Page Cycle	60		80		100		ns	
t_{RPM}	$\overline{RAS}$ Pulse Width, Page Mode	150	10,000	200	10,000	250	10,000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	100	10,000	135	10,000	165	10,000	ns	
I_{DD4}	V_{DD} Supply Current Page Mode, Minimum t_{PC}, Minimum t_{CAS}		38		30		26	mA	9

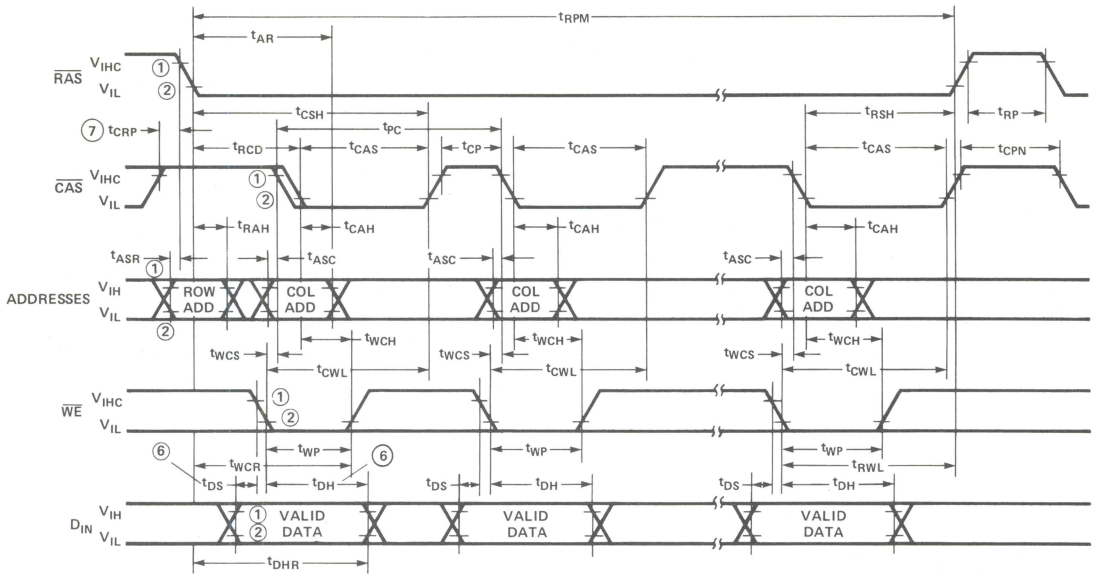
WAVEFORMS

PAGE MODE READ CYCLE

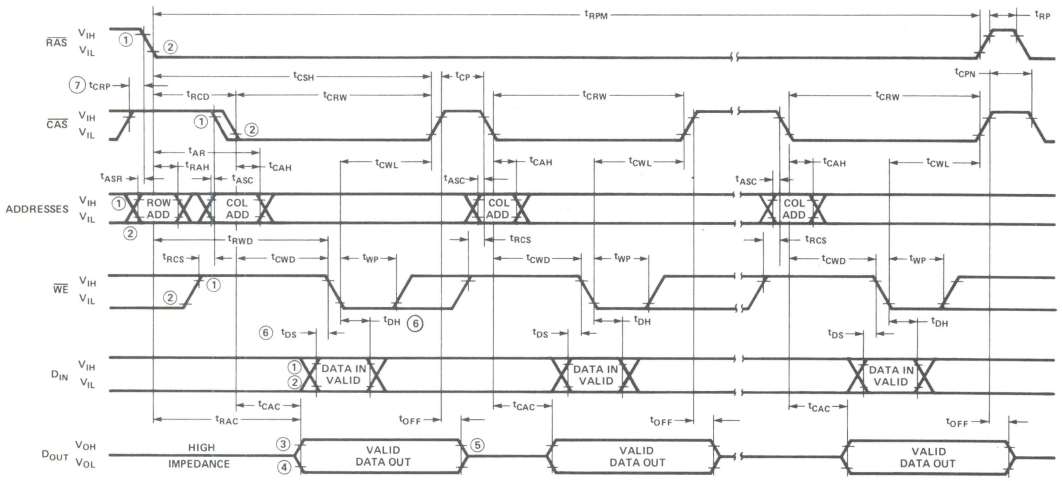


NOTES:
1,2. $V_{IH\ MIN}$ AND $V_{IL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF INPUT SIGNALS.
3,4. $V_{OH\ MIN}$ AND $V_{OL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF D_{OUT}.
5. t_{OFF} IS MEASURED TO $|I_{OUT}| \leq |I_{LO}|$.
6. t_{RCH} IS REFERENCED TO THE TRAILING EDGE OF $\overline{CAS}$ OR $\overline{RAS}$, WHICHEVER OCCURS FIRST.
7. ALL VOLTAGES REFERENCED TO V_{SS}.
8. AC CHARACTERISTIC ASSUME t_T = 5ns.
9. SEE THE TYPICAL CHARACTERISTICS SECTION FOR VALUES OF THIS PARAMETER UNDER ALTERNATE CONDITIONS.
10. t_{CRP} REQUIREMENT IS ONLY APPLICABLE FOR $\overline{RAS}$/$\overline{CAS}$ CYCLES PRECEEDED BY A $\overline{CAS}$-ONLY CYCLE (i.e., FOR SYSTEMS WHERE $\overline{CAS}$ HAS NOT BEEN DECODED WITH $\overline{RAS}$).
11. ALL PREVIOUSLY SPECIFIED A.C. AND D.C. CHARACTERISTICS ARE APPLICABLE TO THEIR RESPECTIVE PAGE MODE DEVICE (i.e., 2117-3, S6054 WILL OPERATE AS A 2117-3).

PAGE MODE WRITE CYCLE



PAGE MODE READ-MODIFY-WRITE CYCLE



NOTES: 1,2. $V_{IH\ MIN}$ AND $V_{IL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF INPUT SIGNALS.
3,4. $V_{OH\ MIN}$ AND $V_{OL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF D_{OUT}.
5. t_{OFF} IS MEASURED TO $|I_{OUT}| \leq |I_{LO}|$.
6. t_{DS} AND t_{DH} ARE REFERENCED TO $\overline{CAS}$ OR $\overline{WE}$, WHICHEVER OCCURS LAST.
7. t_{CRP} REQUIREMENT IS ONLY APPLICABLE FOR $\overline{RAS}$/$\overline{CAS}$ CYCLES PRECEEDED BY A $\overline{CAS}$-ONLY CYCLE (i.e., FOR SYSTEMS WHERE $\overline{CAS}$ HAS NOT BEEN DECODED WITH $\overline{RAS}$).

APPLICATIONS

READ CYCLE

A Read cycle is performed by maintaining Write Enable ($\overline{WE}$) high during a $\overline{RAS}/\overline{CAS}$ operation. The output pin of a selected device will remain in a high impedance state until valid data appears at the output at access time.

Device access time, t_{ACC}, is the longer of the two calculated intervals:

1. $t_{ACC} = t_{RAC}$ OR 2. $t_{ACC} = t_{RCD} + t_{CAC}$

Access time from $\overline{RAS}$, t_{RAC}, and access time from $\overline{CAS}$, t_{CAC}, are device parameters. Row to column address strobe delay time, t_{RCD}, are system dependent timing parameters. For example, substituting the device parameters of the 2117-3 yields:

3. $t_{ACC} = t_{RAC} = 200$nsec for 25nsec $\leq t_{RCL} \leq 65$ nsec
   OR
4. $t_{ACC} = t_{RCD} + t_{CAC} = t_{RCD} + 135$ for $t_{RCD} > 65$nsec

Note that if 25nsec $\leq t_{RCD} \leq 65$nsec device access time is determined by equation 3 and is equal to t_{RAC}. If $t_{RCL} > 65$nsec, access time is determined by equation 4. This 40nsec interval (shown in the t_{RCD} inequality in equation 3) in which the falling edge of $\overline{CAS}$ can occur without affecting access time is provided to allow for system timing skew in the generation of $\overline{CAS}$.

REFRESH CYCLES

Each of the 128 rows of the 2117 must be refreshed every 2 milliseconds to maintain data. Any memory cycle:

1. Read Cycle
2. Write Cycle (Early Write, Delayed Write or Read-Modify-Write)
3. $\overline{RAS}$-only Cycle

refreshes the selected row as defined by the low order ($\overline{RAS}$) addresses. Any Write cycle, of course, may change the state of the selected cell. Using a Read, Write, or Read-Modify-Write cycle for refresh is not recommended for systems which utilize "wire-OR" outputs since output bus contention will occur.

A $\overline{RAS}$-only refresh cycle is the recommended technique for most applications to provide for data retention. A $\overline{RAS}$-only refresh cycle maintains the D_{OUT} in the high impedance state with a typical power reduction of 20% over a Read or Write cycle.

$\overline{RAS}/\overline{CAS}$ TIMING

$\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths as defined by t_{RAS} and t_{CAS} respectively. These minimum pulse widths must be maintained for proper device operation and data integrity. A cycle, once begun by driving $\overline{RAS}$ and/or $\overline{CAS}$ low must not be ended or aborted prior to fulfilling the minimum clock signal pulse width(s). A new cycle can not begin until the minimum precharge time, t_{RP}, has been met.

DATA OUTPUT OPERATION

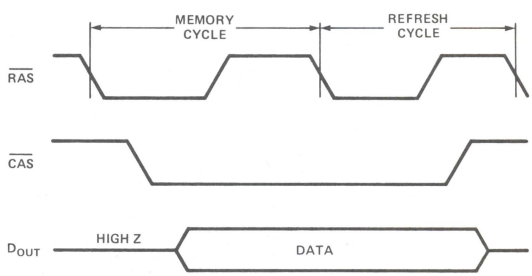
The 2117 Data Output (D_{OUT}), which has three-state capability, is controlled by $\overline{CAS}$. During $\overline{CAS}$ high state ($\overline{CAS}$ at V_{IH}) the output is in the high impedance state. The following table summarizes the D_{OUT} state for various types of cycles.

Intel 2117 Data Output Operation for Various Types of Cycles

Type of Cycle	D_{OUT} State
Read Cycle	Data From Addressed Memory Cell
Fast Write Cycle	HI-Z
$\overline{RAS}$-Only Refresh Cycle	HI-Z
$\overline{CAS}$-Only Cycle	HI-Z
Read/Modify/Write Cycle	Data From Addressed Memory Cell
Delayed Write Cycle	Indeterminate

HIDDEN REFRESH

A feature of the 2117 is that refresh cycles may be performed while maintaining valid data at the output pin. This feature is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a "$\overline{RAS}$-Only" refresh cycle, but with $\overline{CAS}$ held low (see Figure below).



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

POWER ON

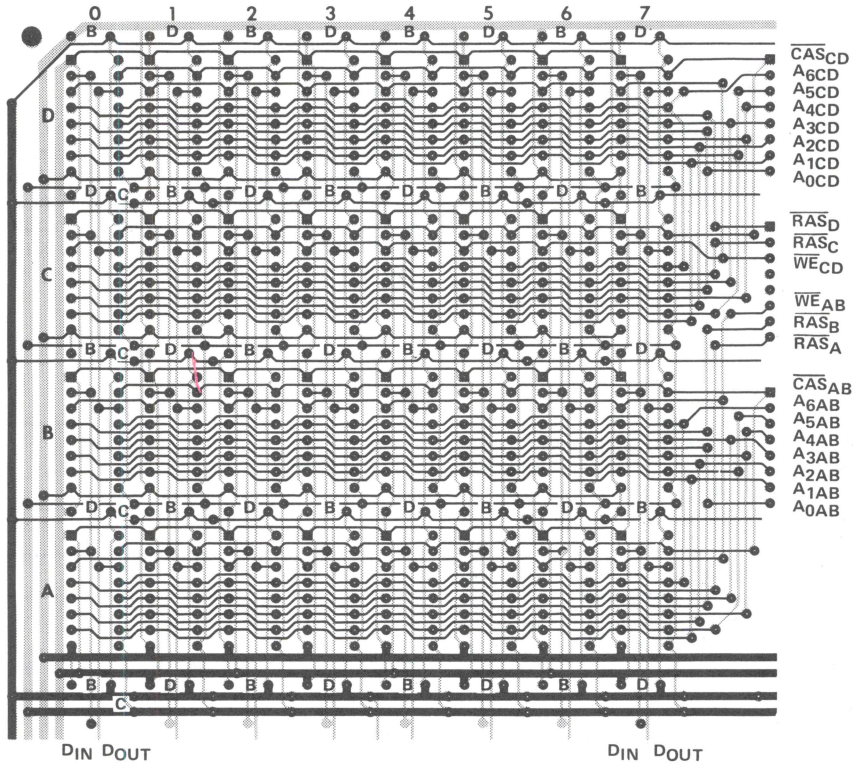
The 2117 requires no power on sequence providing absolute maximum ratings are not exceeded. After the application of supply voltages or after extended periods of bias (greater than 2 milliseconds) without clocks, the device must perform a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock, such as $\overline{RAS}$-Only refresh) prior to normal operation.

POWER SUPPLY DECOUPLING/DISTRIBUTION

It is recommended that a 0.1μF ceramic capacitor be connected between V_{DD} and V_{SS} at every other device in the memory array. A 0.1μF ceramic capacitor should also be connected between V_{BB} and V_{SS} at every other device (preferably the alternate devices to the V_{DD} decoupling). For each 16 devices, a 10μF tantalum or equivalent capacitor should be connected between V_{DD} and V_{SS} near the array. An equal or slightly smaller bulk capacitor is also recommended between V_{BB} and V_{SS} for every 32 devices.

The V_{CC} supply is connected only to the 2117 output buffer and is not used internally. The load current from the V_{CC} supply is dependent only upon the output loading and is associated with the input high level current to a TTL gate and the output leakage currents of any OR-tied 2117's (typically 100μA or less total). Intel recommends that a 0.1 or 0.01μF ceramic capacitor be connected between V_{CC} and V_{SS} for every eight memory devices.

Due to the high frequency characteristics of the current waveforms, the inductance of the power supply distribution system on the array board should be minimized. It is recommended that the V_{DD}, V_{BB}, and V_{SS} supply lines be gridded both horizontally and vertically at each device in the array. This technique allows use of double sided circuit boards with noise performance equal to or better than multi-layered circuit boards.



DECOUPLING CAPACITORS
D = 0.1μF TO V_{DD} TO V_{SS}
B = 0.1μF V_{BB} TO V_{SS}
C = 0.01μF V_{CC} TO V_{SS}

SAMPLE P.C. BOARD LAYOUT EMPLOYING VERTICAL AND HORIZONTAL GRIDDING ON ALL POWER SUPPLIES.

BOARD ORGANIZATION: 64K WORDS BY 8-BITS.

64K BYTE STORAGE ARRAY LAYOUT

ADVANCE INFORMATION
Characteristics are subject to change without notice.

2141
4096 X 1 BIT STATIC RAM

	2141-2	2141-3	2141-4	2141-5	2141L-3	2141L-4	2141L-5
Max. Access Time (ns)	120	150	200	250	150	200	250
Max. Active Current (mA)	70	70	55	55	40	40	40
Max. Standby Current (mA)	20	20	12	12	5	5	5

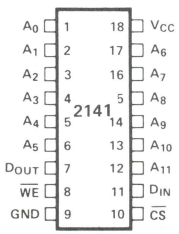
- **HMOS Technology**
- **Industry Standard 2147 Pinout**
- **Completely Static Memory — No Clock or Timing Strobe Required**
- **Equal Access and Cycle Times**
- **Single +5V Supply**
- **Automatic Power-Down**
- **Directly TTL Compatible — All Inputs and Outputs**
- **Separate Data Input and Output**
- **Three-State Output**
- **High Density 18-Pin Package**

The Intel® 2141 is a 4096-bit static Random Access Memory organized as 4096 words by 1-bit using HMOS, a high-performance MOS technology. It uses a uniquely innovative design approach which provides the ease-of-use features associated with non-clocked static memories and the reduced standby power dissipation associated with clocked static memories. To the user this means low standby power dissipation without the need for clocks, address setup and hold times, nor reduced data rates due to cycle times that are longer than access times.

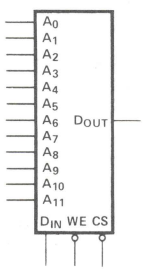
$\overline{CS}$ controls the power-down feature. In less than a cycle time after $\overline{CS}$ goes high — deselecting the 2141 — the part automatically reduces its power requirements and remains in this low power standby mode as long as $\overline{CS}$ remains high. This device feature results in system power savings as great as 85% in larger systems, where the majority of devices are de-selected.

The 2141 is placed in an 18-pin package configured with the industry standard pinout, the same as the 2147. It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. The data is read out nondestructively and has the same polarity as the input data. A data input and a separate three-state output are used.

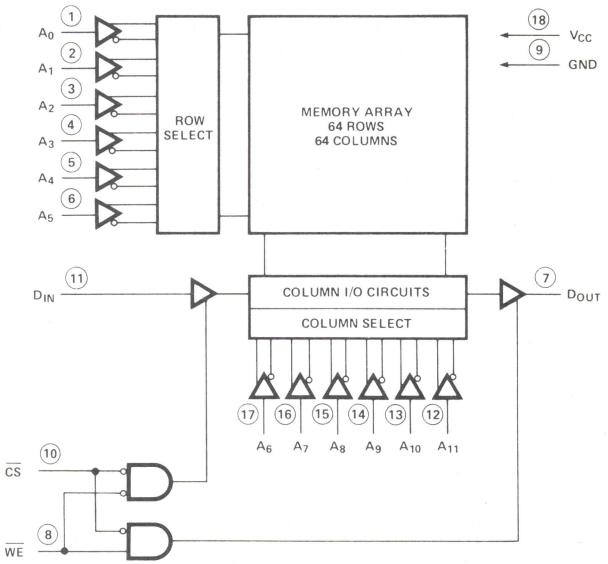
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0–A_{11}	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND	GROUND
$\overline{CS}$	CHIP SELECT		
D_{IN}	DATA INPUT		
D_{OUT}	DATA OUTPUT		

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH Z	STANDBY
L	L	WRITE	HIGH Z	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

ADVANCE INFORMATION
Characteristics subject to change without notice

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -10°C to 85°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin With
Respect to Ground ..... -0.5V to +7V
D.C. Output Current ..... 20 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ±10% unless otherwise noted.

Symbol	Parameter	2141-2/-3 Min.	2141-2/-3 Typ.[1]	2141-2/-3 Max.	2141-4/-5 Min.	2141-4/-5 Typ.[1]	2141-4/-5 Max.	2141L-3/L-4/L-5 Min.	2141L-3/L-4/L-5 Typ.[1]	2141L-3/L-4/L-5 Max.	Unit	Conditions
I_{LI}	Input Load Current (All Input Pins)		0.01	10		0.01	10		0.01	10	µA	V_{CC}=Max., V_{IN}= GND to V_{CC}
$\|I_{LO}\|$	Output Leakage Current		0.1	10		0.1	10		0.1	10	µA	$\overline{CS}$=V_{IH}, V_{CC}=Max., V_{OUT}=GND to 4.5V
I_{CC}	Operating Current		45			40			30		mA	T_A=25°C; V_{CC}=Max. $\overline{CS}$=V_{IL}, Outputs Open
				70			55			40	mA	T_A=0°C; V_{CC}=Max. $\overline{CS}$=V_{IL}, Outputs Open
I_{SB}	Standby Current			20			12			5	mA	V_{CC}=Min. to Max., $\overline{CS}$=V_{IH}
I_{PO}[2]	Peak Power-On Current			40			30			18	mA	V_{CC}=GND to V_{CC} Min. $\overline{CS}$=Lower of V_{CC} or V_{IH} Min.
V_{IL}	Input Low Voltage	-0.3		0.8	-0.3		0.8	-0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		6.0	2.0		6.0	2.0		6.0	V	
V_{OL}	Output Low Voltage			0.4			0.4			0.4	V	I_{OL} = 4.0mA
V_{OH}	Output High Voltage	2.4			2.4			2.4			V	I_{OH} = -200µA

Notes: 1. Typical limits are at V_{CC} = 5V, T_A = +25°C, and specified loading.
2. I_{CC} exceeds I_{SB} maximum during power-on, as shown in Graph 1. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected; otherwise, power-on current approaches I_{CC} active.

A.C. TEST CONDITIONS

Input Pulse Levels	GND to 3.5 Volts
Input Rise and Fall Times	10 nsec
Input and Output Timing Reference Levels	1.5 Volts
Output Load	1 TTL Load plus 100pF

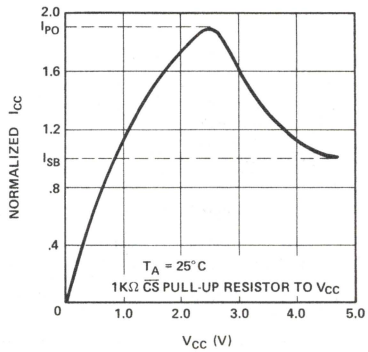
CAPACITANCE[3]

T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Max.	Unit	Conditions
C_{IN}	Input Capacitance	5	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	10	pF	V_{OUT} = 0V

Note 3. This parameter is sampled and not 100% tested.

GRAPH 1
TYPICAL POWER-ON CURRENT
VS. POWER SUPPLY VOLTAGE



ADVANCE INFORMATION
Characteristics are subject to change without notice.

A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V±5%, unless otherwise noted.

READ CYCLE

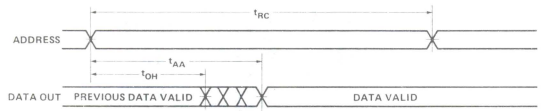
Symbol	Parameter	2141-2 Min.	2141-2 Max.	2141-3/L-3 Min.	2141-3/L-3 Max.	2141-4/L-4 Min.	2141-4/L-4 Max.	2141-5/L-5 Min.	2141-5/L-5 Max.	Unit
t_{RC}	Read Cycle Time	120		150		200		250		ns
t_{AA}	Address Access Time		120		150		200		250	ns
t_{ACS1}[1]	Chip Select Access Time		120		150		200		250	ns
t_{ACS2}[2]	Chip Select Access Time		130		160		200		250	ns
t_{OH}	Output Hold from Address Change	10		10		10		10		ns
t_{LZ}	Chip Selection to Output in Low Z	10		10		10		10		ns
t_{HZ}	Chip Deselection to Output in High Z	0	60	0	60	0	60	0	60	ns
t_{PU}	Chip Selection to Power Up Time	0		0		0		0		ns
t_{PD}	Chip Deselection to Power Down Time		60		80		100		100	ns

WRITE CYCLE

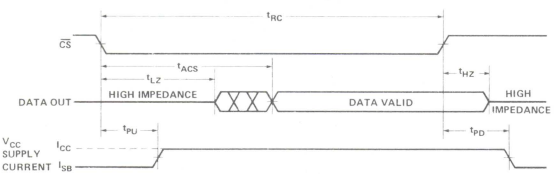
Symbol	Parameter	2141-2 Min.	2141-2 Max.	2141-3/L-3 Min.	2141-3/L-3 Max.	2141-4/L-4 Min.	2141-4/L-4 Max.	2141-5/L-5 Min.	2141-5/L-5 Max.	Unit
t_{WC}	Write Cycle Time	120		150		200		250		ns
t_{CW}	Chip Selection to End of Write	110		135		180		230		ns
t_{AW}	Address Valid to End of Write	110		135		180		230		ns
t_{AS}	Address Setup Time	0		0		0		0		ns
t_{WP}	Write Pulse Width	60		70		100		150		ns
t_{WR}	Write Recovery Time	10		15		20		20		ns
t_{DW}	Data Valid to End of Write	50		60		90		130		ns
t_{DH}	Data Hold Time	10		15		15		15		ns
t_{WZ}	Write Enabled to Output in High Z	0	60	0	60	0	60	0	60	ns
t_{OW}	Output Active from End of Write	0		0		0		0		ns

WAVEFORMS

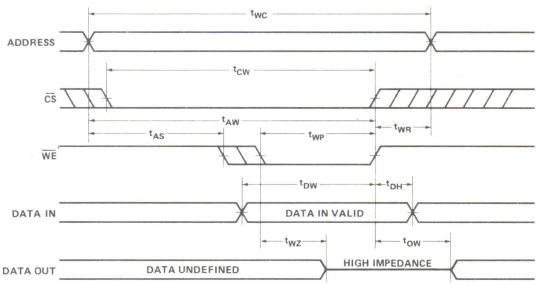
READ CYCLE NO. 1[3,4]



READ CYCLE NO. 2[3,5]



WRITE CYCLE



Notes:
1. Chip deselected for greater than 55ns prior to selection.
2. Chip deselected for a finite time that is less than 55ns prior to selection. (If the deselect time is 0ns, the chip is by definition selected and access occurs according to Read Cycle No. 1.)
3. $\overline{WE}$ is high for Read Cycles.
4. Device is continuously selected, $\overline{CS}$ = V_{IL}.
5. Addresses valid prior to or coincident with $\overline{CS}$ transition low.

ADVANCE INFORMATION
Characteristics are subject to change without notice.

DEVICE DESCRIPTION

The 2141 is produced with HMOS, a new high-performance MOS technology which incorporates on-chip substrate bias generation to achieve high-performance. This process, combined with new design ideas, gives the 2141 its unique features. Both low power and ease-of-use have been obtained in a single part. The low-power feature is controlled with the Chip Select input, which is not a clock and does not have to be cycled. Multiple read or write operations are possible during a single select period. Access times are equal to cycle times, resulting in data rates up to 8.3 MHz for the 2141-2. This is considerably higher performance than for clocked static designs.

Whenever the 2141 is deselected, it automatically reduces its power requirements to a fraction of the active power, as shown in Figure 1. This is achieved by switching off the power to unnecessary portions of the internal peripheral circuitry. This feature adds up to significant system power savings. The average power per device declines as system size grows because a continually higher portion of the memory is deselected. Device power dissipation asymptotically approaches the standby power level, as shown in Figure 2.

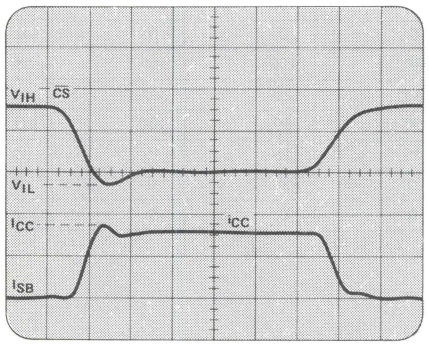


FIGURE 1. i_{CC} WAVEFORM.

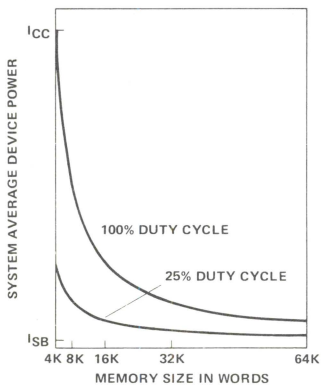


FIGURE 2. AVERAGE DEVICE DISSIPATION VS. MEMORY SIZE.

There is no functional constraint on the amount of time the 2141 is deselected. However, there is a relationship between deselect time and Chip Select access time. With no compensation, the automatic power switch would cause an increase in Chip Select access time, since some time is lost in repowering the device upon selection. A feature of the 2141 design is its ability to compensate for this loss. The amount of compensation is a function of deselect time, as shown in Figure 3. For short deselect times, Chip Select access time becomes slower than address access time, since full compensation typically requires 60ns. For longer deselect times, Chip Select access time actually becomes faster than address access time because the compensation more than offsets the time lost in powering up. The spec accounts for this characteristic by specifying two Chip Select access times, t_{ACS1} and t_{ACS2}.

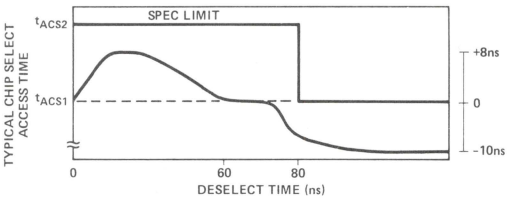


FIGURE 3. t_{ACS} VS. DESELECT TIME.

The power switching characteristic of the 2141 requires more careful decoupling than would be required of a constant power device. It is recommended that a 0.1μF ceramic capacitor be used on every other device, with a 22μF to 47μF bulk electrolytic decoupler every 32 devices. The actual values to be used will depend on board layout, trace widths and duty cycle. Power supply gridding is recommended for PC board layout. A very satisfactory grid can be developed on a two-layer board with vertical traces on one side and horizontal traces on the other, as shown in Figure 4.

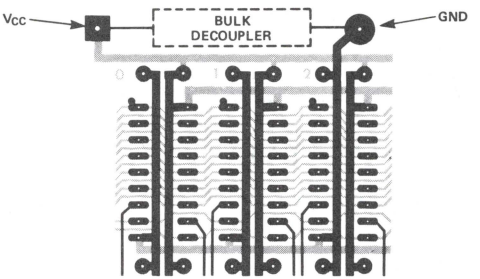


FIGURE 4. PC LAYOUT.

Terminations are recommended on input signal lines to the 2141 devices. In high speed systems, fast drivers can cause significant reflections when driving the high impedance inputs of the 2141. Terminations may be required to match the impedance of the line to the driver. The type of termination used depends on designer preference and may be parallel .resistive or resistive-capacitive. The latter reduces terminator power dissipation.

2142
1024 X 4 BIT STATIC RAM

	2142-2	2142-3	2142	2142L2	2142L3	2142L
Max. Access Time (ns)	200	300	450	200	300	450
Max. Power Dissipation (mw)	525	525	525	370	370	370

- **High Density 20 Pin Package**
- **Access Time Selections From 200-450ns**
- **Identical Cycle and Access Times**
- **Low Operating Power Dissipation .1mW/Bit Typical**
- **Single +5V Supply**
- **No Clock or Timing Strobe Required**
- **Completely Static Memory**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Common Data Input and Output Using Three-State Outputs**

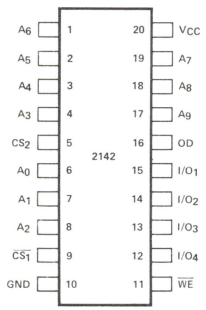
The Intel® 2142 is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits using N-channel Silicon-Gate MOS technology. It uses fully DC stable (static) circuitry throughout — in both the array and the decoding — and therefore requires no clocks or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

The 2142 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply.

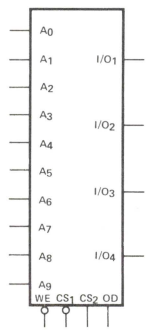
The 2142 is placed in a 20-pin package. Two Chip Selects ($\overline{CS}_1$ and CS_2) are provided for easy and flexible selection of individual packages when outputs are OR-tied. An Output Disable is included for direct control of the output buffers.

The 2142 is fabricated with Intel's N-channel Silicon-Gate technology — a technology providing excellent protection against contamination permitting the use of low cost plastic packaging.

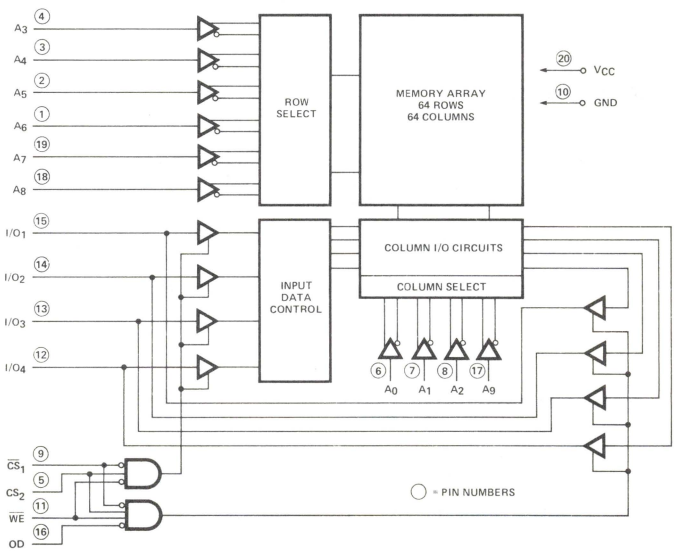
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0–A_9	ADDRESS INPUTS	OD	OUTPUT DISABLE
$\overline{WE}$	WRITE ENABLE	V_{CC}	POWER (+5V)
$\overline{CS}_1$, CS_2	CHIP SELECT	GND	GROUND
I/O_1–I/O_4	DATA INPUT/OUTPUT		

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -10°C to 80°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin
With Respect to Ground ..... -0.5V to +7V
Power Dissipation 1.0W
D.C. Output Current 10mA

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise noted.

SYMBOL	PARAMETER	2142-2, 2142-3, 2142 Min.	Typ.[1]	Max.	2142L2, 2142L3, 2142L Min.	Typ.[1]	Max.	UNIT	CONDITIONS
I_{LI}	Input Load Current (All Input Pins)			10			10	µA	V_{IN} = 0 to 5.25V
$\|I_{LO}\|$	I/O Leakage Current			10			10	µA	$\overline{CS}$ = 2.4V, $V_{I/O}$ = 0.4V to V_{CC}
I_{CC1}	Power Supply Current		80	95			65	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0 mA, T_A = 25°C
I_{CC2}	Power Supply Current			100			70	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0 mA, T_A = 0°C
V_{IL}	Input Low Voltage	-0.5		0.8	-0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		6.0	2.0		6.0	V	
I_{OL}	Output Low Current	2.1	6.0		2.1	6.0		mA	V_{OL} = 0.4V
I_{OH}	Output High Current	-1.0	-1.4		-1.0	-1.4		mA	V_{OH} = 2.4V
I_{OS}[2]	Output Short Circuit Current			40			40	mA	$V_{I/O}$ = GND to V_{CC}

NOTE: 1. Typical values are for T_A = 25°C and V_{CC} = 5.0V.
2. Duration not to exceed 30 seconds.

CAPACITANCE

T_A = 25°C, f = 1.0 MHz

SYMBOL	TEST	MAX	UNIT	CONDITIONS
$C_{I/O}$	Input/Output Capacitance	5	pF	$V_{I/O}$ = OV
C_{IN}	Input Capacitance	5	pF	V_{IN} = OV

NOTE: This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels ..... 0.8 Volt to 2.4 Volt
Input Rise and Fall Times ..... 10 nsec
Input and Output Timing Levels ..... 1.5 Volts
Output Load ..... 1 TTL Gate and C_L = 100 pF

A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise noted.

READ CYCLE [1]

SYMBOL	PARAMETER	2142-2, 2142L2 Min.	2142-2, 2142L2 Max.	2142-3, 2142L3 Min.	2142-3, 2142L3 Max.	2142, 2142L Min.	2142, 2142L Max.	UNIT
t_{RC}	Read Cycle Time	200		300		450		ns
t_A	Access Time		200		300		450	ns
t_{OD}	Output Enable to Output Valid		70		100		120	ns
t_{ODX}	Output Enable to Output Active	20		20		20		ns
t_{CO}	Chip Selection to Output Valid		70		100		120	ns
t_{CX}	Chip Selection to Output Active	20		20		20		ns
t_{OTD}	Output 3-state from Disable		60		80		100	ns
t_{OHA}	Output Hold from Address Change	50		50		50		ns

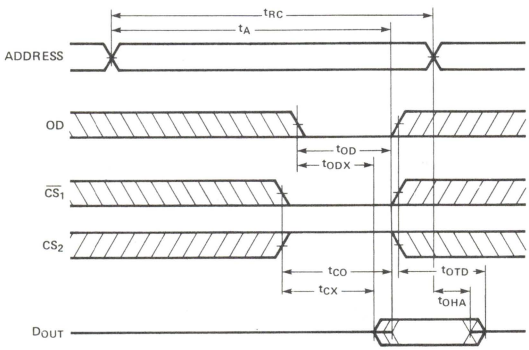
WRITE CYCLE [2]

SYMBOL	PARAMETER	2142-2, 2142L2 Min.	2142-2, 2142L2 Max.	2142-3, 2142L3 Min.	2142-3, 2142L3 Max.	2142, 2142L Min.	2142, 2142L Max.	UNIT
t_{WC}	Write Cycle Time	200		300		450		ns
t_W	Write Time	120		150		200		ns
t_{WR}	Write Release Time	0		0		0		ns
t_{OTD}	Output 3-state from Disable		60		80		100	ns
t_{DW}	Data to Write Time Overlap	120		150		200		ns
t_{DH}	Data Hold From Write Time	0		0		0		ns

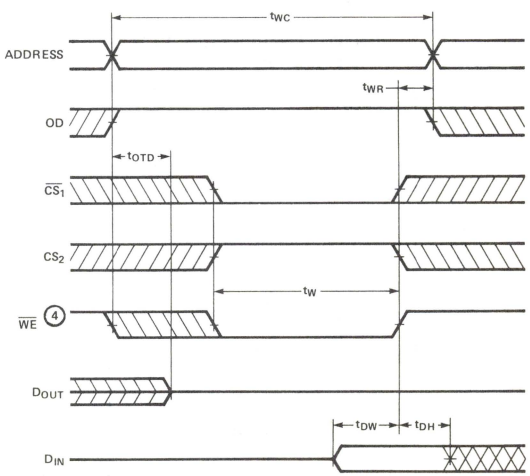
NOTES:
1. A Read occurs during the overlap of a low $\overline{CS}$ and a high $\overline{WE}$.
2. A Write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

WAVEFORMS

READ CYCLE ③



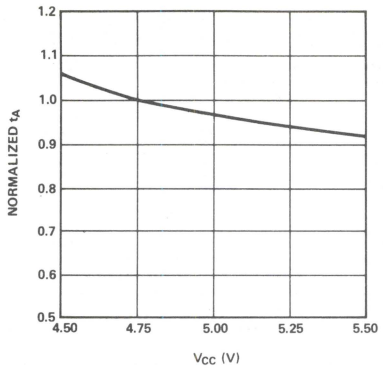
WRITE CYCLE



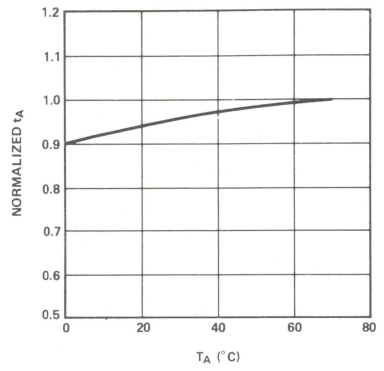
NOTES:
③ $\overline{WE}$ is high for a Read Cycle.
④ $\overline{WE}$ must be high during all address transitions.

TYPICAL D.C. AND A.C. CHARACTERISTICS

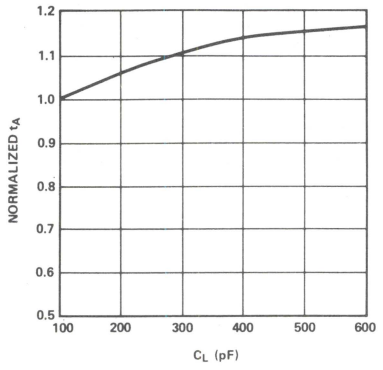
NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE



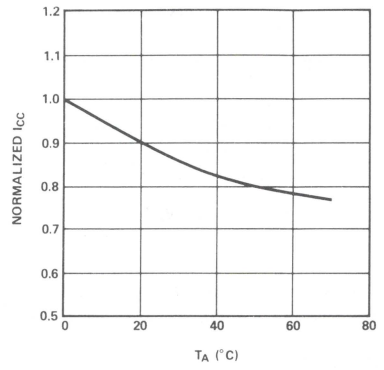
NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE



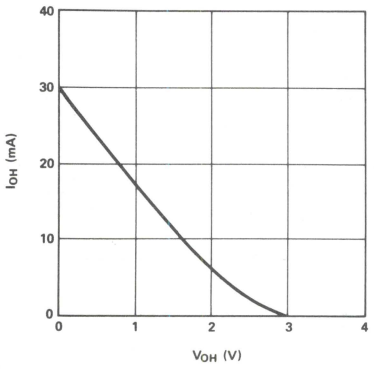
NORMALIZED ACCESS TIME VS. OUTPUT LOAD CAPACITANCE



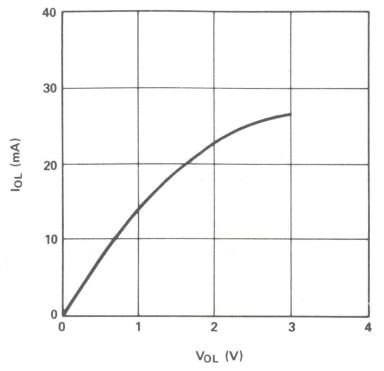
NORMALIZED POWER SUPPLY CURRENT VS. AMBIENT TEMPERATURE



OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



M2142
1024 X 4 BIT STATIC RAM

	2142
Max. Access Time (ns)	450
Max. Power Dissipation (mw)	550

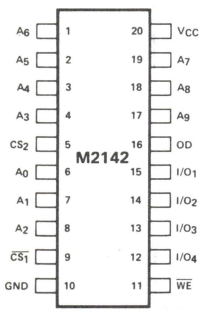
- **High Density 20 Pin Package**
- **Access Time-450ns**
- **Identical Cycle and Access Times**
- **Low Operating Power Dissipation .1mW/Bit Typical**
- **Single +5V Supply**
- **No Clock or Timing Strobe Required**
- **Completely Static Memory**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Common Data Input and Output Using Three-State Outputs**

The Intel® M2142 is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits using N-channel Silicon-Gate MOS technology. It uses fully DC stable (static) circuitry throughout — in both the array and the decoding — and therefore requires no clocks or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

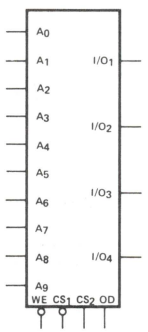
The M2142 is designed for memory applications where high performance, large bit storage, and simple interfacing are important design objectives. It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply.

The M2142 is placed in a 20-pin package. Two Chip Selects ($\overline{CS}_1$ and CS_2) are provided for easy and flexible selection of individual packages when outputs are OR-tied. An Output Disable is included for direct control of the output buffers.

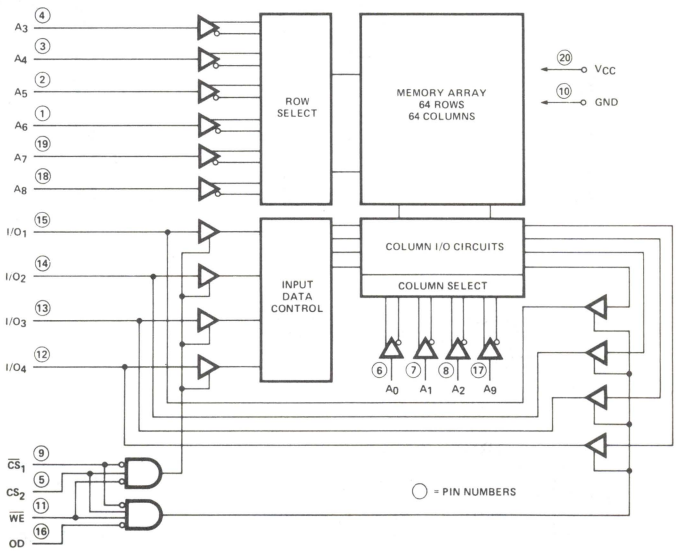
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0–A_9	ADDRESS INPUTS	OD	OUTPUT DISABLE
$\overline{WE}$	WRITE ENABLE	V_{CC}	POWER (+5V)
$\overline{CS}_1$, CS_2	CHIP SELECT	GND	GROUND
I/O_1–I/O_4	DATA INPUT/OUTPUT		

2147
4096 X 1 BIT STATIC RAM

	2147-3	2147	2147L
Max. Access Time (ns)	55	70	70
Max. Active Current (mA)	180	160	140
Max. Standby Current (mA)	30	20	10

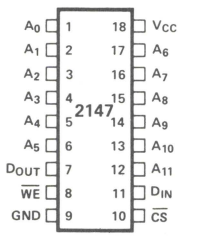
- **HMOS Technology**
- **Completely Static Memory — No Clock or Timing Strobe Required**
- **Equal Access and Cycle Times**
- **Single +5V Supply**
- **Automatic Power-Down**
- **High Density 18-Pin Package**
- **Directly TTL Compatible — All Inputs and Outputs**
- **Separate Data Input and Output**
- **Three-State Output**

The Intel® 2147 is a 4096-bit static Random Access Memory organized as 4096 words by 1-bit using HMOS, a high-performance MOS technology. It uses a uniquely innovative design approach which provides the ease-of-use features associated with non-clocked static memories and the reduced standby power dissipation associated with clocked static memories. To the user this means low standby power dissipation without the need for clocks, address setup and hold times, nor reduced data rates due to cycle times that are longer than access times.

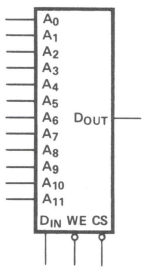
$\overline{CS}$ controls the power-down feature. In less than a cycle time after $\overline{CS}$ goes high — deselecting the 2147 — the part automatically reduces its power requirements and remains in this low power standby mode as long as $\overline{CS}$ remains high. This device feature results in system power savings as great as 85% in larger systems, where the majority of devices are de-selected.

The 2147 is placed in an 18-pin package configured with the industry standard pinout. It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. The data is read out nondestructively and has the same polarity as the input data. A data input and a separate three-state output are used.

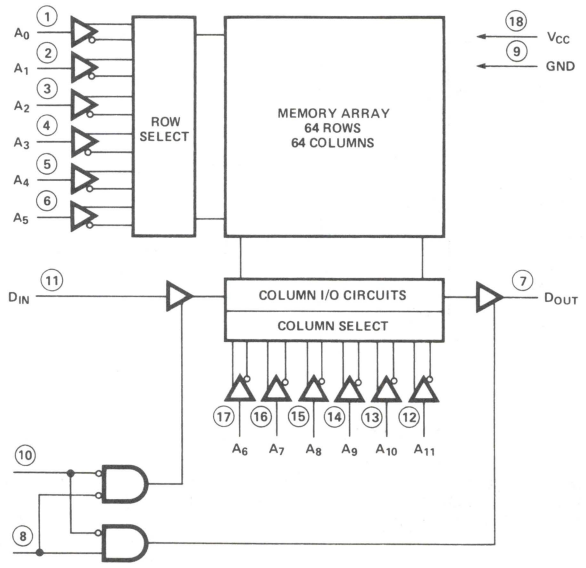
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0–A_{11}	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND	GROUND
$\overline{CS}$	CHIP SELECT		
D_{IN}	DATA INPUT		
D_{OUT}	DATA OUTPUT		

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH Z	STANDBY
L	L	WRITE	HIGH Z	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -10°C to 85°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin With
Respect to Ground ..... -0.5V to +7V
D.C. Output Current ..... 20 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS [1]

T_A = 0°C to 70°C, V_{CC} = +5V ±5%, unless otherwise noted.

Symbol	Parameter	2147-3 Min.	2147-3 Typ. [2]	2147-3 Max.	2147 Min.	2147 Typ. [2]	2147 Max.	2147L Min.	2147L Typ. [2]	2147L Max.	Unit	Test Conditions
I_{LI}	Input Load Current (All Input Pins)		0.01	10		0.01	10		0.01	10	µA	V_{CC}=MAX, V_{IN}=GND to V_{CC}
$\|I_{LO}\|$	Output Leakage Current		0.1	50		0.1	50		0.1	50	µA	$\overline{CS}$=V_{IH}, V_{CC}=Max., V_{OUT}=GND to 4.5V
I_{CC}	Operating Current		120	170		100	150		100	135	mA	T_A=25°C; V_{CC}=Max., $\overline{CS}$=V_{IL}, Outputs Open
				180			160			140	mA	T_A=0°C; V_{CC}=Max., $\overline{CS}$=V_{IL}, Outputs Open
I_{SB}	Standby Current		18	30		12	20		7	10	mA	V_{CC}=Min. to Max. $\overline{CS}$=V_{IH}
I_{PO} [3]	Peak Power-On Current		35	70		25	50		15	30	mA	V_{CC}=GND to V_{CC} Min., $\overline{CS}$=Lower of V_{CC} or V_{IH} Min.
V_{IL}	Input Low Voltage	-0.3		0.8	-0.3		0.8	-0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		6.0	2.0		6.0	2.0		6.0	V	
V_{OL}	Output Low Voltage			0.4			0.4			0.4	V	I_{OL} = 8mA
V_{OH}	Output High Voltage	2.4			2.4			2.4			V	I_{OH} = -4.0mA

Notes:
1. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. Typical limits are at V_{CC} = 5V, T_A = +25°C, and specified loading.
3. I_{CC} exceeds I_{SB} maximum during power on, as shown in Graph 7. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected; otherwise, power-on current approaches I_{CC} active.

A.C. TEST CONDITIONS

Input Pulse Levels	GND to 3.5 Volts
Input Rise and Fall Times	10 nsec
Input and Output Timing Reference Levels	1.5 Volts
Output Load	See Figure 1

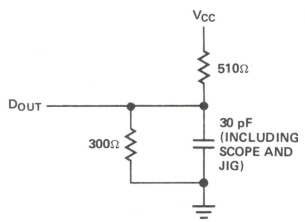


Figure 1. Output Load

CAPACITANCE

T_A = 25°C, f = 1.0MHz [4]

Symbol	Parameter	Max.	Unit	Conditions
C_{IN}	Input Capacitance	5	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	7	pF	V_{OUT} = 0V

Note 4. This parameter is sampled and not 100% tested.

A.C. CHARACTERISTICS

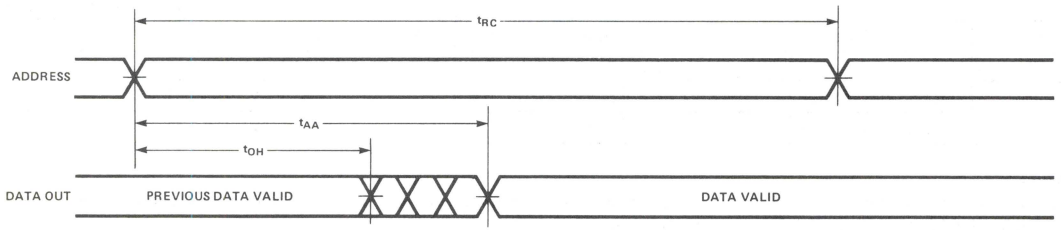
T_A = 0°C to 70°C, V_{CC} = +5V±5%, unless otherwise noted.

READ CYCLE

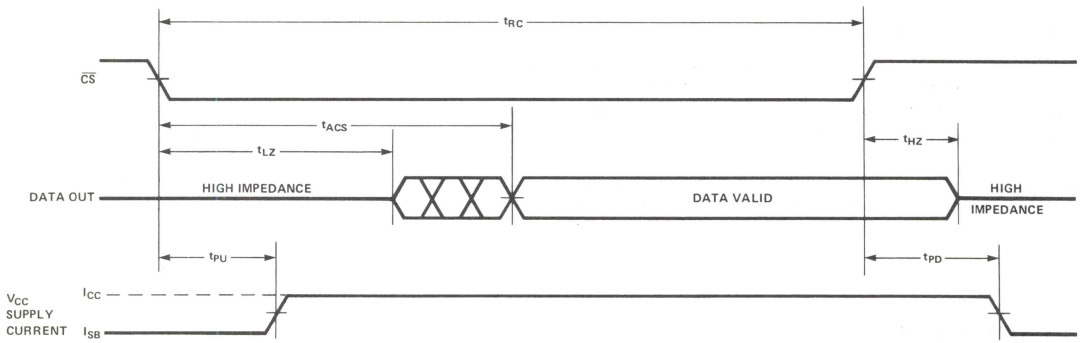
Symbol	Parameter	2147-3 Min.	2147-3 Max.	2147, 2147L Min.	2147, 2147L Max.	Unit	Test Conditions
t_{RC}	Read Cycle Time	55		70		ns	
t_{AA}	Address Access Time		55		70	ns	
t_{ACS1}	Chip Select Access Time		55		70	ns	Note 1
t_{ACS2}	Chip Select Access Time		65		80	ns	Note 2
t_{OH}	Output Hold from Address Change	5		5		ns	
t_{LZ}	Chip Selection to Output in Low Z	10		10		ns	
t_{HZ}	Chip Deselection to Output in High Z	0	40	0	40	ns	
t_{PU}	Chip Selection to Power Up Time	0		0		ns	
t_{PD}	Chip Deselection to Power Down Time		30		30	ns	

WAVEFORMS

READ CYCLE NO. 1 [3,4]



READ CYCLE NO. 2 [3,5]



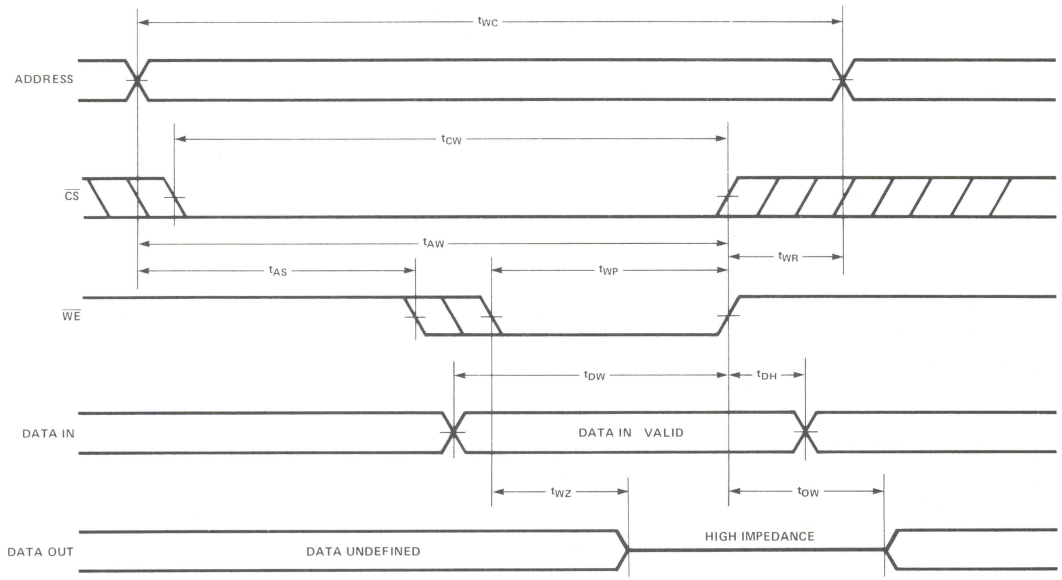
Notes: 1. Chip deselected for greater than 55ns prior to selection.
2. Chip deselected for a finite time that is less than 55ns prior to selection. (If the deselect time is 0ns, the chip is by definition selected and access occurs according to Read Cycle No. 1.)
3. $\overline{WE}$ is high for Read Cycles.
4. Device is continuously selected, $\overline{CS}$ = V_{IL}.
5. Addresses valid prior to or coincident with $\overline{CS}$ transition low.

A.C. CHARACTERISTICS (Continued)

WRITE CYCLE

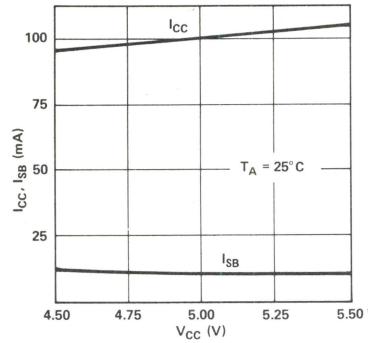
Symbol	Parameter	2147-3 Min.	2147-3 Max.	2147,2147L Min.	2147,2147L Max.	Unit	Test Conditions
t_{WC}	Write Cycle Time	55		70		ns	
t_{CW}	Chip Selection to End of Write	45		55		ns	
t_{AW}	Address Valid to End of Write	45		55		ns	
t_{AS}	Address Setup Time	0		0		ns	
t_{WP}	Write Pulse Width	35		40		ns	
t_{WR}	Write Recovery Time	10		15		ns	
t_{DW}	Data Valid to End of Write	25		30		ns	
t_{DH}	Data Hold Time	10		10		ns	
t_{WZ}	Write Enabled to Output in High Z	0	30	0	35	ns	
t_{OW}	Output Active from End of Write	0		0		ns	

WRITE CYCLE

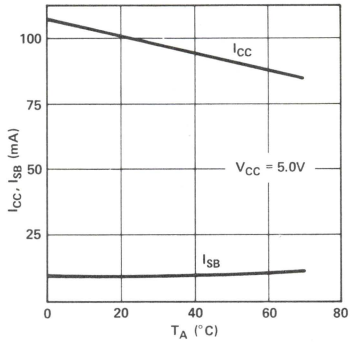


TYPICAL D.C. AND A.C. CHARACTERISTICS

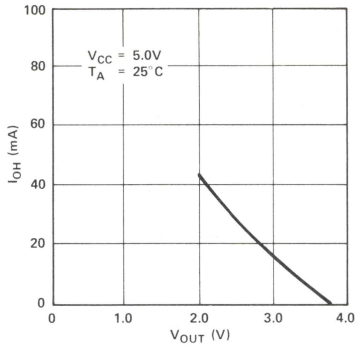
GRAPH 1
SUPPLY CURRENT[1] VS.
SUPPLY VOLTAGE



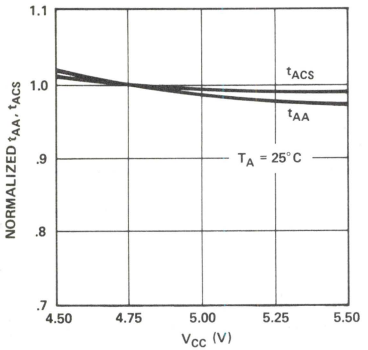
GRAPH 2
SUPPLY CURRENT[1] VS.
AMBIENT TEMPERATURE



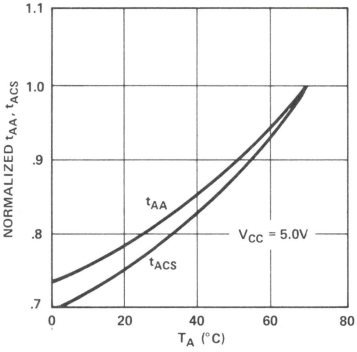
GRAPH 3
OUTPUT SOURCE CURRENT VS.
OUTPUT VOLTAGE



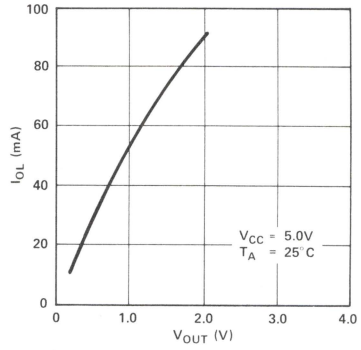
GRAPH 4
NORMALIZED ACCESS TIME
VS. SUPPLY VOLTAGE



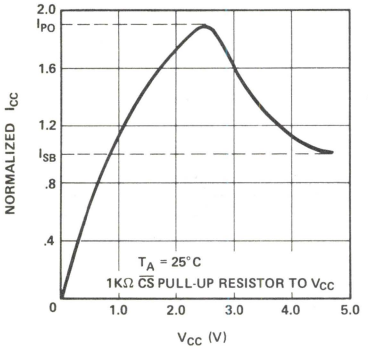
GRAPH 5
NORMALIZED ACCESS TIME VS.
AMBIENT TEMPERATURE



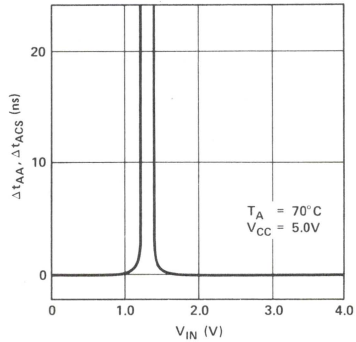
GRAPH 6
OUTPUT SINK CURRENT VS.
OUTPUT VOLTAGE



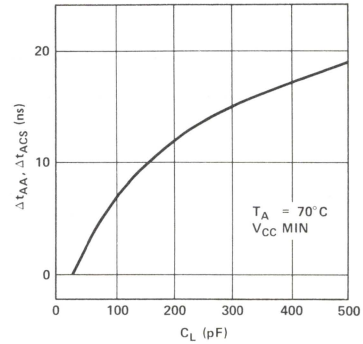
GRAPH 7
TYPICAL POWER-ON CURRENT
VS. POWER SUPPLY VOLTAGE



GRAPH 8
ACCESS TIME CHANGE VS.
INPUT VOLTAGE



GRAPH 9
ACCESS TIME CHANGE VS.
OUTPUT LOADING



Note 1. The supply current curves shown in Graphs 1 and 2 are for the 2147.
The supply current curves for the 2147L and 2147-3 can be calculated by scaling proportionately.

DEVICE DESCRIPTION

The 2147 is produced with HMOS, a new high-performance MOS technology which incorporates on-chip substrate bias generation combined with device scaling to achieve high-performance. The speed-power product of this process has been measured at 1pj, approximately four times better than previous MOS processes.

This process, combined with new design ideas, gives the 2147 its unique features. High speed, low power and ease-of-use have been obtained in a single part. The low-power feature is controlled with the Chip Select input, which is not a clock and does not have to be cycled. Multiple read or write operations are possible during a single select period. Access times are equal to cycle times, resulting in data rates of 14.3 MHz and 18 MHz for the 2147 and 2147-3, respectively. This is considerably higher performance than for clocked static designs.

Whenever the 2147 is deselected, it automatically reduces its power requirements to a fraction of the active power, as shown in Figure 1. This is achieved by switching off the power to unnecessary portions of the internal peripheral circuitry. This feature adds up to significant system power savings. The average power per device declines as system size grows because a continually higher portion of the memory is deselected. Device power dissipation asymptotically approaches the standby power level, as shown in Figure 2.

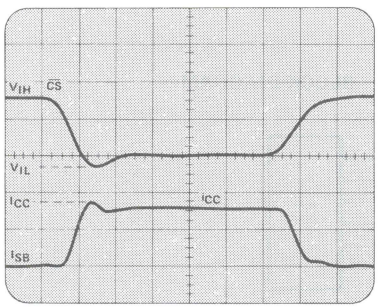


FIGURE 1. i_{CC} WAVEFORM.

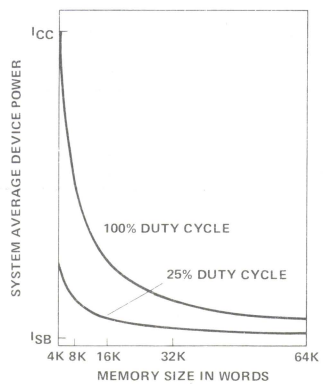


FIGURE 2. AVERAGE DEVICE DISSIPATION VS. MEMORY SIZE.

There is no functional constraint on the amount of time the 2147 is deselected. However, there is a relationship between deselect time and Chip Select access time. With no compensation, the automatic power switch would cause an increase in Chip Select access time, since some time is lost in repowering the device upon selection. A feature of the 2147 design is its ability to compensate for this loss. The amount of compensation is a function of deselect time, as shown in Figure 3. For short deselect times, Chip Select access time becomes slower than address access time, since full compensation typically requires 40ns. For longer deselect times, Chip Select access time actually becomes faster than address access time because the compensation more than offsets the time lost in powering up. The spec accounts for this characteristic by specifying two Chip Select access times, t_{ACS1} and t_{ACS2}.

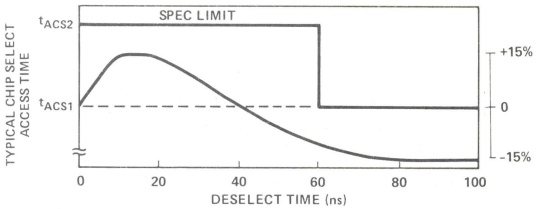


FIGURE 3. t_{ACS} VS. DESELECT TIME.

The power switching characteristic of the 2147 requires more careful decoupling than would be required of a constant power device. It is recommended that a 0.1μF to 0.3μF ceramic capacitor be used on every other device, with a 22μF to 47μF bulk electrolytic decoupler every 16 devices. The actual values to be used will depend on board layout, trace widths and duty cycle. Power supply gridding is recommended for PC board layout. A very satisfactory grid can be developed on a two-layer board with vertical traces on one side and horizontal traces on the other, as shown in Figure 4.

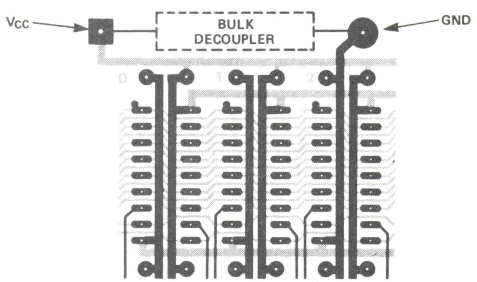


FIGURE 4. PC LAYOUT.

Terminations are recommended on input signal lines to the 2147 devices. In high speed systems, fast drivers can cause significant reflections when driving the high impedance inputs of the 2147. Terminations may be required to match the impedance of the line to the driver. The type of termination used depends on designer preference and may be parallel resistive or resistive-capacitive. The latter reduces terminator power dissipation.

ADVANCE INFORMATION
Characteristics are subject to change without notice

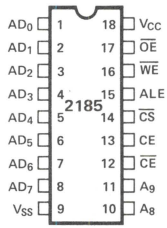
2185
1024 X 8 BIT STATIC RAM

- **Low Operating Power Dissipation**
- **Low Standby Power Dissipation**
- **Single 5V Power Supply**
- **High Density 18 Pin Package**
- **Fully Static Operation**
- **Fully Multiplexed Address and Data Lines**
- **Directly Compatible with the MCS-85 and MCS-48 Microprocessor**
- **No Clock or Timing Strobe Required**

The Intel®2185 is an 8192-bit static Random Access Memory organized as 1024 words by 8-bit using N-channel Silicon-Gate MOS technology. It uses a uniquely innovative design approach which provides the ease of use features associated with non clocked static memories and the reduced standby power dissipation associated with clocked static memories. To the user this means low standby power dissipation without the need for clocks, address setup and hold times.

The 2185 is housed in an 18 pin package featuring a fully multiplexed address and data bus. It is directly compatible with TTL in all respects: inputs, outputs and a single 5V supply.

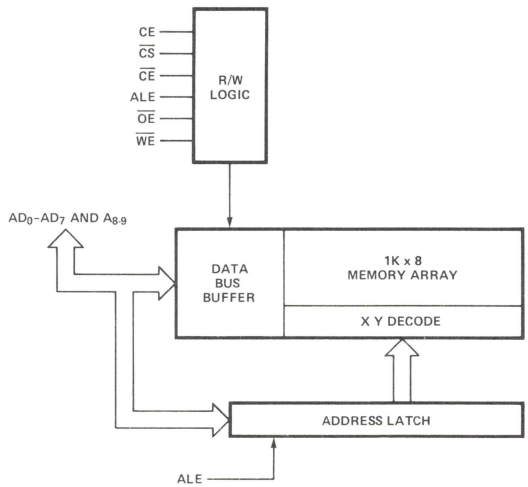
PIN CONFIGURATION



PIN NAMES

A_{8-9}	ADDRESS LINE
AD_0-AD_7	ADDRESS AND DATA LINES
$\overline{CS}$	CHIP SELECT
CE, $\overline{CE}$	CHIP ENABLE
ALE	ADDRESS LATCH ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE

BLOCK DIAGRAM



3101, 3101A
16 x 4 BIT HIGH SPEED RAM

- **Fast Access Time -- 35 nsec. max. over 0-75° C Temperature Range.** (3101A)
- **Simple Memory Expansion through Chip Select Input -- 17 nsec. max. over 0-75° C Temperature Range.** (3101A)
- **DTL and TTL Compatible -- Low Input Load Current: 0.25mA. max.**
- **OR-Tie Capability -- Open Collector Outputs.**
- **Fully Decoded -- on Chip Address Decode and Buffer.**
- **Minimum Line Reflection -- Low Voltage Diode Input Clamp.**
- **Ceramic and Plastic Package -- 16 Pin Dual In-Line Configuration.**

The Intel® 3101 and 3101A are high speed fully decoded 64 bit random access memories, organized 16 words by 4 bits. Their high speed makes them ideal in scratch pad applications. An unselected chip will not generate noise at its output during writing of a selected chip. The output is held high on an unselected chip regardless of the state of the read/write signal.

The use of Schottky barrier diode clamped transistors to obtain fast switching speeds results in higher performance than equivalent devices with gold diffusion processes.

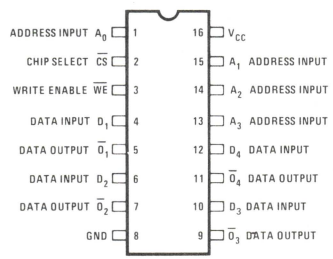
The Intel 3101 and 3101A are packaged in either hermetically sealed 16 pin ceramic packages, or in low cost silicone packages, and their performance is specified over a temperature range from 0° C to 75° C.

The storage cells are addressed through an on chip 1 of 16 binary decoder using four input address leads.

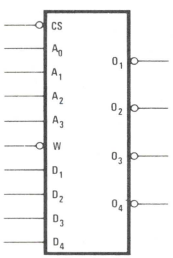
A separate Chip Select lead allows easy selection of an individual package when outputs are OR-tied.

In addition to the address leads and the Chip Select lead, there is a write input which allows data presented at the data leads to be entered at the addressed storage cells.

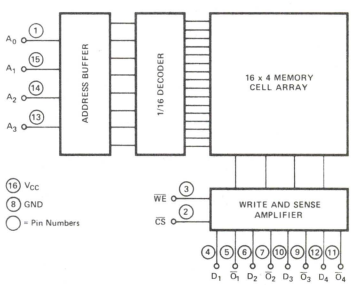
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

D_1–D_4	DATA INPUTS	$\overline{CS}$	CHIP SELECT INPUT
A_0–A_3	ADDRESS INPUTS	$\overline{O}_1$–$\overline{O}_4$	DATA OUTPUTS
$\overline{WE}$	WRITE ENABLE	V_{CC}	POWER (+5V)

TRUTH TABLE

CHIP SELECT	WRITE ENABLE	OPERATION	OUTPUT
LOW	LOW	WRITE	HIGH
LOW	HIGH	READ	COMPLEMENT OF WRITTEN DATA
HIGH	LOW	–	HIGH
HIGH	HIGH	–	HIGH

Absolute Maximum Ratings*

Temperature Under Bias:	Ceramic	−65°C to +125°C
	Plastic	−65°C to +75°C
Storage Temperature		−65°C to +160°C
All Output or Supply Voltages		−0.5 to +7 Volts
All Input Voltages		−1.0 to +5.5 Volts
Output Currents		100 mA

*COMMENT:

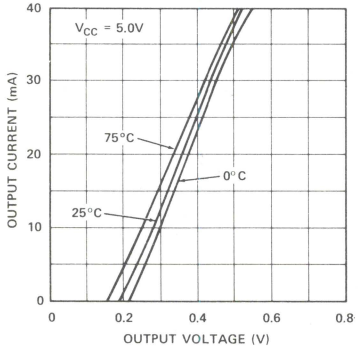
Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%

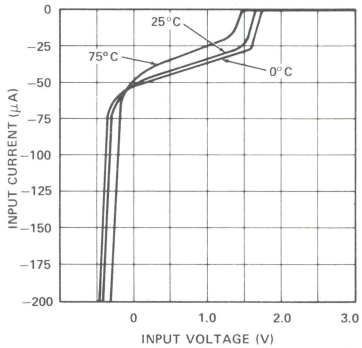
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
I_{FA}	ADDRESS INPUT LOAD CURRENT		−0.25	mA	V_{CC} =5.25V, V_A =0.45V
I_{FD}	DATA INPUT LOAD CURRENT		−0.25	mA	V_{CC} =5.25V, V_D =0.45V
I_{FW}	WRITE INPUT LOAD CURRENT		−0.25	mA	V_{CC} =5.25V, V_W =0.45V
I_{FS}	CHIP SELECT INPUT LOAD CURRENT		−0.25	mA	V_{CC} =5.25V, V_S =0.45V
I_{RA}	ADDRESS INPUT LEAKAGE CURRENT		10	μA	V_{CC} =5.25V, V_A =5.25V
I_{RD}	DATA INPUT LEAKAGE CURRENT		10	μA	V_{CC} =5.25V, V_D =5.25V
I_{RW}	WRITE INPUT LEAKAGE CURRENT		10	μA	V_{CC} =5.25V, V_W =5.25V
I_{RS}	CHIP SELECT INPUT LEAKAGE CURRENT		10	μA	V_{CC} =5.25V, V_S =5.25V
V_{CA}	ADDRESS INPUT CLAMP VOLTAGE		−1.0	V	V_{CC} =4.75V, I_A =−5.0 mA
V_{CD}	DATA INPUT CLAMP VOLTAGE		−1.0	V	V_{CC} =4.75V, I_D =−5.0 mA
V_{CW}	WRITE INPUT CLAMP VOLTAGE		−1.0	V	V_{CC} =4.75V, I_W =−5.0 mA
V_{CS}	CHIP SELECT INPUT CLAMP VOLTAGE		−1.0	V	V_{CC} =4.75V, I_S =−5.0 mA
V_{OL}	OUTPUT "LOW" VOLTAGE		0.45	V	V_{CC} =4.75V, I_{OL} = 15 mA Memory Stores "Low"
I_{CEX}	OUTPUT LEAKAGE CURRENT		100	μA	V_{CC} =5.25V, V_{CEX} =5.25V V_S =2.5V
I_{CC}	POWER SUPPLY CURRENT		105	mA	V_{CC} =5.25V, V_A =V_S =V_D =0V
V_{IL}	INPUT "LOW" VOLTAGE		0.85	V	V_{CC} =5.0V
V_{IH}	INPUT "HIGH" VOLTAGE	2.0		V	V_{CC} =5.0V

Typical Characteristics

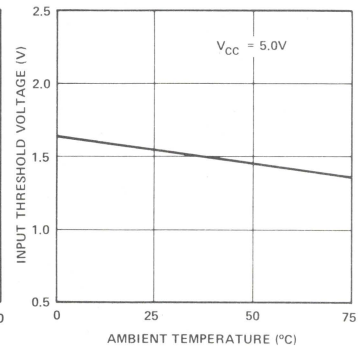
OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE



INPUT CURRENT VS. INPUT VOLTAGE



INPUT THRESHOLD VOLTAGE VS. AMBIENT TEMPERATURE



Switching Characteristics

Conditions of Test:

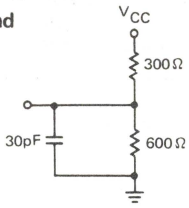
Input Pulse amplitudes: 2.5V

Input Pulse rise and fall times of 5 nanoseconds between 1 volt and 2 volts

Speed measurements are made at 1.5 volt levels

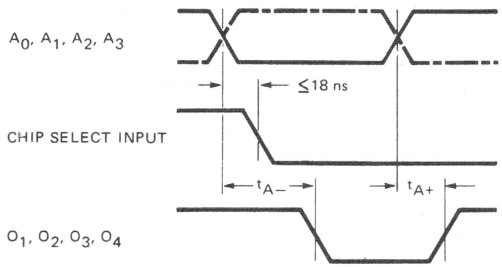
Output loading is 15mA and 30 pF

15 mA Test Load

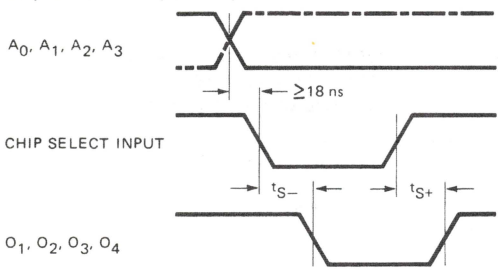


READ CYCLE

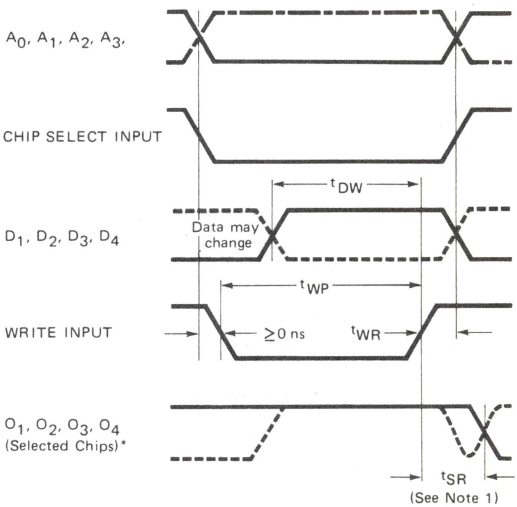
Address to Output Delay



Chip Select to Output Delay



WRITE CYCLE



*Outputs of unselected chips remain high during write cycle.

NOTE 1: t_{SR} is associated with a read cycle following a write cycle and does not affect the access time.

A.C. Characteristics T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%

READ CYCLE					
SYMBOL	PARAMETER	3101A LIMITS (ns)		3101 LIMITS (ns)	
		MIN.	MAX.	MIN.	MAX.
t_{S+}, t_{S-}	Chip Select to Output Delay	5	17	5	42
t_{A-}, t_{A+}	Address to Output Delay	10	35	10	60

WRITE CYCLE					
SYMBOL	TEST	3101A LIMITS (ns)		3101 LIMITS (ns)	
		MIN.	MAX.	MIN.	MAX.
t_{SR}	Sense Amplifier Recovery Time		35		50
t_{WP}	Write Pulse Width	25		40	
t_{DW}	Data-Write Overlap Time	25		40	
t_{WR}	Write Recovery Time	0		5	

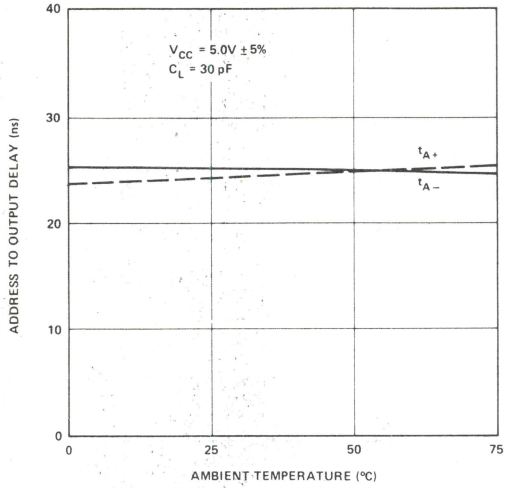
CAPACITANCE[2] T_A = 25° C

C_{IN}	INPUT CAPACITANCE (All Pins)	10 pF maximum
C_{OUT}	OUTPUT CAPACITANCE	12 pF maximum

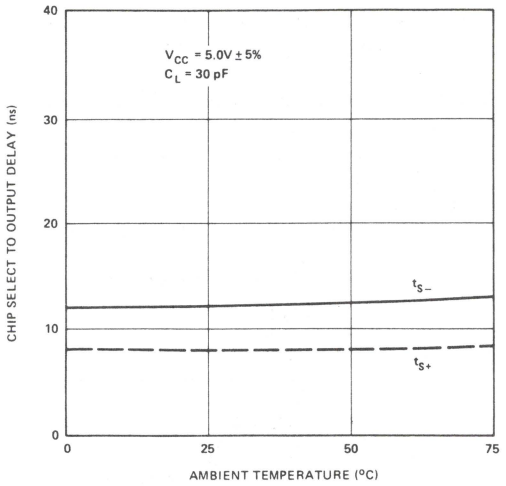
NOTE 2: This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, V_{bias} = 2V, V_{CC} = 0V, and T_A = 25°C.

Typical A.C. Characteristics

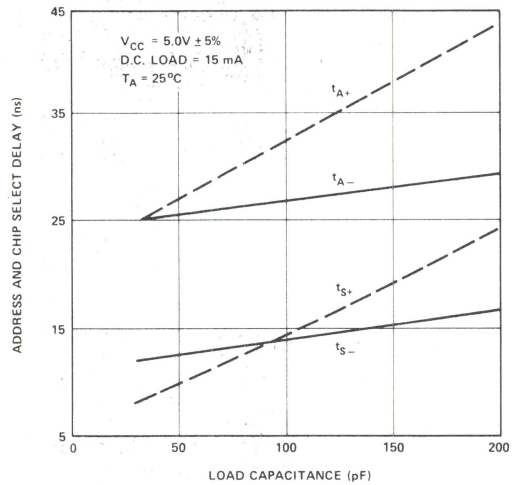
ADDRESS TO OUTPUT DELAY
VS.
AMBIENT TEMPERATURE



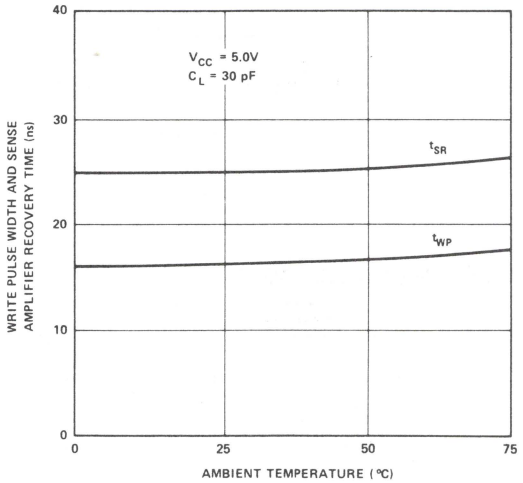
CHIP SELECT TO OUTPUT DELAY
VS.
AMBIENT TEMPERATURE



ADDRESS & CHIP SELECT TO OUTPUT DELAY
VS.
LOAD CAPACITANCE



WRITE PULSE WIDTH & SENSE
AMPLIFIER RECOVERY TIME
VS. AMBIENT TEMPERATURE

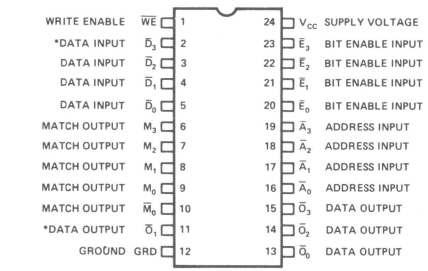


3104
16 BIT CONTENT ADDRESSABLE MEMORY

- **Organization – 4 Words x 4 Bits**
- **Max. Delay of 30 nsec Over 0° C to 75° C Temperature**
- **Open Collector Outputs – OR Tie Capability**
- **High Current Sinking Capability – 15 mA max.**
- **Low Input Load Current – 0.25 mA max.**
- **DTL & TTL Compatible**
- **Bit Enable Input – Bit Masking**
- **Standard 24 Pin Dual In-Line**

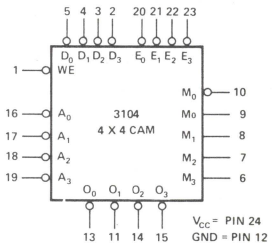
The Intel 3104 is a high speed 16 bit Content Addressable Memory (CAM). It is a linear select 4 word by 4 bit array which is designed to compare data on its inputs with data already stored in its memory and to indicate a match when these data are identical. This equality search is performed on all bits in parallel. The 3104 can also be used as a read/write RAM with linear selection addressing.

PIN CONFIGURATION

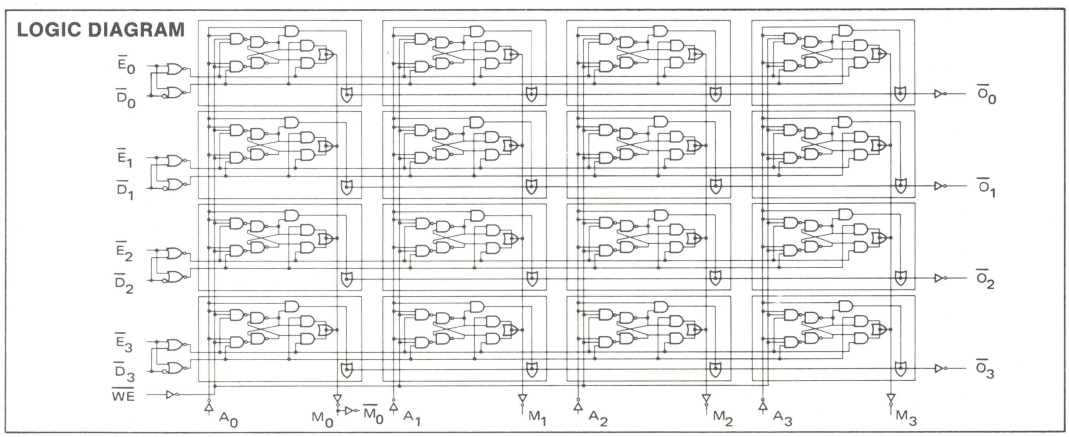


*DATA IN and DATA OUT are of the same logic levels. For a chip that is not selected, the data output is at a high level.

LOGIC SYMBOL



LOGIC DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias	−65°C to +125°C
Storage Temperature	−65°C to +160°C
All Output or Supply Voltages	−0.5 to +7 Volts
All Input Voltages	−1.0 to +5.5 Volts
Output Currents	100 mA

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

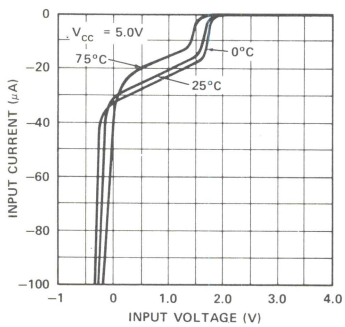
D.C. Characteristics $T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0V \pm 5\%$; unless otherwise specified.

SYMBOL	PARAMETER	LIMIT MIN.	LIMIT TYP.	LIMIT MAX.	UNIT	TEST CONDITIONS
I_{FA}	ADDRESS INPUT LOAD CURRENT			−0.25	mA	$V_{CC} = 5.25V$ $V_A = .45V$
I_{FE}	BIT ENABLE INPUT LOAD CURRENT			−0.25	mA	$V_{CC} = 5.25V$ $V_E = .45V$
I_{FW}	WRITE ENABLE INPUT LOAD CURRENT			−0.25	mA	$V_{CC} = 5.25V$ $V_W = .45V$
I_{FD}	DATA INPUT LOAD CURRENT			−0.25	mA	$V_{CC} = 5.25V$ $V_D = .45V$
I_{RA}	ADDRESS INPUT LEAKAGE CURRENT			10	μA	$V_{CC} = 5.25V$ $V_A = 5.25V$
I_{RE}	BIT ENABLE INPUT LEAKAGE CURRENT			10	μA	$V_{CC} = 5.25V$ $V_E = 5.25V$
I_{RW}	WRITE ENABLE INPUT LEAKAGE CURRENT			10	μA	$V_{CC} = 5.25V$ $V_W = 5.25V$
I_{RD}	DATA INPUT LEAKAGE CURRENT			10	μA	$V_{CC} = 5.25V$ $V_D = 5.25V$
I_{CEX}	OUTPUT LEAKAGE CURRENT (ALL OUTPUTS)			50	μA	$V_{CC} = 5.25V$ $V_{CEX} = 5.25V$
V_{OL}	OUTPUT "LOW" VOLTAGE (ALL OUTPUTS)			0.45	V	$V_{CC} = 4.75V$ $I_{OL} = 15mA$
V_{IL}	INPUT "LOW" VOLTAGE (ALL INPUTS)			0.85	V	$V_{CC} = 5V$
V_{IH}	INPUT "HIGH" VOLTAGE (ALL INPUTS)	2.0			V	$V_{CC} = 5V$
I_{CC}	POWER SUPPLY CURRENT			125	mA	$V_{CC} = 5.25V$ OUTPUTS HIGH
C_{IN}**	INPUT CAPACITANCE		5		pF	$V_{IN} = +2.0V$, $V_{CC} = 0.0V$ f = 1 MHz
C_{OUT}**	OUTPUT CAPACITANCE		8		pF	$V_{OUT} = +2.0V$, $V_{CC} = 0.0V$ f = 1 MHz

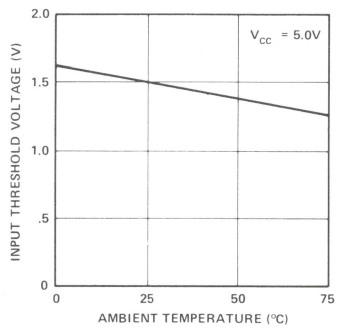
**This parameter is periodically sampled and is not 100% tested.

Typical D.C. Characteristics

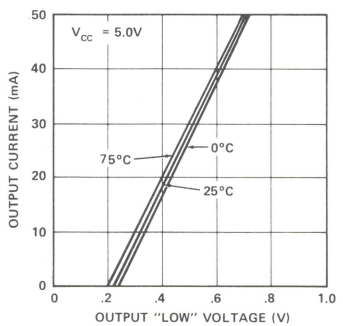
INPUT CURRENT VS. INPUT VOLTAGE



INPUT THRESHOLD VOLTAGE VS. TEMPERATURE



OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE



Switching Characteristics

Conditions of Test:

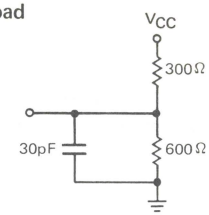
Input Pulse amplitudes · · 2.5V

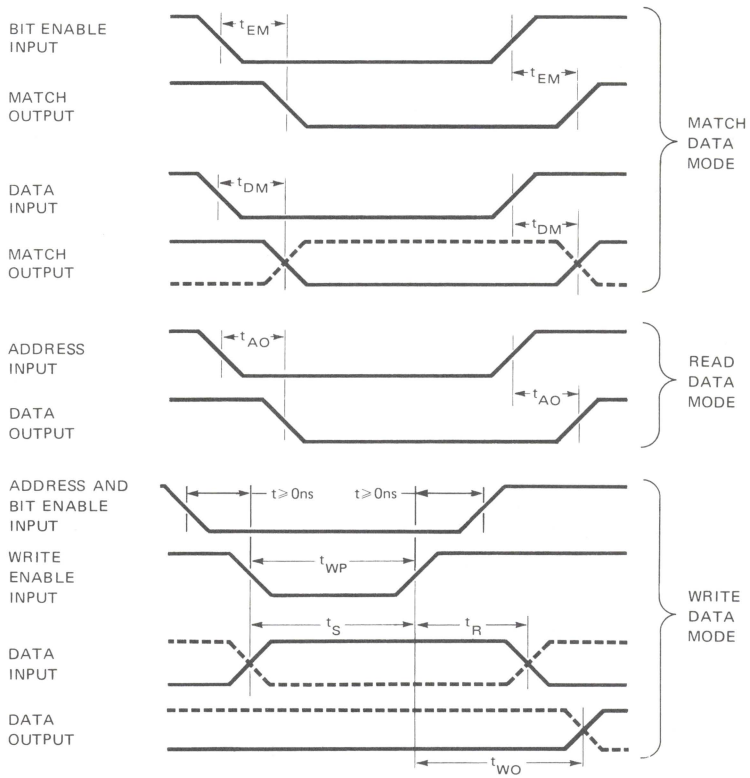
Input pulse rise and fall times of 5 nanoseconds between 1 volt and 2 volts

Speed measurements are made at 1.5 volt levels

Output loading is 15 mA and 30 pF

15mA Test Load





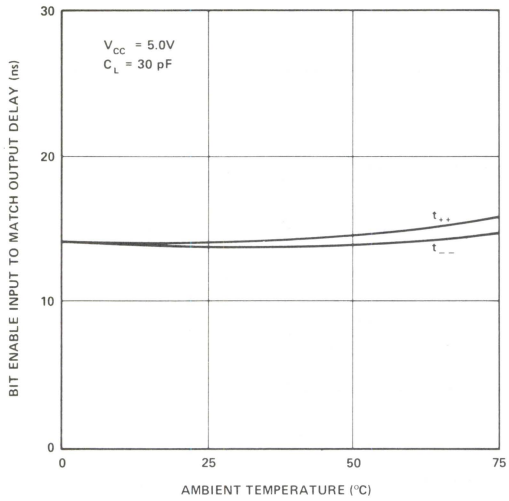
A.C. Characteristics T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%; unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.(1)	MAX.	
t_{EM}	BIT ENABLE INPUT TO MATCH OUTPUT DELAY		15	30	ns
t_{DM}	DATA INPUT TO MATCH OUTPUT DELAY		16	30	ns
t_{AO}	ADDRESS INPUT TO OUTPUT DELAY		14	30	ns
t_{WP}	WRITE ENABLE PULSE WIDTH	40	25		ns
t_{WO}	WRITE ENABLE TO OUTPUT DELAY		–	40	ns
t_S	SET-UP TIME ON DATA INPUT		–	40	ns
t_R	RELEASE TIME ON DATA INPUT	0	–		ns

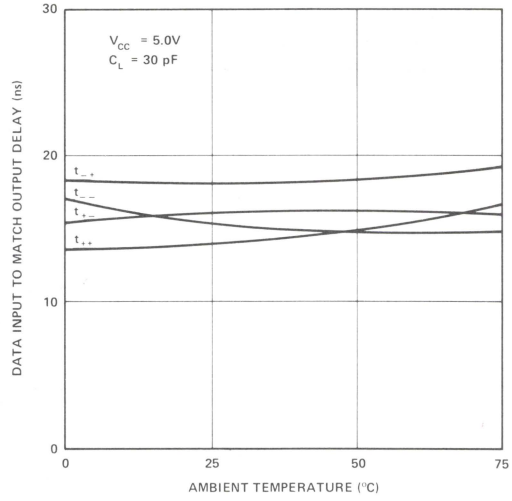
Note 1. Typical values are at nominal voltages and T_A = 25°C.

Typical A.C. Characteristics

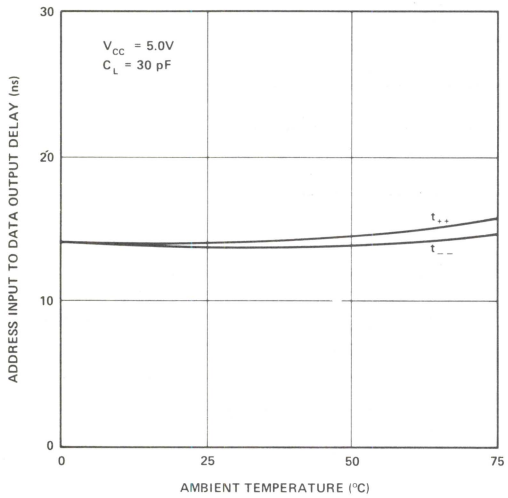
BIT ENABLE INPUT TO MATCH OUTPUT DELAY VS. TEMPERATURE



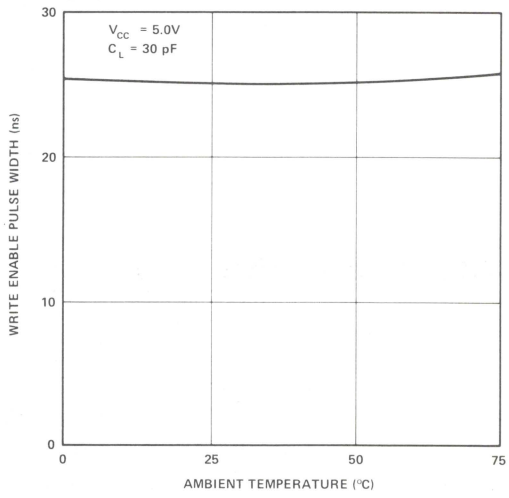
DATA INPUT TO MATCH OUTPUT DELAY VS. TEMPERATURE



ADDRESS INPUT TO DATA OUTPUT DELAY VS. TEMPERATURE



WRITE ENABLE PULSE WIDTH VS. TEMPERATURE



5101 FAMILY
256 x 4 BIT STATIC CMOS RAM

P/N	Typ. Current @ 2V (μA)	Typ. Current @ 5V (μA)	Max Access (ns)
5101L	0.14	0.2	650
5101L-1	0.14	0.2	450
5101L-3	0.70	1.0	650

- **Single +5V Power Supply**
- **Ideal for Battery Operation (5101L)**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Three-State Output**

The Intel® 5101 is an ultra-low power 1024-bit (256 words X 4 bits) static RAM fabricated with an advanced ion-implanted silicon gate CMOS technology. The device has two chip enable inputs. Minimum standby current is drawn by this device when CE2 is at a low level. When deselected the 5101 draws from the single 5-volt supply only 10 microamps. This device is ideally suited for low power applications where battery operation or battery backup for non-volatility are required.

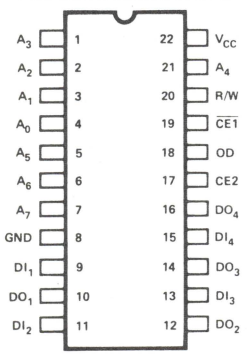
The 5101 uses fully DC stable (static) circuitry; it is not necessary to pulse chip select for each address transition. The data is read out non-destructively and has the same polarity as the input data. All inputs and outputs are directly TTL compatible. The 5101 has separate data input and data output terminals. An output disable function is provided so that the data inputs and outputs may be wire OR-ed for use in common data I/O systems.

The 5101L has the additional feature of guaranteed data retention at a power supply voltage as low as 2.0 volts.

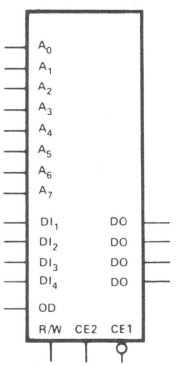
A pin compatible N-channel static RAM, the Intel® 2101A, is also available for low cost applications where a 256 X 4 organization is needed.

The Intel ion-implanted, silicon gate, Complementary MOS (CMOS) process allows the design and production of ultra-low power, high performance memories.

PIN CONFIGURATION



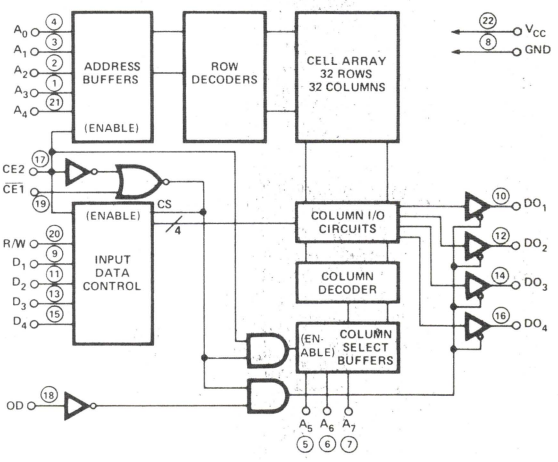
LOGIC SYMBOL



TRUTH TABLE

$\overline{CE_1}$	CE_2	OD	R/W	D_{IN}	Output	Mode
H	X	X	X	X	High Z	Not Selected
X	L	X	X	X	High Z	Not Selected
X	X	H	H	X	High Z	Output Disabled
L	H	H	L	X	High Z	Write
L	H	L	L	X	D_{IN}	Write
L	H	L	H	X	D_{OUT}	Read

BLOCK DIAGRAM



Absolute Maximum Ratings *

Ambient Temperature Under Bias . . . . .–10°C to 80°C
Storage Temperature . . . . . -65°C to +150°C
Voltage On Any Pin
With Respect to Ground . . . . -0.3V to V_{CC} +0.3V
Maximum Power Supply Voltage . . . . . +7.0V
Power Dissipation . . . . . 1 Watt

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	5101L and 5101L-1 Limits Min.	Typ.[1]	Max.	5101L-3 Limits Min.	Typ.[1]	Max.	Units	Test Conditions
I_{L2}[2]	Input Current		5			5		nA	
$\|I_{LO}\|$[2]	Output Leakage Current			1			1	µA	$\overline{CE1}$=2.2V, V_{OUT}= 0 to V_{CC}
I_{CC1}	Operating Current		9	22		9	22	mA	V_{IN}=V_{CC}, Except $\overline{CE1} \leqslant$ 0.65V, Outputs Open
I_{CC2}	Operating Current		13	27		13	27	mA	V_{IN}=2.2V, Except $\overline{CE1} \leqslant$ 0.65V, Outputs Open
I_{CCL}[2]	Standby Current			10			200	µA	CE2 $\leqslant$ 0.2V, T_A= 70° C
V_{IL}	Input Low Voltage	-0.3		0.65	-0.3		0.65	V	
V_{IH}	Input High Voltage	2.2		V_{CC}	2.2		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4			0.4	V	I_{OL}=2.0 mA
V_{OH}	Output High Voltage	2.4			2.4			V	I_{OH}= -1.0 mA

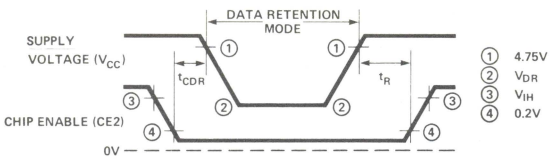
Low V_{CC} Data Retention Characteristics (For 5101L, 5101L-1 and 5101L-3) T_A = 0° C to 70° C

Symbol	Parameter	Min.	Typ.[1]	Max.	Units	Test Conditions	
V_{DR}	V_{CC} for Data Retention	2.0			V		
I_{CCDR1}	5101L or 5101L-1 Data Retention Current		0.14	10	µA	CE2 $\leqslant$ 0.2V	V_{DR}=2.0V, T_A=70° C
I_{CCDR2}	5101L-3 Data Retention Current		0.70	200	µA		V_{DR}=2.0V, T_A=70° C
t_{CDR}	Chip Deselect to Data Retention Time	0			ns		
t_R	Operation Recovery Time	t_{RC}[3]			ns		

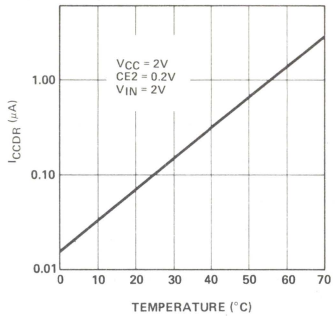
NOTES:

1. Typical values are T_A = 25°C and nominal supply voltage.
2. Current through all inputs and outputs included in I_{CCL} measurement.
3. t_{RC} = Read Cycle Time.

Low V_{CC} Data Retention Waveform



Typical I_{CCDR} Vs. Temperature



RAM

A.C. Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

READ CYCLE

Symbol	Parameter	5101L-1 Limits (ns) Min.	5101L-1 Limits (ns) Max.	5101L and 5101L-3 Limits (ns) Min.	5101L and 5101L-3 Limits (ns) Max.
t_{RC}	Read Cycle	450		650	
t_A	Access Time		450		650
t_{CO1}	Chip Enable ($\overline{CE\ 1}$) to Output		400		600
t_{CO2}	Chip Enable (CE 2) to Output		500		700
t_{OD}	Output Disable to Output		250		350
t_{DF}	Data Output to High Z State	0	130	0	150
t_{OH1}	Previous Read Data Valid with Respect to Address Change	0		0	
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0		0	

WRITE CYCLE

t_{WC}	Write Cycle	450		650	
t_{AW}	Write Delay	130		150	
t_{CW1}	Chip Enable ($\overline{CE\ 1}$) to Write	350		550	
t_{CW2}	Chip Enable (CE 2) to Write	350		550	
t_{DW}	Data Setup	250		400	
t_{DH}	Data Hold	50		100	
t_{WP}	Write Pulse	250		400	
t_{WR}	Write Recovery	50		50	
t_{DS}	Output Disable Setup	130		150	

A. C. CONDITIONS OF TEST

Input Pulse Levels: +0.65 Volt to 2.2 Volt

Input Pulse Rise and Fall Times: 20nsec

Timing Measurement Reference Level: 1.5 Volt

Output Load: 1 TTL Gate and C_L = 100pF

Capacitance[2]

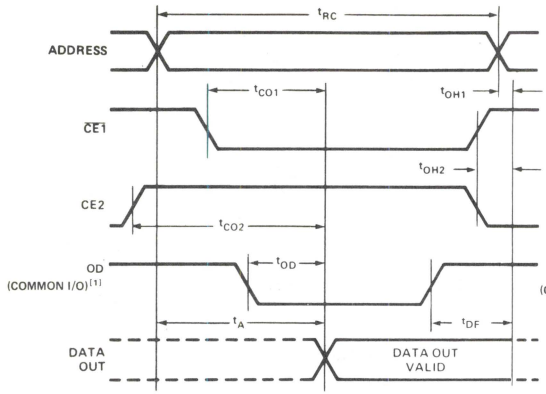
T_A = 25°C, f = 1MHz

Symbol	Test	Limits (pF) Typ.	Limits (pF) Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
C_{OUT}	Output Capacitance V_{OUT} = 0V	8	12

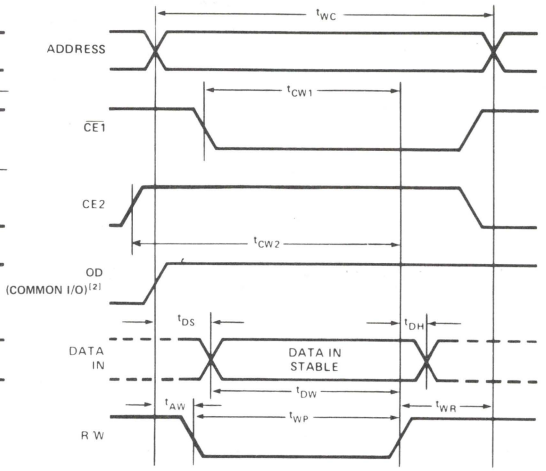
NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.

Waveforms

READ CYCLE



WRITE CYCLE



NOTES:

1. OD may be tied low for separate I/O operation.
2. During the write cycle, OD is "high" for common I/O and "don't care" for separate I/O operation.

MILITARY TEMP.

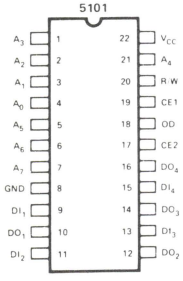
M5101-4, M5101L-4
256 x 4 BIT STATIC CMOS RAM

- **Military Temperature Range: −55°C to +125°C**
- **Ultra Low Standby Current: 200 nA/Bit**
- **Fast Access Time—800ns**
- **Single +5V Power Supply**
- **CE2 Controls Unconditional Standby Mode**
- **Three-State Output**

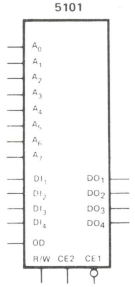
The Intel® M5101 is an ultra-low power 256 X 4 CMOS RAM specified over the −55°C to +125°C temperature range. The RAM uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. When deselected with CE2 low, the M5101 draws from the single 5-volt supply only 200 microamps at 125°C.

The Intel® M5101 is fabricated with an ion-implanted, silicon gate, Complementary MOS (CMOS) process. This technology allows the design and production of ultra-low power, high performance memories.

PIN CONFIGURATION
5101



LOGIC SYMBOL
5101



PIN NAMES

DI_1, DI_4	DATA INPUT	OD	OUTPUT DISABLE
A_0 – A_7	ADDRESS INPUTS	DO_1 – DO_4	DATA OUTPUT
R/W	READ/WRITE INPUT	V_{CC}	POWER (+5V)
$\overline{CE1}$, CE2	CHIP ENABLE		

Absolute Maximum Ratings *

Ambient Temperature Under Bias . . . −65°C to 135°C
Storage Temperature . . . . . −65°C to +150°C
Voltage On Any Pin
With Respect to Ground . . . . −0.3V to V_{CC} +0.3V
Maximum Power Supply Voltage . . . . . +7.0V
Power Dissipation . . . . . 1 Watt

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics for M5101-4, M5101L-4

T_A = −55°C to 125°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}[2]	Input Current		8		nA	V_{IN} = 0 to 5.25V
I_{LOH}[2]	Output High Leakage			2	μA	$\overline{CE1}$=2.2V, V_{OUT} = V_{CC}
I_{LOL}[2]	Output Low Leakage			2	μA	$\overline{CE1}$=2.2V, V_{OUT}=0.0V
I_{CC1}	Operating Current		11	25	mA	V_{IN} = V_{CC} Except $\overline{CE1}$ ⩽0.01V Outputs Open
I_{CC2}	Operating Current		20	32	mA	V_{IN} = 2.2V Except $\overline{CE1}$ ⩽0.5V Outputs Open
I_{CCL}[2]	Standby Current		2	200	μA	V_{IN} = 0 to V_{CC}, Except CE2 ⩽ 0.2V
V_{IL}	Input "Low" Voltage	-0.3		0.5	V	
V_{IH}	Input "High" Voltage	V_{CC}-2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage			0.4	V	I_{OL} = 2.0mA
V_{OH}	Output "High" Voltage	V_{CC}-2.0			V	I_{OH} = 1.0mA

NOTES: 1. Typical values are T_A = 25°C and nominal supply voltage. 2. Current through all inputs and outputs included in I_{CCL}.

MILITARY TEMP

Low V_{CC} Data Retention Characteristics (For M5101L-4) T_A = -55°C to 125°C

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions	
V_{DR}	V_{CC} for Data Retention	2.0			V	$CE2 \leqslant 0.2V$	
I_{CCDR}	Data Retention Current		2	200	µA		V_{DR} = 2.0V
t_{CDR}	Chip Deselect to Data Retention Time	0			ns		
t_R	Operation Recovery Time	t_{RC}[2]			ns		

NOTES: 1. Typical values are T_A = 25°C and nominal supply voltage.
2. t_{RC} = Read Cycle Time.

A.C. Characteristics for M5101-4, M5101L-4

READ CYCLE T_A = -55°C to 125°C, V_{CC} = 5V ±5%, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	800			ns	(See below)
t_A	Access Time			800	ns	
t_{CO1}	Chip Enable ($\overline{CE1}$) to Output			700	ns	
t_{CO2}	Chip Enable (CE2) to Output			850	ns	
t_{OD}	Output Disable To Output			350	ns	
t_{DF}	Data Output to High Z State	0		150	ns	
t_{OH1}	Previous Read Data Valid with Respect to Address Change	0			ns	
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	800			ns	(See below)
t_{AW}	Write Delay	150			ns	
t_{CW1}	Chip Enable ($\overline{CE1}$) To Write	550			ns	
t_{CW2}	Chip Enable (CE2) To Write	550			ns	
t_{DW}	Data Setup	400			ns	
t_{DH}	Data Hold	100			ns	
t_{WP}	Write Pulse	400			ns	
t_{WR}	Write Recovery	50			ns	
t_{DS}	Output Disable Setup	150			ns	

A. C. CONDITIONS OF TEST

Input Pulse Levels: 0.5 Volt to V_{CC}-2.0 Volt
Input Pulse Rise and Fall Times: 20nsec
Timing Measurement Reference Level: 1.5 Volt
Output Load: 1 TTL Gate and C_L = 100pF

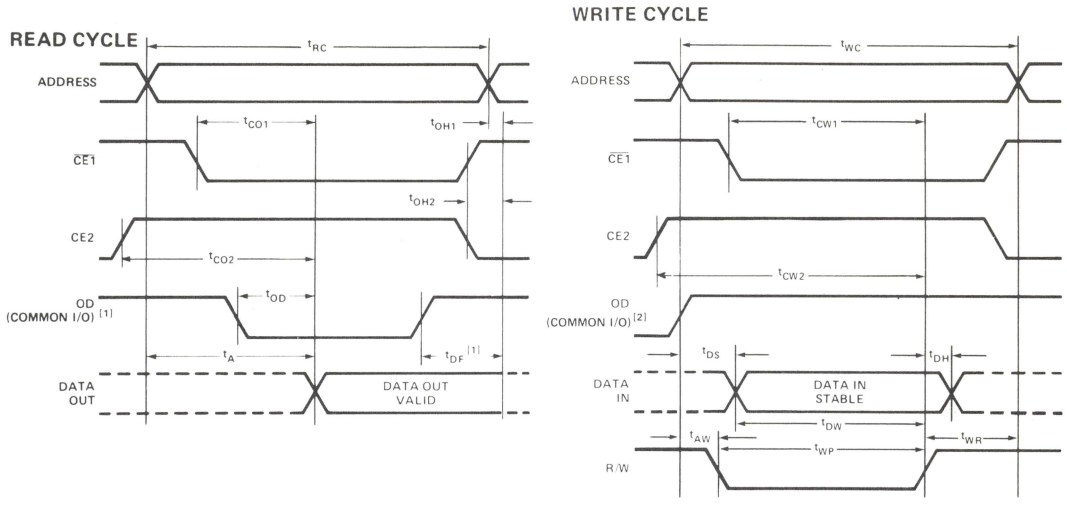
Capacitance[3] T_A = 25°C, f = 1MHz

Symbol	Test	Limits (pF)	
		Typ.	Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
C_{OUT}	Output Capacitance V_{OUT} = 0V	8	12

NOTE: 3. This parameter is periodically sampled and is not 100% tested.

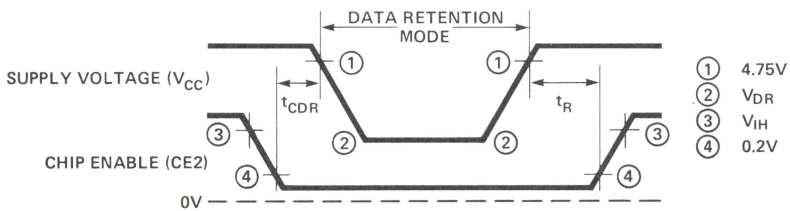
MILITARY TEMP.

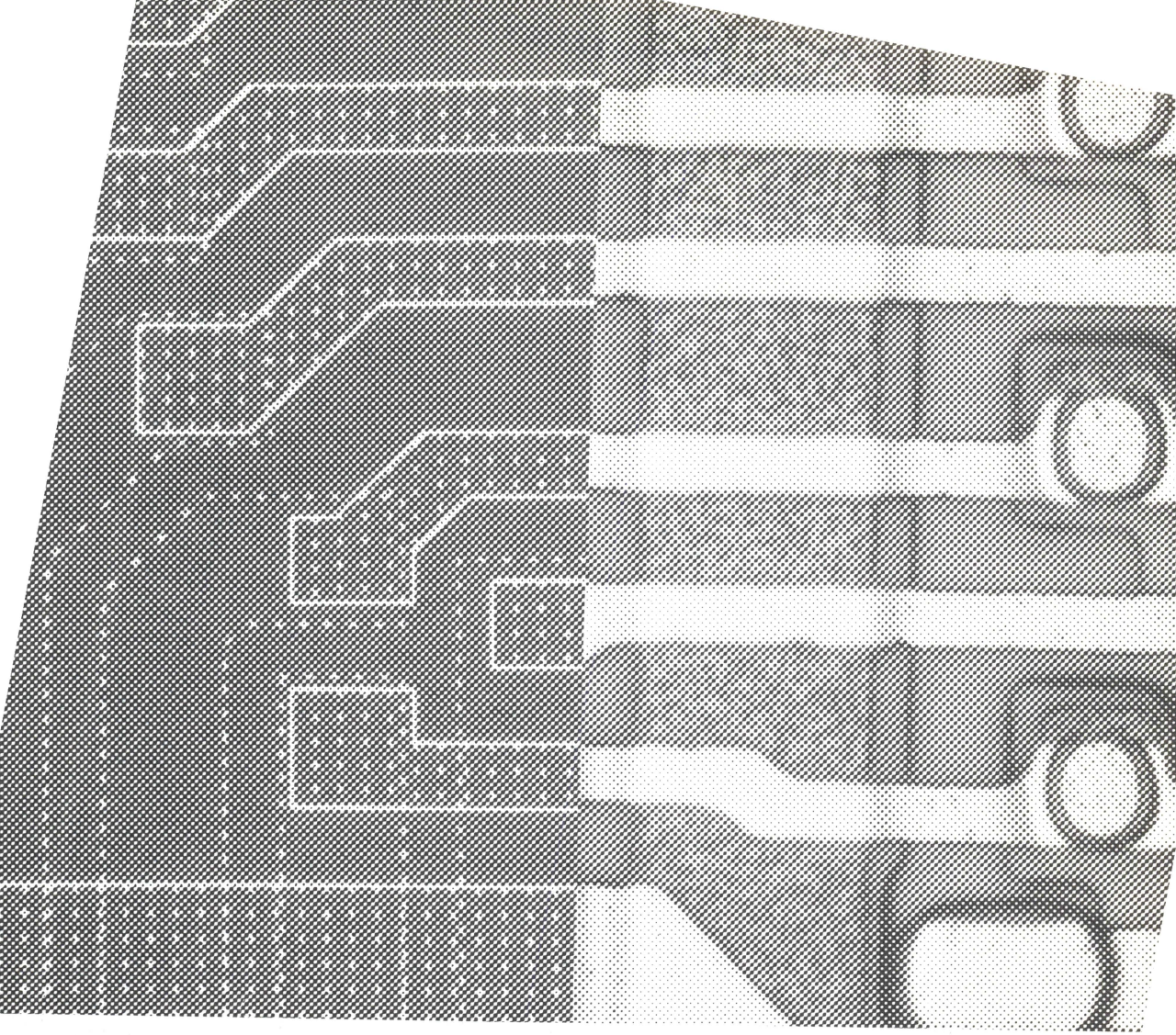
Waveforms



NOTES: 1. OD may be tied low for separate I/O operation.
2. During the write cycle, OD is "high" for common I/O and "don't care" for separate I/O operation.

Low V_{CC} Data Retention





4 Read Only Memory

MOS ROM AND PROM FAMILY

	Type	No. of Bits	Organization	No. of Pins	Output[1]	Maximum Access (ns)	Maximum Power Dissipation (mW)	Operating Temperature Range (°C)	Power Supply (V)	Page No.
MOS ROM	**2308**	8192	1024 x 8	24	T.S.	450	840	0 to 70	5V ± 5% 12V ± 5% −5V ± 5%	4-18
	2316A	16384	2048 x 8	24	T.S.	850	515	0 to 70	5V ± 5%	4-22
	2316E	16384	2048 x 8	24	T.S.	450	630	0 to 70	5V ± 10%	4-25
	M2316E	16384	2048 x 8	24	T.S.	TBD	TBD	−55 to 125	5V ± 10%	4-28
	2332	32768	4096 x 8	24	T.S.	TBD	TBD	0 to 70	5V ± 10%	4-29
	2364	65536	8192 x 8	28	T.S.	TBD	TBD	0 to 70	5V ± 10%	4-30
ONE TIME PROGRAMMABLE PROM	**2608**	8192	1024 x 8	24	T.S.	450	800	0 to 70	5V ± 5% 12V ± 5% −5V ± 5%	4-31
	2616	16384	2048 x 8	24	T.S.	450	525	0 to 70	5V ± 5%	4-34
MOS EPROM	**1702A**	2048	256 x 8	24	T.S.	1μs	885	0 to 70	5V ± 5% −9V ± 5%	4-5
	1702A-2	2048	256 x 8	24	T.S.	650	959	0 to 70	5V ± 5% −9V ± 5%	
	1702A-6	2048	256 x 8	24	T.S.	1.5μs	885	0 to 70	5V ± 5% −9V ± 5%	
	4702A	2048	256 x 8	24	T.S.	1.7μs		0 to 70	5V ± 5% −10V ± 5%	4-14
	M1702A	2048	256 x 8	24	T.S.	850	960	−55 to 100	5V ± 10% −9V ± 10%	4-9
	1702AL	2048	256 x 8	24	T.S.	1μs	221	0 to 70	5V ± 5% −9V ± 5%	4-11
	1702AL-2	2048	256 x 8	24	T.S.	650	221	0 to 70	5V ± 5% −9V ± 5%	
	2704	4096	512 x 8	24	T.S.	450	800	0 to 70	5V ± 5% 12V ± 5% −5V ± 5%	4-38
	2708	8192	1024 x 8	24	T.S.	450	800	0 to 70	5V ± 5% 12V ± 5% −5V ± 5%	
	2708L	8192	1024 x 8	24	T.S.	450	425	0 to 70	5V ± 5% 12V ± 5% −5V ± 5%	4-38
	2708-1	8192	1024 x 8	24	T.S.	350	800	0 to 70	5V ± 5% 12V ± 5% −5V ± 5%	
	M2708	8192	1024 x 8	24	T.S.	450	750	−55 to 100	5V ± 10% 12V ± 10% −5V ± 10%	4-41
	2716	16384	2048 x 8	24	T.S.	450	525/132[2]	0 to 70	5V ± 5%	4-44
	M2716	16384	2048 x 8	24	T.S.			−55 to 125	5V ± 10%	4-49
	2732	32768	4096 x 8	24	T.S.			0 to 70	5V ± 10%	4-50
	2758	8192	1024 x 8	24	T.S.	450	525/132[2]	0 to 70	5V ± 5%	4-51

Notes: 1. TS is a three state output.
2. The 2716/2758 has a standby power down feature.

ROM and PROM Programming Instructions 4-69

BIPOLAR PROM FAMILY

Type	No. of Bits	Organization	No. of Pins	Output[1]	Maximum Access (ns)	Maximum Power Dissipation (mW)	Operating Temperature Range (°C)	Power Supply	Page No.
3602A	2048	512x4	16	O.C.	70	735	0 to 75	5V ± 5%	4-55
3602A-2	2048	512x4	16	O.C.	60	735	0 to 75	5V ± 5%	
3622A	2048	512x4	16	T.S.	70	735	0 to 75	5V ± 5%	
3622A-2	2048	512x4	16	T.S.	60	735	0 to 75	5V ± 5%	
3604A	4096	512x8	24	O.C.	70	895	0 to 75	5V ± 5%	4-58
3604A-2	4096	512x8	24	O.C.	60	895	0 to 75	5V ± 5%	
3604AL	4096	512x8	24	O.C.	90	685/135[2]	0 to 75	5V ± 5%	
3624A	4096	512x8	24	T.S.	70	895	0 to 75	5V ± 5%	
3624A-2	4096	512x8	24	T.S.	60	895	0 to 75	5V ± 5%	
M3604A	4096	512x8	24	O.C.	90	1045	-55 to 125	5V ± 10%	4-61
M3624A	4096	512x8	24	T.S.	90	1045	-55 to 125	5V ± 10%	
3605	4096	1024x4	18	O.C.	70	735	0 to 75	5V ± 5%	4-63
3605-2	4096	1024x4	18	O.C.	60	735	0 to 75	5V ± 5%	
3625	4096	1024x4	18	T.S.	70	735	0 to 75	5V ± 5%	
3625-2	4096	1024x4	18	T.S.	60	735	0 to 75	5V ± 5%	
3608	8192	1024x8	24	O.C.	80	998	0 to 75	5V ± 5%	4-66
3608-4	8192	1024x8	24	O.C.	100	998	0 to 75	5V ± 5%	
3628	8192	1024x8	24	O.C.	80	998	0 to 75	5V ± 5%	
3628-4	8192	1024x8	24	O.C.	100	998	0 to 75	5V ± 5%	

Notes: 1. O.C. and T.S. are open collector and three-state output respectively.
2. The 3604AL has a low power dissipation feature.

| ROM and PROM Programming Instructions | 4-69 |

BIPOLAR PROM CROSS REFERENCE

Part Number	Prefix and Manufacturer	Organization	Intel Part Number	
			Direct Replacement	For New Designs[1]
5340-1	MMI	512 x 8	M3624A	
5341-1	MMI	512 x 8	M3624A	
5604C	IM–Intersil	512 x 4	3602A	
5605C	IM–Intersil	512 x 8	3604A	
5624C	IM–Intersil	512 x 4	3622A	
5625C	IM–Intersil	512 x 8	3624A	
6305-1	MMI	512 x 4	3602A-2	
6306-1	MMI	512 x 4	3622A-2	
6340-1	MMI	512 x 8	3604A	
6341-1	MMI	512 x 8	3624A	
6352-1	MMI	1024 x 4	3605-2	
6353-1	MMI	1024 x 4	3625-2	
6380-1	MMI	1024 x 8	3608	
6381-1	MMI	1024 x 8	3628	
74S472	TI	512 x 8		3624A
74S473	TI	512 x 8		3604A
74S474	TI	512 x 8	3624A	
74S475	TI	512 x 8	3604A	
74S570	National	512 x 4	3602A	
74S571	National	512 x 4	3622A	
7620-5	HM–Harris	512 x 4	3602A	
7621-5	HM–Harris	512 x 4	3622A	
7640-2	HM–Harris	512 x 8		M3604A
7640-5	HM–Harris	512 x 8	3604A	
7641-2	HM–Harris	512 x 8		M3624A
7641-5	HM–Harris	512 x 8	3624A	
7642-5	HM–Harris	1024 x 4	3605	
7643-5	HM–Harris	1024 x 4	3625	
7644-5	HM–Harris	1024 x 4		3625
7680-5	HM–Harris	1024 x 8	3608	
7681-5	HM–Harris	1024 x 8	3628	
82S115	N–Signetics	512 x 8		3624A
82S115	S–Signetics	512 x 8		M3624A
82S130	N–Signetics	512 x 4		3602A
82S131	N–Signetics	512 x 4		3622A
82S140	N–Signetics	512 x 8	3604A-2	
82S141	N–Signetics	512 x 8	3624A-2	
82S136	N–Signetics	1024 x 4	3605-2	
82S137	N–Signetics	1024 x 4	3625-2	
82S180	N–Signetics	1024 x 8		3608
82S181	N–Signetics	1024 x 8		3628
82S184	N–Signetics	2048 x 4		3608
82S185	N–Signetics	2048 x 4		3628
87S295	National	512 x 8	3604A	
87S296	National	512 x 8	3624A	
93436C	Fairchild	512 x 4		3602A-2
93438C	Fairchild	512 x 8		3604A-2
93438M	Fairchild	512 x 8		M3604A
93446C	Fairchild	512 x 4		3622A-2
93448C	Fairchild	512 x 8		3624A-2
93448M	Fairchild	512 x 8		M3624A
93452C	Fairchild	1024 x 4	3605-2	
93453C	Fairchild	1024 x 4	3625-2	

NOTE: 1. The Intel® PROMs have the same pin configuration and differ only in access time from the PROMs in the first column. The exceptions are the 6350, 6351, 82S115, and 82S184/85 which have different pin configurations.

1702A

2K (256 x 8) UV ERASABLE PROM

1702A-2	0.65 us Max.
1702A	1.0 us Max.
1702A-6	1.5 us Max.

- **Fast Access Time: Max. 650 ns (1702A–2)**
- **Fast Programming: 2 Minutes for all 2048 Bits**
- **All 2048 Bits Guaranteed* Programmable: 100% Factory Tested**
- **Static MOS: No Clocks Required**
- **Inputs and Outputs DTL and TTL Compatible**
- **Three-State Output: OR-tie Capability**

The 1702A is a 256 word by 8-bit electrically programmable ROM ideally suited for uses where fast turn-around and pattern experimentation are important. The 1702A undergoes complete programming and functional testing prior to shipment, thus insuring 100% programmability.

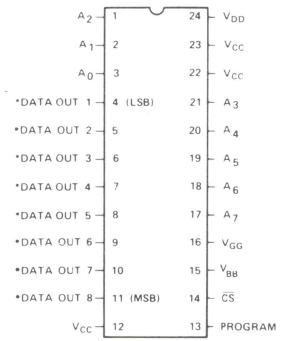
Initially all 2048 bits of the 1702A are in the "0" state (output low). Information is introduced by selectively programming "1"s (output high) in the proper bit location. The 1702A is packaged in a 24 pin dual in-line package with a transparent lid. The transparent lid allows the user to expose the 1702A to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device.

The circuitry of the 1702A is completely static. No clocks are required. Access times from 650ns to 1.5μs are available. A 1702AL family is available (see 1702AL data sheets for specifications) for those systems requiring lower power dissipation than the 1702A.

The 1702A is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

*Intel's liability shall be limited to replacing any unit which fails to program as desired.

PIN CONFIGURATION

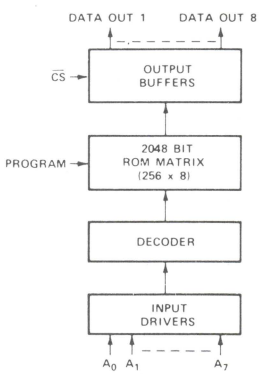


*THIS PIN IS THE DATA INPUT LEAD DURING PROGRAMMING

PIN NAMES

A_0–A_7	Address Inputs
$\overline{CS}$	Chip Select Input
D_{OUT1}–D_{OUT8}	Data Outputs

BLOCK DIAGRAM



NOTE: In the read mode a logic 1 at the address inputs and data outputs is a high and logic 0 is a low.

U.S. Patent No. 3660819

PIN CONNECTIONS

The external lead connections to the 1702A differ, depending on whether the device is being programmed or used in read mode (see following table). In the programming mode, the data inputs 1-8 are pins 4-11 respectively. *The programming voltages and timing are shown in the ROM and PROM Programming instructions section, page 4-84.*

MODE \ PIN	12 (V_{CC})	13 (Program)	14 ($\overline{CS}$)	15 (V_{BB})	16 (V_{GG})	22 (V_{CC})	23 (V_{CC})	24 (V_{DD})
Read	V_{CC}	V_{CC}	GND	V_{CC}	V_{GG}	V_{CC}	V_{CC}	V_{DD}
Programming	GND	Program Pulse	GND	V_{BB}	Pulsed V_{GG}	GND	GND	Pulsed V_{DD}

Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . −10°C to +80°C
Storage Temperature . . . . . −65°C to +125°C
Soldering Temperature of Leads (10 sec) . . . . . +300°C
Power Dissipation . . . . . 2 Watts
Read Operation: Input Voltages and Supply Voltages with respect to V_{CC} . . . . . +0.5V to −20V
Program Operation: Input Voltages and Supply Voltages with respect to V_{CC} . . . . . −48V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = −9V ±5%, V_{GG} = −9V ±5%, unless otherwise noted.

READ OPERATION

Symbol	Test	1702A, 1702A-6 Limits Min.	Typ.[1]	Max.	1702A-2 Limits Min.	Typ.[1]	Max.	Unit	Conditions
I_{LI}	Address and Chip Select Input Load Current			1			1	μA	V_{IN} = 0.0V
I_{LO}	Output Leakage Current			1			1	μA	V_{OUT} = 0.0V, $\overline{CS}$ = V_{IH2}
I_{DD1}[1]	Power Supply Current		35	50		40	60	mA	$\overline{CS}$ = V_{IH2}, I_{OL} = 0.0mA, T_A = 25°C, Continuous
I_{DD2}	Power Supply Current		32	46		37	55	mA	$\overline{CS}$ = 0.0V, I_{OL} = 0.0mA, T_A = 25°C, Continuous
I_{DD3}	Power Supply Current		38	60		43	65	mA	$\overline{CS}$ = V_{IH2}, I_{OL} = 0.0mA, T_A = 0°C, Continuous
I_{CF1}	Output Clamp Current		8	14		7	13	mA	V_{OUT} = -1.0V, T_A = 0°C, Continuous
I_{CF2}	Output Clamp Current		7	13		6	12	mA	V_{OUT} = -1.0V, T_A = 25°C, Continuous
I_{GG}	Gate Supply Current			1			1	μA	
V_{IL1}	Input Low Voltage for TTL Interface	-1		0.65	-1		0.65	V	
V_{IL2}	Input Low Voltage for MOS Interface	V_{DD}		V_{CC}-6	V_{DD}		V_{CC}-6	V	
V_{IH1}	Addr. Input High Voltage	V_{CC}-2		V_{CC}+0.3	V_{CC}-2		V_{CC}+0.3	V	
V_{IH2}	Chip Sel. Input High Volt.	V_{CC}-2		V_{CC}+0.3	V_{CC}-1.5		V_{CC}+0.3	V	
I_{OL}	Output Sink Current	1.6	4		1.6	4		mA	V_{OUT} = 0.45V
I_{OH}	Output Source Current	-2.0			-2.0			mA	V_{OUT} = 0.0V
V_{OL}	Output Low Voltage		-3	0.45		-3	0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	3.5	4.5		3.5	4.5		V	I_{OH} = -200μA

Note 1: Typical values are at nominal voltages and T_A = 25°C.

A.C. Characteristics

T_A = 0° C to +70° C, V_{CC} = +5V ±5%, V_{DD} = −9V ±5%, V_{GG} = −9V ±5% unless otherwise noted

Symbol	Test	1702A Limits Min.	1702A Limits Max.	1702A-2 Limits Min.	1702A-2 Limits Max.	1702A-6 Limits Min.	1702A-6 Limits Max.	Unit
Freq.	Repetition Rate		1		1.6		0.66	MHz
t_{OH}	Previous Read Data Valid		0.1		0.1		0.1	μs
t_{ACC}	Address to Output Delay		1		0.65		1.5	μs
t_{CS}	Chip Select Delay		0.1		0.3		0.6	μs
t_{CO}	Output Delay From $\overline{CS}$		0.9		0.35		0.9	μs
t_{OD}	Output Deselect		0.3		0.3		0.3	μs

PROM/ROM

Capacitance * T_A = 25°C

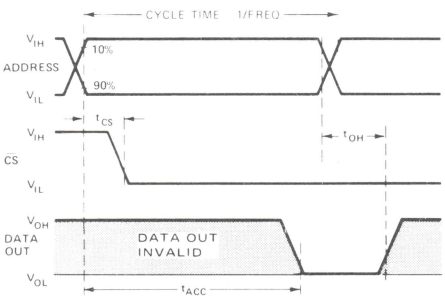
SYMBOL	TEST	TYPICAL	MAXIMUM	UNIT	CONDITIONS
C_{IN}	Input Capacitance	8	15	pF	$V_{IN} = V_{CC}$, $\overline{CS} = V_{CC}$, $V_{OUT} = V_{CC}$, $V_{GG} = V_{CC}$ — All unused pins are at A.C. ground
C_{OUT}	Output Capacitance	10	15	pF	

*This parameter is periodically sampled and is not 100% tested.

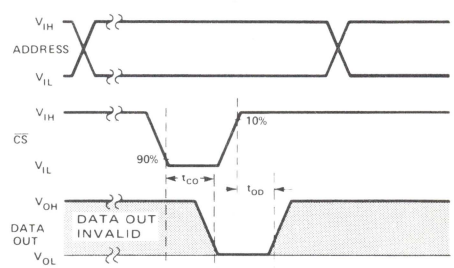
Switching Characteristics

Conditions of Test:
Input pulse amplitudes: 0 to 4V; t_R, t_F ≤50 ns
Output load is 1 TTL gate; measurements made at output of TTL gate (t_{PD}≤15 ns), C_L=15pF

A) READ OPERATION

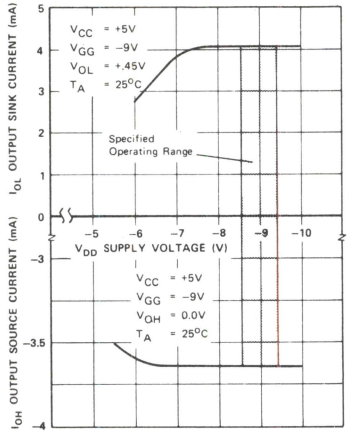


B) DESELECTION OF DATA OUTPUT IN OR-TIE OPERATION

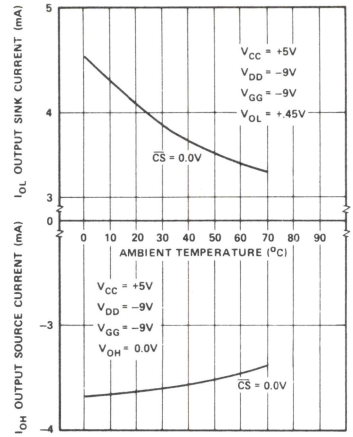


Typical Characteristics

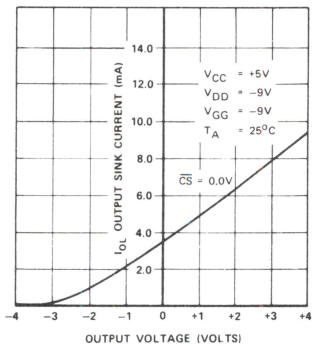
OUTPUT CURRENT VS. V_{DD} SUPPLY VOLTAGE



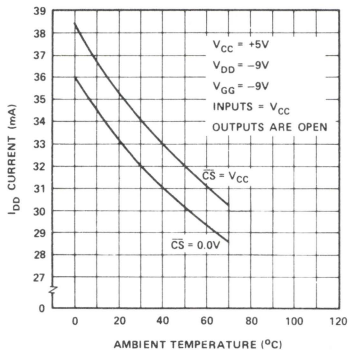
OUTPUT CURRENT VS. TEMPERATURE



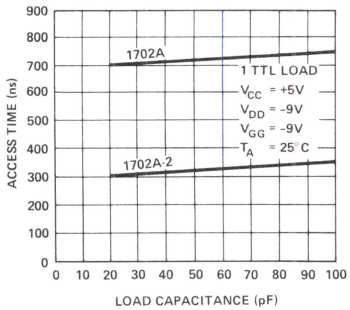
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



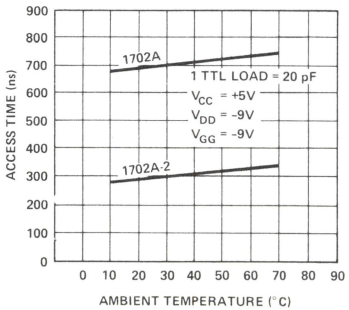
I_{DD} CURRENT VS. TEMPERATURE



ACCESS TIME VS. LOAD CAPACITANCE



ACCESS TIME VS. TEMPERATURE

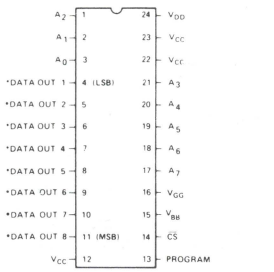


M1702A
2K (256 x 8) UV ERASABLE PROM
−55°C to +100°C OPERATION

- **Fast Access Time: Max. 850 ns**
- **Completely Static**
- **Inputs and Outputs DTL and TTL Compatible**
- **All 2048 Bits Factory Tested Prior to Shipment**
- **Three-State Output**
- **24 Pin Dip**

The Intel® M1702A is a 256-word by 8-bit ultraviolet light erasable and electrically reprogrammable EPROM which is specified over the −55°C to +100°C temperature range. The M1702A has a transparent lid which allows the user to expose the M1702A to UV light to erase the bit pattern. A new pattern can then be written into the device.

PIN CONFIGURATION



*THIS PIN IS THE DATA INPUT LEAD DURING PROGRAMMING

*REFER TO THE 1702A DATA SHEET FOR PIN CONNECTIONS DURING READ AND PROGRAM

Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . −65°C to 110°C
Storage Temperature . . . . . −65°C to +125°C
Soldering Temperature of Leads (10 sec) . . . . . +300°C
Power Dissipation . . . . . 2 Watts
Read Operation: Input Voltages and Supply Voltages with respect to V_{CC} . . . . . +0.5V to −20V
Program Operation: Input Voltages and Supply Voltages with respect to V_{CC} . . . . . −48V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics
READ OPERATION

T_A = −55°C to 100°C, V_{CC} = +5V ±10%, V_{DD} = −9V ±10%, V_{GG} = −9V ±10% unless otherwise noted.

Symbol	Test	Min.	Typ.[1]	Max.	Unit	Conditions
I_{LI}	Address and Chip Select Input Load Current			10	μA	V_{IN} = 0.0V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 0.0V, $\overline{CS}$ = V_{IH2}
I_{DD1}[1]	Power Supply Current		35	50	mA	$\overline{CS}$ = V_{IH2}, I_{OL} = 0.0mA, T_A = 25°C, Continuous
I_{DD2}	Power Supply Current		32	46	mA	$\overline{CS}$ = 0.0V, I_{OL} = 0.0mA, T_A = 25°C, Continuous
I_{DD3}	Power Supply Current		38	65	mA	$\overline{CS}$ = V_{IH2}, I_{OL} = 0.0mA, T_A = −55°C, Continuous
I_{CF}	Output Clamp Current		8	11	mA	V_{OUT} = −1.0V, T_A = −55°C, Continuous
I_{GG}	Gate Supply Current			10	μA	
V_{IL1}	Input Low Voltage for TTL Interface	−1		0.65	V	
V_{IL2}	Input Low Voltage for MOS Interface	V_{DD}		V_{CC}−6	V	
V_{IH1}	Address Input High Voltage	V_{CC}−2		V_{CC}+0.3	V	
V_{IH2}	Chip Select Input High Voltage	V_{CC}−1.5		V_{CC}+0.3	V	
I_{OL}	Output Sink Current	1.6	4		mA	V_{OUT} = 0.45V
I_{OH}	Output Source Current	−2.0			mA	V_{OUT} = 0.0V
V_{OL}	Output Low Voltage		−3	0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	3.5	4.5		V	I_{OH} = −200μA

Note 1. Typical values are at nominal voltages and T_A = 25°C.

A.C. Characteristics

T_A = -55°C to 100°C, V_{CC} = +5V ±10%, V_{DD} = -9V ±10%, V_{GG} = -9V ±10% unless otherwise noted.

Symbol	Test	Limits Min.	Limits Max.	Unit
Freq.	Repetition Rate		1.2	MHz
t_{OH}	Previous Read Data Valid		0.1	μs
t_{ACC}	Address to Output Delay		0.85	μs
t_{CS}	Chip Select Delay		0.5	μs
t_{CO}	Output Delay From $\overline{CS}$		0.35	μs
t_{OD}	Output Deselect		0.3	μs

Capacitance * T_A = 25°C

SYMBOL	TEST	TYPICAL	MAXIMUM	UNIT	CONDITIONS
C_{IN}	Input Capacitance	8	15	pF	$V_{IN} = V_{CC}$, $\overline{CS} = V_{CC}$, $V_{OUT} = V_{CC}$, $V_{GG} = V_{CC}$ — All unused pins are at A.C. ground
C_{OUT}	Output Capacitance	10	15	pF	

*This parameter is sampled and is not 100% tested.

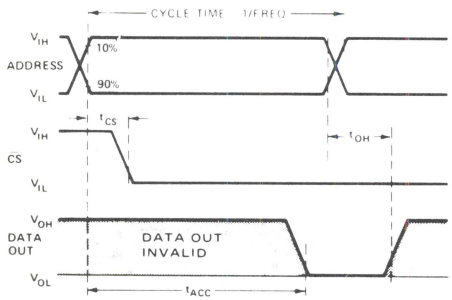
Switching Characteristics

Conditions of Test:

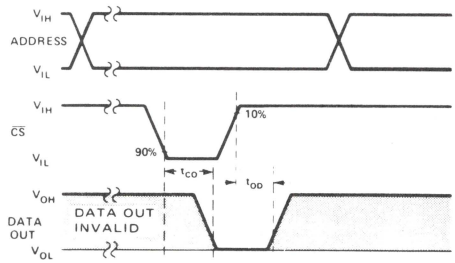
Input pulse amplitudes: 0 to 4V; t_R, t_F ≤50 ns

Output load is 1 TTL gate; measurements made at output of TTL gate (t_{PD}≤15 ns), C_L = 15pF

A) READ OPERATION



B) DESELECTION OF DATA OUTPUT IN OR-TIE OPERATION



ERASING AND PROGRAMMING PROCEDURE

The erasing and programming procedure of the M1702A is the same as the 0°C to 70°C 1702A. The procedure is discussed in Section IV, page 4-83, of the data catalog.

2K (256 x 8) UV ERASABLE LOW POWER PROM

Part No.	MAXIMUM ACCESS (μs)	t_{DVGG} (μs)
1702AL	1.0	0.4
1702AL-2	0.65	0.3

- **Clocked V_{GG} Mode for Low Power Dissipation**
- **Fast Programming: 2 Minutes for all 2048 Bits**
- **All 2048 Bits Guaranteed* Programmable: 100% Factory Tested**
- **Inputs and Outputs DTL and TTL Compatible**
- **Three-State Output: OR-tie Capability**

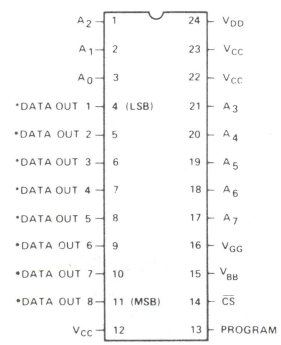
The 1702AL is a 256 word by 8 bit electrically programmable ROM and is the same chip as the industry standard 1702A. The programming and erasing specifications are identical to the 1702A. The 1702AL operates with the V_{GG} clocked to reduce the power dissipation.

Initially all 2048 bits of the 1702AL are in the "0" state (output low). Information is introduced by selectively programming "1"s (output high) in the proper bit location. The 1702AL is packaged in a 24 pin dual in-line package with a transparent lid. The transparent lid allows the user to expose the 1702AL to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device.

The 1702AL is fabricated with silicon gate technology. This low threshold technology allows the design and production of high performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

*Intel's liability shall be limited to replacing any unit which fails to program as desired.

PIN CONFIGURATION

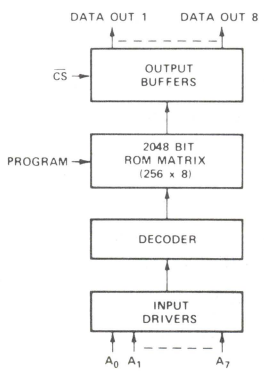


*THIS PIN IS THE DATA INPUT LEAD DURING PROGRAMMING

PIN NAMES

A_0–A_7	Address Inputs
$\overline{CS}$	Chip Select Input
D_{OUT1}–D_{OUT8}	Data Outputs

BLOCK DIAGRAM



NOTE: In the read mode a logic 1 at the address inputs and data outputs is a high and logic 0 is a low.

U.S. Patent No. 3660819

PIN CONNECTIONS

The external lead connections to the 1702AL differ, depending on whether the device is being programmed or used in read mode (see following table). In the programming mode, the data inputs 1-8 are pins 4-11 respectively. *The programming voltages and timing are shown in the Data Catalog ROM and PROM Programming Instructions section, page 4-83.*

MODE \ PIN	12 (V_{CC})	13 (Program)	14 (CS)	15 (V_{BB})	16 (V_{GG})	22 (V_{CC})	23 (V_{CC})	24 (V_{DD})
Read	V_{CC}	V_{CC}	GND	V_{CC}	Clocked V_{GG}	V_{CC}	V_{CC}	V_{DD}
Programming	GND	Program Pulse	GND	V_{BB}	Pulsed V_{GG}	GND	GND	Pulsed V_{DD}

Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . −10°C to +80°C
Storage Temperature . . . . . −65°C to +125°C
Soldering Temperature of Leads (10 sec) . . . . . +300°C
Power Dissipation . . . . . 2 Watts
Read Operation: Input Voltages and Supply Voltages with respect to V_{CC} . . . . . +0.5V to −20V
Program Operation: Input Voltages and Supply Voltages with respect to V_{CC} . . . . . −48V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = −9V ±5%, V_{GG}[1] = −9V ±5%, unless otherwise noted.

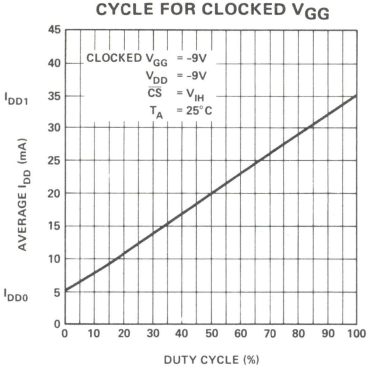
READ OPERATION

Symbol	Test	1702AL Limits Min.	Typ.[2]	Max.	1702AL-2 Limits Min.	Typ.[2]	Max.	Unit	Conditions
I_{LI}	Address and Chip Select Input Load Current			1			1	μA	V_{IN} = 0.0V
I_{LO}	Output Leakage Current			1			1	μA	V_{OUT} = 0.0V, $\overline{CS}$ = V_{CC}-2
I_{DDO1}[1]	Power Supply Current		7	10		7	10	mA	T_A=25°C $\overline{CS}$=V_{IH}, V_{GG}=V_{CC},
I_{DDO2}	Power Supply Current			15			15	mA	T_A=0°C I_{OL}=0.0mA
I_{DD1}[1]	Power Supply Current		35	50		35	50	mA	$\overline{CS}$ = V_{CC} -2, I_{OL} = 0.0mA, T_A = 25°C, Continuous
I_{DD2}	Power Supply Current		32	46		32	46	mA	$\overline{CS}$ = 0.0V, I_{OL} = 0.0mA, T_A = 25°C, Continuous
I_{DD3}	Power Supply Current		38	60		38	60	mA	$\overline{CS}$ = V_{CC} -2, I_{OL} = 0.0mA, T_A = 0°C, Continuous
I_{CF1}	Output Clamp Current		8	14		5.5	8	mA	V_{OUT} = -1.0V, T_A = 0°C, Continuous
I_{CF2}	Output Clamp Current		7	13		5	7	mA	V_{OUT} = -1.0V, T_A = 25°C, Continuous
I_{GG}	Gate Supply Current			1			1	μA	
V_{IL1}	Input Low Voltage for TTL Interface	-1		0.65	-1		0.65	V	
V_{IL2}	Input Low Voltage for MOS Interface	V_{DD}		V_{CC}-6	V_{DD}		V_{CC}-6	V	
V_{IH}	Address and Chip Select Input High Voltage	V_{CC}-2		V_{CC}+0.3	V_{CC}-2		V_{CC}+0.3	V	
I_{OL}	Output Sink Current	1.6	4		1.6	4		mA	V_{OUT} = 0.45V
I_{OH}	Output Source Current	-2.0			-2.0			mA	V_{OUT} = 0.0V
V_{OL}	Output Low Voltage		-3	0.45		-3	0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	3.5	4.5		3.5	4.5		V	I_{OH} = -200μA

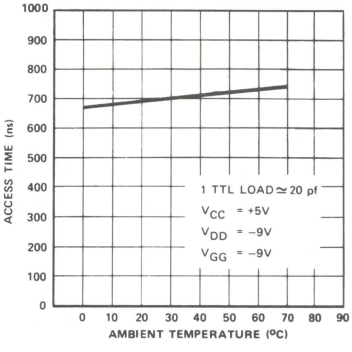
NOTES: 1. The 1702AL is operated with the V_{GG} clocked to obtain low power dissipation. The average I_{DD} will vary between I_{DD0} and I_{DD1} (at 25°C) depending on the V_{GG} duty cycle (see curve opposite). 2. Typical values are at nominal voltage and T_A = 25°C.

TYPICAL CHARACTERISTICS

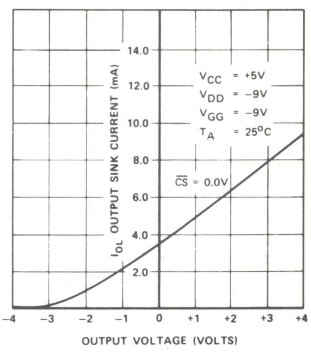
AVERAGE CURRENT VS. DUTY CYCLE FOR CLOCKED V_{GG}



ACCESS TIME VS. TEMPERATURE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



PROM/ROM

A.C. CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$, $V_{DD} = -9V \pm 5\%$ unless otherwise noted

Symbol	Test	1702AL Limits Min.	1702AL Limits Max.	1702AL-2 Limits Min.	1702AL-2 Limits Max.	Unit
Freq.	Repetition Rate		1		1.6	MHz
t_{ACC}	Address to output delay		1		0.65	μs
t_{DVGG}	Clocked V_{GG} set up	0.4		0.3		μs
t_{CS}	Chip select delay		0.1		0.3	μs
t_{CO}	Output delay from $\overline{CS}$		0.9		0.35	μs
t_{OD}	Output deselect		0.3		0.3	μs
t_{OHC}	Data out hold in clocked V_{GG} mode		5		5	μs

CAPACITANCE $T_A = 25°C$

SYMBOL	TEST	TYPICAL	MAXIMUM	UNIT	CONDITIONS
C_{IN}	Input Capacitance	8	15	pF	$V_{IN} = V_{CC}$, $\overline{CS} = V_{CC}$, $V_{OUT} = V_{CC}$, $V_{GG} = V_{CC}$ — All unused pins are at A.C. ground
C_{OUT}	Output Capacitance	10	15	pF	
$C_{V_{GG}}$	V_{GG} Capacitance (Note 1)		30	pF	

*This parameter is periodically sampled and is not 100% tested.

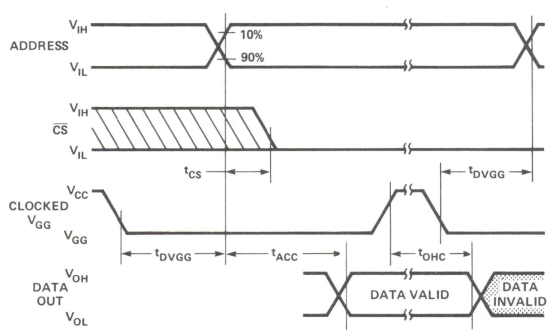
SWITCHING CHARACTERISTICS

Conditions of Test:

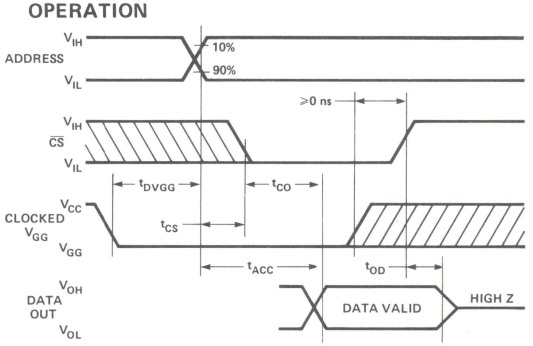
Input pulse amplitudes: 0 to 4V; t_R, $t_F \leqslant 50$ ns

Output load is 1 TTL gate; measurements made at output of TTL gate ($t_{PD} \leqslant 15$ ns), C_L = 15pF

A. READ OPERATION



B. DESELECTION OF DATA OUTPUT IN OR-TIE OPERATION



4702A
2K (256 x 8) UV ERASABLE PROM

- **Access Time: 1.7 usec Max.**
- **Fast Programming: 2 Minutes for all 2048 Bits**
- **Ultraviolet Erasable and Electronically Reprogrammable**
- **Fully Decoded, 256 x 8 Organization**
- **Static MOS: No Clocks Required**
- **Inputs and Outputs TTL Compatible**
- **Three-State Output: OR-Tie Capability**
- **Standard Operating Temperature Range of 0° to 70° C**
- **Also Available with -40° to +85° C Operating Range**

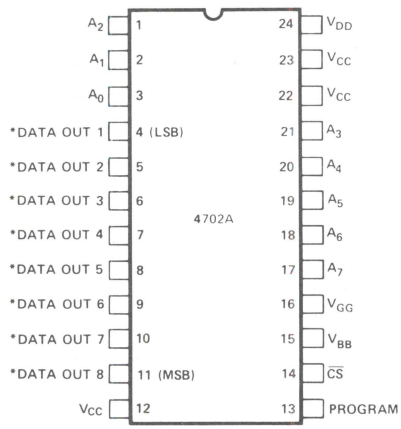
The 4702A is a 256 word by 8 bit electrically programmable ROM ideally suited for microcomputer system development where fast turn-around and pattern experimentation are important. The 4702A undergoes complete programming and functional testing on each bit position prior to shipment, thus insuring 100% programmability.

The 4702A is packaged in a 24 pin dual-in-line package with a transparent quartz lid. The transparent quartz lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device. This procedure can be repeated as many times as required.

The circuitry of the 4702A is entirely static; no clocks are required.

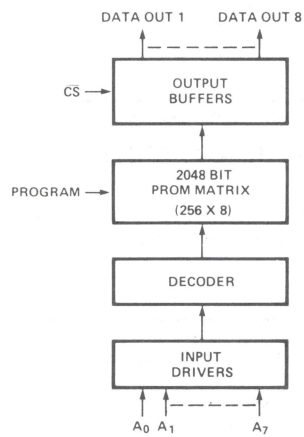
The 4702A is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

PIN CONFIGURATION



*THIS PIN IS THE DATA INPUT LEAD DUPING PROGRAMMING.

BLOCK DIAGRAM



PIN NAMES

A_0-A_7	ADDRESS INPUTS
$\overline{CS}$	CHIP SELECT INPUT
DO_1- DO_2	DATA OUTPUTS

Pin Connections

The Programming voltages and timings are shown in the Data Catalog ROM and PROM programming instruction section, page 4-83.

The external lead connections to the 4702A differ, depending on whether the device is being programmed (1) or used in read mode. (See following table.)

MODE \ PIN	12 (V_{CC})	13 (Program)	14 ($\overline{CS}$)	15 (V_{BB})	16 (V_{GG})	22 (V_{CC})	23 (V_{CC})
Read	V_{CC}	V_{CC}	GND	V_{CC}	V_{GG}	V_{CC}	V_{CC}
Programming	GND	Program Pulse	GND	V_{BB}	Pulsed V_{GG} (V_{IL4P})	GND	GND

Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +125°C
Soldering Temperature of Leads (10 sec) . . . . . +300°C
Power Dissipation . . . . . 2 Watts
Read Operation: Input Voltages and Supply Voltages with respect to V_{CC} . . . . . +0.5V to −20V
Program Operation: Input Voltages and Supply Voltages with respect to V_{CC} . . . . . −48V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

READ OPERATION

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = +5V±5%, V_{DD} = -10V±5%, V_{GG} = -10V±5%, unless otherwise noted.

SYMBOL	TEST	MIN.	TYP.[2]	MAX.	UNIT	CONDITIONS
I_{LI}	Address and Chip Select Input Load Current			10	μA	V_{IN} = 0.0V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 0.0V, $\overline{CS}$ = V_{CC} −2
I_{DD1}	Power Supply Current		39	54	mA	$\overline{CS}$ = V_{CC} −2, I_{OL} = 0.0mA, T_A = 25°C
I_{DD2}	Power Supply Current		36	50	mA	$\overline{CS}$ = 0.0, I_{OL} = 0.0mA, T_A = 25°C
I_{DD3}	Power Supply Current		43	63	mA	$\overline{CS}$ = V_{CC} −2, I_{OL} = 0.0mA, T_A = 0°C
I_{CF1}	Output Clamp Current		8	14	mA	V_{OUT} = 1.0V, T_A = 0°C
I_{CF2}	Output Clamp Current			13	mA	V_{OUT} = −1.0V, T_A = 25°C
I_{GG}	Gate Supply Current			10	μA	
V_{IL1}	Input Low Voltage for TTL Interface	−1.0		0.65	V	
V_{IL2}	Input Low Voltage for MOS Interface	V_{DD}		V_{CC} −6	V	
V_{IH}	Address and Chip Select Input High Voltage	V_{CC} −2		V_{CC} +0.3	V	
I_{OL}	Output Sink Current	1.6	4		mA	V_{OUT} = 0.45V
V_{OL}	Output Low Voltage		7	0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	3.5			V	I_{OH} = −100 μA

Continuous Operation

Note 1: In the programming mode, the data inputs 1–8 are pins 4–11 respectively. $\overline{CS}$ = GND.
Note 2: Typical values are at nominal voltages and T_A = 25°C.

A.C. Characteristics

T_A = 0° C to +70°C, V_{CC} = +5V ±5%, V_{DD} = -10V ±5%, V_{GG} = -10V ±5% unless otherwise noted

SYMBOL	TEST	MINIMUM	TYPICAL	MAXIMUM	UNIT
Freq.	Repetition Rate			1	MHz
t_{OH}	Previous read data valid			100	ns
t_{ACC}	Address to output delay			1.7	μs
t_{CS}	Chip select delay			800	ns
t_{CO}	Output delay from $\overline{CS}$			900	ns
t_{OD}	Output deselect			300	ns

Capacitance* T_A = 25°C

SYMBOL	TEST	MINIMUM	TYPICAL	MAXIMUM	UNIT	CONDITIONS
C_{IN}	Input Capacitance		8	15	pF	$V_{IN}=V_{CC}$, $CS=V_{CC}$, $V_{OUT}=V_{CC}$, $V_{GG}=V_{CC}$ — All unused pins are at A.C. ground
C_{OUT}	Output Capacitance		10	15	pF	

*This parameter is periodically sampled and is not 100% tested.

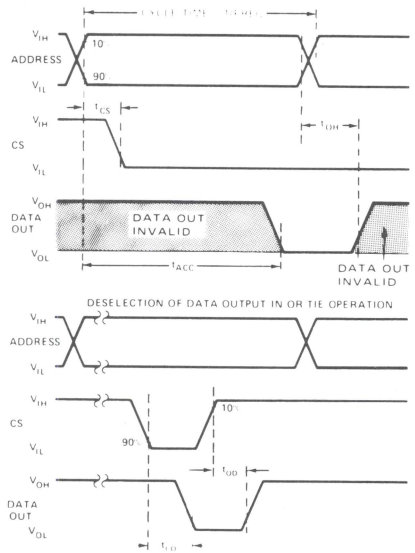
Switching Characteristics

Conditions of Test:

Input pulse amplitudes: 0 to 4V; t_R, t_F ≤50 ns.

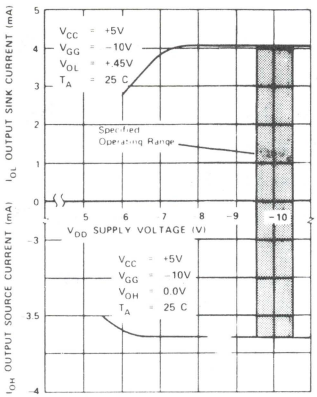
a) For output load = 1 TTL gate; measurements made at output of TTL gate (t_{PD} ≤15 ns)

b) For pure capacitive load of 75pf.

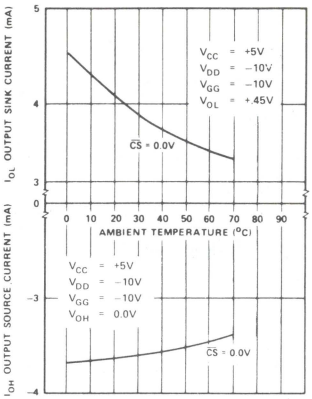


Typical Characteristics

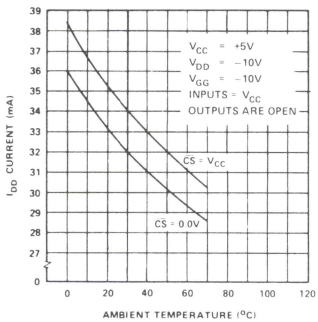
OUTPUT CURRENT VS. V_{DD} SUPPLY VOLTAGE



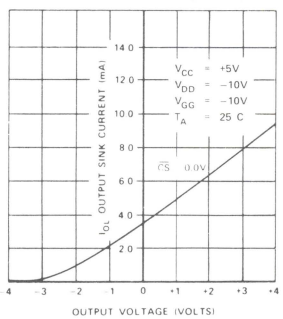
OUTPUT CURRENT VS. TEMPERATURE



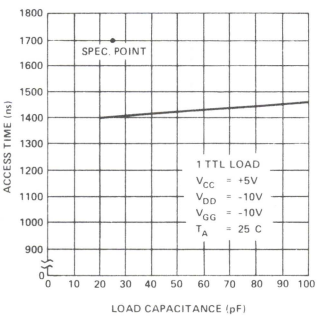
I_{DD} CURRENT VS. TEMPERATURE



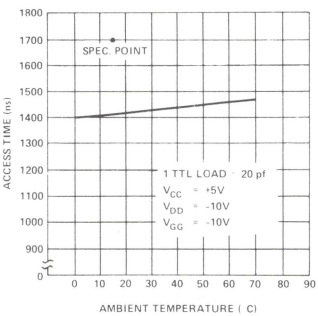
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



ACCESS TIME VS. LOAD CAPACITANCE



ACCESS TIME VS. TEMPERATURE



PROM/ROM

2308/8308*
8K (1K x 8) ROM

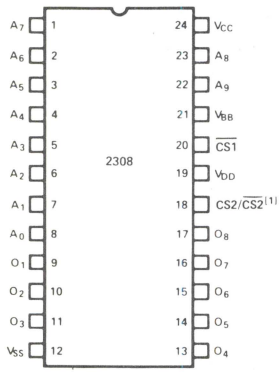
- **Fast Access Time: 450 ns**
- **Standard Power Supplies: +12V, ±5V**
- **TTL Compatible: All Inputs and Outputs**
- **Programmable Chip Select Input for Easy Memory Expansion**
- **Three-State Output: OR-Tie Capability**
- **Fully Decoded: On Chip Address Decode**
- **Inputs Protected: All Inputs Have Protection Against Static Charge**
- **Pin Compatible to 2708 EPROM and 2608 PROM**

The Intel 2308 is a 8192 bit static MOS read only memory organized as 1024 words by 8-bits. This ROM is designed for memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

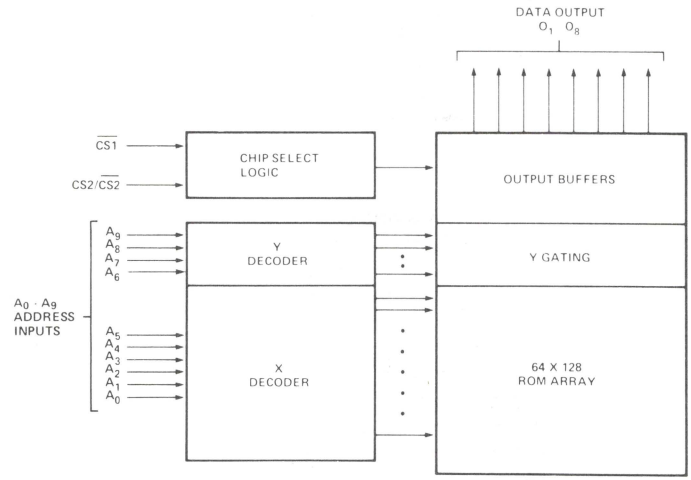
The inputs and outputs are TTL compatible. The chip select input (CS2/$\overline{CS2}$) is programmable. An active high or low level chip select input can be defined by the designer and the desired chip select logic level is fixed at Intel during the masking process. The programmable chip select input, as well as OR-tie compatibility on the outputs, facilitates easy memory expansion. A cost-effective system development program may be implemented by using the Intel 2708 8K UV EPROM for prototyping and the lower cost 2608 PROM and 2308 ROM for production.

The 2308 read only memory is fabricated with N-channel silicon gate technology. This technology provides the designer with high performance, easy-to-use MOS circuits.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

A_0-A_9	ADDRESS INPUTS
O_1-O_8	DATA OUTPUTS
$\overline{CS}_1$	CHIP SELECT INPUT
CS2/$\overline{CS2}$[1]	PROGRAMMABLE CHIP SELECT INPUT

NOTE 1. THE CS2/CS2 LOGIC LEVELS MUST BE SPECIFIED BY THE USER AS EITHER A LOGIC 1 (V_{IH}) OR LOGIC 0 (V_{IL}). A LOGIC 0 SHOULD BE SPECIFIED IN ORDER TO BE COMPATIBLE WITH THE 2708/2608.

***8308 specifications are identical to the 2308 specifications.**

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . -25°C to +85°C
Storage Temperature . . . . . -65°C to +150°C
Voltage On Any Pin With Respect
To V_{BB} . . . . . -0.3V to 20V
Power Dissipation . . . . . 1.0 Watt

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

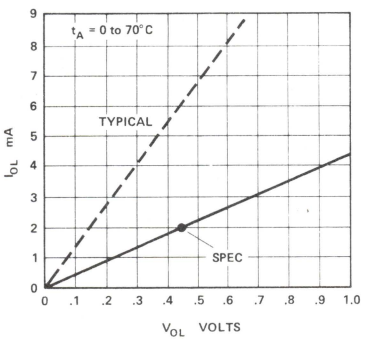
D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5V ±5%; V_{DD} = 12V ±5%, V_{BB} = -5V ±5%, V_{SS} = 0V Unless Otherwise Specified.

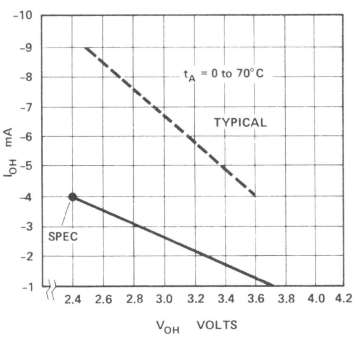
Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[1]	Max.		
I_{LI}	Input Load Current (All Input Pins Except $\overline{CS}_1$)		1	10	μA	V_{IN} = 0 to 5.25V
I_{LCL}	Input Load Current on $\overline{CS}_1$			1.6	mA	V_{IN} = 0.45V
I_{LPC}	Input Peak Load Current on $\overline{CS}_1$			4	mA	0.8V ≤ V_{IN} < 3.3V
I_{LKC}	Input Leakage Current on $\overline{CS}_1$			10	μA	V_{IN} = 3.3V to 5.25V
I_{LO}	Output Leakage Current			10	μA	Chip Deselected
V_{IL}	Input "Low" Voltage	V_{SS}-1		0.8V	V	
V_{IH}	Input "High" Voltage	3.3		V_{CC}+1.0	V	
V_{OL}	Output "Low" Voltage			0.45	V	I_{OL} = 2mA
V_{OH1}	Output "High" Voltage	2.4			V	I_{OH} = -4mA
V_{OH2}	Output "High" Voltage	3.7			V	I_{OH} = -1mA
I_{CC}	Power Supply Current V_{CC}		10	15	mA	
I_{DD}	Power Supply Current V_{DD}		32	60	mA	
I_{BB}	Power Supply Current V_{BB}		10μA	1	mA	
P_D	Power Dissipation		460	840	mW	

NOTE 1: Typical values for T_A = 25° C and nominal supply voltage

D.C. OUTPUT CHARACTERISTICS



D.C. OUTPUT CHARACTERISTICS



A.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5V ±5%; V_{DD} = +12V ±5%, V_{BB} = -5V ±5%, V_{SS} = 0V, Unless Otherwise Specified.

Symbol	Parameter	Limits[2]		Unit
		Typ.	Max.	
t_{ACC}	Address to Output Delay Time	200	450	ns
t_{CO1}	Chip Select 1 to Output Delay Time	85	160	ns
t_{CO2}	Chip Select 2 to Output Delay Time	125	220	ns
t_{DF}	Chip Deselect to Output Data Float Time	125	220	ns

NOTE 2: Refer to conditions of Test for A.C. Characteristics. Add 50 nanoseconds (worst case) to specified values at V_{OH} = 3.7V @ I_{OH} = -1mA, C_L = 100pF.

CONDITIONS OF TEST FOR A.C. CHARACTERISTICS

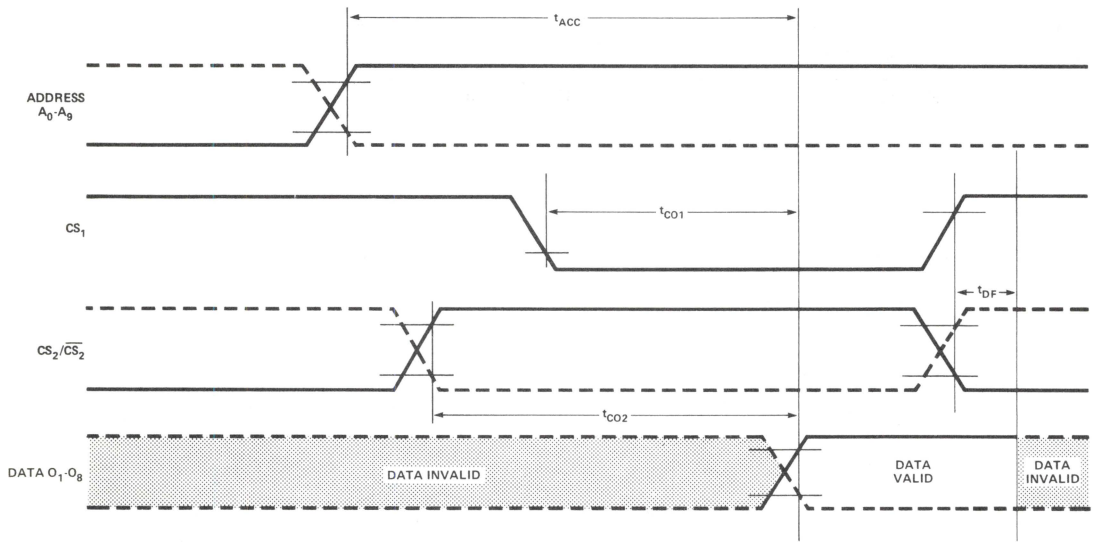
Output Load . . . . . 1 TTL Gate, and C_{LOAD} = 100pF
Input Pulse Levels . . . . . .65V to 3.3V
Input Pulse Rise and Fall Times . . . . . 20 nsec
Timing Measurement Reference Level
. . . . . 2.4V V_{IH}, V_{OH}; 0.8V V_{IL}, V_{OL}

CAPACITANCE*

T_A = 25°C, f = 1 MHz, V_{BB} = -5V, V_{DD}, V_{CC} and all other pins tied to V_{SS}.

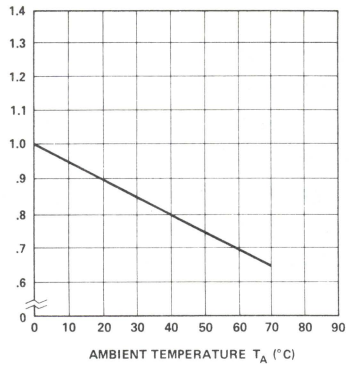
Symbol	Test	Limits	
		Typ.	Max.
C_{IN}	Input Capacitance		6pF
C_{OUT}	Output Capacitance		12pF

*This parameter is periodically sampled and is not 100% tested.

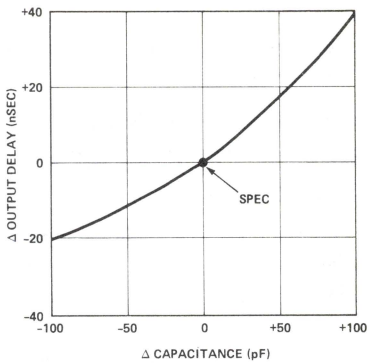


TYPICAL CHARACTERISTICS (Nominal supply voltages unless otherwise noted.)

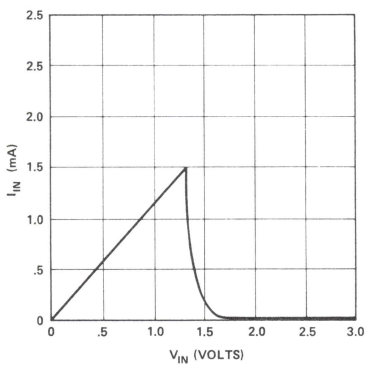
I_{DD} VS. TEMPERATURE (NORMALIZED)



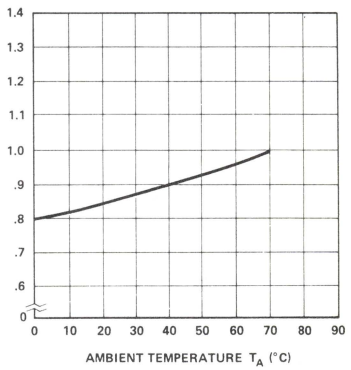
Δ OUTPUT CAPACITANCE VS. Δ OUTPUT DELAY



$\overline{CS}_1$ INPUT CHARACTERISTICS



T_{ACC} VS. TEMPERATURE (NORMALIZED)



PROM/ROM

2316A/4316A/8316A*
16K (2K x 8) ROM

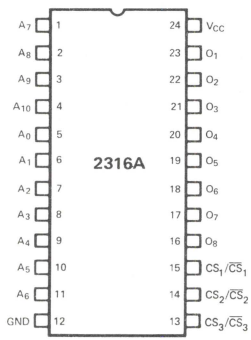
- **Single +5 Volts Power Supply Voltage**
- **Guaranteed 850ns Access Time**
- **Directly TTL Compatible—All Inputs and Outputs**
- **Three Programmable Chip Select Inputs for Easy Memory Expansion**
- **Three-State Output—OR-Tie Capability**
- **Fully Decoded—On Chip Address Decode**
- **Inputs Protected—All Inputs Have Protection Against Static Charge**

The Intel 2316A is a 16,384 bit static MOS read only memory organized as 2048 words by 8 bits. This ROM is designed for memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

The inputs and outputs are fully TTL compatible. This device operates with a single +5V power supply. The three chip select inputs are programmable. Any combination of active high or low level chip select inputs can be defined by the designer and the desired chip select logic level is fixed during the masking process. These three programmable chip select inputs, as well as OR-tie compatibility on the outputs, facilitates easy memory expansion.

The 2316A read only memory is fabricated with N-channel silicon gate technology. This technology provides the designer with high performance, easy-to-use MOS circuits. Only a single +5V power supply is needed and all devices are directly TTL compatible.

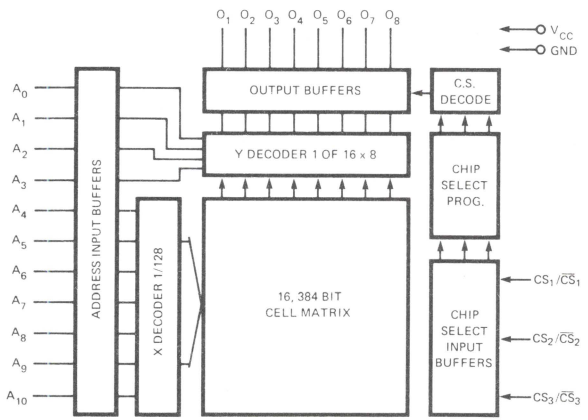
PIN CONFIGURATION



PIN NAMES

A_0-A_{10}	ADDRESS INPUTS
O_1-O_8	DATA OUTPUTS
CS_1-CS_3	PROGRAMMABLE CHIP SELECT INPUTS

BLOCK DIAGRAM



*All 4316A and 8316A specifications are identical to the 2316A specifications.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . -10°C to 80°C
Storage Temperature . . . . . -65°C to +150°C
Voltage On Any Pin With Respect To Ground . . . . . -0.5V to +7V
Power Dissipation . . . . . 1.0 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

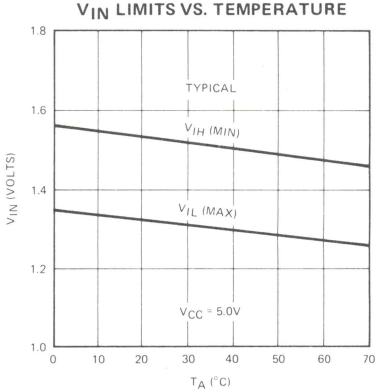
D.C. AND OPERATING CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5V ±5% unless otherwise specified

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.(1)	MAX.		
I_{LI}	Input Load Current (All Input Pins)		1	10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	Output Leakage Current			10	μA	CS = 2.2V, V_{OUT} = 4.0V
I_{LOL}	Output Leakage Current			-20	μA	CS = 2.2V, V_{OUT} = 0.45V
I_{CC}	Power Supply Current		40	98	mA	All inputs 5.25V Data Out Open
V_{IL}	Input "Low" Voltage	-0.5		0.8	V	
V_{IH}	Input "High" Voltage	2.0		V_{CC}+1.0V	V	
V_{OL}	Output "Low" Voltage			0.45	V	I_{OL} = 2.0 mA
V_{OH}	Output "High" Voltage	2.2			V	I_{OH} = -100 μA

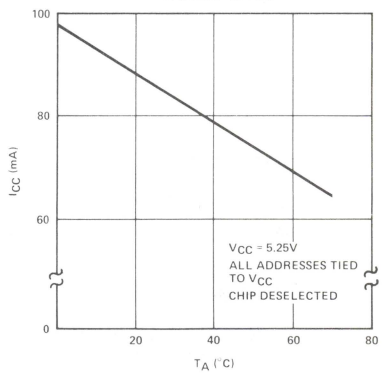
(1) Typical values for T_A = 25°C and nominal supply voltage.

TYPICAL D.C. CHARACTERISTICS

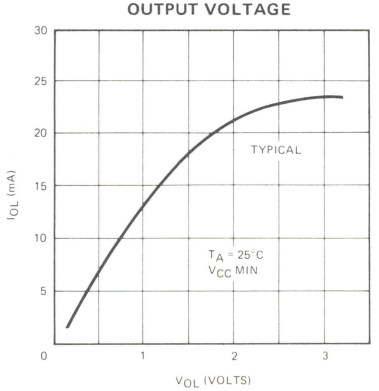
V_{IN} LIMITS VS. TEMPERATURE



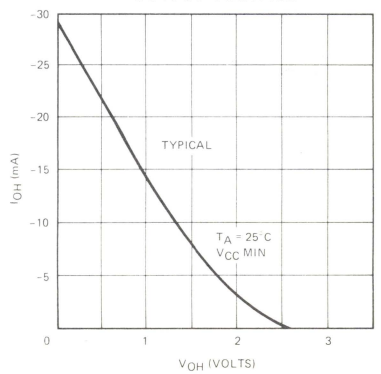
STATIC I_{CC} VS. AMBIENT TEMPERATURE WORST CASE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



A.C. Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$ unless otherwise specified

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.(1)	MAX.	
t_A	Address to Output Delay Time		400	850	nS
t_{CO}	Chip Select to Output Enable Delay Time			300	nS
t_{DF}	Chip Deselect to Output Data Float Delay Time	0		300	nS

CONDITIONS OF TEST FOR A.C. CHARACTERISTICS

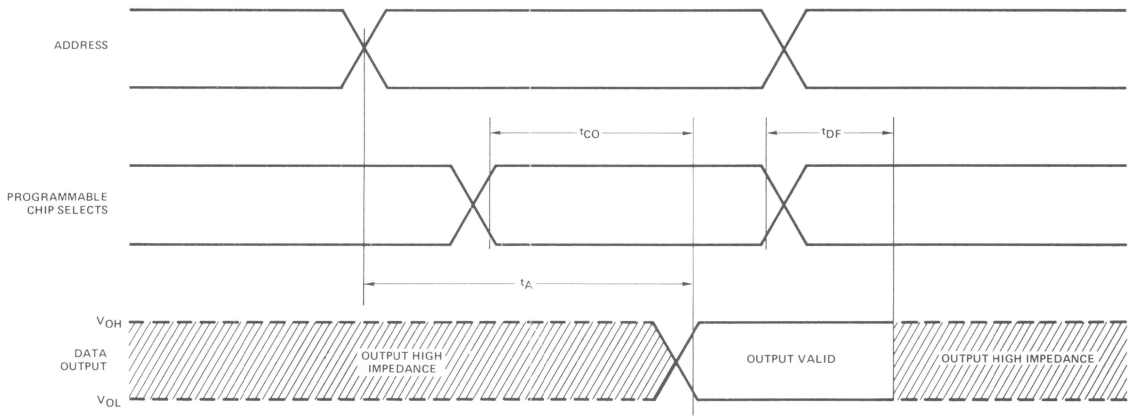
Output Load . . . 1 TTL Gate, and $C_{LOAD} = 100$ pF
Input Pulse Levels . . . . . 0.8 to 2.0V
Input Pulse Rise and Fall Times . (10% to 90%) 20 nS
Timing Measurement Reference Level
Input 1.5V
Output . . . . . 0.45V to 2.2V

CAPACITANCE(2) $T_A = 25°C$, f = 1 MHz

SYMBOL	TEST	LIMITS	
		TYP.	MAX.
C_{IN}	All Pins Except Pin Under Test Tied to AC Ground	4 pF	10 pF
C_{OUT}	All Pins Except Pin Under Test Tied to AC Ground	8 pF	15 pF

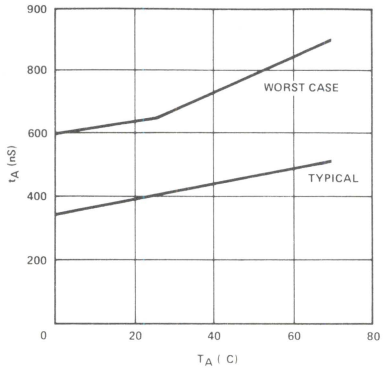
(2) This parameter is periodically sampled and is not 100% tested.

A.C. Waveforms

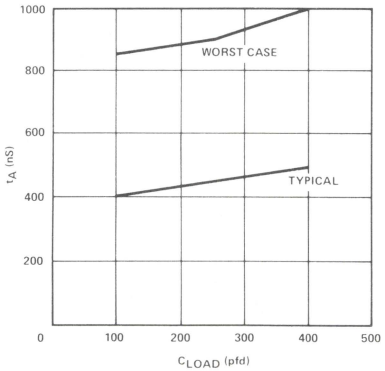


Typical A.C. Characteristics

ACCESS TIME VS. AMBIENT TEMPERATURE



ACCESS TIME VS. LOAD CAPACITANCE



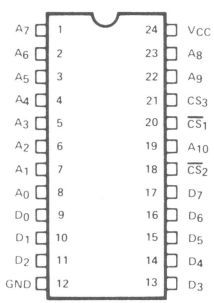
2316E
16K (2K x 8) ROM

- **Fast Access Time—450 ns Max.**
- **Single +5V ± 10% Power Supply**
- **Intel MCS 80 and 85 Compatible**
- **Three Programmable Chip Selects for Simple Memory Expansion and System Interface**
- **EPROM/ROM Pin Compatible for Cost-Effective System Development**
- **Completly Static Operation**
- **Inputs and Outputs TTL Compatible**
- **Three-State Output for Direct Bus Interface**

The Intel® 2316E is a 16,384-bit static, N-channel MOS read only memory (ROM) organized as 2048 words by 8 bits. Its high bit density is ideal for large, non-volatile data storage applications such as program storage. The three-state outputs and TTL input/output levels allow for direct interface with common system bus structures. The 2316E single +5V power supply and 450 ns access time are both ideal for usage with high performance microcomputers such as the Intel MCS™-80 and MCS™-85 devices.

A cost-effective system development program may be implemented by using the pin compatible Intel 2716 16K UV EPROM for prototyping and the lower cost 2616 PROM and 2316E ROM for production. The 2716 is fully compatible to the 2316E in all respects. The three 2316E programmable chip selects may be defined by the user and are fixed during the masking process. To simplify the conversion from 2716 prototyping to 2316E production, it is recommended that the 2316E programmable chip select logic levels be defined the same as that shown in the below data sheet pin configuration. This pin configuration and these chip select logic levels are the same as the 2716.

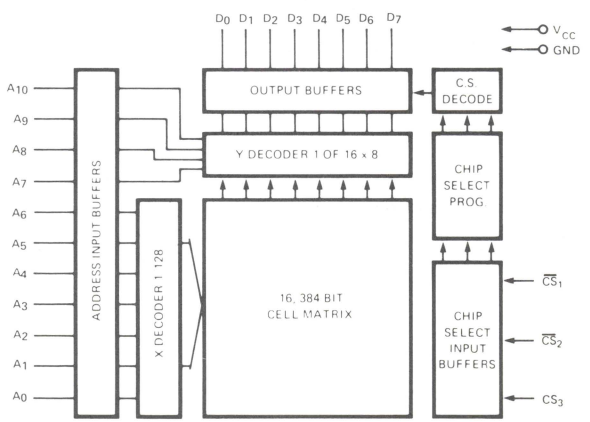
PIN CONFIGURATION



PIN NAMES

A_0–A_{10}	ADDRESS INPUTS
O_7–O_0	DATA OUTPUTS
CS_1–CS_3	CHIP SELECT INPUTS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . .–10°C to 80°C
Storage Temperature . . . . . .–65°C to +150°C
Voltage On Any Pin With Respect
to Ground . . . . . –0.5V to +7V
Power Dissipation . . . . . 1.0 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5V ±10%, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.(1)	MAX.		
I_{LI}	Input Load Current (All Input Pins)			10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	Output Leakage Current			10	μA	Chip Deselected, V_{OUT} = 4.0V
I_{LOL}	Output Leakage Current			–20	μA	Chip Deselected, V_{OUT} = 0.4V
I_{CC}	Power Supply Current		70	120	mA	All Inputs 5.25V Data Out Open
V_{IL}	Input "Low" Voltage	–0.5		0.8	V	
V_{IH}	Input "High" Voltage	2.2		V_{CC}+1.0V	V	
V_{OL}	Output "Low" Voltage			0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output "High" Voltage	2.4			V	I_{OH} =– 400 μA

NOTE: 1. Typical values for T_A = 25°C and nominal supply voltage.

A.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN.	MAX.	
t_A	Address to Output Delay Time		450	ns
t_{CO}	Chip Select to Output Enable Delay Time		120	ns
t_{DF}	Chip Deselect to Output Data Float Delay Time	10	100	ns

CONDITIONS OF TEST FOR A.C. CHARACTERISTICS

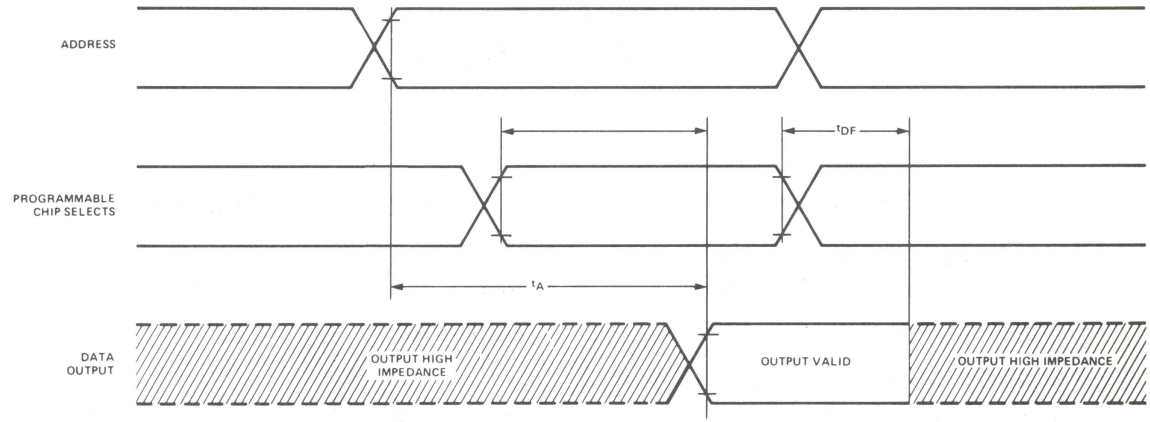
Output Load . . . . . 1 TTL Gate and C_L = 100 pF
Input Pulse Levels . . . . . .0.8 to 2.4V
Input Pulse Rise and Fall Times (10% to 90%) . . . . . 20 ns
Timing Measurement Reference Level
Input . . . . . 1V and 2.2V
Output . . . . . .0.8V and 2.0V

CAPACITANCE(2) T_A = 25°C, f = 1 MHz

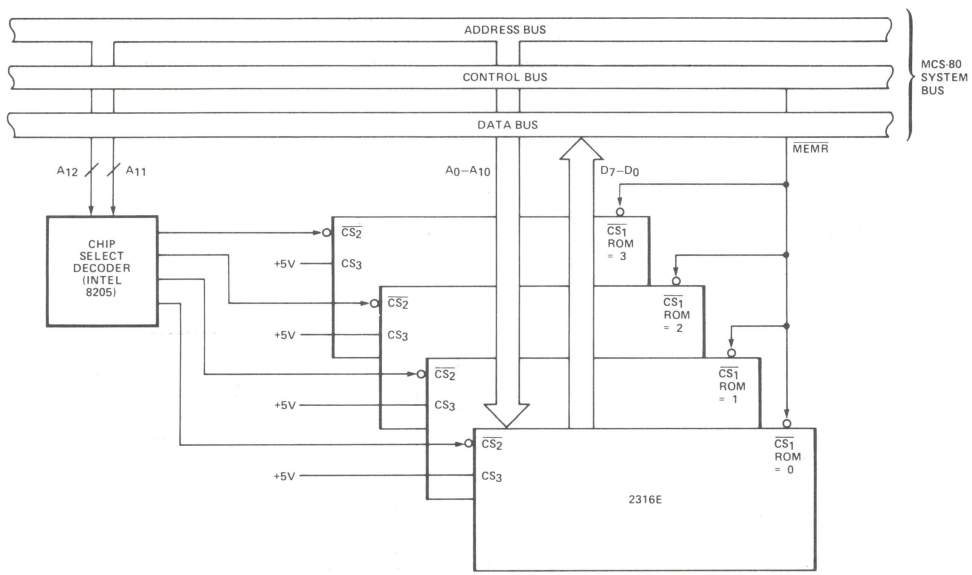
SYMBOL	TEST	LIMITS	
		TYP.	MAX.
C_{IN}	All Pins Except Pin Under Test Tied to AC Ground	5 pF	10 pF
C_{OUT}	All Pins Except Pin Under Test Tied to AC Ground	10 pF	15 pF

NOTE: 2. This parameter is periodically sampled and is not 100% tested.

A.C. Waveforms



Typical System Application (8K × 8 ROM Memory)



MILITARY TEMP.
ADVANCE
INFORMATION
Characteristics are subject to change without notice.

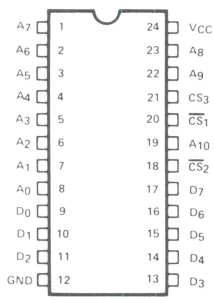
M2316E
16K (2K × 8) ROM

- **Single +5V ± 10% Power Supply**
- **Three Programmable Chip Selects for Simple Memory Expansion and System Interface**
- **EPROM/ROM Pin Compatible for Cost-Effective System Development**
- **Completly Static Operation**
- **Inputs and Outputs TTL Compatible**
- **Three-State Output for Direct Bus Interface**

The Intel® M2316E is a 16,384-bit static, N-channel MOS read-only memory (ROM) organized as 2048 words by 8 Its high bit density is ideal for large, non-volatile data storage applications such as program storage. The three outputs and TTL input/output levels allow for direct interface with common system bus structures. The M2316E sir +5V power supply and fast access time is ideal for usage with high performance microcomputers such as Intel M8080A.

A cost-effective system development program may be implemented by using the pin compatible Intel® M2716 16K UV EPROM for prototyping and the lower cost M2316E ROM for production. The three M2316E programmable chip selects may be defined by the user and are fixed during the masking process. To simplify the conversion from M2716 prototyping to M2316E production, it is recommended that the M2316E programmable chip select logic levels be defined the same as that shown in the below data sheet pin configuration. This pin configuration and these chip select logic levels are the same as the M2716.

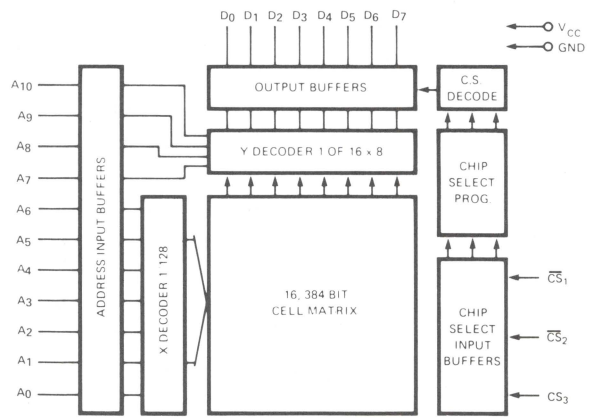
PIN CONFIGURATION



PIN NAMES

A_0–A_{10}	ADDRESS INPUTS
D_7–D_0	DATA OUTPUTS
CS_1–CS_3	CHIP SELECT INPUTS

BLOCK DIAGRAM



ADVANCE INFORMATION
Characteristics are subject to change without notice

2332
32K (4K x 8) ROM

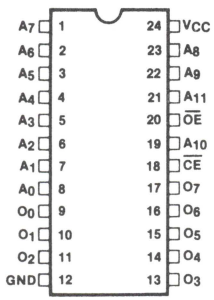
- **Single +5V ± 10% Power Supply**
- **Pin Compatible to Intel® 2716 and 2732 EPROMs**
- **300ns Max. Access Time**
- **Low Power Dissipation:**
  40mA Max. Average Current
  15mA Max. Standby Current
- **Edge Enabled With Static Array**
- **Inputs and Outputs TTL Compatible**
- **Three-State Output for Direct Bus Interface**
- **Output Enable for MCS-85™ and MCS-86™ Compatibility**

The Intel® 2332 is a single +5V supply, 32,768-bit N-channel MOS read only memory organized as 4096 words by 8-bits. It has static memory cells and clocked peripheral circuitry, giving a fast device access time with low active power dissipation. The 2332 features an automatic standby power mode. When deselected by $\overline{CE}$, the active power dissipation is reduced from 40mA to 15mA, a 60% reduction.

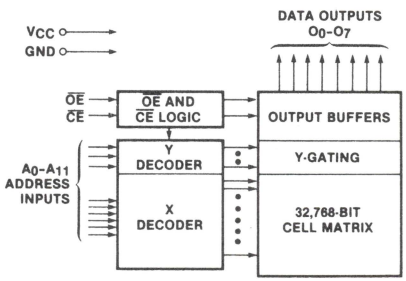
The 2332 is ideal for microprocessor systems, especially those with common input and output bus structures. The separate output control, $\overline{OE}$, eliminates bus contention. The 300ns access time, three-state outputs, address latches, and TTL input/output levels further simplify system design.

A cost effective system development program may be implemented by using the pin compatible Intel® 2732, 32K UV EPROM for prototyping and the 2732 ROM for volume production. The 2732 is fully compatible to the 2332 in all respects.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

A_0-A_{10}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS

ADVANCE INFORMATION
Characteristics are subject to change without notice

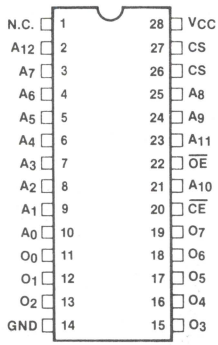
2364
64K (8K × 8) BIT ROM

- **Single +5V ±10% Power Supply**
- **Inputs and Outputs TTL Compatible**
- **Pin Compatible to Intel® 2732 EPROM**
- **Three-State Output for Direct Bus Interface**
- **Low Power Mode**
- **MCS-80 and MCS-85 Compatible**

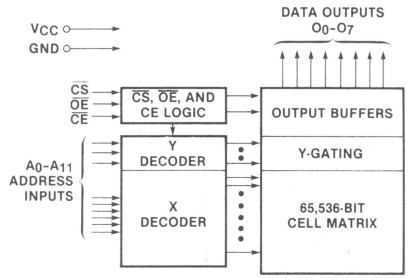
The Intel® 2364 is a single +5V, 65,536-bit N-channel MOS read only memory organized as 8192 words by 8 bits. Its high bit density is ideal for large, non-volatile data storage, such as program storage. The three-state outputs and TTL input/output levels allow for direct interface with common bus structures. The 2364 has a low power mode which reduces the active power dissipation by over 50%.

A cost-effective system development program may be implemented by using the Intel® 2732 32K UV EPROM for prototyping and the 2364 ROM for production. The lower 24 pins of the 2364 are the same as the 2732 to facilitate board designs in making the transition from EPROM to ROM.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

A_0-A_{12}	ADDRESSES
$\overline{OE}$	OUTPUT ENABLE
$\overline{CE}$	CHIP ENABLE
CS	CHIP SELECT
N.C.	NO CONNECTION

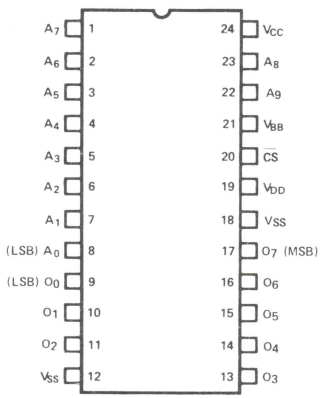
2608
8K (1K x 8) FACTORY PROGRAMMABLE PROM

- **Fast Access Time — 450 ns Max.**
- **Pin Compatible to 2708 EPROM and 2308 ROM**
- **Static — No Clocks Required**
- **Data Inputs and Outputs TTL Compatible**
- **Three-State Outputs — OR-Tie Capability**

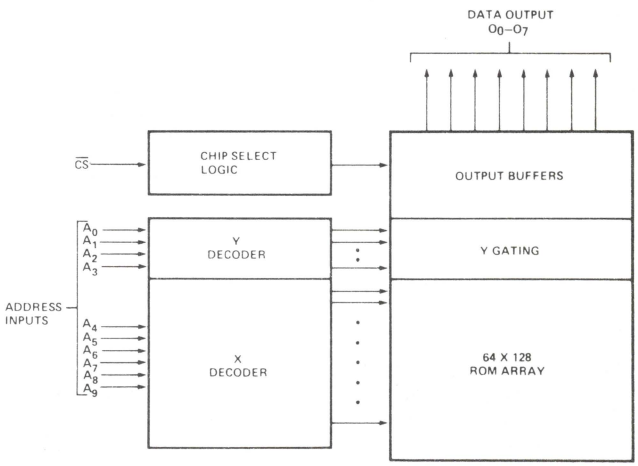
The Intel® 2608 is a 8192-bit, one-time factory-programmable MOS PROM organized as 1K words by 8 bits. The electrical characteristics are specified over the 0°C to 70°C operating temperature range with 5% power supply variation. The 2608 features are ideally suited for microprocessor systems: 450 ns maximum access time, three-state outputs for common bussing, and TTL inputs/outputs for easy interfacing.

A cost-effective system development program may be implemented by using the Intel® 2708 EPROM for pattern experimentation, the 2608 for first incremental 2308 ROM delivery and the 2308 for volume production. The 2608 is fully compatible to the 2708 in all respects. The fast factory 2608 code pattern turnaround time gives a rapid transition from EPROM to ROM for production.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

A_0-A_9	ADDRESS INPUTS
O_1-O_8	DATA OUTPUTS/INPUTS
$\overline{CS}$	CHIP SELECT/WRITE ENABLE INPUT

MODE SELECTION

	PIN NUMBER						
MODE	DATA I/O 9-11 13-17	ADDRESS INPUTS 1-8, 22,23	V_{SS} 12	V_{DD} 19	$\overline{CS}$ 20	V_{BB} 21	V_{CC} 24
READ	D_{OUT}	A_{IN}	GND	+12	V_{IL}	-5	+5
DESELECT	HIGH IMPEDANCE	DON'T CARE	GND	+12	V_{IH}	-5	+5

Absolute Maximum Ratings*

Temperature Under Bias	-25°C to +85°C
Storage Temperature	-65°C to +125°C
V_{DD} With Respect to V_{BB}	+20V to -0.3V
V_{CC} and V_{SS} With Respect to V_{BB}	+15V to -0.3V
All Input or Output Voltages With Respect to V_{BB}	+15V to -0.3V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = +12V ±5%, V_{BB}[1] = -5V ±5%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Min.	Typ.[2]	Max.	Unit	Conditions
I_{LI}	Address and Chip Select Input Sink Current		1	10	μA	V_{IN} = 5.25V or V_{IN} = V_{IL}
I_{LO}	Output Leakage Current		1	10	μA	V_{OUT} = 5.5V, $\overline{CS}$/WE = 5V
I_{DD}[3]	V_{DD} Supply Current		50	65	mA	Worst Case Supply Currents:
I_{CC}[3]	V_{CC} Supply Current		6	10	mA	All Inputs High
I_{BB}[3]	V_{BB} Supply Current		30	45	mA	$\overline{CS}$/WE = 5V; T_A = 0°C
V_{IL}	Input Low Voltage	V_{SS}		0.65	V	
V_{IH}	Input High Voltage	3.0		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.6mA
V_{OH1}	Output High Voltage	3.7			V	I_{OH} = -100μA
V_{OH2}	Output High Voltage	2.4			V	I_{OH} = -1mA
P_D	Power Dissipation			800	mW	T_A = 70°C

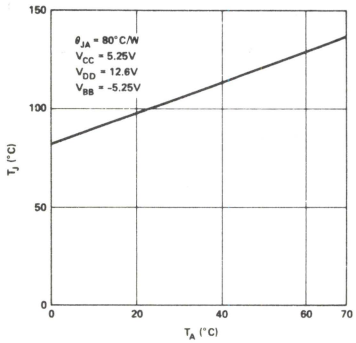
NOTES: 1. V_{BB} must be applied prior to V_{CC} and V_{DD}. V_{BB} must also be the last power supply switched off.

2. Typical values are for T_A = 25°C and nominal supply voltages.

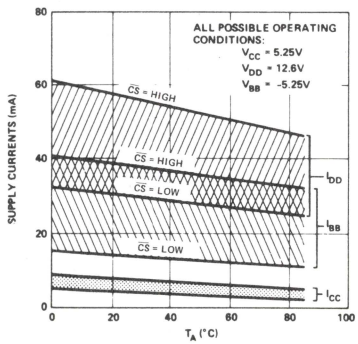
3. The total power dissipation is specified at 800 mW. It is not calculated by summing the various currents (I_{DD}, I_{CC}, and I_{BB}) multiplied by their respective voltages since current paths exist between the various power supplies and V_{SS}. The I_{DD}, I_{CC}, and I_{BB} currents should be used to determine power supply capacity only.

Typical Characteristics

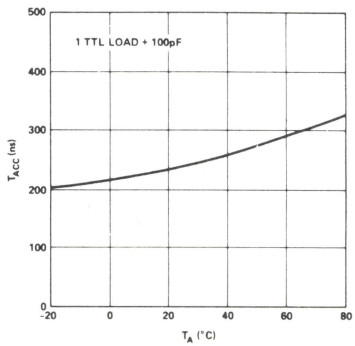
MAXIMUM JUNCTION TEMPERATURE VS. AMBIENT TEMPERATURE



RANGE OF SUPPLY CURRENTS VS. TEMPERATURE



ACCESS TIME VS. TEMPERATURE



A. C. Characteristics

$T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 5\%$, $V_{DD} = +12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$, unless otherwise noted.

Symbol	Parameter	Limits			Units
		Min.	Typ.	Max.	
t_{ACC}	Address to Output Delay		280	450	ns
t_{CO}	Chip Select to Output Delay		60	120	ns
t_{DF}	Chip Deselect to Output Float	0		120	ns
t_{OH}	Address to Output Hold	0			ns

CAPACITANCE[1] $T_A = 25°C$, f = 1 MHz

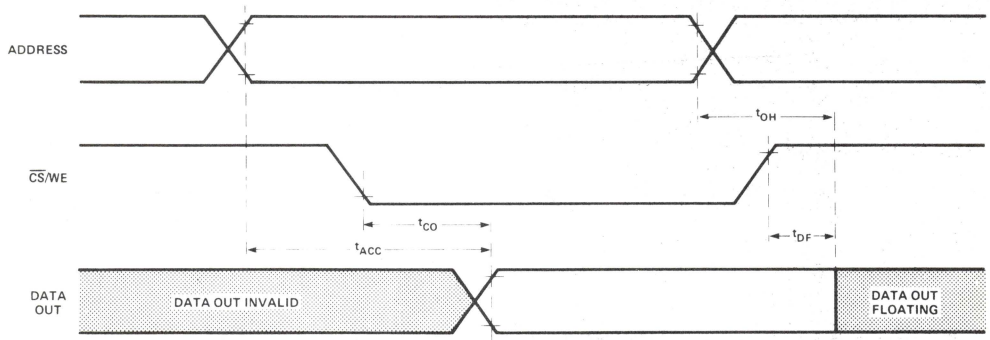
Symbol	Parameter	Typ.	Max.	Unit.	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

Note: 1. This parameter is periodically sampled and is not 100% tested.

A.C. TEST CONDITIONS:

Output Load: 1 TTL gate and $C_L = 100$ pF
Input Rise and Fall Times: ≤20 ns
Timing Measurement Reference Levels: 0.8V and 2.8V for inputs; 0.8V and 2.4V for outputs.
Input Pulse Levels: 0.65V to 3.0V

Waveforms



2616*
16K (2K x 8) FACTORY PROGRAMMABLE PROM

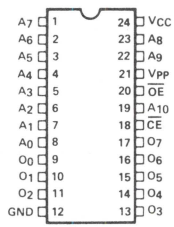
- **Single +5V Power Supply**
- **Low Power Dissipation**
  - **525 mW Max. Active Power**
  - **132 mW Max. Standby Power**
- **Pin Compatible to Intel® 2716 EPROM and 2316E ROM**
- **Fast Access Time — 450 ns Max.**
- **Inputs and Outputs TTL Compatible**
- **Completely Static**

The Intel® 2616 is a 16,384-bit, one-time factory-programmable MOS PROM organized as 2048 words by 8 bits. The 2616 operates from a single +5V power supply, has a static standby mode, and is TTL input/output compatible. It is specified over the 0°C to 70°C operating temperature with 5% power supply variation.

A cost-effective system development program may be implemented quickly into production by using the Intel® 2716 EPROM for pattern experimentation, the 2616 for fast first incremental 2316E ROM delivery, and the 2316E for volume production. The 2616 is fully compatible to the 2716 in all respects. The fast factory 2616 code pattern turnaround time gives rapid transition from EPROM to ROM for production.

The 2616 has a static standby mode which reduces the power dissipation without increasing access time. The maximum active power dissipation is 525 mW, while the maximum standby power dissipation is only 132 mW — a 75% saving.

PIN CONFIGURATION*



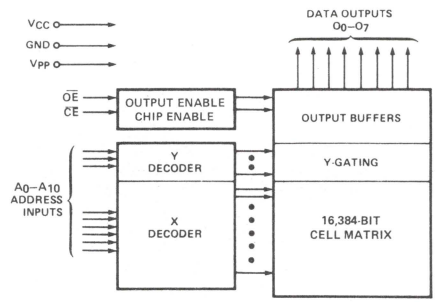
MODE SELECTION

MODE \ PINS	CE (18)	OE (20)	VPP (21)	VCC (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z

PIN NAMES

A_0–A_9	ADDRESSES
$\overline{CE}$/PGM	CHIP ENABLE/PROGRAM
$\overline{OE}$	OUTPUT ENABLE
O_0–O_7	OUTPUTS

BLOCK DIAGRAM



Pin 18 and pin 20 have been named to conform with the entire family of 16K, 32K, and 64K EPROMs and ROMs.

Absolute Maximum Ratings*

Temperature Under Bias . . . . . -10°C to +80°C
Storage Temperature . . . . . -65°C to +125°C
All Input or Output Voltages with
Respect to Ground . . . . . +6V to -0.3V

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION

D.C. and Operating Characteristics

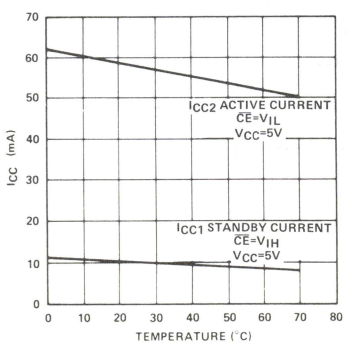
T_A = 0°C to 70°C, V_{CC}[1,2] = +5V ±5%, V_{PP}[2] = V_{CC} ±0.6V

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[3]	Max.		
I_{LI}	Input Load Current			10	μA	V_{IN} = 5.25V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 5.25V
I_{PP1}[2]	V_{PP} Current			5	mA	V_{PP} = 5.85V
I_{CC1}[2]	V_{CC} Current (Standby)		10	25	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}
I_{CC2}[2]	V_{CC} Current (Active)		57	100	mA	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
V_{IL}	Input Low Voltage	-0.1		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -400 μA

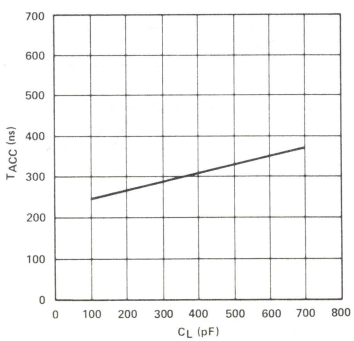
NOTES: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC}. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for T_A = 25°C and nominal supply voltages.

Typical Characteristics

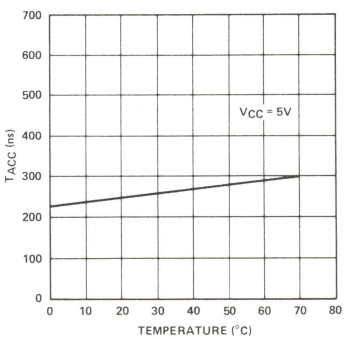
I_{CC} CURRENT vs. TEMPERATURE



ACCESS TIME vs. CAPACITANCE



ACCESS TIME vs. TEMPERATURE



A.C. Characteristics

$T_A = 0°C$ to $70°C$, V_{CC}[1] = +5V ±5%, V_{PP}[2] = V_{CC} ±0.6V

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[4]	Max.		
t_{ACC}	Address to Output Delay		250	450	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay Delay		280	450	ns	$\overline{OE} = V_{IL}$
t_{OE}	Output Enable to Output Delay			120	ns	$\overline{CE} = V_{IL}$
t_{DF}	Output Enable High to Output Float	0		100	ns	$\overline{CE} = V_{IL}$
t_{OH}	Address to Output Hold	0			ns	$\overline{CE} = \overline{OE} = V_{IL}$

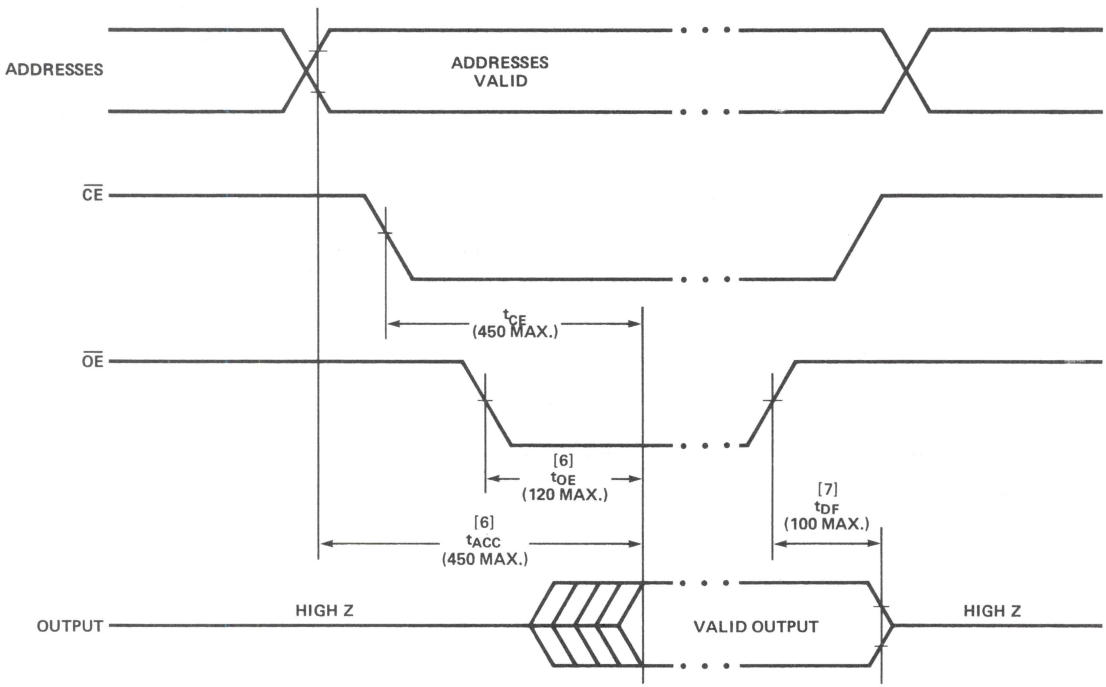
Capacitance[4] $T_A = 25°C$, f = 1 MHz

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

A.C. Test Conditions:

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤20 ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

A.C. Waveforms[5]



NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously of after V_{PP}.
2. V_{PP} may be connected directly to V_{CC}. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for $T_A = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested.
5. All times shown in praentheses are minimum times and are nsec unless otherwise specified.
6. $\overline{OE}$ may be delayed up to 330ns after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
7. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

DEVICE OPERATION

The modes of operation of the 2616 are listed in Table I. It should be noted that all inputs are at TTL levels. Only a single +5V power supply is required since V_{PP} may be connected to V_{CC}.

TABLE I. MODE SELECTION

MODE \ PINS	$\overline{CE}$ (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z

READ MODE

The 2616 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs 120 ns (t_{OE}) after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The 2616 has a standby mode which reduces the active power dissipation by 75%, from 525 mW to 132 mW. The 2616 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedence state, independent of the $\overline{OE}$ input.

OUTPUT DESELECTION

The outputs of two or more 2616s may be OR-tied together on the same data bus. Only one 2616 should have its output selected ($\overline{OE}$ low) to prevent data bus contention between 2616s in this configuration. The outputs of the other 2616s should be deselected by raising the $\overline{OE}$ input to a TTL high level.

2708/8708*
8K AND 4K UV ERASABLE PROM

	Max. Power	Max. Access	Organization
2708	800 mW	450 ns	1K x 8
2708L	425 mW	450 ns	1K x 8
2708-1	800 mW	350 ns	1K x 8
2704	800 mW	450 ns	512 x 8

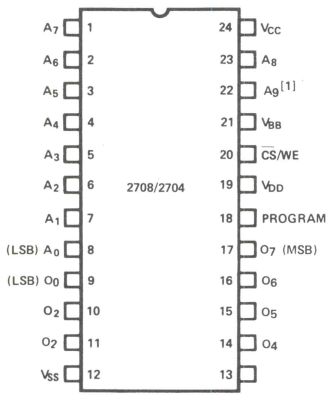
- **Low Power Dissipation — 425 mW Max. (2708L)**
- **Fast Access Time — 350 ns Max. (2708-1)**
- **Pin Compatible to Intel® 2308 ROM**
- **Static — No Clocks Required**
- **Data Inputs and Outputs TTL Compatible during both Read and Program Modes**
- **Three-State Outputs — OR-Tie Capability**

The Intel® 2708 is a 8192-bit ultraviolet light erasable and electrically reprogrammable EPROM, ideally suited where fast turnaround and pattern experimentation are important requirements. All data inputs and outputs are TTL compatible during both the read and program modes. The outputs are three-state, allowing direct interface with common system bus structures. A pin-for-pin mask programmed ROM, the Intel® 2308, is available for large volume production runs of systems initially using the 2708.

The 2708L at 425 mW is available for systems requiring lower power dissipation than from the 2708. A power dissipation savings of over 50%, without any sacrifice in speed, is obtained with the 2708L. The 2708L has high input noise immunity and is specified at 10% power supply tolerance. A high-speed 2708-1 is also available at 350 ns for microprocessors requiring fast access times. For smaller size systems there is the 4096-bit 2704 which is organized as 512 words by 8 bits. All these devices have the same programming and erasing specifications of the 2708. The 2704 electrical specifications are the same as the 2708.

The 2708 family is fabricated with the N-channel silicon gate FAMOS technology and is available in a 24-pin dual in-line package.

PIN CONFIGURATION

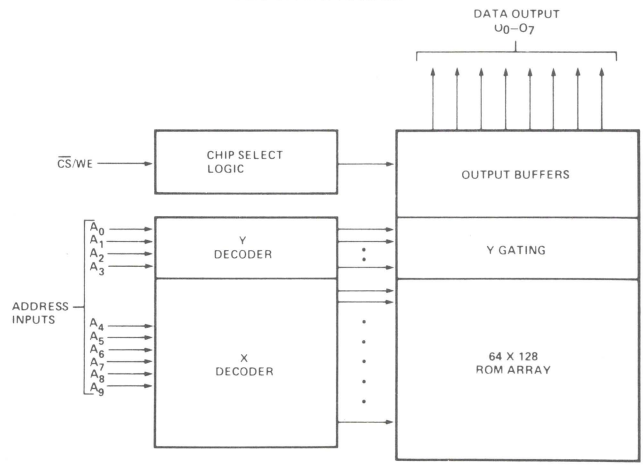


NOTE 1: PIN 22 MUST BE CONNECTED TO V_{SS} FOR THE 2704.

PIN NAMES

A_0-A_9	ADDRESS INPUTS
O_1-O_8	DATA OUTPUTS/INPUTS
$\overline{CS}$/WE	CHIP SELECT/WRITE ENABLE INPUT

BLOCK DIAGRAM



PIN CONNECTION DURING READ OR PROGRAM

	PIN NUMBER							
MODE	DATA I/O 9-11, 13-17	ADDRESS INPUTS 1-8, 22, 23	V_{SS} 12	PROGRAM 18	V_{DD} 19	$\overline{CS}$/WE 20	V_{BB} 21	V_{CC} 24
READ	D_{OUT}	A_{IN}	GND	GND	+12	V_{IL}	-5	+5
DESELECT	HIGH IMPEDANCE	DON'T CARE	GND	GND	+12	V_{IH}	-5	+5
PROGRAM	D_{IN}	A_{IN}	GND	PULSED 26V	+12	V_{IHW}	-5	+5

***All 8708 specifications are identical to the 2708 specifications.**

PROGRAMMING

The programming specifications are described in the PROM/ROM Programming Instructions on page 4-83.

Absolute Maximum Ratings*

Temperature Under Bias	−25°C to +85°C
Storage Temperature	−65°C to +125°C
V_{DD} With Respect to V_{BB}	+20V to −0.3V
V_{CC} and V_{SS} With Respect to V_{BB}	+15V to −0.3V
All Input or Output Voltages With Respect to V_{BB} During Read	+15V to −0.3V
$\overline{CS}$/WE Input With Respect to V_{BB} During Programming	+20V to −0.3V
Program Input With Respect to V_{BB}	+35V to −0 3V
Power Dissipation	1.5W

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PROM/ROM

DC and AC Operating Conditions During Read

	2708	2708-1	2708L
Temperature Range	0°C – 70°C	0°C – 70°C	0°C – 70°C
V_{CC} Power Supply	5V ± 5%	5V ± 5%	5V ± 10%
V_{DD} Power Supply	12V ± 5%	12V ± 5%	12V ± 10%
V_{BB} Power Supply	−5V ± 5%	−5V ± 5%	−5V ± 10%

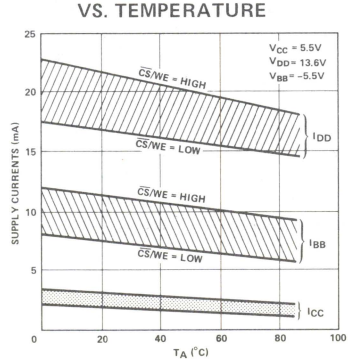
READ OPERATION

D.C. and Operating Characteristics

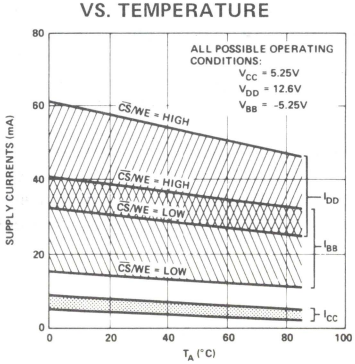
Symbol	Parameter	2708, 2708-1 Limits			2708L Limits			Units	Test Conditions
		Min.	Typ.[2]	Max.	Min.	Typ.[2]	Max.		
I_{LI}	Address and Chip Select Input Sink Current		1	10		1	10	μA	V_{IN} = 5.25V or V_{IN} = V_{IL}
I_{LO}	Output Leakage Current		1	10		1	10	μA	V_{OUT} = 5.5V, CS/WE = 5V
I_{DD}[3]	V_{DD} Supply Current		50	65		21	28	mA	Worst Case Supply Currents[4]: All Inputs High; $\overline{CS}$/WE = 5V; T_A = 0°C
I_{CC}[3]	V_{CC} Supply Current		6	10		2	4	mA	
I_{BB}[3]	V_{BB} Supply Current		30	45		10	14	mA	
V_{IL}	Input Low Voltage	V_{SS}		0.65	V_{SS}		0.65	V	
V_{IH}	Input High Voltage	3.0		V_{CC}+1	2.2		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45			0.4	V	I_{OL} = 1.6mA (2708, 2708-1)
									I_{OL} = 2mA (2708L)
V_{OH1}	Output High Voltage	3.7			3.7			V	I_{OH} = −100 μA
V_{OH2}	Output High Voltage	2.4			2.4			V	I_{OH} = −1 mA
PD	Power Dissipation			800			325	mW	T_A = 70°C
							425	mW	T_A = 0°C

NOTES:
1. V_{BB} must be applied prior to V_{CC} and V_{DD}. V_{BB} must also be the last power supply switched off
2. Typical values are for T_A = 25°C and nominal supply voltages.
3. The total power disiipation is not calculated by summing the various currents (I_{DD}, I_{CC}, and I_{BB}) multiplied by their respective voltages since current paths exist between the various power supplies and V_{SS}. The I_{DD}, I_{CC}, and I_{BB} currents should be used to determine power supply capacity only.
4. I_{BB} for the 2708L is specified in the programmed state and is 18 mA maximum in the unprogrammed state.

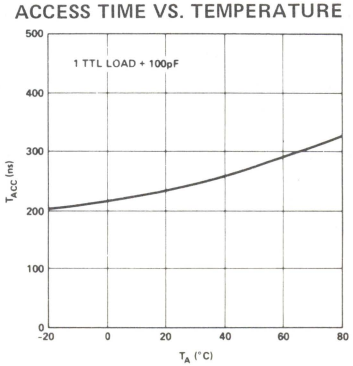
2708L RANGE OF SUPPLY CURRENTS VS. TEMPERATURE



2708 AND 2708-1 RANGE OF SUPPLY CURRENTS VS. TEMPERATURE



ACCESS TIME VS. TEMPERATURE



A. C. Characteristics

Symbol	Parameter	2708-1 Limits Min.	Typ.	Max.	2708, 2708L, Limits Min.	Typ.	Max.	Units
t_{ACC}	Address to Output Delay		280	350		280	450	ns
t_{CO}	Chip Select to Output Delay		60	120		60	120	ns
t_{DF}	Chip Deselect to Output Float	0		120	0		120	ns
t_{OH}	Address to Output Hold	0			0			ns

CAPACITANCE[1] $T_A = 25°C$, f = 1 MHz

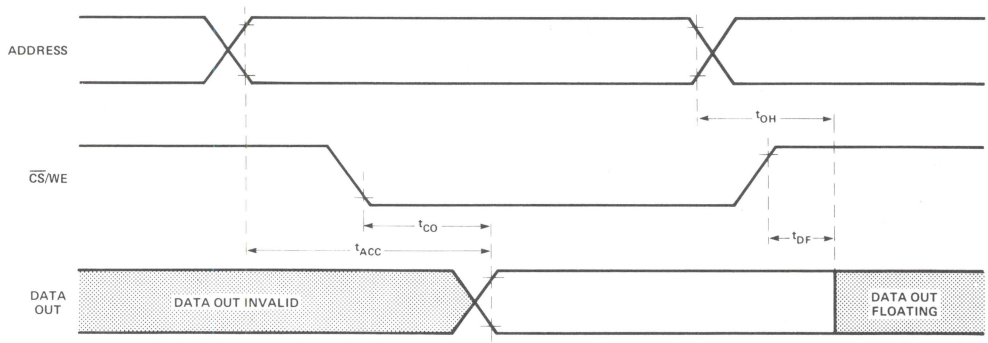
Symbol	Parameter	Typ.	Max.	Unit.	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

Note: 1. This parameter is periodically sampled and is not 100% tested.

A.C. TEST CONDITIONS:

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤20 ns
Timing Measurement Reference Levels: 0.8V and 2.8V for inputs; 0.8V and 2.4V for outputs.
Input Pulse Levels: 0.65V to 3.0V

Waveforms



ERASURE CHARACTERISTICS

The erasure characteristics of the 2708 family are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical device in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the 2708 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available form Intel which should be placed over the 2708 window to prevent unintentional erasure.

The recommended erasure procedure (see page 4-83) for the 2708 family is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The device should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

EXTENDED TEMP. RANGE

M2708
8K (1K x 8) UV ERASABLE PROM

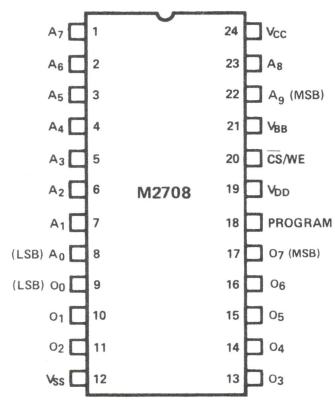
- **Extended Temperature Range: -55° C to 100° C**
- **Fast Programming: Typ. 100 sec. For All 8K Bits**
- **Low Power During Programming**
- **Access Time: 450 ns Max.**
- **Standard Power Supplies: +12V, +5V, -5V**
- **Static: No Clocks Required**
- **Inputs and Outputs TTL Compatible During Both Read and Program Modes**
- **Three-State Output: OR-Tie Capability**
- **Hermetic Package: 24 Pin DIP**

The Intel M2708 is a high speed 8192 bit erasable and electrically reprogrammable ROM (EPROM) ideally suited where fast turn around and pattern experimentation are important requirements.

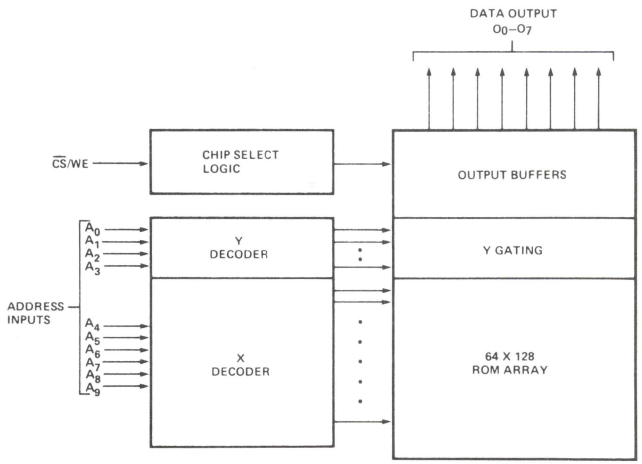
The M2708 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the devices.

The M2708 is fabricated with the time proven N-channel silicon gate technology.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

A_0-A_9	ADDRESS INPUTS
O_1-O_8	DATA OUTPUTS
$\overline{CS}$/WE	CHIP SELECT/WRITE ENABLE INPUT

PIN CONNECTION DURING READ OR PROGRAM

	PIN NUMBER							
MODE	DATA I/O 9-11, 13-17	ADDRESS INPUTS 1-8, 22, 23	V_{SS} 12	PROGRAM 18	V_{DD} 19	$\overline{CS}$/WE 20	V_{BB} 21	V_{CC} 24
READ	D_{OUT}	A_{IN}	GND	GND	+12	V_{IL}	-5	+5
DESELECT	HIGH IMPEDANCE	DON'T CARE	GND	GND	+12	V_{IH}	-5	+5
PROGRAM	D_{IN}	A_{IN}	GND	PULSED V_{IHP}	+12	V_{IHW}	-5	+5

EXTENDED TEMP. RANGE

Absolute Maximum Ratings*

Temperature Under Bias	-65°C to 110°C
Storage Temperature	-65°C to +125°C
V_{DD} With Respect to V_{BB}	+20V to -0.3V
V_{CC} and V_{SS} With Respect to V_{BB}	+15V to -0.3V
All Input or Output Voltages With Respect to V_{BB} During Read	+15V to -0.3V
$\overline{CS}$/WE Input With Respect to V_{BB} During Programming	+20V to -0.3V
Program Input With Respect to V_{BB}	+35V to -0 3V
Power Dissipation	1.8W

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION

D.C. and Operating Characteristics

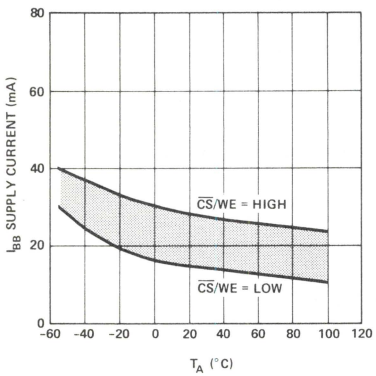
T_A = -55°C to 100°C, V_{CC} = +5V ±10%, V_{DD} = +12V ±10%, V_{BB}[1] = -5V ±10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Min.	Typ.[2]	Max.	Unit	Conditions
I_{LI}	Address and Chip Select Input Sink Current		1	10	μA	V_{IN} = 5.5 V or V_{IN} = V_{IL}
I_{LO}	Output Leakage Current		1	10	μA	V_{OUT} = 5.5 V, $\overline{CS}$/WE = 5V
I_{DD}[3]	V_{DD} Supply Current		50	80	mA	Worst Case Supply Currents:
I_{CC}[3]	V_{CC} Supply Current		6	15	mA	All Inputs High
I_{BB}[3]	V_{BB} Supply Current		30	60	mA	$\overline{CS}$/WE = 5V; T_A = -55°C
V_{IL}	Input Low Voltage	V_{SS}		0.65	V	
V_{IH}	Input High Voltage	3.0		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.6mA
V_{OH1}	Output High Voltage	3.7			V	I_{OH} = -100μA
V_{OH2}	Output High Voltage	2.4			V	I_{OH} = -1mA
P_D	Power Dissipation			750	mW	T_A = 100°C

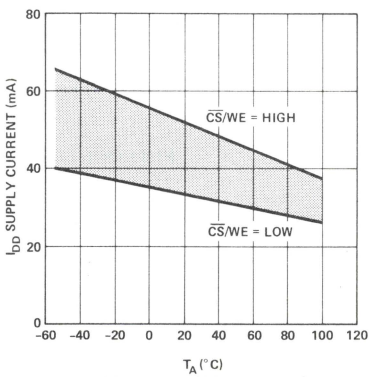
NOTES:
1. V_{BB} must be applied prior to V_{CC} and V_{DD}. V_{BB} must also be the last power supply switched off.
2. Typical values are for T_A = 25°C and nominal supply voltages.
3. The total power dissipation of the 2704/2708 is specified at 750 mW. It is not calculated by summing the various currents (I_{DD}, I_{CC}, and I_{BB}) multiplied by their respective voltages since current paths exist between the various power supplies and V_{SS}. The I_{DD}, I_{CC}, and I_{BB} currents should be used to determine power supply capacity only.

Typical D.C. Characteristics

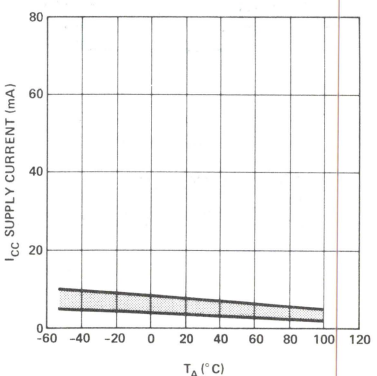
I_{BB} CURRENT VS. TEMPERATURE



I_{DD} CURRENT VS. TEMPERATURE



I_{CC} CURRENT VS. TEMPERATURE



EXTENDED TEMP. RANGE

A.C. Characteristics

T_A = -55°C to 100°C, V_{CC} = +5V ±10%, V_{DD} = +12V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{ACC}	Address to Output Delay		280	450	ns
t_{CO}	Chip Select to Output Delay		60	120	ns
t_{DF}	Chip De-Select to Output Float	0		120	ns
t_{OH}	Address to Output Hold	0			ns

Capacitance[1] T_A = 25°C, f = 1MHz

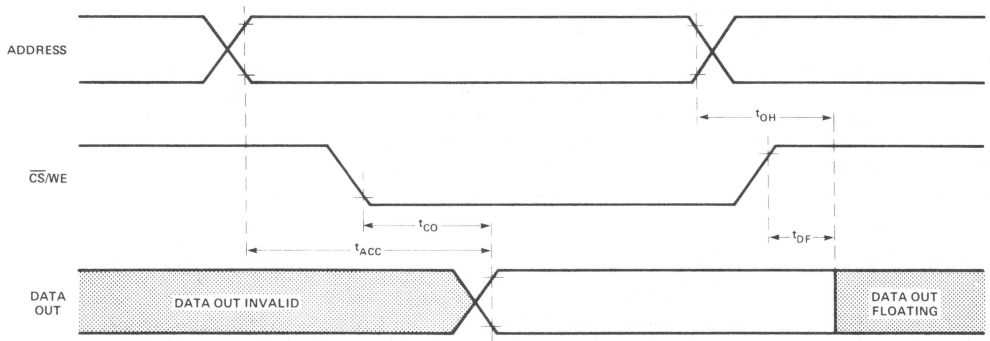
Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	V_{IN}=0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT}=0V

Note 1. This parameter is sampled and not 100% tested.

A.C. TEST CONDITIONS:

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤20 ns
Timing Measurement Reference Levels: 0.8V and 2.8V for inputs; 0.8V and 2.4V for outputs
Input Pulse Levels: 0.65V to 3.0V

Waveforms



ERASURE CHARACTERISTICS

The erasure characteristics of the M2708 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical M2708 in approximately 3 years, while it would take approximatley 1 week to cause erasure when exposed to direct sunlight. If the M2708 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the M2708 window to prevent unintentional erasure.

The recommended erasure procedure (see page 4-83) for the M2708 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The M2708 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

2716*
16K (2K x 8) UV ERASABLE PROM

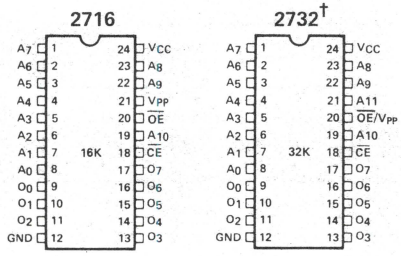
- **Fast Access Time**
  - **— 350 ns Max. 2716-1**
  - **— 390 ns Max. 2716-2**
  - **— 450 ns Max. 2716**
- **Single +5V Power Supply**
- **Low Power Dissipation**
  - **— 525 mW Max. Active Power**
  - **— 132 mW Max. Standby Power**
- **Pin Compatible to Intel® 5V ROMs (2316E, 2332, and 2364) and 2732 EPROM**
- **Simple Programming Requirements Single Location Programming Programs with One 50 ms Pulse**
- **Inputs and Outputs TTL Compatible during Read and Program**
- **Completely Static**

The Intel® 2716 is a 16,384-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2716 operates from a single 5-volt power supply, has a static standby mode, and features fast single address location programming. It makes designing with EPROMs faster, easier and more economical. For production quantities, the 2716 user can convert rapidly to Intel's pin-for-pin compatible 16K ROM (the 2316E) or the new 32K and 64K ROMs (the 2332 and 2364 respectively).

The 2716, with its single 5-volt supply and with an access time up to 350 ns, is ideal for use with the newer high performance +5V microprocessors such as Intel's 8085 and 8086. The 2716 is also the first EPROM with a static standby mode which reduces the power dissipation without increasing access time. The maximum active power dissipation is 525 mW while the maximum standby power dissipation is only 132 mW, a 75% savings.

The 2716 has the simplest and fastest method yet devised for programming EPROMs — single pulse TTL level programming. No need for high voltage pulsing because all programming controls are handled by TTL signals. Now, it is possible to program on-board, in the system, in the field. Program any location at any time — either individually, sequentially or at random, with the 2716's single address location programming. Total programming time for all 16,384 bits is only 100 seconds.

PIN CONFIGURATION*



†Refer to 2732 data sheet for specifications

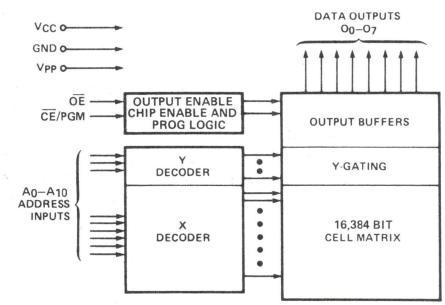
PIN NAMES

A_0–A_9	ADDRESSES
$\overline{CE}$/PGM	CHIP ENABLE/PROGRAM
$\overline{OE}$	OUTPUT ENABLE
O_0–O_7	OUTPUTS

MODE SELECTION

MODE \ PINS	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

BLOCK DIAGRAM



Pin 18 and pin 20 have been renamed to conform with the entire family of 16K, 32K, and 64K EPROMs and ROMs. The die, fabrication process, and specifications remain the same and are totally uneffected by this change.

PROGRAMMING

The programming specifications are described in the Data Catalog PROM/ROM Programming Insutrctions on Page 4-83.

Absolute Maximum Ratings*

Temperature Under Bias . . . . . -10°C to +80°C
Storage Temperature . . . . . -65°C to +125°C
All Input or Output Voltages with Respect to Ground . . . . . +6V to -0.3V
V_{PP} Supply Voltage with Respect to Ground During Program . . . . . +26.5V to -0.3V

**COMMENT:* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Conditions During Read

	2716	2716-1	2716-2
Temperature Range	0°C – 70°C	0°C – 70°C	0°C – 70°C
V_{CC} Power Supply [1,2]	5V ± 5%	5V ± 10%	5V ± 5%
V_{PP} Power Supply [2]	V_{CC} ± 0.6V [3]	V_{CC} ± 0.6V [3]	V_{CC} ± 0.6V [3]

PROM/ROM

READ OPERATION

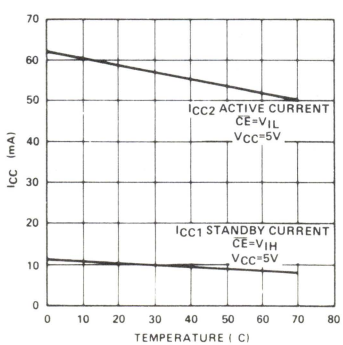
D.C. and Operating Characteristics

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[4]	Max.		
I_{LI}	Input Load Current			10	µA	V_{IN} = 5.25V
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = 5.25V
I_{PP1} [2]	V_{PP} Current			5	mA	V_{PP} = 5.85V
I_{CC1} [2]	V_{CC} Current (Standby)		10	25	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}
I_{CC2} [2]	V_{CC} Current (Active)		57	100	mA	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
V_{IL}	Input Low Voltage	-0.1		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -400 µA

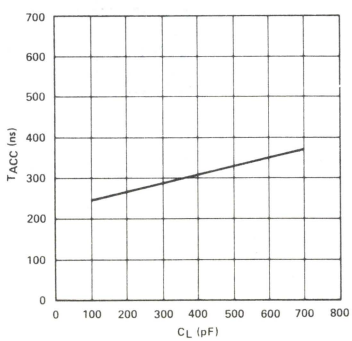
NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. The tolerance of 0.6V allows the use of a driver circuit for switching the V_{PP} supply pin from V_{CC} in read to 25V for programming.
4. Typical values are for T_A = 25°C and nominal supply voltages.
5. This parameter is only sampled and is not 100% tested.

Typical Characteristics

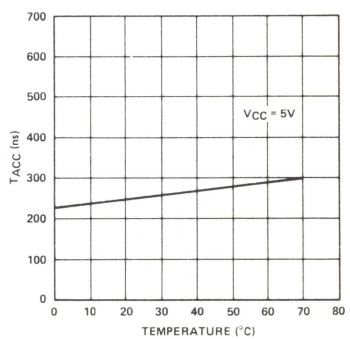
I_{CC} CURRENT vs. TEMPERATURE



ACCESS TIME vs. CAPACITANCE



ACCESS TIME vs. TEMPERATURE



A.C. Characteristics

Symbol	Parameter	2716 Limits			2716-1 Limits			2716-2 Limits			Unit	Test Conditions
		Min	Typ[4]	Max	Min	Typ[4]	Max	Min	Typ[4]	Max		
t_{ACC}	Address to Output Delay			450			350			390	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay			450			350			390	ns	$\overline{OE} = V_{IL}$
t_{OE}	Output Enable to Output Delay			120			120			120	ns	$\overline{CE} = V_{IL}$
t_{DF}	Output Enable High to Output Float	0		100	0		100	0		100	ns	$\overline{CE} = V_{IL}$
t_{OH}	Address to Output Hold	0			0			0			ns	$\overline{CE} = \overline{OE} = V_{IL}$

PROM/ROM

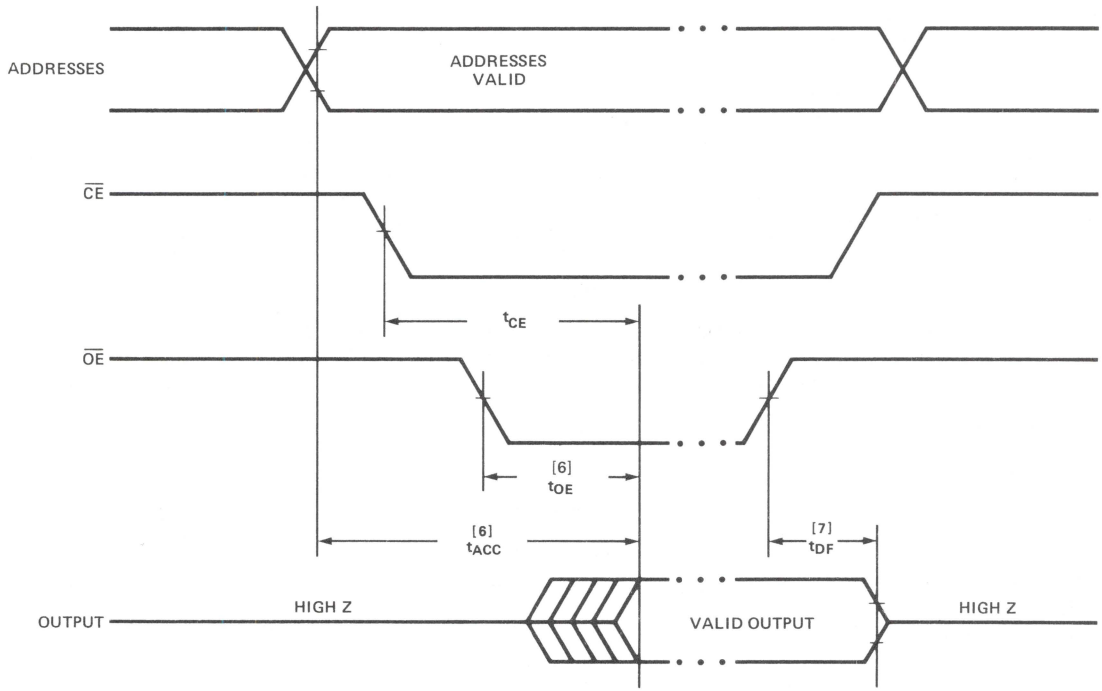
Capacitance[5] $T_A = 25°C$, f = 1 MHz

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

A.C. Test Conditions:

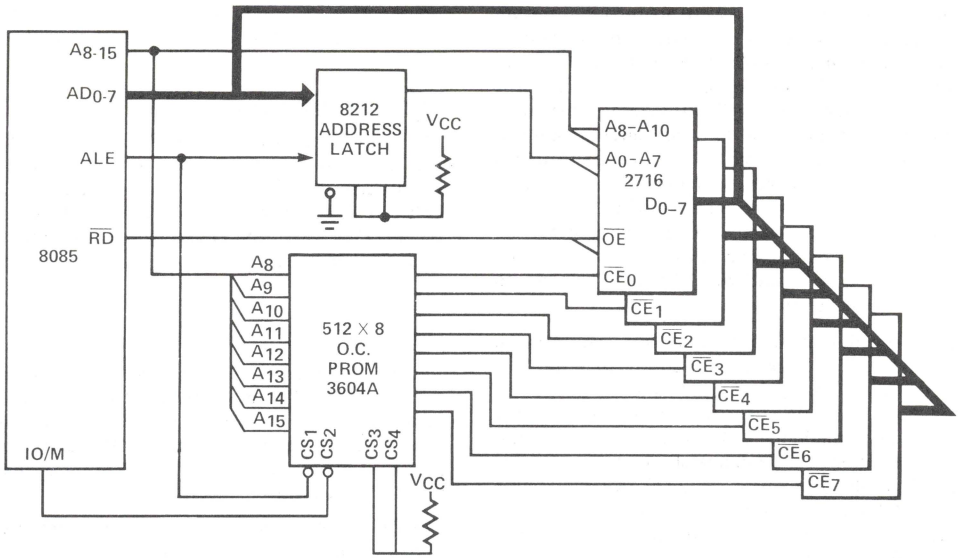
Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤20 ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

A. C. Waveforms (1)



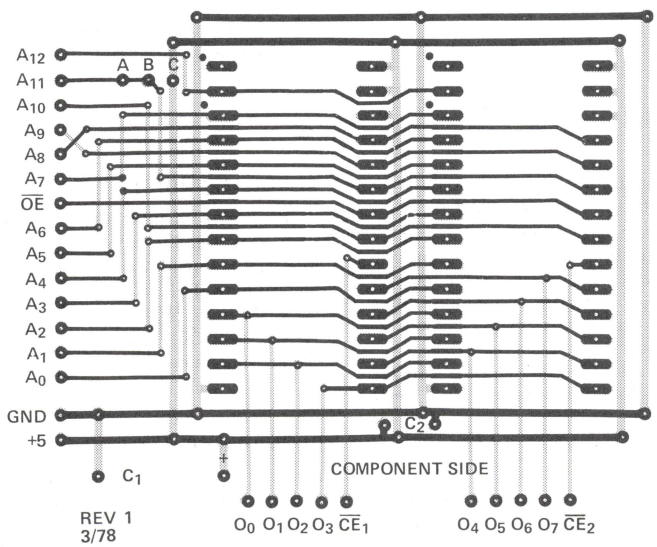
NOTE: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. The tolerance of 0.6V allows the use of a driver circuit for switching the V_{PP} supply pin from V_{CC} in read to 25V for programming.
4. Typical values are for $T_A = 25°C$ and nominal supply voltages.
5. This parameter is only sampled and is not 100% tested.
6. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
7. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

TYPICAL 16K EPROM SYSTEM



- This scheme accomplished by using $\overline{CE}$ (PD) as the primary decode. $\overline{OE}$ (CS) is now controlled by previously unused signal. RD now controls data on and off the bus by way of $\overline{OE}$.
- A selected 2716 is available for systems which require $\overline{CE}$ access of less than 450 ns for decode network operation.
- The use of a PROM as a decoder allows for:
  a) ALE is required for Edge Enabled devices (32K and 64K), and is optional for 2716.
  b) Compatibility with upward (and downward) memory expansion.
  c) Easy assignment of ROM memory modules, compatible with PL/M modular software concepts.

8K, 16K, 32K, 64K 5V EPROM/ROM FAMILY
PRINTED CIRCUIT BOARD LAYOUT



ERASURE CHARACTERISTICS

The erasure characteristics of the 2716 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical 2716 in approximately 3 years, while it would take approximatley 1 week to cause erasure when exposed to direct sunlight. If the 2716 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 2716 window to prevent unintentional erasure.

The recommended erasure procedure (see Data Catalog page 4-83) for the 2716 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The 2716 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

DEVICE OPERATION

The five modes of operation of the 2716 are listed in Table I. It should be noted that all inputs for the five modes are at TTL levels. The power supplies required are a +5V V_{CC} and a V_{PP}. The V_{PP} power supply must be at 25V during the three programming modes, and must be at 5V in the other two modes.

TABLE I. MODE SELECTION

MODE \ PINS	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

READ MODE

The 2716 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs 120 ns (t_{OE}) after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The 2716 has a standby mode which reduces the active power dissipation by 75%, from 525 mW to 132 mW. The 2716 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedence state, independent of the $\overline{OE}$ input.

OUTPUT DESELECTION

The outputs of two or more 2716s may be OR-tied together on the same data bus. Only one 2716 should have its output selected ($\overline{OE}$ low) to prevent data bus contention between 2716s in this configuration. The outputs of the other 2716s should be deselected by raising the $\overline{OE}$ input to a TTL high level.

PROGRAMMING

Initially, and after each erasure, all bits of the 2716 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 2716 is in the programming mode when the V_{PP} power supply is at 25V and $\overline{OE}$ is at V_{IH}. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 msec, active high, TTL program pulse is applied to the $\overline{CE}$/PGM input. A program pulse must be applied at each address location to be programmed. You can program any location at any time — either individually, sequentially, or at random. The program pulse has a maximum width of 55 msec. The 2716 must not be programmed with a DC signal applied to the $\overline{CE}$/PGM input.

Programming of multiple 2716s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled 2716s may be connected together when they are programmed with the same data. A high level TTL pulse applied to the $\overline{CE}$/PGM input programs the paralleled 2716s.

PROGRAM INHIBIT

Programming of multiple 2716s in parallel with different data is also easily accomplished. Except for $\overline{CE}$/PGM, all like inputs (including $\overline{OE}$) of the parallel 2716s may be common. A TTL level program pulse applied to a 2716's $\overline{CE}$/PGM input with V_{PP} at 25V will program that 2716. A low level $\overline{CE}$/PGM input inhibits the other 2716 from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify may be performed wth V_{PP} at 25V. Except during programming and program verify, V_{PP} must be at 5V.

MILITARY TEMP. ADVANCE INFORMATION
Characteristics are subject to change without notice.

M2716
16K (2K x 8) UV ERASABLE PROM

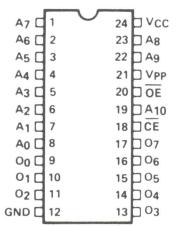
- **−55°C to +125°C Operation**
- **Single +5V Power Supply**
- **Single Programming Requirements**
  - **— Single Location Programming**
  - **— Programs with One 50 ms Pulse**
- **Static Power-Down Mode**
- **Pin Compatible to Intel® M2316E ROM**
- **±10% Power Supply Tolerance**
- **Inputs and Outputs TTL Compatible during Read and Program**

The Intel® M2716 is a 16,384-bit ultraviolet erasable and electrically programmable read only memory (EPROM) specified over the −55°C to 125°C temperature range. The M2716 operates from a single +5V power supply, has a static power-down mode, and features fast, single-address location programming. It makes designing with EPROMs faster, easier and more economical. For production quantities, the M2716 user can convert rapidly to Intel's pin-for-pin compatible 16K ROM — the M2316E.

The M2716 has a static power-down mode which reduces the power dissipation without increasing access time. The active power dissipation is reduced by over 60% in the standby power mode.

The M2716 has the simplest and fastest method devised yet for programming EPROMs — single pulse TTL level programming. No need for high voltage pulsing because all programming controls are handled by TTL signals. Now it is possible to program on-board, in the system, in the field. Program any location at any time — either individually, sequentially or at random, with the M2716's single-address location programming. Total programming time for all 16,384 bits is only 100 seconds.

PIN CONFIGURATION



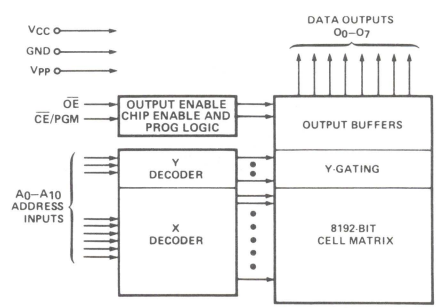
PIN NAMES

A_0–A_9	ADDRESSES
$\overline{CE}$/PGM	CHIP ENABLE/PROGRAM
$\overline{OE}$	OUTPUT ENABLE
O_0–O_7	OUTPUTS

MODE SELECTION

MODE \ PINS	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

BLOCK DIAGRAM



ADVANCE INFORMATION
Characteristics are subject to change without notice.

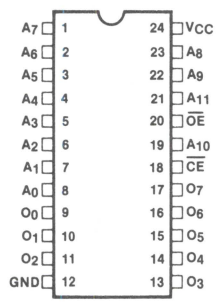
2732
32K (4K x 8) UV ERASABLE PROM

- **Single +5V ±10% Power Supply**
- **Simple Programming Requirements**
  - **Single Location Programming**
  - **Programs with One 50 ms Pulse**
- **Low Power Mode**
- **Pin Compatible to Intel® 2332 ROM**
- **Inputs and Outputs TTL Compatible during Read and Program**
- **MCS-80 and MCS-85 Compatible**

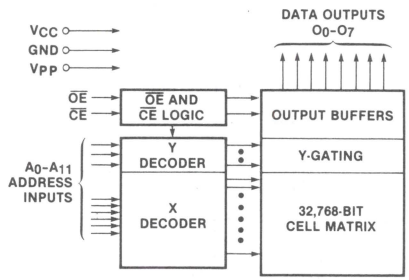
The Intel® 2732 is a 32,768-bit ultraviolet erasable and electrically programmable read only memory (EPROM). The 2732 operates from a single +5V power supply, has a low power mode, and features fast, single-address location programming. It makes designing with EPROMs faster, easier and more economical. For production quantities, the 2732 user can convert rapidly to Intel's pin-for-pin compatible 32K ROM — the 2332.

The 2732 has the simplest and fastest method devised for programming EPROMs — single pulse TTL level programming. No need for high voltage pulsing because all programming controls are handled by TTL signals. It is possible to program on-board, in the system, in the field. Program any location at any time — either individually or sequentially or at random, with the 2732's single-address location programming. Total programming time for all 32,768 bits is only 200 seconds.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

A_0-A_{10}	ADDRESSES
CE	CHIP ENABLE
OE	OUTPUT ENABLE
O_0-O_7	OUTPUTS

2758*
8K (1K x 8) UV ERASABLE LOW POWER PROM

- **Single +5V Power Supply**
- **Simple Programming Requirements**
  Single Location Programming
  Programs with One 50 ms Pulse
- **Low Power Dissipation**
  525 mW Max. Active Power
  132 mW Max. Standby Power
- **Fast Access Time: 450 ns Max. in Active and Standby Power Modes**
- **Inputs and Outputs TTL Compatible during Read and Program**
- **Completely Static**
- **Three-State Outputs for OR-Ties**

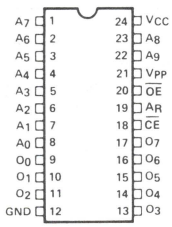
PROM/ROM

The Intel® 2758 is a 8192-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2758 operates from a single 5-volt power supply, has a static standby mode, and features fast single address location programming. It makes designing with EPROMs faster, easier and more economical. The total programming time for all 8192 bits is 50 seconds.

The 2758 has a static standby mode which reduces the power dissipation without increasing access time. The maximum active power dissipation is 525 mW, while the maximum standby power dissipation is only 132 mW, a 75% savings. Power-down is achieved by applying a TTL-high signal to the $\overline{CE}$ input.

A 2758 system may be designed for total upwards compatibility with Intel's 16K 2716 EPROM (see Applications Note 30). The 2758 maintains the simplest and fastest method yet devised for programming EPROMs – single pulse TTL-level programming. There is no need for high voltage pulsing because all programming controls are handled by TTL signals. Now it is possible to program on-board, in the system, in the field. Program any location at any time – either individually, sequentially, or at random, with the single address location programming.

PIN CONFIGURATION*



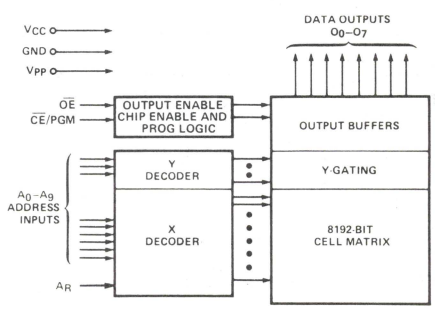
MODE SELECTION

MODE \ PINS	$\overline{CE}$/PGM (18)	A_R (19)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	V_{IL}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IL}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IL}	V_{IH}	+25	+5	High Z

PIN NAMES

A_0–A_9	ADDRESSES
$\overline{CE}$/PGM	CHIP ENABLE/PROGRAM
$\overline{OE}$	OUTPUT ENABLE
O_0–O_7	OUTPUTS
A_R	SELECT REFERENCE INPUT LEVEL

BLOCK DIAGRAM



Pin 18 and pin 20 have been renamed to conform with the entire family of 16K, 32K, and 64K EPROMs and ROMs. The die, fabrication process, and specifications remain the same and are totally uneffected by this change.

PROGRAMMING

The programming specifications are described in the Data Catalog PROM/ROM Programming Instructions on page 4-83.

Absolute Maximum Ratings*

Temperature Under Bias . . . . . -10°C to +80°C
Storage Temperature . . . . . -65°C to +125°C
All Input or Output Voltages with
Respect to Ground . . . . . +6V to -0.3V
V_{PP} Supply Voltage with Respect
to Ground During Programming . . . . . +26.5V to -0.3V

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION

D.C. and Operating Characteristics

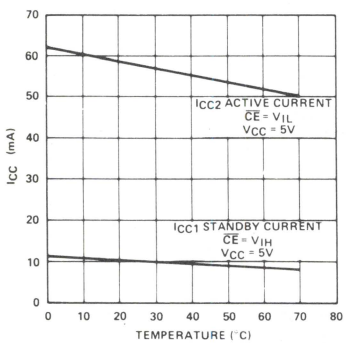
T_A = 0°C to 70°C, V_{CC}[1,2] = +5V ±5%, V_{PP}[2] = V_{CC} ±0.6V[3]

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[4]	Max.		
I_{LI}	Input Load Current			10	µA	V_{IN} = 5.25V
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = 5.25V
I_{PP1}[2]	V_{PP} Current			5	mA	V_{PP} = 5.85V
I_{CC1}[2]	V_{CC} Current (Standby)		10	25	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}
I_{CC2}[2]	V_{CC} Current (Active)		57	100	mA	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
A_R[5]	Select Reference Input Level	-0.1		0.8	V	I_{IN} = 10 µA
V_{IL}	Input Low Voltage	-0.1		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC} + 1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -400 µA

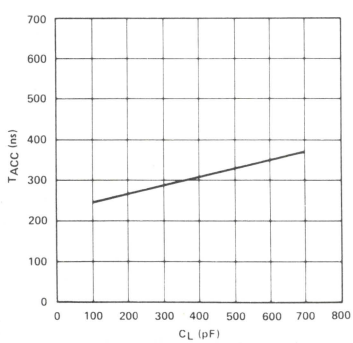
NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. The tolerance of 0.6V allows the use of a driver circuit for switching the V_{PP} supply pin from V_{CC} in read to 25V for programming.
4. Typical values are for T_A = 25°C and nominal supply voltages.
5. A_R is a reference voltage level which requires an input current of only 10 µA. The 2758 S1865 is also available which has a reference voltage level of V_{IH} instead of V_{IL}.

Typical Characteristics

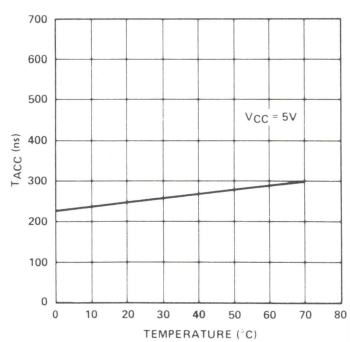
I_{CC} CURRENT vs. TEMPERATURE



ACCESS TIME vs. CAPACITANCE



ACCESS TIME vs. TEMPERATURE



A.C. Characteristics

$T_A = 0°C$ to $70°C$, V_{CC}[1] = +5V ±5%, V_{PP}[2] = V_{CC} ±0.6V[3]

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[4]	Max.		
t_{ACC}	Address to Output Delay		250	450	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay		280	450	ns	$\overline{OE} = V_{IL}$
t_{OE}	Output Enable to Output Delay			120	ns	$\overline{CE} = V_{IL}$
t_{DF}	Output Enable High to Output Float	0		100	ns	$\overline{CE} = V_{IL}$
t_{OH}	Address to Output Hold	0			ns	$\overline{CE} = \overline{OE} = V_{IL}$

Capacitance[5] $T_A = 25°C$, f = 1 MHz

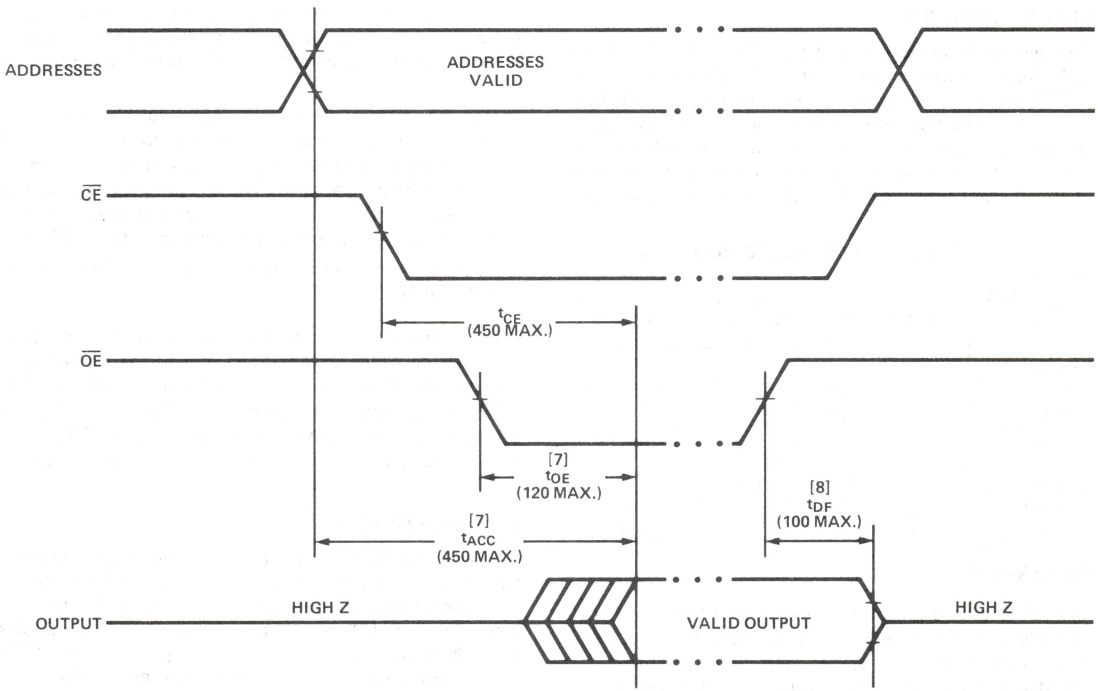
Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

NOTE: Please refer to page 2 for notes.

A.C. Test Conditions:

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤20 ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

A.C. Waveforms[6]



NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. The tolerance of 0.6V allows the use of a driver circuit for switching the V_{PP} supply pin from V_{CC} in read to 25V for programming.
4. Typical values are for $T_A = 25°C$ and nominal supply voltages.
5. This parameter is only sampled and is not 100% tested.
6. All times shown in parentheses are minimum times and are nsec unless otherwise specified.
7. $\overline{OE}$ may be delayed up to 330ns after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
8. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

ERASURE CHARACTERISTICS

The erasure characteristics of the 2758 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical 2758 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the 2758 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 2758 window to prevent unintentional erasure.

The recommended erasure procedure (see Data Catalog page 4-83) for the 2758 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated does (i.e., UV intensity X exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12,000 μW/cm^2 power rating. The 2758 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

DEVICE OPERATION

The five modes of operation of the 2758 are listed in Table 1. It should be noted that all inputs for the five modes are at TTL levels. The power supplied required are a +5V V_{CC} and a V_{PP}. The V_{PP} power supply must be at 25V during the two programming modes, and must be at 5V in the other three modes. In all operational modes, A_R must be at V_{IL} (except for the 2758 S1865 which has A_R at V_{IH}).

TABLE I. MODE SELECTION

MODE \ PINS	$\overline{CE}$/PGM (18)	A_R (19)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	V_{IL}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IL}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IL}	V_{IH}	+25	+5	High Z

READ MODE

The 2758 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs 120 ns (t_{OE}) after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The 2758 has a standby mode which reduces the active power dissipation by 75%, from 525 mW to 132 mW. The 2758 is placed in the standby mode by applying a TTL high signal to $\overline{CE}$ input. When in standby mode, the outputs are in a high impedence state, independent of the OE input.

OUTPUT DESELECTION

The outputs of two or more 2758s may be OR-tied together on the same data bus. Only one 2758 should have its output selected ($\overline{OE}$ low) to prevent data bus contention between 2758s in this configuration. The outputs of the other 2758s should be deselected by raising the $\overline{OE}$ input to a TTL high level.

PROGRAMMING

Initially, and after each erasure, all bits of the 2758 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 2758 is in the programming mode when the V_{PP} power supply is at 25V and $\overline{OE}$ is at V_{IH}. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 msec, active high, TTL program pulse is applied to the $\overline{CE}$/PGM input. A program pulse must be applied at each address location to be programmed. You can program any location at any time — either individually, sequentially, or at random. The program pulse has a maximum width of 55 msec.

The 2758 must be programmed with a DC signal applied to the $\overline{CE}$/PGM input.

Programming of multiple 2758s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled 2758s may be connected together when they are programmed with the same data. A high level TTL pulse applied to the $\overline{CE}$/PGM input programs the paralleled 2758s.

PROGRAM INHIBIT

Programming of multiple 2758s in parallel with different data is also easily accomplished. Except for $\overline{CE}$/PGM, all like inputs(including $\overline{OE}$) of the parallel 2758s may be common. A TTL level program pulse applied to a 2758's $\overline{CE}$/PGM input with V_{PP} at 25V will program that 2758. A low level $\overline{CE}$/PGM input inhibits the other 2758 from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify may be performed with V_{PP} at 25V. Except during programming and program verify, V_{PP} must be at 5V.

3602A, 3622A FAMILY
2K (512 x 4) HIGH-SPEED PROM

	3602A-2 3622A-2	3602A 3622A
Typ. T_A(ns)	45	55
Max. T_A(ns)	60	70

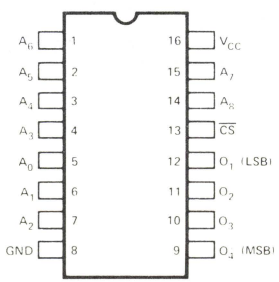
- Low Power Dissipation --0.3mW/Bit
- Open Collector (3602A) or Three State (3622A) Outputs
- Simple Memory Expansion-- Chip Select Input Lead
- Replaces Two 256×4 PROMs Without Increasing Board Area
- Polycrystalline Silicon Fuse For Higher Reliability
- Hermetic 16-Pin DIP

The Intel® 3602A/3622A are 2048-bit bipolar PROMs organized as 512 words by 4 bits. The fast second generation 3602A/3622A replaces its Intel predecessor, the 3602/3622. A higher speed version, the 3602A-2/3622A-2, is now available at 60 ns. All 3602A/3622A specifications, except programming, are the same as the 3602/3622. Once programmed, the 3602A/3622A are interchangeable with the 3602/3622.

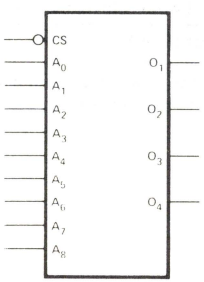
The PROMs are manufactured with all outputs initially logically high. Logic low levels can be electrically programmed in selected bit locations. Both open collector and three-state outputs are available. The power dissipation is typically 0.2 mW/bit.

The pin configuration of the PROMs is the same as the popular 1K bit, 256 X 4 PROMs with the exception that CS_2 (pin 14) is address A_8. The bit density of existing 256 X 4 PROM systems can be easily doubled without an increase in area with the 3602A/3622A. These PROMs like the 256 X 4 PROMs, are in 16-pin dual in-line package.

PIN CONFIGURATION



LOGIC SYMBOL



PROGRAMMING

The programming specifications are described in the Data Catalog PROM/ROM Programming Instructions on page 4-89.

Absolute Maximum Ratings*

Temperature Under Bias . . . . . -65°C to +125°C
Storage Temperature . . . . . -65°C to +160°C
Output or Supply Voltages . . . . . -0.5V to 7 Volts
All Input Voltages . . . . . -1.6V to 5.6V
Output Currents 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D. C. Characteristics: All Limits Apply for V_{CC} = +5.0V ±5%, T_A = 0°C to +75°C

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[1]	Max.		
I_{FA}	Address Input Load Current		-0.05	-0.25	mA	V_{CC} = 5.25V, V_A = 0.45V
I_{FS}	Chip Select Input Load Current		-0.05	-0.25	mA	V_{CC} = 5.25V, V_S = 0.45V
I_{RA}	Address Input Leakage Current			40	μA	V_{CC} = 5.25V, V_A = 5.25V
I_{RS}	Chip Select Input Leakage Current			40	μA	V_{CC} = 5.25V, V_S = 5.25V
V_{CA}	Address Input Clamp Voltage		-0.9	-1.5	V	V_{CC} = 4.75V, I_A = -10mA
V_{CS}	Chip Select Input Clamp Voltage		-0.9	-1.5	V	V_{CC} = 4.75V, I_S = -10mA
V_{OL}	Output Low Voltage		0.3	0.45	V	V_{CC} = 4.75V, I_{OL} = 15mA
I_{CEX}	Output Leakage Current			40	μA	V_{CC} = 5.25V, V_{CE} = 5.25V
I_{CC}	Power Supply Current		110	140	mA	V_{CC}=5.25V, V_{A0}→V_{A8} = 0V $\overline{CS}$ = 0V
V_{IL}	Input "Low" Voltage			0.85	V	V_{CC} = 5.0V
V_{IH}	Input "High" Voltage	2.0			V	V_{CC} = 5.0V

3622A, 3622A-2 ONLY

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
$\|I_O\|$	Output Leakage for High Impedance Stage			40	μA	V_O=5.25V or 0.45V, V_{CC}=5.25V, $\overline{CS}$=2.4V
I_{SC}[2]	Output Short Circuit Current	-20	-25	-70	mA	V_O = 0V, V_{CC} = 4.75V
V_{OH}	Output High Voltage	2.4			V	I_{OH}=-2.4mA, V_{CC} = 4.75V

NOTES: 1. Typical values are at 25° C and at nominal voltage.
2. Unmeasured outputs are open during this test.

A. C. Characteristics V_{CC} = +5V ±5%, T_A = 0°C to +75°C

SYMBOL	PARAMETER	MAX. LIMIT		UNIT	CONDITIONS
		3602A-2 3622A-2	3602A 3622A		
t_{A++}, t_{A--} t_{A+-}, t_{A-+}	Address to Output Delay	60	70	ns	$\overline{CS}$ = V_{IL} to Select the PROM
t_{S++}	Chip Select to Output Delay	30	30	ns	
t_{S--}	Chip Select to Output Delay	30	30	ns	

Capacitance [1] T_A = 25°C, f = 1 MHz

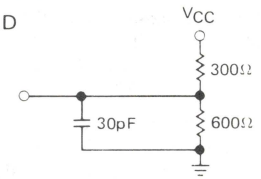
SYMBOL	PARAMETER	LIMITS		UNIT	TEST CONDITIONS
		TYP.	MAX.		
C_{INA}	Address Input Capacitance	4	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{INS}	Chip-Select Input Capacitance	6	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{OUT}	Output Capacitance	7	12	pF	V_{CC} = 5V V_{OUT} = 2.5V

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

Switching Characteristics

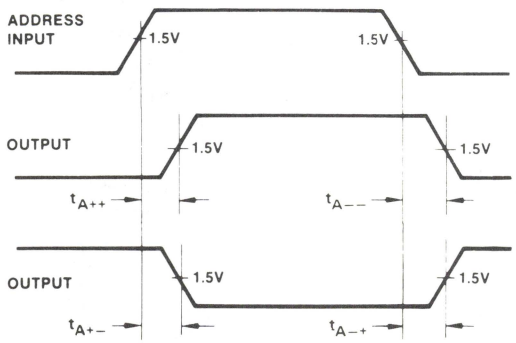
Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 15 mA and 30 pF
Frequency of test - 2.5 MHz

15 mA TEST LOAD

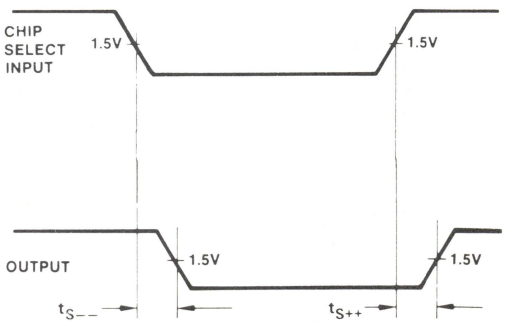


Waveforms

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY



PROM/ROM

3604A, 3624A FAMILY
4K (512 x 8) HIGH-SPEED PROM

	3604A-2 3624A-2	3604A 3624A	3604AL
Max. T_A(ns)	60	70	90
Max. I_{CC}(mA)	170	170	130/25*

*Standby Current When The Chip is Deselected.

- Fast Access Time --60ns Max (3604A-2, 3624A-2)
- Low Standby Power Dissipation (3604AL) --32 μW/Bit Max
- Open Collector (3604A) or Three State (3624A) Outputs
- Four Chip Select Inputs For Easy Memory Expansion
- Polycrystalline Silicon Fuse For Higher Reliability
- Hermetic 24 Pin DIP

The Intel® 3604A/3624A are 4096-bit bipolar PROMs organized as 512 words by 8 bits. The fast second generation 3604A/3624A replaces its Intel predecessor, the 3604/3624. Higher speed PROMs, the 3604A-2/3624A-2, are now available at 60 ns. All 3604A/3624A specifications, except programming, are the same as or better than the 3604/3624. Once programmed, the 3604A/3624A are interchangeable with the 3604/3624

The PROMs are manufactured with all outputs initially logically high. Logic low levels can be electrically programmed in selected bit locations. Both open collector and three-state outputs are available. Low standby power dissipation can be achieved with the 3604AL. The standby power dissipation is approximately 20% of the active power dissipation.

The 3604A/3624A are available in a hermetic 24-pin dual in-line package. These PROMs are manufactured with the time-proven polycrystalline silicon fuse technology.

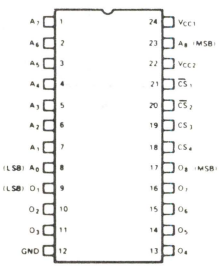
Mode/Pin Connection		Pin 22	Pin 24
READ:	3604A, 3604A-2 3624A, 3624A-2	No Connect or 5V	5V
	3604AL	+5V	Must be Left Open
PROGRAM:	3604A, 3604A-2 3624A, 3624A-2	Pulsed 12.5V	Pulsed 12.5V
	3604AL	Pulsed 12.5V	Pulsed 12.5V
STANDBY:	3604AL	Power dissipation is automatically reduced whenever the 3604AL is deselected.	

PIN NAMES

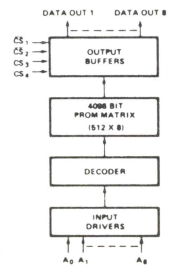
A_0–A_8	ADDRESS INPUTS
$\overline{CS}_1$–$\overline{CS}_2$ CS_3–CS_4	CHIP SELECT INPUTS [1]
O_1–O_8	DATA OUTPUTS

[1] To select the PROM $\overline{CS}_1 = \overline{CS}_2 = 0$ and $CS_3 = CS_4 = 1$.

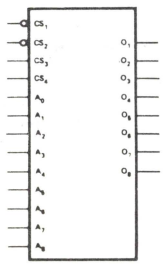
PIN CONFIGURATION



BLOCK DIAGRAM



LOGIC SYMBOL



PROGRAMMING

The programming specifications are described in the Data Catalog PROM/ROM Programming Instructions on page 4-89.

Absolute Maximum Ratings*

Temperature Under Bias . . . . . -65°C to +125°C
Storage Temperature . . . . . -65°C to +160°C
Output or Supply Voltages . . . . . -0.5V to 7 Volts
All Input Voltages . . . . . -1.6 to 5.5V
Output Currents 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D. C. Characteristics: All Limits Apply for V_{CC} = +5.0V ±5%, T_A = 0°C to +75°C

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{FA}	Address Input Load Current		-0.05	-0.25	mA	V_{CC} = 5.25V, V_A = 0.45V
I_{FS}	Chip Select Input Load Current		-0.05	-0.25	mA	V_{CC} = 5.25V, V_S = 0.45V
I_{RA}	Address Input Leakage Current			40	μA	V_{CC} = 5.25V, V_A = 5.25V
I_{RS}	Chip Select Input Leakage Current			40	μA	V_{CC} = 5.25V, V_S = 5.25V
V_{CA}	Address Input Clamp Voltage		-0.9	-1.5	V	V_{CC} = 4.75V, I_A = -10 mA
V_{CS}	Chip Select Input Clamp Voltage		-0.9	-1.5	V	V_{CC} = 4.75V, I_S = -10 mA
V_{OL}	Output Low Voltage		0.3	0.45	V	V_{CC} = 4.75V, I_{OL} = 15 mA
I_{CEX}	Output Leakage Current			100	μA	V_{CC} = 5.25V, V_{CE} = 5.25V
I_{CC1}	Power Supply Current (3604A, 3604A-2, 3624A, and 3624A-2)		130	170	mA	V_{CC1} = 5.25V, V_{A0}→V_{A8} = 0V, $\overline{CS}_1$ = $\overline{CS}_2$ = 0V, CS_3 = CS_4 = 5.25V
I_{CC2}	Power Supply Current (3604AL) Active		100	130	mA	V_{CC2} = 5.25V, V_{CC1} = Open $\overline{CS}_1$ = $\overline{CS}_2$ = 0.45V, CS_3 = CS_4 = 2.4V
	Standby		15	25	mA	$\overline{CS}_1$ = $\overline{CS}_2$ = 2.5V
V_{IL}	Input "Low" Voltage			0.85	V	V_{CC} = 5.0V
V_{IH}	Input "High" Voltage	2.0			V	V_{CC} = 5.0V

3624A FAMILY ONLY

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
$\|I_O\|$	Output Leakage for High Impedance Stage			100	μA	V_O=5.25V or 0.45V, V_{CC}=5.25V, $\overline{CS}_1$=$\overline{CS}_2$=2.4V
I_{SC}[2]	Output Short Circuit Current	-20	-25	-70	mA	V_O = 0V, V_{CC} = 4.75V
V_{OH}	Output High Voltage	2.4			V	I_{OH}=-2.4mA, V_{CC} = 4.75V

NOTES: 1. Typical values are at 25° C and at nominal voltage.
2. Unmeasured outputs are open during this test.

A. C. Characteristics V_{CC} = +5V ±5%, T_A = 0°C to +75°C

SYMBOL	PARAMETER	MAXIMUM LIMITS (ns)			UNIT	TEST CONDITIONS
		3604A-2 3624A-2	3604A 3624A	3604AL		
t_{A++}, t_{A--} t_{A+-}, t_{A-+}	Address to Output Delay	60	70	90	ns	$\overline{CS_1} = \overline{CS_2} = V_{IL}$ and $CS_3 = CS_4 = V_{IH}$ to Select the PROM
t_{S++}	Chip Select to Output Delay	30	30	30	ns	
t_{S--}	Chip Select to Output Delay	30	30	120	ns	

Capacitance [1] T_A = 25°C, f = 1 MHz

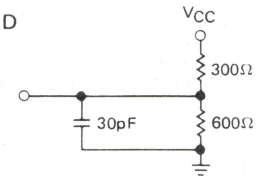
SYMBOL	PARAMETER	LIMITS		UNIT	TEST CONDITIONS	
		TYP.	MAX.			
C_{INA}	Address Input Capacitance	4	10	pF	V_{CC} = 5V	V_{IN} = 2.5V
C_{INS}	Chip-Select Input Capacitance	6	10	pF	V_{CC} = 5V	V_{IN} = 2.5V
C_{OUT}	Output Capacitance	7	15	pF	V_{CC} = 5V	V_{OUT} = 2.5V

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

Switching Characteristics

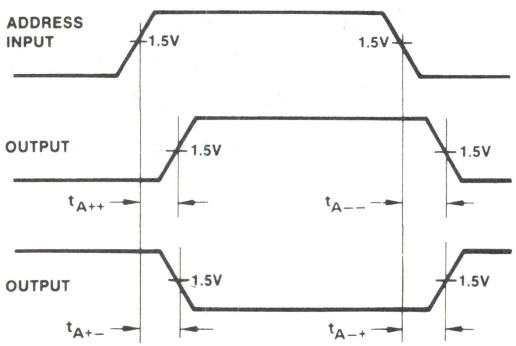
Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 15 mA and 30 pF
Frequency of test - 2.5 MHz

15 mA TEST LOAD

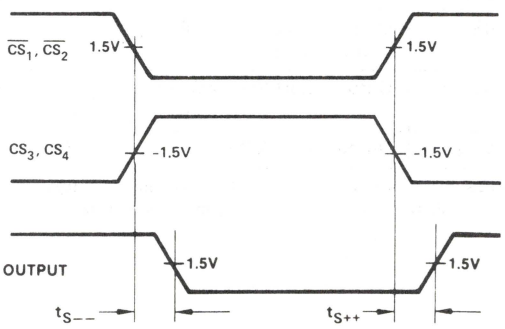


Waveforms

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY



M3604A, M3624A
4K (512 x 8) HIGH-SPEED PROM

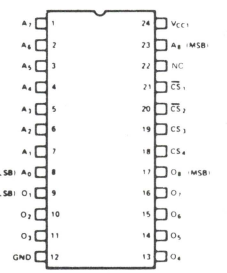
MILITARY TEMP.

- **Military Temperature Range −55°C to +125°C**
- **Fast Access Time—90nsec Maximum**
- **Open Collector (M3604A) or Three-State (M3624A) Outputs**
- **Four Chip Select Inputs For Easy Memory Expansion**
- **Polycrystalline Silicon Fuse For Higher Reliability**
- **Standard Packaging—24Pin Hermetic Dual In-Line Lead Configuration**

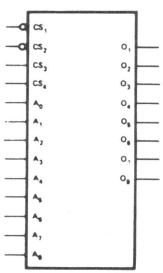
PROM/ROM

The M3604A and M3624A are military temperature range PROMs organized as 512 words by 8 bits. They are manufactured with all outputs high and logic output low levels can be electrically programmed in selected bit locations. The M3604A and M3624A, except for programming, have the same electrical specifications and are direct replacements to their predecessors, the M3604 and M3624.

PIN CONFIGURATION



LOGIC SYMBOL



Absolute Maximum Ratings*

Temperature Under Bias	−65°C to +135 C
Storage Temperature	−65°C to +160°C
Output or Supply Voltages	−0.5V to 7 Volts
All Input Voltages	−1.6V to 5.6V
Output Currents	100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. Characteristics V_{CC} = +5.0V ±10%, T_A = −55°C to +125°C

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{FA}	Address Input Load Current		-0.05	-0.25	mA	V_{CC}= Max, V_A=0.45V
I_{FS}	Chip Select Input Load Current		-0.05	-0.25	mA	V_{CC}= Max, V_S=0.45V
I_{RA}	Address Input Leakage Current			40	μA	V_{CC}= Max, V_A= Max
I_{RS}	Chip Select Input Leakage Current			40	μA	V_{CC}= Max, V_S= Max
V_{CA}	Address Input Clamp Voltage		-0.9	−1.5	V	V_{CC}= Min, I_A= −10mA
V_{CS}	Chip Select Input Clamp Voltage		-0.9	−1.5	V	V_{CC}= Min, I_S= −10mA
V_{OL}	Output Low Voltage		0.3	0.45	V	V_{CC}= Min, I_{OL}= 10mA
I_{CEX}	Output Leakage Current			100	μA	V_{CC}= Max, V_{CE}= Max
I_{CC1}	Power Supply Current (M3604A)			190	mA	V_{CC1}= Max, V_{A0}→V_{A8}=0V, $\overline{CS_1}$=$\overline{CS_2}$=0V, CS_3=CS_4= 5.5V
V_{IL}	Input "Low" Voltage			0.8	V	V_{CC}= 5.0V, T_A=25°C
V_{IH}	Input "High" Voltage	2.0			V	V_{CC}= 5.0V, T_A=25°C

M3624A ONLY

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
$\|I_O\|$	Output Leakage for High Impedance Stage			100	μA	V_O= Max or 0.45V, V_{CC}= Max, $\overline{CS_1}$=$\overline{CS_2}$=2.4V
I_{SC}[2]	Output Short Circuit Current	−20	-25	−80	mA	V_O = 0V
V_{OH}	Output High Voltage	2.4			V	I_{OH}=-2.4mA, V_{CC} = 5V

NOTES: 1. Typical values are at 25° C and at nominal voltage.
2. Unmeasured outputs are open during this test.

A. C. Characteristics V_{CC} = +5.0V ±10%, T_A = −55°C to +125°C

SYMBOL	PARAMETER	LIMITS TYP.[1]	LIMITS MAX.	UNIT	CONDITIONS
t_{A++}, t_{A--} t_{A+-}, t_{A-+}	Address to Output Delay	60	90	ns	$\overline{CS}_1 = \overline{CS}_2 = V_{IL}$ and $CS_3 = CS_4 = V_{IH}$ to Select the PROM
t_{S++}	Chip Select to Output Delay	20	45	ns	
t_{S--}	Chip Select to Output Delay	20	45	ns	

Capacitance[2] T_A = 25°C, f = 1 MHz

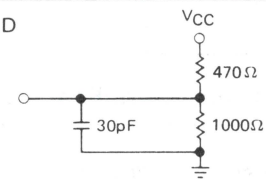
SYMBOL	PARAMETER	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
C_{INA}	Address Input Capacitance	4	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{INS}	Chip-Select Input Capacitance	6	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{OUT}	Output Capacitance	7	15	pF	V_{CC} = 5V V_{OUT} = 2.5V

NOTES: 1. Typical values are at 25°C and nominal voltage.
2. This parameter is only periodically sampled and is not 100% tested.

Switching Characteristics

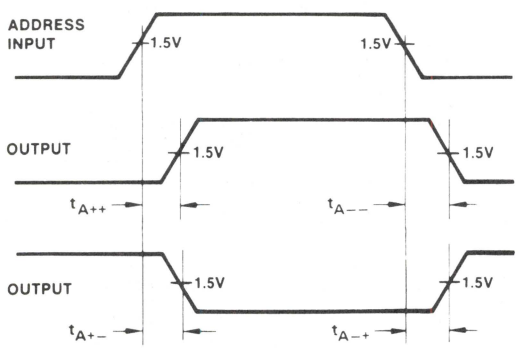
Conditions of Test:
Input pulse amplitudes · 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 10 mA and 30 pF
Frequency of test · 2.5 MHz

10 mA TEST LOAD

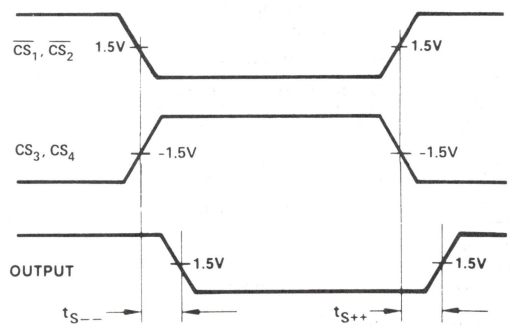


Waveforms

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY



3605, 3625
4K (1K x 4) PROM

3605-2, 3625-2	60 ns Max.
3605, 3625	70 ns Max.

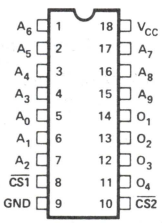
- **Fast Access Time: 45ns Typically**
- **Low Power Dissipation: 0.14mW/Bit Typically**
- **Simple Memory Expansion Two Chip Select Inputs**
- **Open Collector (3605) and Three-State(3625) Outputs**
- **Polycrystalline Silicon Fuse For Higher Reliability**
- **Hermetic 18 Pin DIP**

The Intel® 3605 and 3625 families are high density, 4096-bit bipolar PROMs organized as 1024 words by 4 bits. The 1024 by 4 organization gives ideal word or bit modularity for memory array expansion. The 3605 has open collector outputs and the 3625 has three-state outputs. The 3605 and 3625 are fully specified over the 0°C to 75°C temperature range with ±5% power supply variation. Maximum access times of 60 ns (3605-2/3625-2) and 70 ns (3605/3625) are available at a typical power dissipation of 0.14 mW/bit.

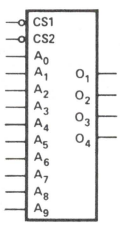
The 3605/3625 are packaged in an 18-pin dual in-line hermetic package with 300 milli-inch centers. Thus, twice the bit density can be achieved with the 3605/3625 in the same memory board area as 512 by 8-bit PROMs in 24-pin packages.

The highly reliable polycrystalline silicon fuse technology is used in the manufacturing of the 3605 and 3625 families. All outputs are initially a logical high and logic low levels can be electrically programmed in selected bit locations.

PIN CONFIGURATION



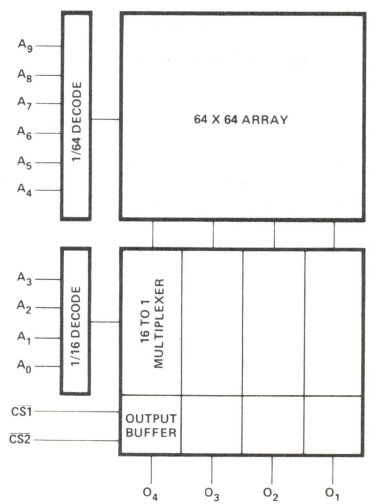
LOGIC SYMBOL



PIN NAMES

$A_0 - A_9$	ADDRESS INPUTS
$\overline{CS}$	CHIP SELECT INPUT
$O_1 - O_4$	OUTPUTS

BLOCK DIAGRAM



PROGRAMMING

The programming specifications are described in the Data Catalog PROM/ROM Programming Instructions on page 4-89.

Absolute Maximum Ratings*

Temperature Under Bias . . . . . -65°C to +125°C
Storage Temperature . . . . . -65°C to +160°C
Output or Supply Voltages . . . . . -0.5V to 7 Volts
All Input Voltages . . . . . -1V to 5.5V
Output Currents 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D. C. Characteristics: All Limits Apply for V_{CC}= +5.0V ±5%, T_A= 0°C to +75°C

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{FA}	Address Input Load Current		-0.05	-0.25	mA	V_{CC}=5.25V, V_A=0.45V
I_{FS}	Chip Select Input Load Current		-0.05	-0.25	mA	V_{CC}=5.25V, V_S=0.45V
I_{RA}	Address Input Leakage Current			40	μA	V_{CC}=5.25V, V_A=5.25V
I_{RS}	Chip Select Input Leakage Current			40	μA	V_{CC}=5.25V, V_S=5.25V
V_{CA}	Address Input Clamp Voltage		-0.9	-1.5	V	V_{CC}=4.75V, I_A=-10mA
V_{CS}	Chip Select Input Clamp Voltage		-0.9	-1.5	V	V_{CC}=4.75V, I_S=-10mA
V_{OL}	Output Low Voltage		0.3	0.45	V	V_{CC}=4.75V, I_{OL}=15mA
I_{CEX}	3605 Output Leakage Current			40	μA	V_{CC}=5.25V, V_{CE}=5.25V
I_{CC}	Power Supply Current		110	140	mA	V_{CC}=5.25V, V_{A0}→V_{A9}=0V, $\overline{CS}_1$=$\overline{CS}_2$=V_{IH}
V_{IL}	Input "Low" Voltage			0.85	V	V_{CC}=5.0V
V_{IH}	Input "High" Voltage	2.0			V	V_{CC}=5.0V

3625, 3625-2 ONLY

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
$\|I_O\|$	Output Leakage for High Impedance Stage			40	μA	V_O=5.25V or 0.45V, V_{CC}= 25V, $\overline{CS}_1$=$\overline{CS}_2$=2.4V
I_{SC}[2]	Output Short Circuit Current	-15	-25	-60	mA	V_O = 0V
V_{OH}	Output High Voltage	2.4			V	I_{OH}=-2.4mA, V_{CC} = 4.75V

NOTES: 1. Typical values are at 25° C and at nominal voltage.
2. Unmeasured outputs are open during this test.

A. C. Characteristics V_{CC} = +5V ±5%, T_A = 0°C to +75°C

Symbol	Parameter	Max. Limits 3605-2 3625-2	Max. Limits 3605 3625	Unit	Conditions
t_{A++}, t_{A--} t_{A+-}, t_{A-+}	Address to Output Delay	60	70	ns	$\overline{CS}_1$=$\overline{CS}_2$=V_{IL} to select the PROM.
t_{S++}	Chip Select to Output Delay	30	30	ns	
t_{S--}	Chip Select to Output Delay	30	30	ns	

Capacitance [1] T_A = 25°C, f = 1 MHz

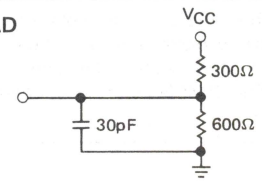
SYMBOL	PARAMETER	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
C_{INA}	Address Input Capacitance	4	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{INS}	Chip-Select Input Capacitance	6	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{OUT}	Output Capacitance	7	12	pF	V_{CC} = 5V V_{OUT} = 2.5V

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

Switching Characteristics

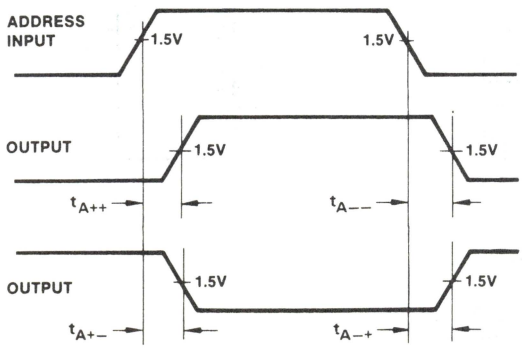
Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 15 mA and 30 pF
Frequency of test - 2.5 MHz

15mA TEST LOAD

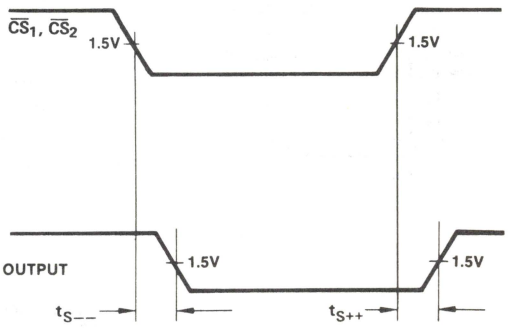


Waveforms

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY



PROM/ROM

3608, 3628
8K (1K X 8) BIPOLAR PROM

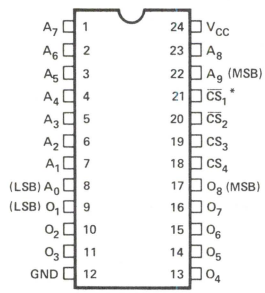
3608, 3628	80 ns Max.
3608-4, 3628-4	100 ns Max.

- **Fast Access Time: 65 ns Typically**
- **Low Power Dissipation: 0.09mW/Bit Typically**
- **Four Chip Select Inputs for Easy Memory Expansion**
- **Open Collector (3608) and Three-State (3628) Outputs**
- **Hermetic 24-Pin DIP**
- **Polycrystalline Silicon Fuses for Higher Fuse Reliability**

The Intel® 3608/3628 are fully decoded 8192-bit PROMs organized as 1024 words by 8 bits. The worst case access time of 80 ns is specified over the 0°C to 75°C temperature range and 5% V_{CC} power supply tolerances. There are four chip selects provided to facilitate expanding 3608/3628s into larger PROM arrays. The PROMs use Schottky clamped TTL technology with polycrystalline silicon fuses. All outputs are initially high and logic low levels can be electrically programmed in selected bit locations.

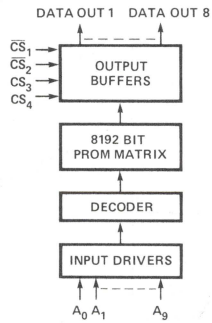
Prior to the 8192 bit 3608/3628, the highest density bipolar PROM available was 4096 bits. The high density of the 3608/3628 now easily doubles the capacity without an increase in area on existing designs currently using 512 words by 8 bit PROMs. There is also little, if any, penalty in power since the 3608/3628 power/bit is approximately one-half that of 4K PROMs. The 3608/3628 are packaged in a hermetic 24-pin dual in-line package.

PIN CONFIGURATION

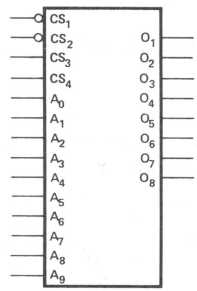


*PROGRAMMING PIN

BLOCK DIAGRAM



LOGIC SYMBOL



PIN NAMES

$A_0 - A_9$	ADDRESS INPUTS
$\overline{CS}_1 - \overline{CS}_2$, $CS_3 - CS_4$	CHIP SELECT INPUTS[1]
$O_1 - O_8$	DATA OUTPUTS

[1] To select the PROM $\overline{CS}_1 = \overline{CS}_2 = V_{IL}$ and $CS_3 = CS_4 = V_{IH}$

PROGRAMMING

The programming specifications are described on page 4-89 of the 1978 Data Catalog.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . -65°C to +125°C
Storage Temperature . . . . . -65°C to +160°C
Output or Supply Voltages . . . . . -0.5V to 7 Volts
All Input Voltages . . . . . -1V to 5.5V
Output Currents 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS: All Limits Apply for V_{CC} = +5.0V ±5%, T_A = 0°C to +75°C

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.[1]	Max.	Unit	
I_{FA}	Address Input Load Current		-0.05	-0.25	mA	V_{CC}=5.25V, V_A=0.45V
I_{FS}	Chip Select Input Load Current		-0.05	-0.25	mA	V_{CC}=5.25V, V_S=0.45V
I_{RA}	Address Input Leakage Current			40	μA	V_{CC}=5.25V, V_A=5.25V
I_{RS}	Chip Select Input Leakage Current			40	μA	V_{CC}=5.25V, V_S4.0V
V_{CA}	Address Input Clamp Voltage		-0.9	-1.5	V	V_{CC}=4.75V, I_A=-10mA
V_{CS}	Chip Select Input Clamp Voltage		-0.9	-1.5	V	V_{CC}=4.75V, I_S=-10mA
V_{OL}	Output Low Voltage		0.3	0.45	V	V_{CC}=4.75V, I_{OL}= 10mA
I_{CEX}	3608 and 3608-4 Output Leakage Current			100	μA	V_{CC}=5.25V, V_{CE}=5.25V
I_{CC}	Power Supply Current		150	190	mA	V_{CC} =5.25V, V_{A0}→V_{A9}=0V, PROM deselected
V_{IL}	Input "Low" Voltage			0.85	V	V_{CC}=5.0V
V_{IH}	Input "High" Voltage	2.0			V	V_{CC}=5.0V

3628,3628-4 ONLY

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
$\|I_O\|$	Output Leakage for High Impedance State			100	μA	V_O=5.25V or 0.45V, V_{CC}=5.25V, $\overline{CS}_1$=$\overline{CS}_2$=2.4V
I_{SC}[2]	Output Short Circuit Current	-20	-25	-80	mA	V_O = 0V
V_{OH}	Output High Voltage	2.4	3.4		V	I_{OH}=-2.4mA, V_{CC} = 4.75V

NOTES: 1. Typical values are at 25°C and at nominal voltage.
2. Unmeasured outputs are open during this test.

A.C. CHARACTERISTICS V_{CC} = +5V ±5%, T_A = 0°C to +75°C

SYMBOL	PARAMETER	MAX. LIMITS 3608 3628	MAX. LIMITS 3608-4 3628-4	UNIT	CONDITIONS
t_A	Address to Output Delay	80	100	ns	$\overline{CS}_1 = \overline{CS}_2 = V_{IL}$
t_{EN}	Output Enable Time	40	45	ns	and $CS_3 = CS_4 = V_{IH}$
t_{DIS}	Output Disable Time	40	45	ns	to select the PROM.

CAPACITANCE [1] T_A = 25°C, f = 1 MHz

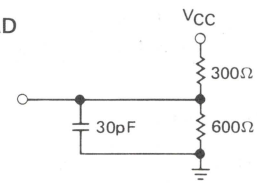
SYMBOL	PARAMETER	TYP. LIMITS TYP.	TYP. LIMITS MAX.	UNIT	TEST CONDITIONS
C_{INA}	Address Input Capacitance	4	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{INS}	Chip-Select Input Capacitance	6	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{OUT}	Output Capacitance	7	15	pF	V_{CC} = 5V V_{OUT} = 2.5V

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

SWITCHING CHARACTERISTICS

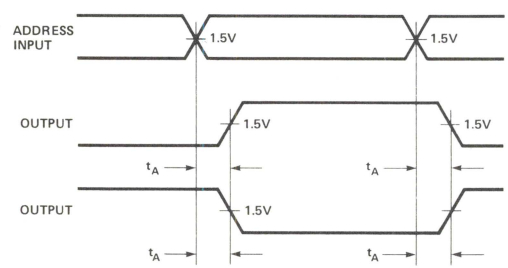
Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 15 mA and 30 pF
Frequency of test - 2.5 MHz

15mA TEST LOAD

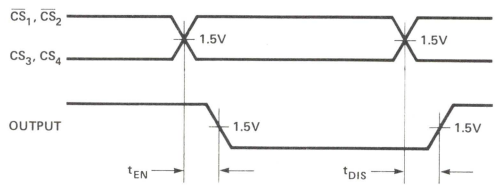


WAVEFORMS

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY



PROM AND ROM PROGRAMMING INSTRUCTIONS

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III. BIPOLAR PROM PROGRAMMING 4-89

I. PROM AND ROM INPUT FORMATS

A. Acceptible Formats

Intel can accept programming and masking information for PROMs, EPROMs, or ROMs in the form of floppy disk, punched paper tape, a master device from which to copy, or computer punched cards. The allowable formats are given in Table 1. The preferred formats for the paper tape and computer card input media are the Intel Intellec Hex and BPNF since these formats are defined to allow detection of errors.

It is desirable that two, preferably different, input media for each customer code be sent so Intel can perform a code verification to detect any errors between the two inputs. This procedure, if followed, can avoid errors due to a mispunched tape/card or sending a defective or improper master device.

All orders must be accompanied by a customer PROM/ROM order form. A copy of the form is contained in this section and additional copies are available from Intel Literature Department, 3065 Bowers Ave., Santa Clara, California 95051.

Table I. Acceptable Formats

Floppy Disk	Paper Tape	Computer Card	Master Device
• Intel Microcomputer Development System Single or Double Density Disk	• Intellec Hex • BPNF • Hex	• Intellec Hex • PN	• Same Density and Pin Compatible to Device which is to be Programmed.

A1. Logic Levels

All data field for Intel's EPROMs/PROMs/ROMs are positive logic. The only exceptions are the 4001 and 4308 ROMs which use negative logic. For the 4001/4308, an "0" is a high output and a "1" is a low output. Consequently, because the BPNP format specifies the voltage level at the output of the device, it is necessary to input an "0" and "1" in the 4001/4308 instruction code as a "P" and "N" respectively. However, for the Hex format, the 4001/4308 input should be specified according to the instruction code logic state, i.e., a "1" or "0." The below example shows the corresponding input for 4001 instruction codes. For comparison, the input for an 8080A is also given as an example.

1. 4001 Instruction Code

4001 Instruction Mnemonic	4001 Instruction Code	Intellec Hex Or Non-Intellec Hex Input	BPNF Input
NOP	0000 0000	00	BPPPPPPPPF
WRM	1110 0000	E0	BNNNPPPPPF

2. 8080A Instruction Code

Instruction Mnemonic	Instruction Code	Intellec Hex Or Non-Intellec Hex Input	BPNF Input
JMP	1100 0011	C3	BPPNNNNPPF
Push D	1101 0101	D5	BPPNPNPNPF

B. Paper Tape Format

The paper tape which should be used is 1" wide paper using 7 or 8-bit ASCII code (such as a Model 33 ASR Teletype produces). The three paper tape formats which should be sent are described in Sections B1 through B3.

B1. Intellec Hex Paper Tape Format

In the Intel Intellec Hex Format, a data field can contain either 8 or 4-bit data. *Two* ASCII hexadecimal characters must be used to represent *both* 8 and 4-bit data. In the case of 4-bit data, only one of the characters is meaningful and must be specified on the Intel PROM/ROM Order Form.

Preceding the first data field and following the last data field there must be a leader/trailer length of at least 25 null characters. Comments (except for a colon) may be placed on the tape leader.

The format described below is readily generated by the Intel Intellec Microcomputer Development System or by systems programmed by the user.

1. RECORD MARK FIELD: Frame 0

   The ASCII code for a colon (:) is used to signal the start of a record.

2. RECORD LENGTH FIELD: Frames 1 and 2

   The number of data bytes in the record is representated by two ASCII hexadecimal digits in this field. The high-order digit is in frame 1. The maximum number of data bytes in a record is 255 (FF in hexadecimal). An end-of-file record contains two ASCII zeros in this field.

3. LOAD ADDRESS FIELD: Frames 3–6

   The four ASCII hexadecimal digits in frames 3–6 give the address at which the data is loaded. The high-order digit is in frame 3, the lower-order digit in frame 6. The first data byte is stored in the location indicated by the load address; successive bytes are stored in successive memory locations. This field in an end-of-file record contains zeros or the starting address of the program.

4. RECORD TYPE FIELD: Frames 7 and 8

   The two ASCII hexadecimal digits in this field specify the record type. The high-order digit is in frame 7. All data records are type 0; end-of-file records are type 1. Other possible values for this field are reserved for future expansion.

5. DATA FIELD: Frames 9 to 9+2*(record length)–1

   A data byte is represented by two frames containing the ASCII characters 0–9 or A–F, which represent a hexadecimal value between 0 and FF (0 and 255 decimal). The high-order digit is in the first frame of each pair. If the data is 4-bit, then either the high or low-order digit represents the data and the other digit of the pair may be any ASCII hexadecimal digit. There are no data bytes in an end-of-file record.

6. CHECKSUM FIELD: Frames 9+2*(record length) to 9+2*(record length)+1

   The checksum field contains the ASCII hexadecimal representation of the two's complement of the 8-bit sum of the 8-bit bytes that result from converting each pair of ASCII hexadecimal digits to one byte of binary, from the record length field to and including the last byte of the data field. Therefore, the sum of all the ASCII pairs in a record after converting to binary, from the record length field to and including the checksum field, is zero.

Intellec Hex Example:

```
: 10310000311A320E03117E31CD40003A9231B7C2EE
: 1031100060310E00117031CD40003A9231B7C2607B
: 10312000312A7E31227A310E03117E31CD40003AB0
: 103130009231B7C260312A8C317CB5CA50310E044D
: 10314000118831CD40003A9231B7C26031C3273186
: 103150000E01117A31CD40000E09119031CD4000A1
: 103160000E0C119231CD40000E09119031CD40006E
: 0A3170007E3196310100000092311B
: 10317C0092310100963180008C31923100009631F1
: 04318E0092319231B7
: 02319400923176
: 00310001CE
```

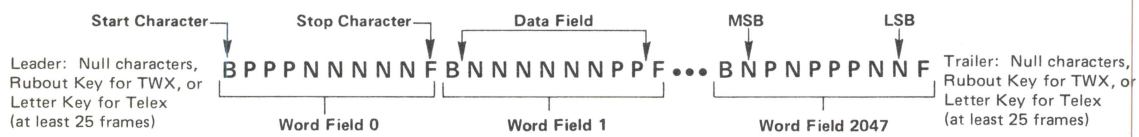
B2. BPNF Paper Tape Format

The format requirements are as follows:

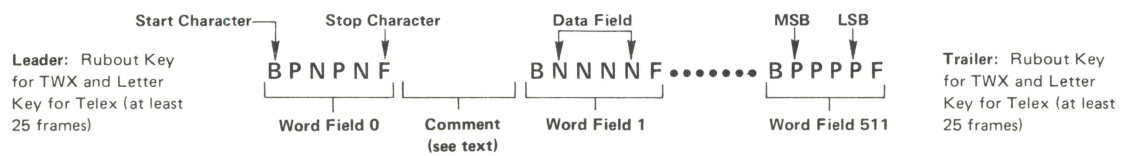
1. All data fields are to be punched in consecutive order, starting with data field 0 (all addresses low). There must be exactly N data fields for a N x 8 or N x 4 device organizations.
2. Each data field must begin with the start character B and end with the stop character F. There must be exactly 8 or 4 data characters between the B and F for a N x 8 or N x 4 organization, respectively.

   NO OTHER CHARACTERS, SUCH AS RUBOUTS, ARE ALLOWED ANYWHERE IN A DATA FIELD. If in preparing a tape an error is made, the entire data field, including the B and F must be rubbed out. *Within the data field, a P results in a high level output, and an N results in a low level output.*
3. Preceding the first data field and following the last data field, there must be a leader/trailer length of at least 25 characters. This should consist of rubout punches (letter key for Telex tapes) or null characters.
4. Between data fields, comments not containing B's or F's may be inserted. Carriage return and line feed characters should be inserted (as a "comment") after each 72 characters. When these carriage returns, etc., are inserted, the tape may be easily listed on the teletype for purposes of error checking. The customer may also find it helpful to insert the word number (as a comment) at least every four word fields.
5. Included in the tape before the leader should be the customer's complete Telex or TWX number and if more than one pattern is being transmitted, the device pattern number.
6. MSB and LSB are the most and least significant bit of the device outputs. Refer to the data sheet for the pin numbers.

Example of BPNF 2048 x 8 format (N = 2048):



Example of 512 x 4 format (N = 512):



B3. Non-Intellec Hex Paper Tape Format

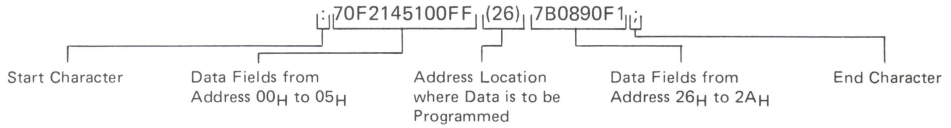
For the non-Intellec Hex Format, a data field can contain either 8 or 4-bit data. *Two* ASCII hexadecimal characters must be used to represent *both* 8 and 4-bit data. In the case of 4-bit data, only one of the characters is meaningful and must be specified on the Intel PROM/ROM Order Form.

Parity is allowed; however, it is not checked. Preceding the first data field and following the last data field there must be a leader/trailer length of at least 25 null characters or rubout punches.

The format requirements are as follows:

1. The start of the first data field is indicated by a colon. After the last data field, a semicolon must be punched to indicate the end. All data fields are to be punched in consecutive order, starting with data field 00_H (all addresses low).
2. *Two* hex characters must be used to represent the data field of both N word x 8-bit and N word x 4-bit devices. For an 8-bit data field, the high order data is represented by the left justified character of the pair. Either character of the pair may be used to represent the word field of a N word x 4-bit device, however, it must be consistent throughout the word field. The other character may be any hex character.

   A field of "don't care" data is allowed. Data after a field of "don't care" will be programmed starting at an address location enclosed in parentheses. In the following example, data is entered in addresses 00_H to 05_H, followed with "don't care" from addresses 06_H to 25_H, data being entered again starting at address location 26_H, and followed with "don't care" data to the last address location.



3. The x character may be used to rubout any erroneous character(s). The # character may be used to rubout an entire line up to the previous carriage return.
4. Spaces are allowed only between *separate* word fields.
5. After each 72 characters, a carriage return followed by a line feed should be punched to allow a print-out of the tape.
6. Comments must be placed only between the tape leader and the start of the first data field.

C. Computer Punched Card Format

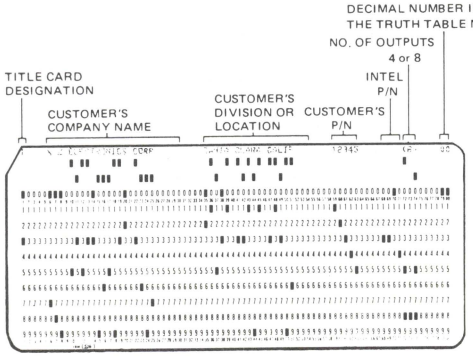
The following general format is applicable to the programming information sent on computer punched cards:

1. An 80 column Hollerith card (interpreted) punched on an IBM 026 or 029 keypunch should be submitted.
2. A single deck must consist of a Title Card followed by the data cards. There will be N/8 or N/14 data cards for N words x 8-bit and N words x 4-bit devices, respectively, in the PN format.

   For the Intellec Hex format, there will be N/32 data cards for both N words x 8-bit and N words x 4-bit devices, and one end of file card.

C1. Intellec Hex Computer Punched Card Format

Two hex characters must be used to represent data for both a N word x 8-bit and N word x 4-bit device. For the latter, only one of the characters is meaningful and must be specified on the Intel PROM/ROM Order Form. The entire data field for all bits must be punched even if it is "don't care".



Column	Data
1	Punch a T
2–3	Blank
4–28	Customer Company Name
29–30	Blank
31–50	Customer's Company Division or location
51–52	Blank
53–61	Customer Part Number
62–63	Blank
64–72	Punch the Intel 4-digit basic part number and in ( ) the number of output bits; e.g., 2708 (8), 2316 (8), or 3605 (4)
73–74	Blank
75–76	Chip number for ROMs with programmable chip select inputs. If not applicable, leave blank.
77–78	Blank
79–80	Punch a 2-digit decimal number to indicate truth table number. The first truth table will be 00, second 01, third 02, etc.

a. N word x 8-bit device

Column	Data
1	Record mark: A colon is used to signal the start of a record.
2–3	Record length: This is the count of the actual data bytes in the record. Column 2 contains the high order digit of the count, Column 3 contains the low order digit. A record length of zero indicates end of file. All frames containing data will have a maximum record length of 10_{HEX} bytes (16 decimal).
4–7	Load address: The four characters starting addresses at which the following data will be loaded. The high order digit of the load address is in Column 4 and the low order digit is in Column 7. The first data byte is stored in the location indicated by the load address. Successive data bytes are stored in successive memory locations. ROMs containing more than 16 bytes of data will use two or more records or cards to transmit the data. Although the load address for the beginning record need not be 0000, each subsequent load address should be "10_H" (16 decimals) greater than the last.
8–9	Record type: A 2-digit code in this field specifies the type of this record. The high order digit of this code is located in Column 8. Currently, all data records are type 0. End-of-file records will be type 1; they are distinguished by a zero RECORD LENGTH field (see above). Other possible values for this field are reserved for future expansion.
10–73	Data
75–75	Checksum: Same as paper tape format.
76–78	Blank
79–80	Punch same 2-digit decimal number as in Title Card.

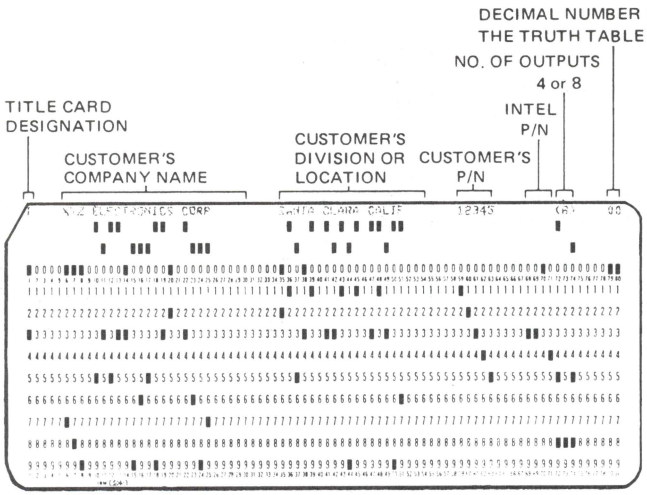
b. N word x 4-bit device

This format is identical to the previously documented 8-bit hexadecimal format with the following exceptions:

Column	Data
10–73	Each memory location is represented by two columns containing the characters 0–9, A–F. Since this is 4-bit data, the user must indicate which character of each pair is to be used as valid data. A single deck must be submitted without mixing first and second characters of the pair.

C2. PN Computer Punched Card Format

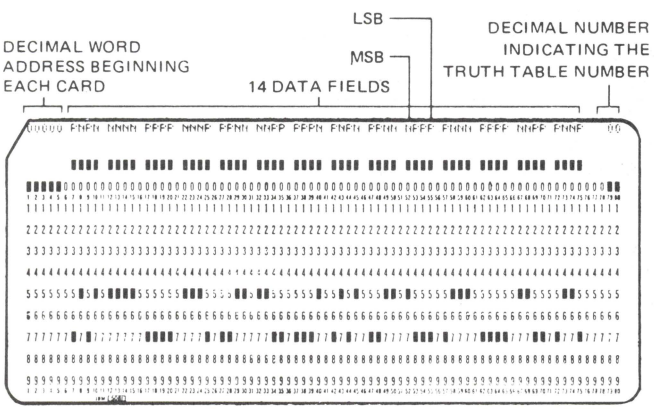
A word field consists of only P's and N's. A punched P will result in an output high level and a punched N in an output low level. The B and F characters, unlike the paper tape format, are illegal characters. The entire data field for all bits must be punched even if it is "don't care". The data field must begin in consecutive order, starting with address 0 (all addresses logically low).



Column	Data
1	Punch a T
2–3	Blank
4–28	Customer Company Name
29–30	Blank
31–50	Customer's Company Division or location
51–52	Blank
53–61	Customer Part Number
62–63	Blank
64–72	Punch the Intel 4-digit basic part number and in ( ) the number of output bits; e.g., 2708 (8), 2316 (8), or 3605 (4)
73–74	Blank
75–76	Chip number for ROMs with programmable chip select inputs. If not applicable, leave blank.
77–78	Blank
79–80	Punch a 2-digit decimal number to indicate truth table number. The first truth table will be 00, second 01, third 02, etc.

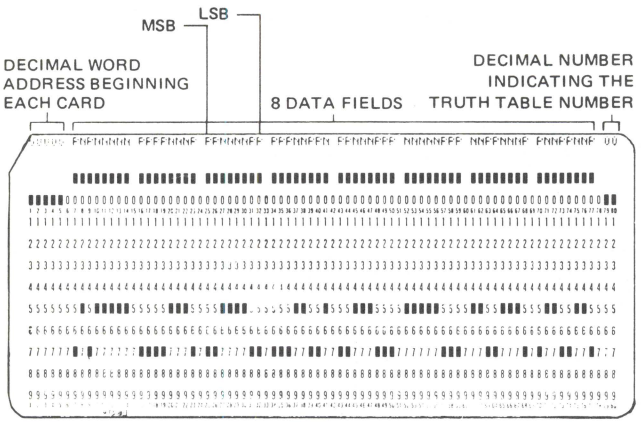
Title Card Format.

For a N words X 4-bit organization only, cards 2 and those following should be punched as shown. Each card specifies the 4-bit output of 14 words.



Column	Data
1-5	Punch the 5 digit decimal equivalent of the binary coded location which begins each card. The address is right justified, i.e., ØØØØØ, ØØØ14, ØØØ28, etc.
6	Blank
7-10	Data Field
11	Blank
12-15	Data Field
16	Blank
17-20	Data Field
21	Blank
22-25	Data Field
26	Blank
27-30	Data Field
31	Blank
32-35	Data Field
36	Blank
37-40	Data Field
41	Blank
42-45	Data Field
46	Blank
47-50	Data Field
51	Blank
52-55	Data Field
56	Blank
57-60	Data Field
61	Blank
62-65	Data Field
66	Blank
67-70	Data Field
71	Blank
72-75	Data Field
76-78	Blank
79-80	Punch same 2 digit decimal number as in title card.

For a N words X 8-bit organization only, cards 2 and those following should be punched as shown. Each card specifies the 8-bit output of 8 words.



Column	Data
1-5	Punch the 5 digit decimal equivalent of the binary coded location which begins each card. The address is right justified, i.e., ØØØØØ, ØØØØ8, ØØØ16, etc.
6	Blank
7-14	Data Field
15	Blank
16-23	Data Field
24	Blank
25-32	Data Field
33	Blank
34-41	Data Field
42	Blank
43-50	Data Field
51	Blank
52-59	Data Field
60	Blank
61-68	Data Field
69	Blank
70-77	Data Field
78	Blank
79-80	Punch same 2 digit decimal number as in title card.

D. Custom PROM/ROM Order Forms

All orders for PROMs/ROMs which are to be electrically or mask programmed at Intel must be submitted with the order forms shown on the following pages. Additional forms are available from Intel Literature Department, 3065 Bowers Ave., Santa Clara, California 95051.

The order forms for the individual PROMs/ROMs are listed in Table II below.

Table II

PROM/ROM Part Number	Order Form Number
MOS EPROMs	A
8741, 8748, 8755	A
2316E, 8316A, 8316AL, 2616	B
2332, 2364	B
8041, 8048	C
2608, 8308	D
8355	E
Bipolar PROMs	F

CUSTOMER EPROM ORDER FORM A

Company _____ Phone # _____

Company Contact _____ Date _____

P.O. # _____ Intel Device P/N _____

For Intel Use Only

S# _____

STD _____

APP _____

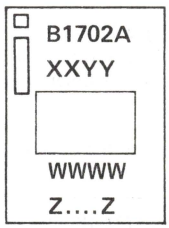
Date _____

All custom MOS EPROM orders must be submitted on this form. Programming information should be sent per the formats described in the Programming Instruction section of the Intel Data Catalog. Additional forms are available from Intel.

MARKING

The marking will consist of the Intel Logo, the product and package type (B1702A), the 4-digit Intel pattern number (WWWW), an internal manufacturing traceability code (XXYY), and the customer part number (Z....Z). The customer part number is limited to a maximum of 9 digits or spaces.

1



1702A MARKING EXAMPLE

FLOPPY DISK

Programming information may be sent on Intel Microcomputer Development System Floppy Disk. When using this input medium the floppy disk file name should be indicated in the Customer Part Number Section below. The type of floppy disk sent should also be indicated by checking one of the appropriate boxes:

☐ Single Density ☐ Double Density

CUSTOMER PART NUMBER

	Customer P/N (Please Fill-In)	Floppy Disk File Name (Please Fill-In)	Intel Pattern Number (Please Do Not Use)
1.			
2.			
3.			
4.			
5.			
6.			
7.			
8.			
9.			
10.			
11.			
12.			
13.			
14.			
15.			
16.			
17.			
18.			
19.			

CUSTOMER 16K, 32K, and 64K ORDER FORM
B

Company _____ Phone # _____

Company Contact _____ Date _____

P.O. # _____ Intel P/N & Pkg _____

For Intel Use Only

S# _____

STD _____

APP _____

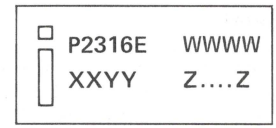
Date _____

A custom 16K/32K/64K ROM order must be submitted on this form. Programming information should be sent per the formats described in the Programming Instruction section of the Intel Data Catalog. Additional forms are available from Intel.

MARKING

The marking will consist of the Intel Logo, the product and package type (P2316E), the 4-digit Intel pattern number (WWWW), a date code (XXYY), and the customer part number (Z....Z). The customer part number is limited to a maximum of 9 digits or spaces.

When authorized by the customer to ship 2616 PROMs against a 2316E order, the PROMs are marked with the dual part number 2616/2316E.



1

P2316E MARKING EXAMPLE

IMPORTANT MASK OPTION SPECIFICATION

The 2316E, 8316A, and 8316AL chip select inputs are mask programmable and must be specified by the user. The chip select logic levels must be specified with one of the below Chip Numbers. The Chip Number will be coded in terms of positive logic where a logic "1" is a high level input. It should be noted that Chip Number 4 for the 2316E is compatible to Intel's 2716 EPROM and 2616 PROM.

Chip Number	CS3	CS2	CS1
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

FLOPPY DISK

Programming information may be sent on Intel Microcomputer Development System Floppy Disk. When using this input medium the floppy disk file name should be indicated in the Customer Part Number Section below. The type of floppy disk sent should also be indicated by checking one of the appropriate boxes:

☐ Single Density ☐ Double Density

CUSTOMER PART NUMBER

	Customer P/N (Please Fill-In)	16K ROM Chip Number (Please Fill-In)	Floppy Disk File Name (Please Fill-In)	Intel Pattern Number (Please Do Not Use)
1.				
2.				
3.				
4.				
5.				
6.				
7.				
8.				

CUSTOMER 8041, 8048 ROM ORDER FORM
C

Company _____ Phone # _____

Company Contact _____ Date _____

P.O. # _____ Package Type: ☐ Plastic ☐ Cerdip

For Intel Use Only

S# _____

STD _____

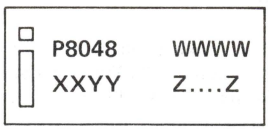
APP _____

Date _____

All custom 8041 and 8048 orders be submitted on this form. Programming information should be sent per the formats described in the Programming Instruction section of the Intel Data Catalog. Additional forms are available from Intel.

MARKING

All devices will be marked as shown at the right figure. The marking will consist of the Intel Logo, the product and package type (P8048), the 4-digit Intel pattern number (WWWW), a date code (XXYY), and the customer part number (Z....Z). The customer part number is limited to a maximum of 9 digits or spaces.



1

P8048 MARKING EXAMPLE

FLOPPY DISK

Programming information may be sent on Intel Microcomputer Development System Floppy Disk. When using this input medium the floppy disk file name should be indicated in the Customer Part Number Section below. The type of floppy disk sent should also be indicated by checking one of the appropriate boxes:

☐ Single Density ☐ Double Density

CUSTOMER PART NUMBER

	Customer P/N (Please Fill-In)	Floppy Disk File Name (Please Fill-In)	Intel Pattern Number (Please Do Not Use)
1.			
2.			
3.			
4.			
5.			
6.			
7.			
8.			
9.			
10.			
11.			
12.			
13.			
14.			
15.			
16.			
17.			
18.			
19.			
20.			

CUSTOMER 8K ROM ORDER FORM D

Company _____ Phone # _____

Company Contact _____ Date _____

P.O. # _____ Intel P/N & Pkg _____

For Intel Use Only

S# _____

STD _____

APP _____

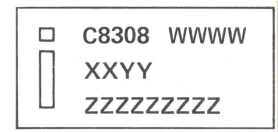
Date _____

All custom 8K ROM orders must be submitted on this form. Programming information should be sent per the formats designated on this order form. Additional forms are available from Intel.

MARKING

The marking will consist of the Intel logo, the product type (C8308), the 4-digit Intel pattern number (WWWW), a date code (XXYY), and a maximum 9-digit number (Z....Z) which is specified by the user. The 9-digit number may be a part number or the chip number.

When authorized by the customer to ship 2608 PROMs against a 2308/8308 order, the PROMs are marked with the dual part number 2608/2308 or 2608/8308.



1

C8308 MARKING EXAMPLE

IMPORTANT MASK OPTION SPECIFICATION

The 2308/8308 CS_2 chip select input is mask programmable and must be specified by the user. The chip select logic level must be specified with one of the below Chip Numbers. The Chip Number will be coded in terms of positive logic where a "1" is a high level input. It should be noted that Chip Number 0 for the 2308/8308 is compatible to Intel's 2708 EPROM and 2608 PROM.

Chip Number	CS_1 (non-programmable)	CS_2 (programmable)
0	0	0
1	0	1

FLOPPY DISK

Programming information may be sent on Intel Microcomputer Development System Floppy Disk. When using this input medium the floppy disk file name should be indicated in the Customer Part Number Section below. The type of floppy disk sent should also be indicated by checking one of the appropriate boxes:

☐ Single Density ☐ Double Density

CUSTOMER PART NUMBER

	Customer P/N (Please Fill-In)	Chip Number (Please Fill-In)	Floppy Disk File Name (Please Fill-In)	Intel Pattern Number (Please Do Not Use)
1.		1.	1.	1.
2.		2.	2.	2.
3.		3.	3.	3.
4.		4.	4.	4.
5.		5.	5.	5.
6.		6.	6.	6.
7.		7.	7.	7.
8.		8.	8.	8.
9.		9.	9.	9.
10.		10.	10.	10.
11.		11.	11.	11.
12.		12.	12.	12.

CUSTOMER 8355 ROM ORDER FORM E

Company _____ Phone # _____

Company Contact _____ Date _____

P.O. # _____ Package Type: ☐ Plastic ☐ Cerdip

For Intel Use Only

S# _____

STD _____

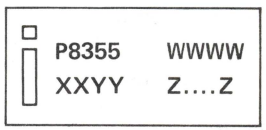
APP _____

Date _____

All custom 8355 orders must be submitted on this form. Programming information should be sent per the formats described in the Programming Instruction section of the Intel Data Catalog. Additional forms are available from Intel.

MARKING

All devices will be marked as shown at the right figure. The marking will consist of the Intel Logo, the product and package type (P8355), the 4-digit Intel pattern number (WWWW), a date code (XXYY), and the customer part number (Z....Z). The customer part number is limited to a maximum of 9 digits or spaces.



1

P8355 MARKING EXAMPLE

FLOPPY DISK

Programming information may be sent on Intel Microcomputer Development System Floppy Disk. When using this input medium the floppy disk file name should be indicated in the Customer Part Number Section below. The type of floppy disk sent should also be indicated by checking one of the appropriate boxes:

☐ Single Density ☐ Double Density

CUSTOMER PART NUMBER

	Customer P/N (Please Fill-In)	Floppy Disk File Name (Please Fill-In)	Intel Pattern Number (Please Do Not Use)
1.			
2.			
3.			
4.			
5.			
6.			
7.			
8.			
9.			
10.			
11.			
12.			
13.			
14.			
15.			
16.			
17.			
18.			
19.			
20.			

CUSTOMER BIPOLAR PROM ORDER FORM F

Company _____ Phone # _____

Company Contact _____ Date _____

P.O. # _____ Intel Device P/N _____

For Intel Use Only

S# _____

STD _____

APP _____

Date _____

All custom bipolar PROM orders must be submitted on this form. Programming information should be sent per the formats described in the Programming Instruction section of the Intel Data Catalog. Additional forms are available from Intel.

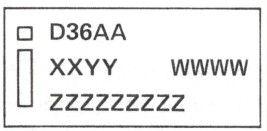
IMPORTANT HEX AND INTELLEC HEX FORMAT INFORMATION

A word field must be 8 bits in the hex format. Consequently for N words by 4-bit devices such as the 3605, it is important that you indicate by checking the box below whether the submitted tape or card deck for programming is right or left justified.

☐ Right Justified ☐ Left Justified

MARKING

All devices will be marked as shown at the right figure. The marking will consist of the Intel Logo, the product and package type (D36AA), the 4-digit Intel pattern number (WWWW), a date code (XXYY), and the customer part number (Z....Z). The customer part number is limited to a maximum of 9 digits or spaces.



1

D36AA MARKING EXAMPLE

FLOPPY DISK

Programming information may be sent on Intel Microcomputer Development System Floppy Disk. When using this input medium the floppy disk file name should be indicated in the Customer Part Number Section below. The type of floppy disk sent should also be indicated by checking one of the appropriate boxes:

☐ Single Density ☐ Double Density

CUSTOMER PART NUMBER

	Customer P/N (Please Fill-In)	Floppy Disk File Name (Please Fill-In)	Intel Pattern Number (Please Do Not Use)
1.			
2.			
3.			
4.			
5.			
6.			
7.			
8.			
9.			
10.			
11.			
12.			
13.			
14.			
15.			

II. MOS EPROMs

A. Erasure Procedure

As stated in the EPROM related data sheets, the recommended erasure procedure to use with EPROMs is to illuminate the window with a UV lamp which has a wavelength of 2537 Angstroms (Å). The data sheets specify a distance of 1 inch and erase times of 10–45 minutes, depending on the type of device and UV lamp. Actually, the amount of time required to erase a device can be concisely stated in terms of the amount of UV energy incident to the window, expressed in Watt-seconds per square centimeter (W-sec/cm^2). Table III lists the required integrated dosgae (UV intensity X exposure time) for the EPROMs currently in production by Intel.

Table III. Required Erase Energy for Device Types

Device Type	2537Å Erase Energy
1702A/4702A	6 W-sec/cm^2
2708/8708	15 W-sec/cm^2
2758, 2716	15 W-sec/cm^2
8741, 8748	15 W-sec/cm^2
8755	15 W-sec/cm^2

The erase energy expressed in Table III includes a guardband to ensure complete erasure of all bits. *It is not sufficient to monitor "first bit" erasure to determine erasure time, as some other bits in the array may not be erased.*

A1. UV Sources

There are several models of UV lamps that can be used to erase EPROMs (see Table IV). The model numbers in the table refer to lamps manufactured by Ultra Violet Products of San Gabriel, California. In addition, there are several other manufacturers, including Data I/O (Issaquah, Wash.), PROLOG (Monterey, Calif.). Prometrics (Chicago, Ill.), and Turner Designs (Mt. View, Calif.). The individual manufacturers should be consulted for detailed product descriptions. Also shown in the table are typical erase times for various combinations of Intel PROMs and lamp intensities.

Table IV.

Model	Power Rating	Minimum Erase Time for Indicated Dosage Without a Filter Over the Bulb	
		6 W-sec 1702A, 4702A	15 W-sec 2708, 8708, 8755 2758, 2716, 8748, 8741
R-52	13000 μW/cm^2	7.7 min	19.2 min
S-52	12000 μW/cm^2	8.3 min	20.7 min
S-68	12000 μW/cm^2	8.3 min	20.7 min
UVS-54	5700 μW/cm^2	17.5 min	43.8 min
UVS-11	5500 μW/cm^2	18.2 min	45.6 min

According to the manufacturers, the output of the UV lamp bulbs decrease with age. The output of the lamp should be verified periodically to ensure that adequate intensities are maintained. If this is not done, bits may be partially erased which will interfere with later programming and/or operation at high temperature.

For lamps other than those listed, the erase time can be determined by using a UV intensity meter, such as the Ultra Violet Products Model J-225. When a meter is used, the intensity should be measured at the same position (distance from the lamp) as the EPROMs to be erased. This will require careful positioning to insure that the sensor will receive the same amount of UV light that the window of the EPROM will receive.

The sensors used with most UV intensity meters show reduced output with constant exposure to UV light. Therefore, they should not be permanently placed inside the erasure enclosure, they should only be used for periodic measurements.

B. 1702A/1702AL Family Programming

The 1702A/1702AL is erased by exposure to high intensity short wave ultraviolet light at a wavelength of 2537Å. The recommended integrated dose (i.e., UV intensity X exposure time) is 6 W-sec/cm^2. An example of an ultraviolet source which can erase the 1702A/1702AL in 10 to 20 minutes is the Model S52 short wave ultraviolet lamp. The lamp should be used without short wave filters and the PROM should be placed within 1 inch away from the lamp tubes.

Initially, all 2048 bits of the PROM are in the "0" state (output low). Information is introduced by selectively programming "1"s (output high) in the proper bit locations.

Word address selection is done by the same decoding circuitry used in the READ mode. All 8 address bits must be in the binary complement state when pulsed V_{CC} and V_{GG} move to their negative levels. The addresses must be held in their binary complement state for a minimum of 25 μsec after V_{DD} and V_{GG} have moved to their negative levels. The addresses must then make the transition to their true state a minimum of 10 μsec before the program pulse is applied. The addresses should be programmed in the sequence 0 through 255 for a minimum of 32 times. The eight output terminals are used as data inputs to determine the information pattern in the 8 bits of each word. A low data input level (–48V) will program a "1" and a high data input level (ground) will leave a "0". All 8 bits of one word are programmed simultaneously by setting the desired bit information patterns on the data input terminals.

During the programming, V_{GG}, V_{DD} and the Program Pulse are pulsed signals. See page 4-12 for required pin connections during programming.

1702A, 1702AL

D.C. and Operating Characteristics for Programming Operation

T_A = 25°C, V_{CC} = 0V, V_{BB} = + 12V ±10%, $\overline{CS}$ = 0V unless otherwise noted

Symbol	Test	Min.	Typ.	Max.	Unit	Conditions
I_{LI1P}	Address and Data Input Load Current			10	mA	V_{IN} = -48V
I_{LI2P}	Program and V_{GG} Load Current			10	mA	V_{IN} = -48V
I_{BB}[1]	V_{BB} Supply Load Current		10		mA	
I_{DDP}[2]	Peak I_{DD} Supply Load Current		200		mA	V_{DD} = V_{PROG} = -48V, V_{GG} = -35V
V_{IHP}	Input High Voltage			0.3	V	
V_{IL1P}	Pulsed Data Input Low Voltage	-46		-48	V	
V_{IL2P}	Address Input Low Voltage	-40		-48	V	
V_{IL3P}	Pulsed Input Low V_{DD} and Program Voltage	-46		-48	V	
V_{IL4P}	Pulsed Input Low V_{GG} Voltage	-35		-40	V	

Notes: 1. The V_{BB} supply must be limited to 100mA max. current to prevent damage to the device.
2. I_{DDP} flows only during V_{DD}, V_{GG} on time. I_{DDP} should not be allowed to exceed 300mA for greater than 100μsec. Average power supply current I_{DDP} is typically 40mA at 20% duty cycle.

1702A, 1702AL
A.C. Characteristics for Programming Operation

$T_{AMBIENT}$ = 25°C, V_{CC} = 0V, V_{BB} = + 12V ±10%, $\overline{CS}$ = 0V unless otherwise noted

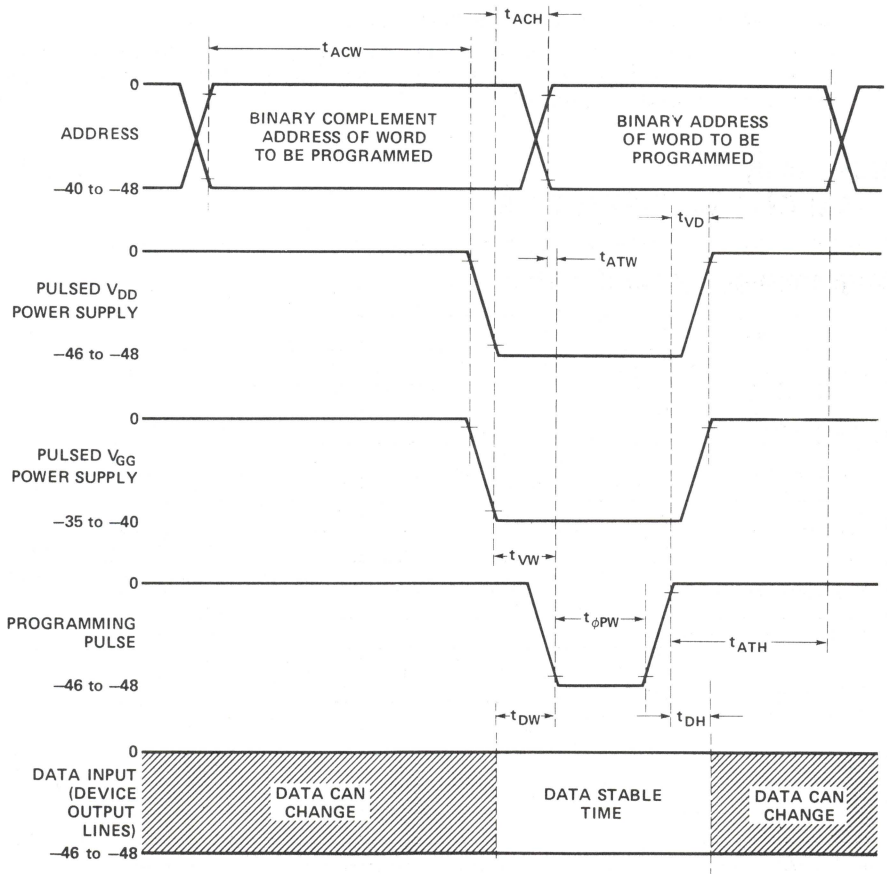
Symbol	Test	Min.	Typ.	Max.	Unit	Conditions
	Duty Cycle (V_{DD}, V_{GG})			20	%	
$t_{\phi PW}$	Program Pulse Width		2	3	ms	V_{GG} = -35V, V_{DD} = V_{PROG} = -48V
t_{DW}	Data Set-Up Time	25			μs	
t_{DH}	Data Hold Time	10			μs	
t_{VW}	V_{DD}, V_{GG} Set-Up	100			μs	
t_{VD}	V_{DD}, V_{GG} Hold	10		100	μs	
t_{ACW}	Address Complement Set-Up	25			μs	
t_{ACH}	Address Complement Hold	25			μs	
t_{ATW}	Address True Set-Up	10			μs	
t_{ATH}	Address True Hold	10			μs	

PROGRAM WAVEFORMS

Conditions of Test:

Input pulse rise and fall times ≤ 1μsec

$\overline{CS}$ = 0V



C. 2708/2704 Family Programming

Initially, and after each erasure, all 8192/4096 bits of the 2708/2704 are in the "1" state (output high). Information is introduced by selectively programming "0" into the desired bit locations. A programmed "0" can only be changed to a "1" by UV erasure.

The circuit is set up for programming operation by raising the CS/WE input (pin 20) to +12V. The word address is selected in the same manner as in the read mode. Data to be programmed are presented, 8 bits in parallel, to the data output lines (O_1–O_8). Logic levels for address and data lines and the supply voltages are the same as for the read mode. After address and data set up, one program pulse per address is applied to the program input (pin 18). One pass through all addresses is defined as a program loop. The number of loops (N) required is a function of the program pulse width (t_{PW}) according to N x t_{PW} $\geqslant$ 100 ms.

The width of the program pulse is from 0.1 to 1 ms. The number of loops (N) is from a minimum of 100 (t_{PW} = 1 ms) to greater than 1000 (t_{PW} = 0.1 ms). There must be N successive loops throuhg all 1024 addresses. *It is not permitted to apply N program pulses to an address and then change to the next address to be programmed.* Caution should be observed regarding the end of a program sequence. The CS/WE falling edge transition must occur before the first address transition when changing from a program to a read cycle. The program pin should also be pulled down to V_{ILP} with an active instead of a passive device. This pin will source a small amount of current (I_{ILL}) when CS/WE is at V_{IHW} (12V) and the program pulse is at V_{ILP}.

Programming Examples (Using N x t_{PW} $\geqslant$ 100 ms)

Example 1: All 8096 bits are to be programmed with a 0.5 ms program pulse width.

The minimum number of program loops is 200. One program loop consists of words 0 to 1023.

Example 2: Words 0 to 100 and 500 to 600 are to be programmed. All other bits are "don't care". The program pulse width is 0.75 ms.

The minimum number of program loops is 133. One program loop consists of words 0 to 1023. The data entered into the "don't care" bits should be all 1's.

Example 3: Same requirements as example 2, but the PROM is now to be *updated* to include data for words 750 to 770.

The minimum number of program loops is 133. One program loop consists of words 0 to 1023. The data entered into the "don't care" bits should be all 1's. Addresses 0 to 100 and 500 to 600 must be re-programmed with their original data pattern.

2704, 2708 Family
PROGRAM CHARACTERISTICS

T_A = 25°C, V_{CC} = 5V ±5%, V_{DD} = +12V ±5%, V_{BB} = −5V ±5%, V_{SS} = 0V, Unless Otherwise Noted.

D.C. Programming Characteristics

Symbol	Parameter		Min.	Typ.	Max.	Units	Test Conditions
I_{LI}	Address and CS/WE Input Sink Current				10	μA	V_{IN} = 5.25V
I_{IPL}	Program Pulse Source Current				3	mA	
I_{IPH}	Program Pulse Sink Current				20	mA	
I_{DD}	V_{DD} Supply Current	2708, 2704		50	65	mA	Worst Case Supply Currents[1]: All Inputs High CS/WE = 5V; T_A = 0°C
		2708L		21	28	mA	
I_{CC}	V_{CC} Supply Current	2708, 2704		6	10	mA	
		2708L		2	4	mA	
I_{BB}	V_{BB} Supply Current	2708, 2704		30	45	mA	
		2708L		10	14	mA	
V_{IL}	Input Low Level (except Program)		V_{SS}		0.65	V	
V_{IH}	Input High Level For all Addresses and Data	2708, 2704	3.0		V_{CC} + 1	V	
		2708L	2.2		V_{CC} + 1	V	
V_{IHW}	CS/WE Input High Level		11.4		12.6	V	Referenced to V_{SS}
V_{IHP}	Program Pulse High Level		25		27	V	Referenced to V_{SS}
V_{ILP}	Program Pulse Low Level		V_{SS}		1	V	$V_{IHP} - V_{ILP}$ 25V min.

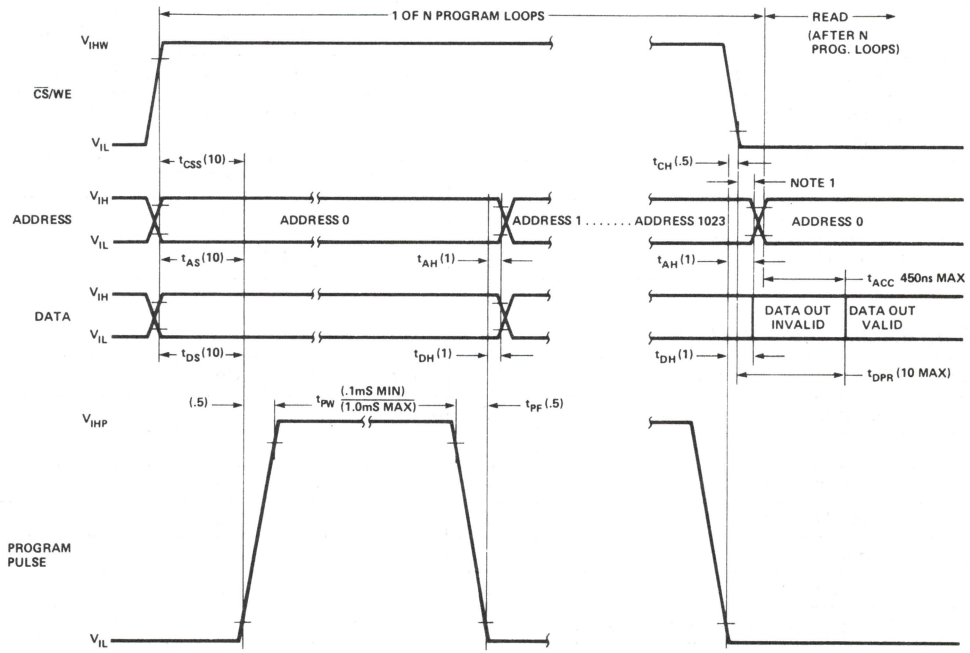
Note 1. I_{BB} for the 2708L is specified in the programmed state and is 18 mA maximum in the unprogrammed state.

A.C. Programming Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{AS}	Address Setup Time	10			μs
t_{CSS}	$\overline{CS}$/WE Setup Time	10			μs
t_{DS}	Data Setup Time	10			μs
t_{AH}	Address Hold Time	1			μs
t_{CH}	$\overline{CS}$/WE Hold Time	.5			μs
t_{DH}	Data Hold Time	1			μs
t_{DF}	Chip Deselect to Output Float Delay	0		120	ns
t_{DPR}	Program To Read Delay			10	μs
t_{PW}	Program Pulse Width	.1		1.0	ms
t_{PR}	Program Pulse Rise Time	.5		2.0	μs
t_{PF}	Program Pulse Fall Time	.5		2.0	μs

NOTE: Intel's standard product warranty applies only to devices programmed to specifications described herein.

2704, 2708 Family
Programming Waveforms



NOTE 1. THE $\overline{CS}$/WE TRANSITION MUST OCCUR AFTER THE PROGRAM PULSE TRANSITION AND BEFORE THE ADDRESS TRANSITION.

NOTE 2. NUMBERS IN ( ) INDICATE MINIMUM TIMING IN μS UNLESS OTHERWISE SPECIFIED.

D. 2716 And 2758 Programming

Initally, and after each erasure, all bits of the 2716/2758 are in the "1" state. Information is introduced by selectively programming "0" into the desired bit locations. A programmed "0" can only be changed to a "1" by UV erasure.

The 2716/2758 is programmed by applying a 50 ms, TTL programming pulse to the $\overline{CE}$/PGM pin with the $\overline{OE}$ input high and the V_{PP} supply at 25V ±1V. Any location may be programmed at any time – either individually, sequentially, or randomly. The programming time for a single bit is only 50 ms and for all bits is approximately 100 and 50 seconds for the 2716 and 2758 respectively. The detailed programming specifications and timing waveforms are given in the following tables and figures.

CAUTION: The V_{CC} and V_{PP} supplied must be sequenced on and off such that V_{CC} is applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP} to prevent damage to the 2716/2758. The maximum allowable voltage during programming which may be applied to the V_{PP} with respect to ground is +26V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding the 26-volt maximum specification. For convenience in programming, the 2716/2758 may be verified with the V_{PP} supply at 25V ±1V. During normal read operation, however, V_{PP} must be at V_{CC}.

2716 AND 2758 PROGRAM CHARACTERISTICS(1)

T_A = 25°C ±5°C, V_{CC}[2] = 5V ±5%, V_{PP}[2,3] = 25V ±1V

D.C. Programming Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{LI}	Input Current (for Any Input)			10	μA	V_{IN} = 5.25V/0.45
I_{PP1}	V_{PP} Supply Current			5	mA	$\overline{CE}$/PGM = V_{IL}
I_{PP2}	V_{PP} Supply Current During Programming Pulse			30	mA	$\overline{CE}$/PGM = V_{IH}
I_{CC}	V_{CC} Supply Current			100	mA	
V_{IL}	Input Low Level	-0.1		0.8	V	
V_{IH}	Input High Level	2.0		V_{CC}+1	V	

A.C. Programming Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	2			μs	
t_{OEH}	$\overline{OE}$ Hold Time	2			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DF}	Output Enable to Output Float Delay	0		120	ns	$\overline{CE}$/PGM = V_{IL}
t_{OE}	Output Enable to Output Delay			120	ns	$\overline{CE}$/PGM = V_{IL}
t_{PW}	Program Pulse Width	45	50	55	ms	
t_{PRT}	Program Pulse Rise Time	5			ns	
t_{PFT}	Program Pulse Fall Time	5			ns	

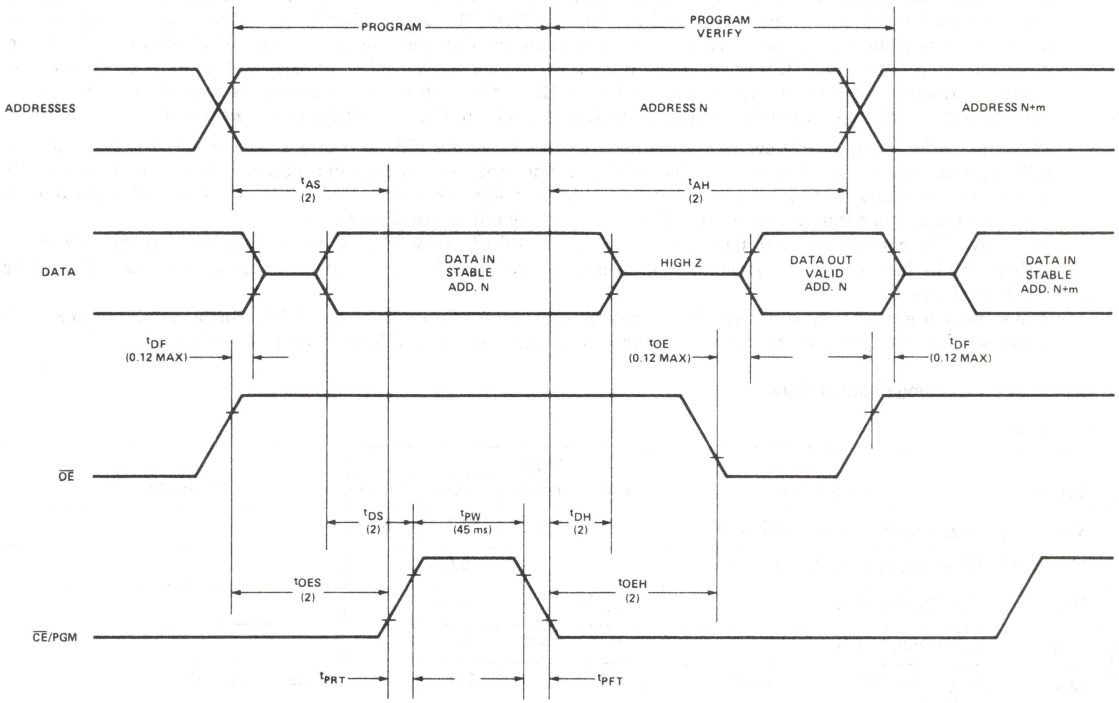
NOTES:
1. Intel's standard product warranty applies only to devices programmed to specifications described herein.
2. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The 2716/2758 must not be inserted into or removed from a board with V_{PP} at 25 ±1V to prevent damage to the device.
3. The maximum allowable voltage which may be applied to the V_{PP} pin during programming is +26V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 26V maximum specification.

A.C. Conditions of Test:

V_{CC} . . . . . 5V ±5%
V_{PP} . . . . . 25V ±1V
Input Rise and Fall Times (10% to 90%) . . . . . 20 ns
Input Pulse Levels . . . . . .0.8V to 2.2V
Input Timing Reference Level . . . . . 1V and 2V
Output Timing Reference Level . . . . . 0.8V and 2V

PROGRAMMING WAVEFORMS

V_{PP} = 25V ±1V, V_{CC} = 5V ±5%



NOTE: ALL TIMES SHOWN IN PARENTHESES ARE MINIMUM TIMES AND ARE μSEC UNLESS OTHERWISE NOTED.

III. BIPOLAR PROM PROGRAMMING

All Intel bipolar PROMs are programmed with the algorithm described below. This algorithm was developed specifically to program the 3602A/3622A, 3604A/3624A, 3605/3625, and 3608/3628. *The algorithm described in this section must be used on the aforementioned PROMs to insure properly and reliably programmed fuses.*

Initially, all bits are in a logic 1 (high) state. To program a bit to a logic 0 (low) state, it is necessary to force 5 mA into the output to be programmed. A series of program pulses must also be applied to the V_{CC} power supply and to any one of the logically low true chip select ($\overline{CS}$) inputs. The logic level of the other chip selects, in the case of PROMs with multiple chip selects, should be such that the PROM is selected during verification.

Program pulses are applied to all outputs of a word in a cycle time. The program pulses are multiplexed during a cycle time to each output of the word to be programmed. If desired, a N word by 8-bit PROM may have its words programmed in two separate groups – the four lower order bits (O_1 to O_4) and the four higher order bits (O_5 to O_8). The operation in this manner is the same as for a N word by 4-bit PROM. For fastest programming time, it is preferred that all eight outputs be programmed at the same time.

The programming specifications are given in Table V and the programming waveforms are shown in Figure 1. The programming procedure (described with nominal specifications) is as follows:

1. A 5 mA current must be forced into the output to be programmed by a current source. The current source must be clamped to V_{CC} by a silicon diode. All the other outputs must be floating until it is their turn for programming. The V_{CC} power supply and the chip select ($\overline{CS}$) input is pulsed as shown in Figures 1 and 2. The width of V_{CC} is linearly increased from 0.2 μs to 8 μs according to the ramp time shown in Figure 3. The total ramp time for a group of four outputs is 180 ms and 360 ms for a group of eight outputs.

   The V_{CC} program pulses are multiplexed during a cycle time to the outputs of the word to be programmed. The cycle time (t_{CYC}) between the V_{CC} program pulses to the same output will increase as the V_{CC} program pulse width increases from 0.2 μs to 8 μs. The time (t_D) between V_{CC} pulses of two different outputs is constant at 1.8 μs.

2. All outputs must be continuously monitored for programming verification. This verification must occur after V_{CC} has been at 4.5V for 90% of t_D and prior to V_{CC} rising to 12.5V. The program/verification cycles must still be applied (with the pulse width still linearly increasing to a maximum of 8 μs) even though the output has been sensed as being programmed. An additional 128 verifications (i.e., 128 program/verify cycles) on each output must be obtained to insure a correctly programmed output. This additional 128 verification is a minimum number and must occur *after* all the bits of the word are sensed as being programmed. Please refer to Figure 1 for the timing waveforms.

   More than 128 program/verify cycles may be required to achieve the 128 verifications on each bit. The cycles should still continue even if one bit fails, since the verifications are not required to be in consecutive sequence. After the 128 verifications have occurred for all bits, a final V_{CC} and CS pulse at a width of 2.5 ms is simultaneously applied to all outputs. Programming should cease if the 128 verifications are not achieved in 800 ms.

3. A 4 mA ±50% current must also be forced into CS_3 (pin 19) of the 3608/3628 family and into CS_4 (pin 18) of the 3604A/3624A family during programming. If desired for commonality the 4 mA may also be forced into CS_4 of the 3604/3624 family.

4. The 4 mA current into the chip select input may be easily accomplished by using a 1.2K resistor connected to a +15V power supply. The voltage on the chip select input will be approximately 10V with the 1.2K resistor.

Table V. Programming Characteristics

$T_A = 25°C$

Symbol	Parameter	Limits Min.	Nom.	Max.	Units	Conditions
V_{IH1}	V_{CC} Program Pulse Amplitude	12	12.5	13	V	
V_{IH2}	$\overline{CS}$ Program Pulse Amplitude	3	5	5.5	V	
V_{IL1}	V_{CC} During Verify	4.25[1]	4.5	4.75	V	
V_{IH2}	$\overline{CS}$ During Verify	0	0.2	0.4	V	
t_{PW1}	V_{CC} Pulse Width at Beginning of Pulse Train	160	200	240	ns	Measured at 12V
t_{PW2}	V_{CC} Pulse Width at End of Pulse Train	7.2	8	8.8	μs	Measured at 12V
T_{CSS}	Chip Select Setup Time	0			ns	Measured from 1.5V on rising edge of $\overline{CS}$ to 5.0V on rising edge of V_{CC}
T_{CSH}	Chip Select Hold Time	100			ns	Measured from 5.0V on falling edge of V_{CC} to 1.5V on falling edge of $\overline{CS}$
T_R	V_{CC} Rise Time	300	400	500	ns	Measured from 5V to 12V on V_{CC}
T_F	V_{CC} Fall Time	50	100	200	ns	Measured from 12V to 5V on V_{CC}
T_{CYC}	Time Between Pulses to Same Output	9	10		μs	Measured at 5V on V_{CC}
T_{OP}	DC Program Time After Verification Has Been Obtained	2.2	2.5	2.8	ms	Measured at 12V
T_D	Time Between V_{CC} Pulses to Successive Outputs	1.5	1.8		μs	Measured at 5V on V_{CC}
T_{RAMP}	Time During Which V_{CC} Pulse Width is Increased Linearly from t_{PW1} to t_{PW2} — 4 outputs	160	180	200	ms	
	8 outputs	320	360	400		
I_{CS}	Current to CS_3 of 3608/3628 or to CS_4 of 3604A/3624A	2	4	6	mA	CS_3 or CS_4 should be driven with a 1.2K resistor from a 15V power supply

NOTE: 1. The minimum V_{IL1} for the 3604AL (low power) is 4.5V

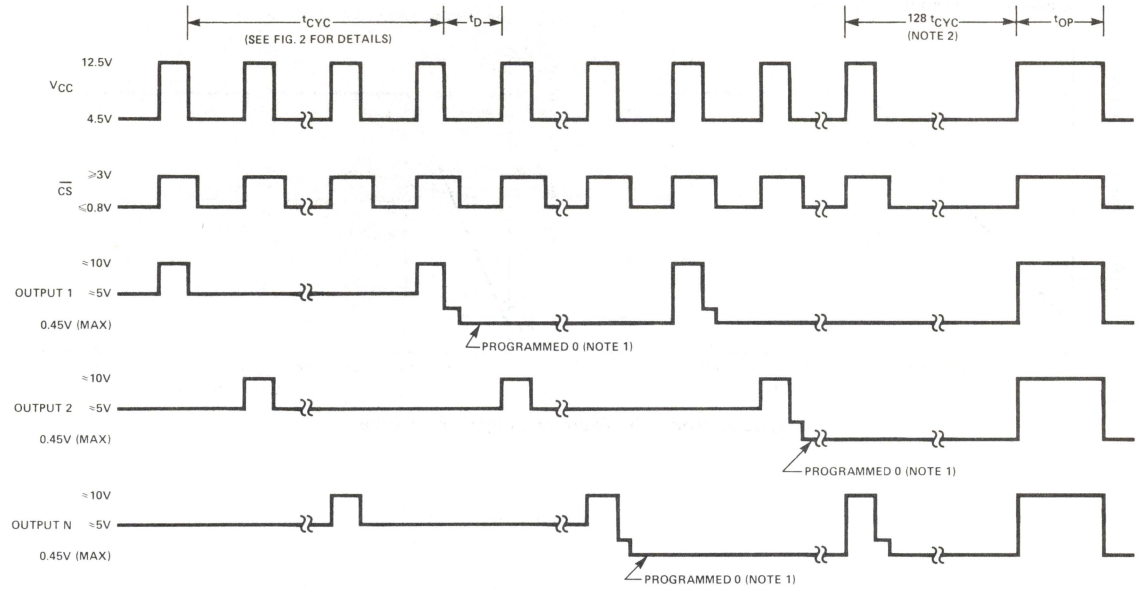


Figure 1. Programming Cycles.

NOTES: 1. PROGRAM VERIFICATION MUST OCCUR AFTER V_{CC} HAS BEEN AT 4.5V FOR 90% OF t_D AND PRIOR TO V_{CC} RISING TO 12.5V. THE PROGRAMMED OUTPUT IS ≤0.45V WHEN $\overline{CS}$ ≤0.8V AND FLOATING WHEN $\overline{CS}$ ≥ 3V.

2. AFTER THE LAST BIT HAS BEEN PROGRAMMED, 128 ADDITIONAL VERIFICATIONS ARE REQUIRED FOR EACH OUTPUT TO BE CORRECTLY PROGRAMMED.

3. AFTER THE 128 PROGRAM VERIFICATIONS, A FINAL 2.5 ms V_{CC} AND $\overline{CS}$ PULSE SHOULD BE APPLIED WHILE SIMULTANEOUSLY ENABLING THE CURRENT SOURCES TO ALL OUTPUTS WHICH ARE TO BE PROGRAMMED.

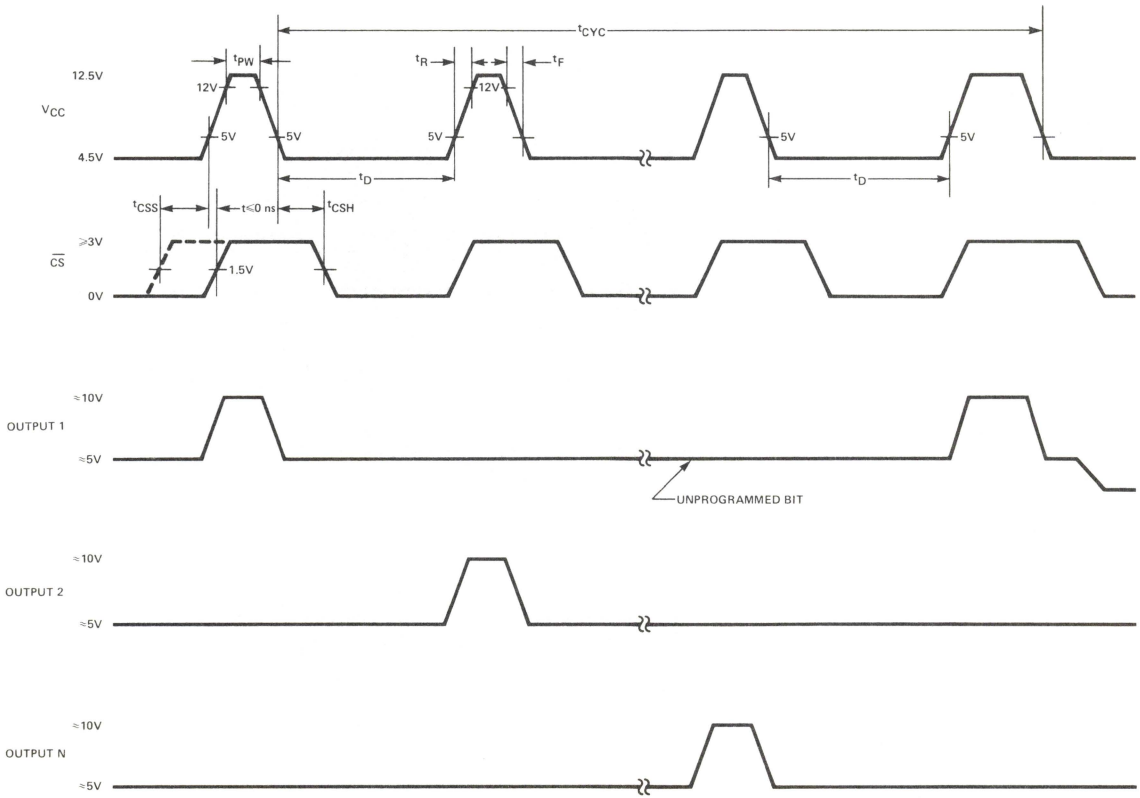


Figure 2. Programming Cycle Details.

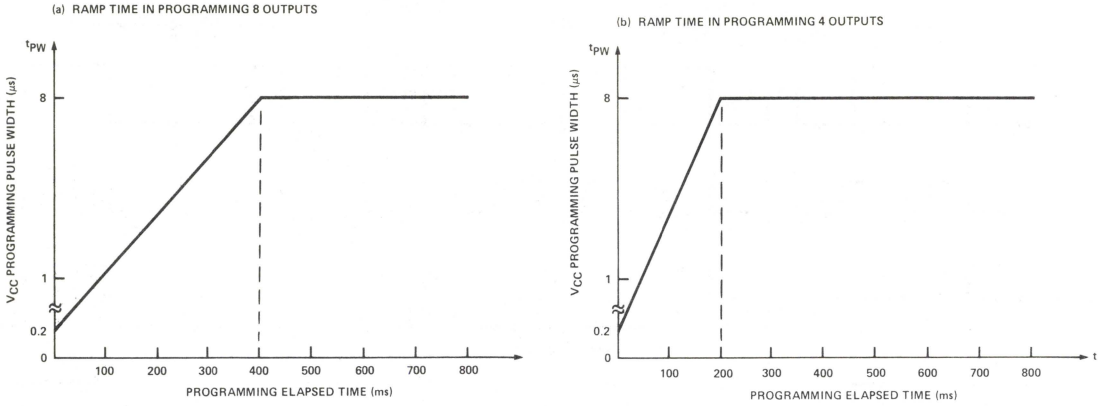
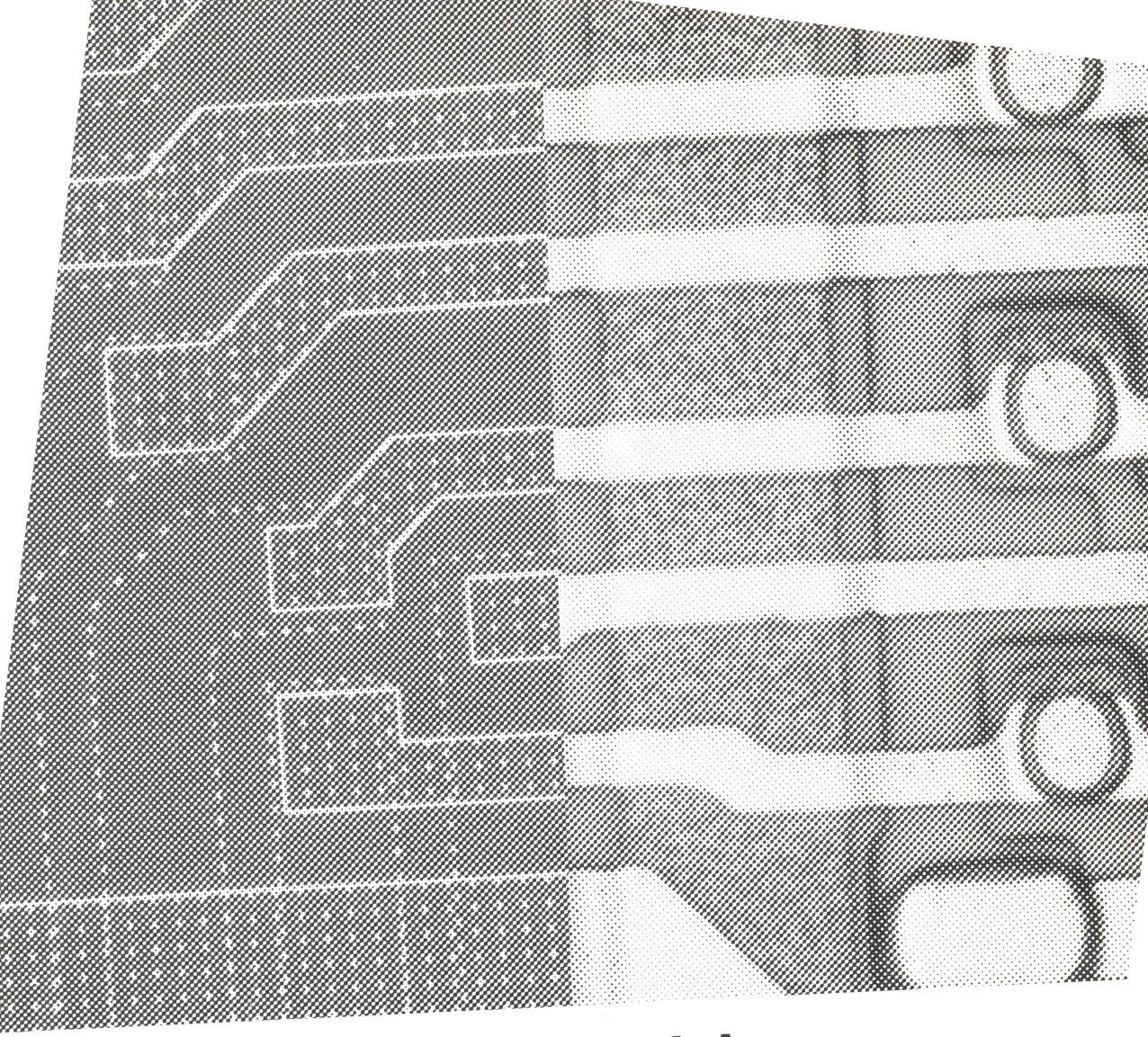


Figure 3. V_{CC} Pulse Width vs. Programming Time.



5 Serial Memory

SERIAL MEMORIES

Type	No. of Bits	Description	No. of Pins	Electrical Characteristics Over Temperature						Page No.
				Data Rep. Rate		Power Dissipation	Input Output	Clock		
				Min.	Max.	Max.[1]	Levels	Levels	Supplies[V]	
2401	2048	Dual 1024-Bit Dynamic Recirculating	16	25kHz	1MHz	350mW	TTL	TTL	+5	5-3
2405	1024	1024-Bit Dynamic Recirculating	16	25kHz	1MHz	350mW	TTL	TTL	+5	5-7
2464	65,536	256 Recirculating Shift Registers of 256 bits each	18		2.5MHz		TTL	TTL	-5, +12	5-7

2401, 2405
2048/1024-BIT DYNAMIC RECIRCULATING SHIFT REGISTERS

- **Single Supply Voltage -- +5 Volts**
- **Fully TTL Compatible -- Inputs, Outputs and Clock**
- **Single Phase Clock**
- **Guaranteed 1 MHz Operation with 100 pF Load, over Temperature Range**
- **Low Power Dissipation -- 120 μw/bit typically at 1 MHz**
- **Low Clock Capacitance -- 7 pF**
- **Write/Recirculate and Chip Select Logic Incorporated on Chip**
- **Standard Configurations -- Dual 1024 Bit -- 2401 Single 1024 Bit -- 2405**

SERIAL MEMORY

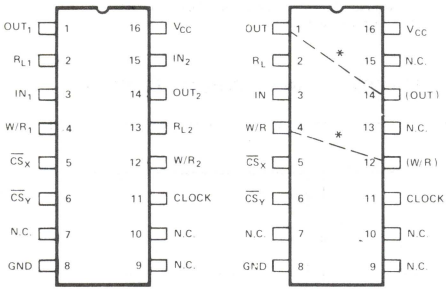
The 2401/2405 are 2048/1024 bit dynamic recirculating shift registers. They are directly TTL compatible in all respects: inputs, outputs, clock and a single +5 volt power supply.

Write/recirculate controls are provided to eliminate the need for external logic elements when recirculating data.

Two chip select inputs have been provided to allow easy selection of an individual package when outputs of several devices have been "OR-tied". A separate internal "pullup" resistor (R_L) is provided which can be externally connected to the output pin to achieve full signal swing.

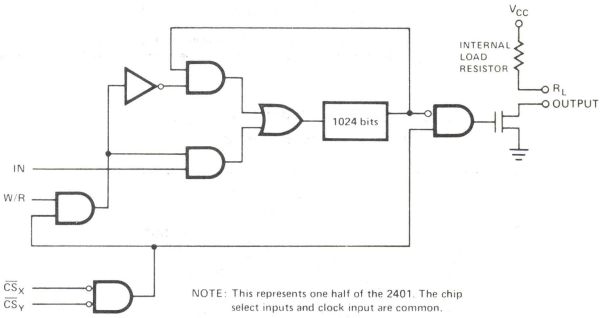
This Intel shift register family is fabricated with N-channel silicon gate technology. This technology provides the designer with high performance, easy to use MOS circuits. Only a single +5V power supply is needed and all devices are directly TTL compatible, including clocks.

PIN CONFIGURATIONS



* DASH LINES INDICATE NECESSARY EXTERNAL PRINTED CIRCUIT BOARD CONNECTIONS FOR PROPER OPERATION OF THE 2405. (SEE APPLICATION SECTION)

LOGIC DIAGRAM



NOTE: This represents one half of the 2401. The chip select inputs and clock input are common.

PIN NAMES

IN	DATA INPUT	OUT	DATA OUTPUT
W/R	WRITE/RECIRCULATE CONTROL	R_L	INTERNAL LOAD RESISTOR
$\overline{CS}_X$, $\overline{CS}_Y$	CHIP SELECT INPUT	N.C.	NO CONNECTION

TRUTH TABLE

FUNCTION	PIN SYMBOL		
	W/R	$\overline{CS}_X$	$\overline{CS}_Y$
WRITE MODE	H	L	L
RECIRCULATE	L	X	X
	X	H	X
	X	X	H
READ MODE	X	L	L

H = Logic High Level L = Logic Low Level
X = Don't Care Condition

Absolute Maximum Ratings*

Ambient Temperature Under Bias: 0° C to 70° C
Storage Temperature: −65° C to +150° C
Power Dissipation: 1W
Voltage on Any Pin with Respect to Ground: −0.5V to +7V

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. Characteristics

T_A = 0°to 70°C, V_{CC} = +5V ±5%, unless otherwise specified.

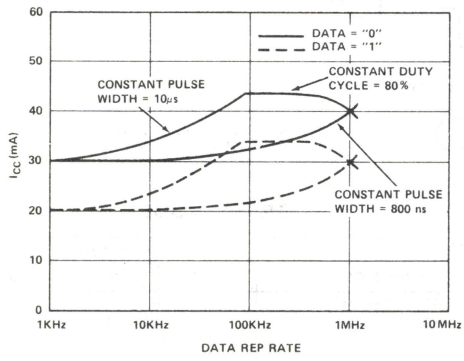
SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.[1]	LIMITS MAX.	UNITS	TEST CONDITIONS
I_{LI}	INPUT LEAKAGE			10	µA	V_{IN} = 5.25V
I_{LO}	OUTPUT LEAKAGE			100	µA	V_{OUT} = 5.25V
I_{CC}	POWER SUPPLY CURRENT		45 50	70 80	mA mA	T_A = 25°C, V_{CC} = 5.25V; 80% DUTY CYCLE T_A = 0°C, V_{CC} = 5.25V; 80% DUTY CYCLE
V_{IH}	INPUT HIGH LEVEL VOLTAGE (ALL INPUTS)	2.2		5.25	V	
V_{IL}	INPUT LOW LEVEL VOLTAGE (ALL INPUTS)	-0.3		0.65	V	
V_{OH}	OUTPUT HIGH LEVEL VOLTAGE	2.4		V_{CC}	V	I_{OH} = -1mA, R_L = 1.5K ± 5% ohms, external
V_{OL}	OUTPUT LOW LEVEL VOLTAGE	0		0.45	V	I_{OL} = 5.0mA, R_L = 1.5K ± 5% ohms, external[2]

NOTES: 1. Typical values are at 25° C and at nominal voltage.
2. The following was used to calculate I_{OL}.

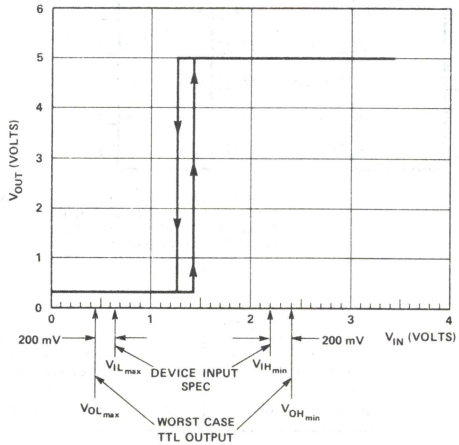
$$I_{OL} = \frac{V_{CC}\ (max.) - V_{OL}\ (max.)}{R_L\ (min.)} + I_{LI}\ (TTL\ device) = \frac{5.25 - 0.45}{1.425} + 1.6 = 4.97mA.$$

Also note that the internal load resistor, R_{LI}, has a value ranging from 500 ohms minimum to 2,200 ohms maximum. The internal load resistor can be used when driving from one 2401/2405 to another 2401/2405 or to other MOS inputs.

POWER SUPPLY CURRENT (I_{CC}) VS. DATA REP RATE



EFFECTIVE INPUT CHARACTERISTIC



A. C. Characteristics T_A = 0°C to 70°C, V_{CC} = +5V ±5%, unless otherwise specified.

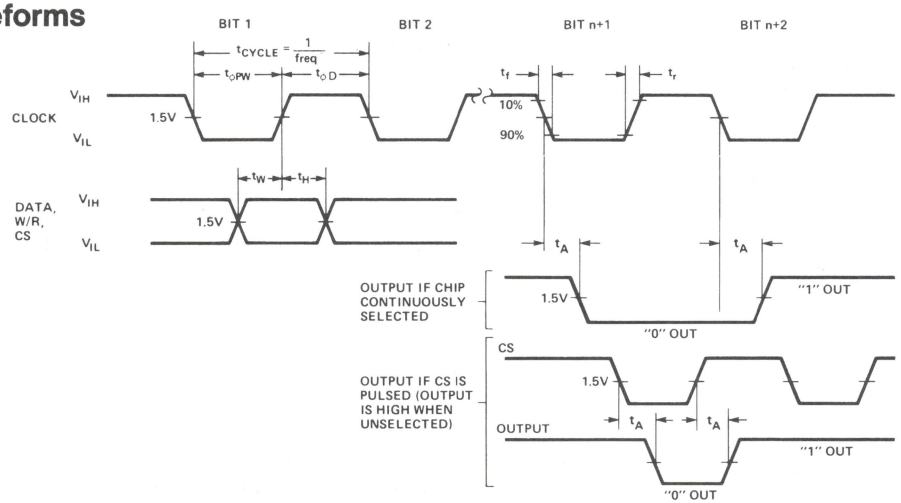
SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS
FREQ. MAX.	MAX. DATA REP. RATE			1	MHz	
FREQ. MIN.	MIN. DATA REP. RATE	1 25[1]			KHz KHz	T_A = 25° C T_A = 70° C
$t_{\phi PW}$	CLOCK PULSE WIDTH	0.80		10	μs	
$t_{\phi D}$	CLOCK PULSE DELAY	0.20 0.20		1000 40	μs μs	T_A = 25° C T_A = 70° C
t_r , t_f	CLOCK RISE AND FALL TIME			50	ns	
t_W	WRITE TIME	200			ns	
t_H	HOLD TIME	150			ns	
t_A	ACCESS TIME FROM CLOCK OR CHIP SELECT		250	500	ns	R_L = 1.5K ± 5% ohm, EXTERNAL C_L = 100pF ONE TTL LOAD

NOTE: 1. 100 kHz in plastic (P) package.

Capacitance T_A = 25° C

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS
C_{IN}	DATA, W/R & CS INPUT CAPACITANCE		4	7	pF	ALL PINS AT AC GROUND; 250 mV PEAK TO PEAK, 1 MHz
C_{OUT}	OUTPUT CAPACITANCE		10	14	pF	
C_ϕ	CLOCK CAPACITANCE		4	7	pF	

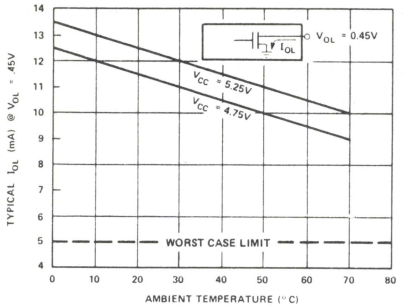
Waveforms



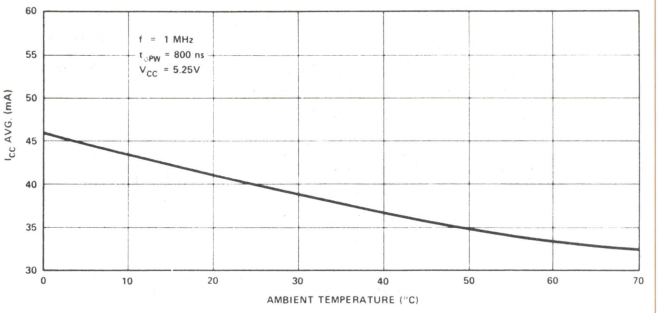
SERIAL MEMORY

D. C. Characteristics

TEMPERATURE DEPENDENCE OF OUTPUT LOW LEVEL SINK CAPABILITY



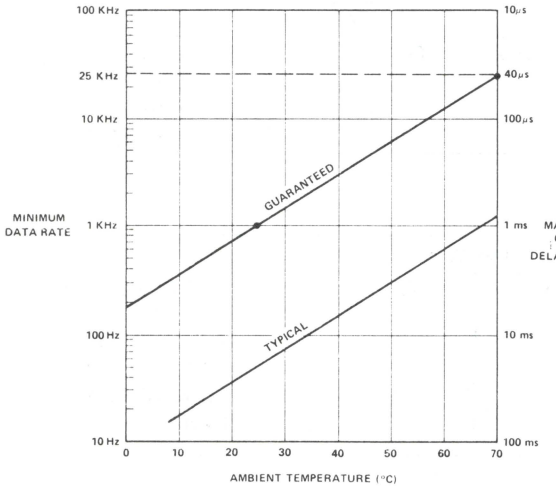
POWER SUPPLY CURRENT (I_{CC}) VS. AMBIENT TEMPERATURE (°C)



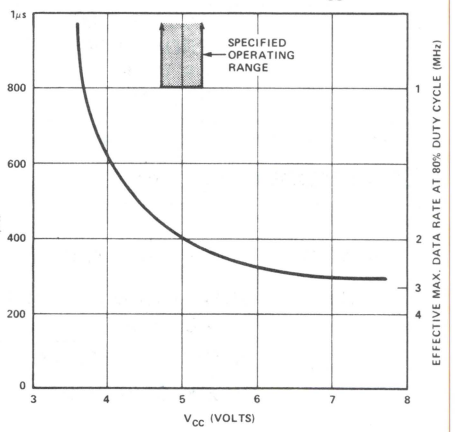
SERIAL MEMORY

A. C. Characteristics

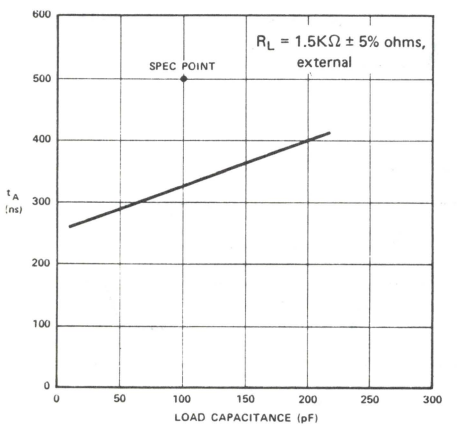
MINIMUM DATA RATE AND MAXIMUM CLOCK DELAY VS. AMBIENT TEMPERATURE FOR CERAMIC (C) PACKAGE



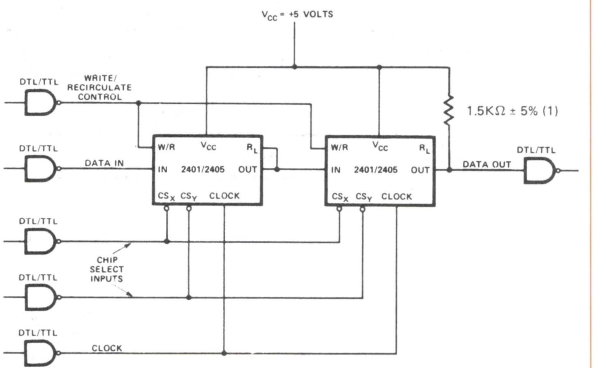
MINIMUM CLOCK PULSE WIDTH AND EFFECTIVE MAXIMUM DATA RATE AT 80% DUTY CYCLE VS. POWER SUPPLY VOLTAGE (V_{CC})



ACCESS TIME VS. LOAD CAPACITANCE



Typical Application Of TTL Compatible Shift Registers



NOTE (1): The 2401/2405 is directly compatible device to device. An external 1.5KΩ ± 5% load resistor is recommended for driving one TTL load with the 2401/2405 output.

ADVANCE INFORMATION
Characteristics are subject to change without notice

2464
65,536 BIT CCD SERIAL MEMORY
Organization: 256 Recirculating Shift Registers of 256 Bits Each

- **TTL-Compatible, 10pF Inputs and Output Including Clocks**
- **130μsec Average Latency**
- **285 nsec Access Time**
- **2.5 MHz Data Rate**
- **Page Mode Operation**
- **Standard +12V, -5V Power Supplies**
- **High Density 18-Pin Package — Standard 300-mil Width**
- **Three-State Output**

The Intel® 2464 is a 65,536-bit CCD serial memory designed for low-cost bulk store, swapping store, and buffer memory applications. The 2464 incorporates several features which allow it to be used in both large and small systems. These features are: TTL-compatible 10pF inputs including clocks, wide dynamic operating range, high performance, operation over the full commercial temperature range, standard 300-mil wide DIP packaging, and versatility.

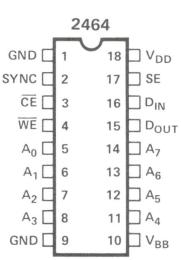
The 2464 is organized as 256 short recirculating loops of 256 bits each. Any one of the 256 loops can be accessed by applying an appropriate 8-bit address along with $\overline{CE}$. All 256 loops shift synchronously under the control of two shift clocks: SE and SYNC. The maximum shift rate is 1MHz for an average latency time of 130μsec, providing very high performance with easily-designed low-frequency clocks.

The short loop approach and subsequent square architecture of the device makes it feasible to use the 2464 as a serial or as a paging device. One distinct advantage of page mode operation is that the data rate can be maximized (2.5 MHz) at the same time the shift rate is minimized, providing high performance at low power dissipation. This is possible because the shift clocks do not determine the data rate in this mode.

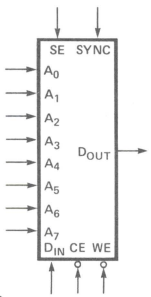
The 2464 generates and uses an internal reference voltage which requires at least 10,000 shift cycles to stabilize, with power supplies at operating levels. After this start-up period, no special action is needed to keep the internal reference voltage stable.

The 2464 is a surface-channel CCD fabricated using an advanced Intel N-channel, Silicon-gate MOS process. This process is an evolution of an existing Intel process used to fabricate 16K dynamic RAMs.

PIN CONFIGURATION



LOGIC SYMBOL



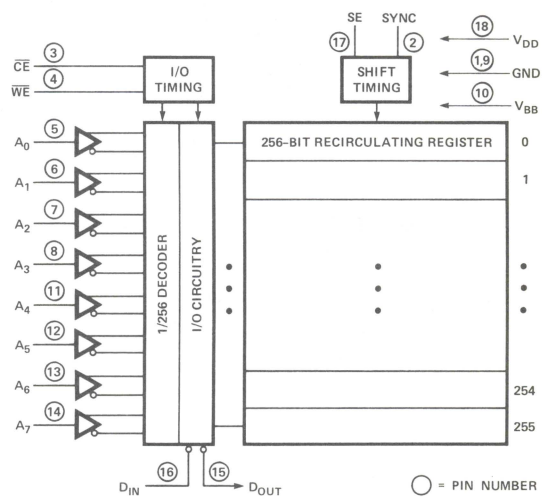
PIN NAMES

A_0-A_7	ADDRESS INPUTS	SE	SENSE ENABLE
D_{IN}	DATA IN	SYNC	SYNCHRONIZE
D_{OUT}	DATA OUT	V_{DD}	+12V
$\overline{WE}$	WRITE ENABLE	V_{BB}	-5V
$\overline{CE}$	CHIP ENABLE	GND	GROUND

TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	OPERATION	OUTPUT
H	X	NOT SELECTED	HIGH Z
L	L	DISABLE OUTPUT	HIGH Z
L	L→H	WRITE	HIGH Z
L	H	READ	D_{OUT}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -10°C to +85°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin with
Respect to Ground ..... -0.3V to +16V
Supply Voltages V_{DD} and GND
with Respect to V_{BB} ..... -0.3V to +20V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = +12V ±5%, V_{BB} = -5V ±5%, unless otherwise specified

Symbol	Parameter	2464 Min.	2464 Typ.[1]	2464 Max.	Unit	Test Conditions
I_{IL}	Low Level Input Current	-10	±1	10	µA	$V_{IN} \leq V_{IL}$
I_{IH}	High Level Input Current	-10	±1	10	µA	$V_{IN} \geq V_{IH}$
$\|I_{LO}\|$	Output Leakage Current		1	10	µA	V_{OUT} = GND to +5V
V_{IL}	Input Low Voltage, All Inputs	-0.3		0.8	V	
V_{IH}	Input High Voltage, All Inputs Including $\overline{CE}$, SYNC and SE	2.2		5.5	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.0mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} =-2.0mA

OPERATING POWER CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = +12V ±5%, V_{BB} = -5V ±5%, unless otherwise specified

Symbol	Parameter	2464 Typ.[1]	2464 Max.	Unit	Test Conditions
$I_{DD\ AVG}$	Average Operating V_{DD} Supply Current	Note 2		mA	
I_{DD1}	I_{DD} Component One	11	18	mA	
I_{DD2}	I_{DD} Component Two	25	38	mA/MHz	
I_{DD3}	I_{DD} Component Three	0.9	1.5	mA	
I_{DD4}	I_{DD} Component Four	2.8	4.5	mA	
I_{BB1}	V_{BB} Standby Current	5	50	µA	
I_{BB2}	V_{BB} Average Active Current	200	400	µA	

CAPACITANCE T_A = 25°C, f = 1.0MHz

Symbol	Parameter	2464 Typ.[1]	2464 Max.	Unit	Test Conditions
C_{IN}	Input Capacitance — All Inputs	5	10	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	5	10	pF	V_{OUT} = 0V

Notes:
1. Typical limits are for V_{DD} = +12V, V_{BB} = -5V, T_A = 25°C and specified loading.
2. $I_{DD\ AVG}$ depends on system operation and can be calculated with the equation below. Refer to page 8 for a complete power discussion.

$$I_{DD\ AVG} = \frac{T_{CE}}{T} I_{DD1} + \frac{N}{T} I_{DD2} + \frac{T_{SSY1}}{T} I_{DD3} + I_{DD4}$$

Where: T = any arbitrary time period representative of device operation, specified in µsec.
T_{CE} = total cumulative t_{CE} time during period T
N = number of SE positive edges during period T
T_{SSY1} = total cumulative t_{SSY1} time during period T

A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = +12V ±5%, V_{BB} = -5V ±5%, unless otherwise specified

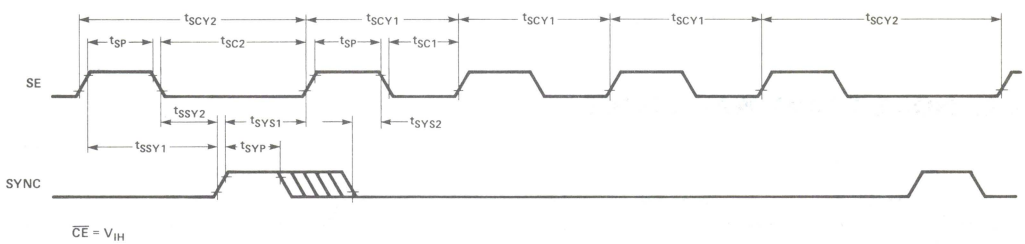
A.C. TEST CONDITIONS

Condition	2464
Input Pulse Levels	0.4V and 2.4V
Input Rise and Fall Times	10 nsec
Input and Output Timing Levels	0.8V and 2.2V
Output Load	1TTL Gate and C_L = 100pF

SEARCH OR REFRESH MODE

Symbol	Parameter	2464		Unit
t_{SCY1}[1]	SE Cycle Time with no SYNC Pulse	750	10^5	ns
t_{SCY2}	SE Cycle Time with SYNC Pulse	1000		ns
t_{SP}	SE Pulse Width	630		ns
t_{SC1}[1]	SE Off Time with No SYNC Pulse	100		ns
t_{SC2}	SE Off Time with SYNC Pulse	350		ns
t_{SSY1}	SE On to SYNC On Time		10^5	ns
t_{SSY2}	SE Off to SYNC On Time	0		ns
t_{SYS1}	SYNC On to SE On Time	340	TBD	ns
t_{SYS2}	SYNC Off to SE Off Time	50		ns
t_{SYP}	SYNC Pulse Width	150		ns
t_{REF}	Time Between Refresh (256 SE Cycles)		TBD	ms

WAVEFORMS

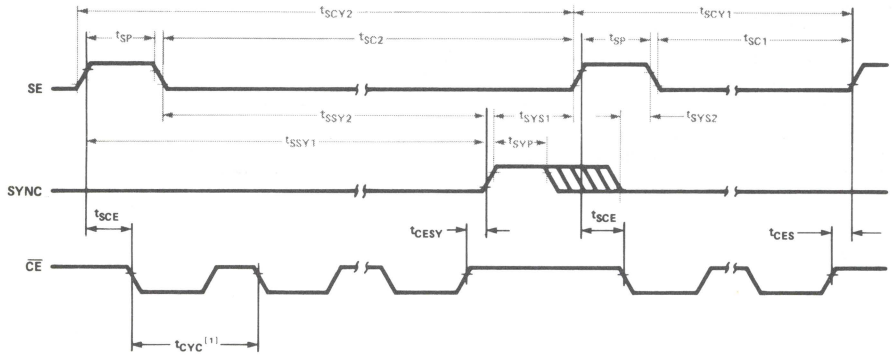


Note: 1. For constant 1 MHz operation, use t_{SCY1} = t_{SCY2} = 1000ns and t_{SC1} = t_{SC2} = 350ns.

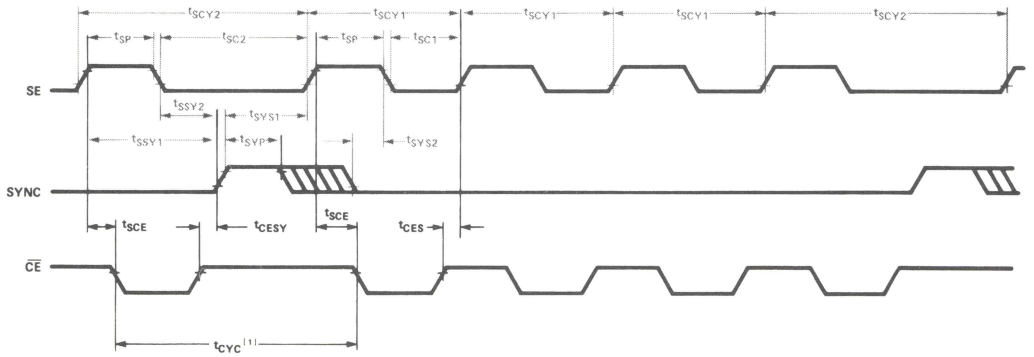
PAGE OR SERIAL MODE

Symbol	Parameter	2464		Unit
t_{SCY1}	SE Cycle Time with No SYNC Pulse	750	10^5	ns
t_{SCY2}	SE Cycle Time with SYNC Pulse	1000		ns
t_{SP}	SE Pulse Width	630		ns
t_{SC1}	SE Off Time with No SYNC Pulse	100		ns
t_{SC2}	SE Off Time with SYNC Pulse	350		ns
t_{SSY1}	SE On to SYNC On Time		10^5	ns
t_{SSY2}	SE Off to SYNC On Time	0		ns
t_{SYS1}	SYNC On to SE On Time	340	TBD	ns
t_{SYS2}	SYNC Off to SE Off Time	50		ns
t_{SYP}	SYNC Pulse Width	150		ns
t_{SCE}	SE On to CE On	355		ns
t_{CESY}	CE Off to SYNC On Time	0		ns
t_{CES}	CE Off to SE On Time	0		ns
t_{REF}	Time Between Refresh (256 SE Cycles)		TBD	ms

PAGE MODE TIMING WAVEFORMS



SERIAL MODE TIMING WAVEFORMS



Note: 1. t_{CYC} = Read, Write or RMW data cycle.

READ CYCLE

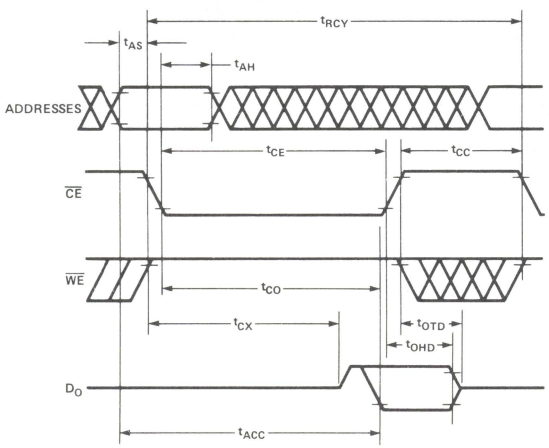
Symbol	Parameter	2464	Unit
t_{ACC}	Address to Output Access Time	285	ns
t_{RCY}	Read Cycle Time	400	ns
t_{AS}	Address Set Up Time	0	ns
t_{AH}	Address Hold Time	80	ns
t_{CE}	CE On Time	285	ns
t_{CC}	CE Off Time	95	ns
t_{CX}	CE to Output Active	10	ns
t_{CO}	CE to Output Valid	275	ns
t_{OHD}	Output Hold from Deselect	10	ns
t_{OTD}	Output Three-State from Deselect	60	ns

WRITE CYCLE

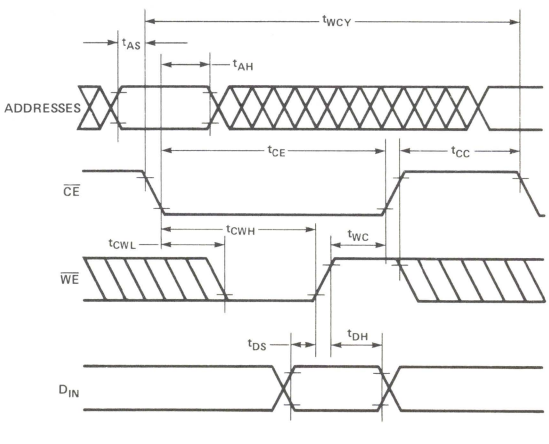
Symbol	Parameter	2464	Unit
t_{WCY}	Write Cycle Time	400	ns
t_{AS}	Address Setup Time	0	ns
t_{AH}	Address Hold Time	80	ns
t_{CE}	CE On Time	285	ns
t_{CC}	CE Off Time	95	ns
t_{CWL}	CE to $\overline{WE}$ Low	10	ns
t_{CWH}	CE to $\overline{WE}$ High	155	ns
t_{WC}	Write to CE Off Time	100	ns
t_{DS}	Data Setup Time	0	ns
t_{DH}	Data Hold Time	80	ns

WAVEFORMS

READ CYCLE



WRITE CYCLE



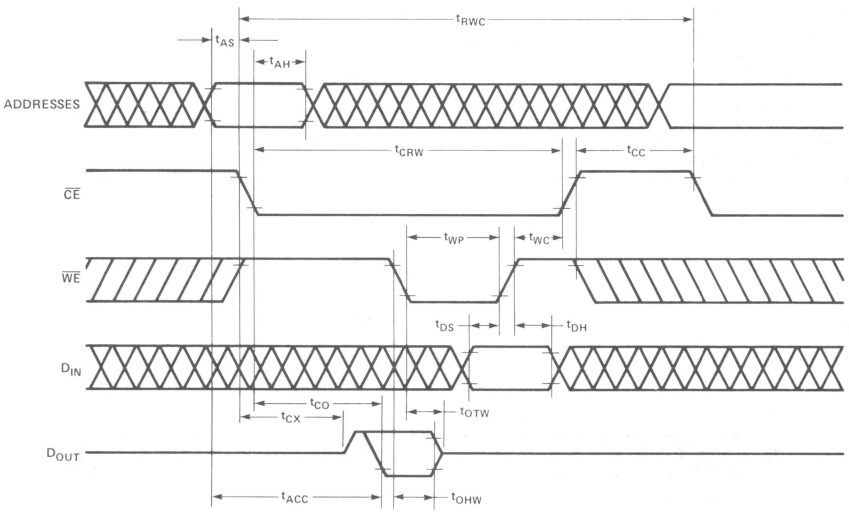
DATA OUT = HIGH IMPEDANCE

READ-MODIFY-WRITE CYCLE

Symbol	Parameter	2464		Unit
t_{ACC}	Address to Output Access Time		285	ns
t_{RWC}	Read-Modify-Write Cycle Time	600		ns
t_{AS}	Address Setup Time	0		ns
t_{AH}	Address Hold Time	80		ns
t_{CRW}	CE Width During RMW	485		ns
t_{CC}	CE Off Time	95		ns
t_{CX}	CE to Output Active	10		ns
t_{CO}	CE to Output Valid		275	ns
t_{OHW}	Output Hold from Write	10		ns
t_{OTW}	Output Three-State from Write		60	ns
t_{WP}	Write Pulse Width	100		ns
t_{WC}	Write to CE Off Time	100		ns
t_{DS}	Data Setup Time	0		ns
t_{DH}	Data Hold Time	80		ns

WAVEFORMS

READ-MODIFY-WRITE CYCLE



DEVICE DESCRIPTION

MODES OF OPERATION

The 2464 can be conceptualized as a drum organized into 256 tracks and 256 pages, as illustrated in Figure 1. Each page consists of 256 bits, one bit from each track.

Access to any random bit is accomplished by first rotating the drum (i.e., shifting the CCD array) to the page containing the desired bit. The time required to do this is referred to as the latency time, and is a function of the SYNC and SE clock rates. The desired bit is then selected from this page through the use of an 8-bit address and $\overline{CE}$.

Additional bits may be accessed from this page simply by changing the 8-bit address and cycling $\overline{CE}$. This capability is the result of a characteristic of CCDs that allows them to pause at a page before resuming rotation. Short loop CCDs characteristically have large pages and are able to pause for relatively long periods. Long loop CCDs have shorter pages and more stringent pause time limitations.

Figure 2a illustrates page mode operation. The 2464 uses an 8-bit address to randomly select any bit in the selected page. $\overline{CE}$ and $\overline{WE}$ are the signals used to control this operation. They function like the control signals of a RAM. In fact, each page can be treated as a 256-bit RAM. Access to other pages requires rotation of the drum.

Figure 2b illustrates serial mode operation, which is actually a subset of page mode operation. Only one bit is removed from a page before rotation to the next page and the next bit. In this fashion, data is serially obtained from a track as the drum is rotated. Although system applications usually limit serial access to a specific track, this is not a limitation of the device. Addresses can be changed on the fly during rotation, selecting bits from different tracks without interruption of the serial data stream. A practical application of this capability is to create long loops by moving from the end of one track to the beginning of the next track.

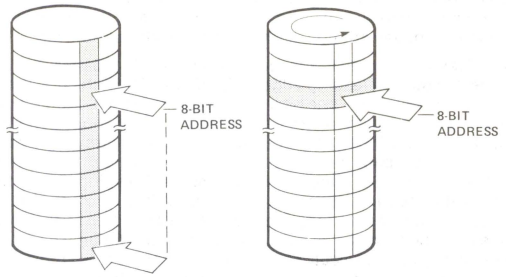


FIGURE 2.

Search mode operation and refresh mode operation are both similar to serial mode operation. The only difference is that $\overline{CE}$ is left high during search and refresh to disable operation of the RAM control circuitry. During this time $\overline{WE}$, D_{IN} and the address lines are ignored by the device. D_{OUT} remains in a high-impedance state. The difference between search mode and refresh mode operation is the rate at which SYNC and SE are clocked. Search mode uses high clock rates to minimize latency times while refresh mode uses low clock rates to minimize power.

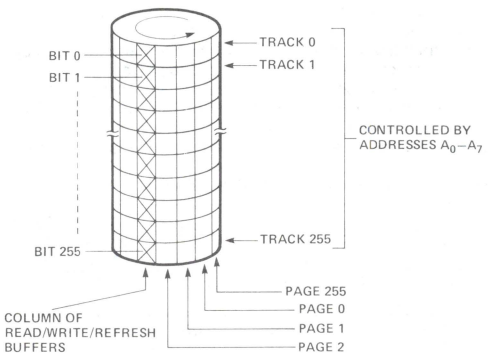


FIGURE 1. ORGANIZATION

SHIFT CONTROL CLOCKS

The relationship between the two shift clocks, SYNC and SE, can best be understood by studying the operation of a single 256-bit loop. Figure 3 is a diagram of one loop that clearly shows the necessary relationships, although it is not an exact circuit schematic.

Each 256-bit loop is actually broken up into four serial registers of 64 bits, with 63 of the 64 bits contained in the array and the 64th bit contained in either the input or output holding register. These four serial registers are internally multiplexed to form the complete 256-bit loop.

A SYNC pulse simultaneously loads four bits from the input holding register into the beginning of the loop (one bit into each 64-bit register) and unloads four new bits from the end of the loop

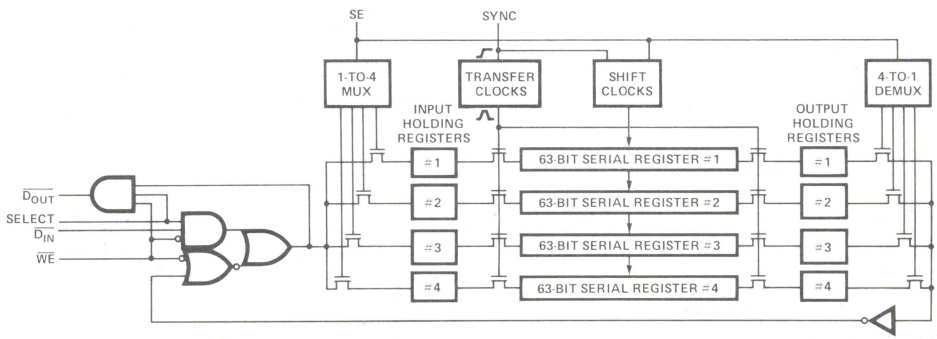


FIGURE 3. REPRESENTATIVE DIAGRAM OF ONE 256 BIT REGISTER

(one bit from each 64-bit register) into the output holding register. At any one time there are a total of 1024 bits, or four pages of information, residing in the holding registers of all 256 loops. These four pages are not randomly accessible to the user.

SE pulses are counted to sequence through the four pages, one at a time. On the first leading edge of SE after a SYNC, the first 256-bit page is available — one bit from each of the 256 No. 1 registers. Data is automatically recirculated into the No. 1 input holding registers, where it can be modified with a Write. The system may remain at this page until a t_{SCY1} or t_{REF} limitation forces the second leading SE edge. When the second leading SE edge occurs, the second page of information is available from the No. 2 registers. Data can no longer be read from or written to the first page until the entire array has completed a full rotation. The third leading edge of SE selects the third page from the No. 3 registers and the fourth edge selects the fourth page from the No. 4 registers. After every fourth SE, a SYNC pulse is required to continue rotation of the CCD array.

The advantage of the 1-for-4 multiplex scheme is power reduction. Although there are 256 SE pulses between refreshes, there are only 64 SYNC pulses and 64 actual shifts of the array. Since a considerable portion of the total power dissipation can be in the CV^2f shift power dissipation, a reduction in shift frequency reduces power. Device performance remains high since latency times and serial data rates are determined by the higher-frequency SE clock.

POWER DISCUSSION

The flexibility of the 2464 can make a calculation of power dissipation complicated. There are three types of data cycles and four types of operating modes. Combined with shift and data frequencies that can be chosen from a very wide dynamic operating range, there are an infinite number of ways the device can be operated.

To solve this problem, an equation has been developed which can determine 2464 power consumption for any condition. This equation appears in the power table and is repeated here.

$$I_{DD\ AVG} = \frac{T_{CE}}{T} I_{DD1} + \frac{N}{T} I_{DD2} + \frac{T_{SSY1}}{T} I_{DD3} + I_{DD4}$$

The first term of the equation represents the power involved in Chip Enabling the device. This term is a function of the duty cycling of $\overline{CE}$ and is therefore calculated as the total amount of time the chip is enabled, T_{CE}, during the time period of interest, T. T_{CE} can be calculated as the chip enable time for one data cycle, t_{CE}, multiplied by the number of data cycles in time T.

The second term of the equation represents SYNC and SE power dissipation. The SYNC and SE power term is frequency related, although it does not matter to the power calculation whether the SYNC and SE clocks are distributed or operated in burst-mode. The internal 2464 design only uses the edges of these signals and power is a function of the number of edges, not the duration of the SYNC and SE pulses. N is defined as the number of SE pulses during time T.

The third term is the power dissipation related to device operation during the time between the fourth SE pulse and the following SYNC pulse. During this time the 2464 uses a small amount of power. For absolute lowest refresh power, the separation between the two pulses should be kept to a minimum. The fourth, and final power term is the constant power dissipation used in the internal TTL-to-MOS level translation of the three asynchronous signals $\overline{CE}$, SYNC and SE.

Table 1 contains a table of the average power dissipation for each mode of operation, at the frequencies shown. In each case, time T has been chosen to be a time period over which operation is periodic to calculate average power dissipation. In the case of page mode, this is the cycle time of $\overline{CE}$. For serial mode and search mode, this is the cycle time of SYNC. For refresh mode, the refresh time of the part has been chosen.

POWER CALCULATION EXAMPLE

The versatility of the 2464 allows the user to define mixed mode operation. Since this involves a more complicated power calculation than for single mode operation, an example is worked out here. A cycle is defined which searches at 1MHz for a 2K block of data (Search mode), then transfers the data block at 2.5MHz from eight consecutive pages (Page mode), and finally wraps the device around to the starting position to complete a refresh (Refresh mode). This entire operation occurs during time T.

The average search time is 128μsec (128 shifts at 1MHz). Once the first page of interest is found, the 2464 drops into page mode and pulls the first 256-bit page of data at 2.5MHz in 102.4 μsec (256 x 400ns). A shift requiring 1 μsec loads the second 256-bit page, then read operation is continued. A full 2K block is transferred by reading a total of 8 consecutive pages and requires 826.2μsec (8 x 102.4 μsec + 7 x 1 μsec). Following data transfer, the 2464 enters refresh mode for the time remaining defined by the cycle T.

For fastest operation, the remaining 121 shifts take 121μsec for a total cycle time of 1075.2μsec. The typical average power dissipation required is 117mW, as shown in the first exercise in Table 2. The second exercise points out an interesting feature of the 2464. The latency time is independent of refresh time. As an example, the cycle time can be extended to T = 4ms (assuming refresh specifications allow this) while maintaining the 128μsec average latency time. The typical average power required falls to only 72mW because the device spends 3msec out of the total 4msec in a low power refresh mode. As the summary in Table 3 shows, 2464 power dissipation falls as the time between block requests increases, even though performance is maintained.

TABLE 2. POWER CALCULATION EXAMPLE

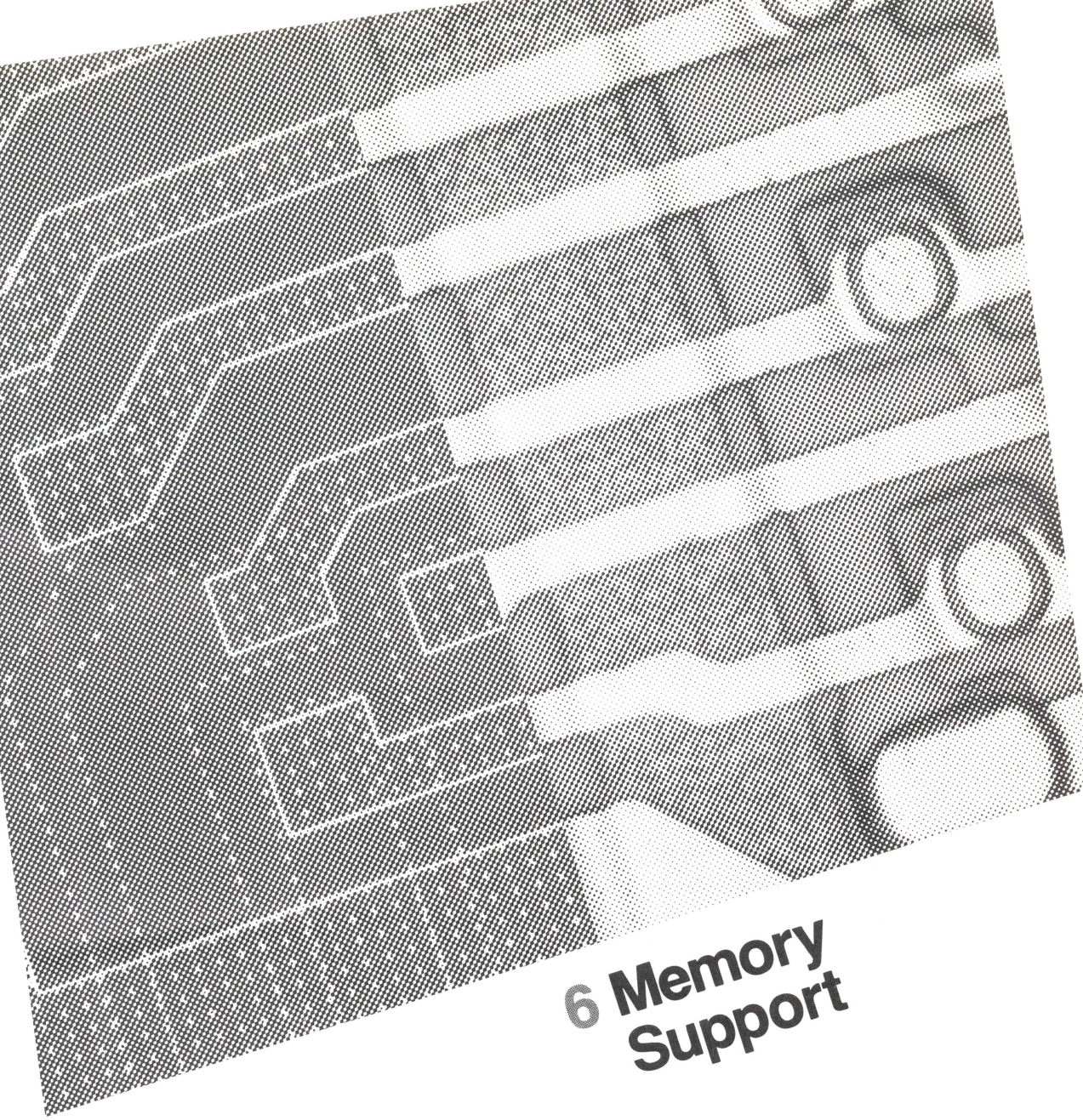
	T	$\frac{T_{CE}}{T}$	$\frac{N}{T}$ (MHz)	$\frac{T_{SSY1}}{T}$	Typical $I_{DD\ AVG}$ (mA)	Typical $P_{DD\ AVG}$ (mW)
Exer. 1	1.08 msec	0.536	0.239	0.229	14.76	177
Exer. 2	4.0 msec	0.143	0.064	0.061	6.0	72

TABLE 3. SUMMARY OF EXAMPLE

	Exercise 1	Exercise 2
Block Size	2048 Bits	2048 Bits
Avg. Latency Time	130 μsec	130 μsec
Data Rate	2.5 MHz	2.5 MHz
T	1.08 msec	4.0 msec
Typical Power Dissipation	177mW	72mW

TABLE 1. TYPICAL POWER DISSIPATIONS

Mode of Operation	T (μs)	$\frac{T_{CE}}{T}$	$\frac{N}{T}$ (MHz)	$\frac{T_{SSY1}}{T}$	Typical $I_{DD\ AVG}$ (mA)	Typical $P_{DD\ AVG}$ (mW)
Page Mode at 2.5 MHz	0.4	0.7	0	0.25	10.7	129
Serial Mode at 1 MHz	4.0	0.28	1.0	0.16	30.5	366
Search Mode for 130μsec Avg. Latency	4.0	0	1.0	0.16	27.4	329
for 400μsec Avg. Latency	12.4	0	0.323	0.05	10.8	129
Refresh Mode for 2msec Refresh	2000	0	0.128	0.02	6.0	72
for 4msec Refresh	4000	0	0.064	0.01	4.4	53
for 10msec Refresh	10,000	0	0.0256	0.004	3.4	41



6 Memory Support

MEMORY SUPPORT CIRCUITS

	Type	Description	No. of Pins	Electrical Characteristics Over Temperature		Supplies[V]	Page No.
				Input to Output Delay Max.	Power Dissipation[1] Maximum		
SCHOTTKY BIPOLAR	**3205**	1 of 8 Binary Decoder	16	18ns	350mW	+5	6-3
	3207A	Quad Bipolar to MOS Level Shifter and Driver	16	25ns	900mW	+5, +16, +19	6-7
	3207A-1	Quad Bipolar to MOS Level Shifter and Driver	16	25ns	1040mW	+5, +19, +22	6-11
	3208A	Hex Sense Amp for MOS Memories	18	20ns	600mW	+5	6-13
	3222	4K Dynamic RAM Refresh Controller	22	—	600mW	+5	6-19
	3232	4K Dynamic RAM Address Multiplexer and Refresh Counter	24	20ns	750 mW	+5	6-25
	3242	16K Dynamic RAM Address Multiplexer and Refresh Counter	28	20ns	825mW	+5	6-29
	3245	Quad TTL to MOS Driver for 4K RAMs	16	32ns	388mW	+12, +5	6-33
	3404	High Speed 6-Bit Latch	16	12ns	375mW	+5	6-3
	3408A	Hex Sense Amp and Latch for MOS Memories	18	25ns	625mW	+5	6-13
CMOS	**5235**	Quad Low Power TTL to MOS Driver for 4K RAMs	16	125ns	240mW	12	6-37
	5235-1	High Speed Quad Low Power TTL to MOS Driver for 4K RAMs	16	95ns	240mW	12	

Note 1. Power Dissipation calculated with maximum power supply current and nominal supply voltages.

3205, 3404
3205 HIGH SPEED 1 OUT OF 8 BINARY DECODER
3404 HIGH SPEED 6-BIT LATCH

- **18ns Max. Delay Over 0°C to 75°C Temperature: 3205**
- **12ns Max. Data to Output Delay Over 0°C to 75°C Temperature: 3404**
- **Directly Compatible With DTL and TTL Logic Circuits**
- **Totem-Pole Output**
- **Low Input Load Current: .25mA Max., 1/6 Standard TTL input Load**
- **Minimum Line Reflection: Low Voltage Diode Input Clamp**
- **Outputs Sink 10mA Min.**
- **16-Pin Dual In-Line Package**
- **Simple Expansion: Enable Inputs**

3205

The 3205 decoder can be used for expansion of systems which utilize memory components with active low chip select input. When the 3205 is enabled, one of its eight outputs goes "low", thus a single row of a memory system is selected. The 3 chip enable inputs on the 3205 allow easy memory expansion. For very large memory systems, 3205 decoders can be cascaded such that each decoder can drive 8 other decoders for arbitrary memory expansions.

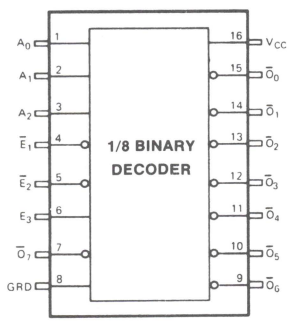
3404

The Intel 3404 contains six high speed latches organized as independent 4-bit and 2-bit latches. They are designed for use as memory data registers, address registers, or other storage elements. The latches act as high speed inverters when the "Write" input is "low".

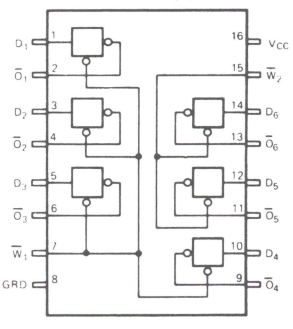
The Intel 3404 is packaged in a standard 16-pin dual-in-line package; and its performance is specified over the temperature range of 0°C to +75°C, ambient. The use of Schottky barrier diode clamped transistors to obtain fast switching speeds results in higher performance than equivalent devices made with a gold diffusion process.

PIN CONFIGURATION

3205



3404



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias:	Ceramic	−65°C to +125°C
	Plastic	−65°C to +75°C
Storage Temperature		−65°C to +160°C
All Output or Supply Voltages		−0.5 to +7 Volts
All Input Voltages		−1.0 to +5.5 Volts
Output Currents		125 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%

3205, 3404

SYMBOL	PARAMETER	LIMIT MIN.	LIMIT MAX.	UNIT	TEST CONDITIONS
I_F	INPUT LOAD CURRENT		−0.25	mA	V_{CC} = 5.25V, V_F = 0.45V
I_R	INPUT LEAKAGE CURRENT		10	µA	V_{CC} = 5.25V, V_R = 5.25V
V_C	INPUT FORWARD CLAMP VOLTAGE		−1.0	V	V_{CC} = 4.75V, I_C = −5.0 mA
V_{OL}	OUTPUT "LOW" VOLTAGE		0.45	V	V_{CC} = 4.75V, I_{OL} = 10.0 mA
V_{OH}	OUTPUT HIGH VOLTAGE	2.4		V	V_{CC} = 4.75V, I_{OH} = −1.5 mA
V_{IL}	INPUT "LOW" VOLTAGE		0.85	V	V_{CC} = 5.0V
V_{IH}	INPUT "HIGH" VOLTAGE	2.0		V	V_{CC} = 5.0V
I_{SC}	OUTPUT HIGH SHORT CIRCUIT CURRENT	−40	−120	mA	V_{CC} = 5.0V, V_{OUT} = 0V
V_{OX}	OUTPUT "LOW" VOLTAGE @ HIGH CURRENT		0.8	V	V_{CC} = 5.0V, I_{OX} = 40 mA

3205 ONLY

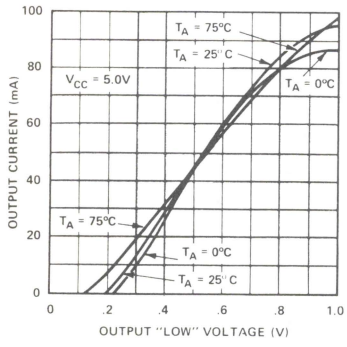
I_{CC}	POWER SUPPLY CURRENT		70	mA	V_{CC} = 5.25V, Outputs Open

3404 ONLY

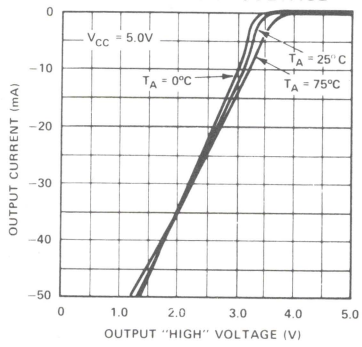
I_{CC}	POWER SUPPLY CURRENT		75	mA	V_{CC} = 5.25V, Outputs Open
I_{FW1}	WRITE ENABLE LOAD CURRENT PIN 7		−1.00	mA	V_{CC}=5.25V, V_W=0.45V
I_{FW2}	WRITE ENABLE LOAD CURRENT PIN 15		−0.50	mA	V_{CC}=5.25V, V_W=0.45V
I_{RW}	WRITE ENABLE LEAKAGE CURRENT		10	µA	V_R=5.25V

TYPICAL CHARACTERISTICS

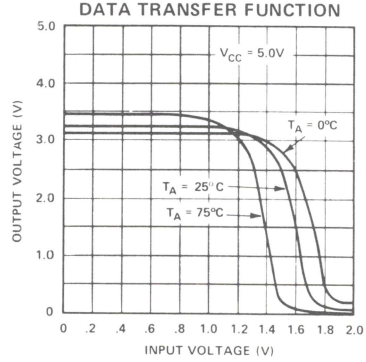
OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE



OUTPUT CURRENT VS. OUTPUT "HIGH" VOLTAGE



DATA TRANSFER FUNCTION



3205 HIGH SPEED 1 OUT OF 8 BINARY DECODER

SWITCHING CHARACTERISTICS

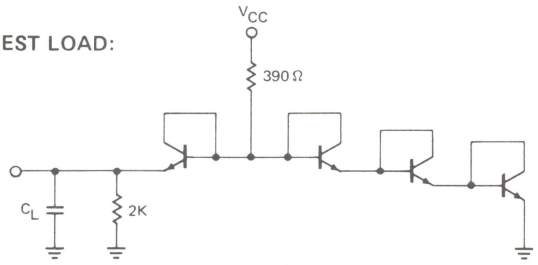
CONDITIONS OF TEST:

Input pulse amplitudes: 2.5V

Input rise and fall times: 5 nsec between 1V and 2V

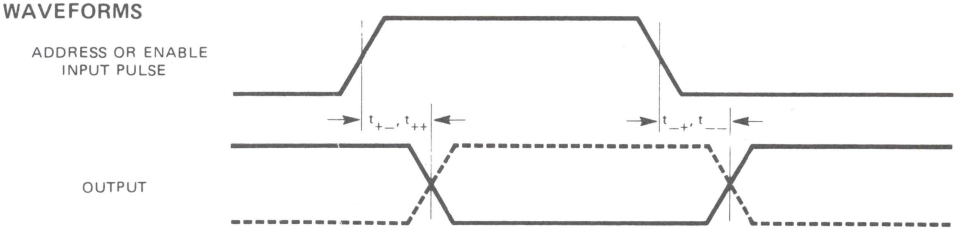
Measurements are made at 1.5V

TEST LOAD:



All Transistors 2N2369 or Equivalent. C_L = 30 pF

TEST WAVEFORMS



A.C. CHARACTERISTICS

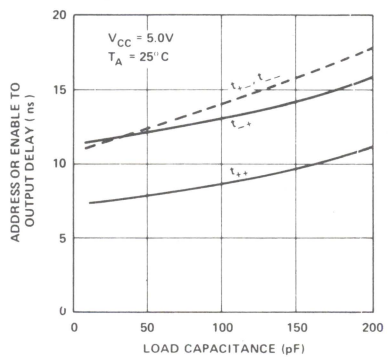
T_A = 0°C to +75°C, V_{CC} = 5.0V ±5% unless otherwise specified.

SYMBOL	PARAMETER		MAX. LIMIT	UNIT	TEST CONDITIONS
t_{++}	ADDRESS OR ENABLE TO OUTPUT DELAY		18	ns	
t_{-+}			18	ns	
t_{+-}			18	ns	
t_{--}			18	ns	
C_{IN} (1)	INPUT CAPACITANCE	P3205	4(typ.)	pF	f = 1 MHz, V_{CC} = 0V
		C3205	5(typ.)	pF	V_{BIAS} = 2.0V, T_A = 25°C

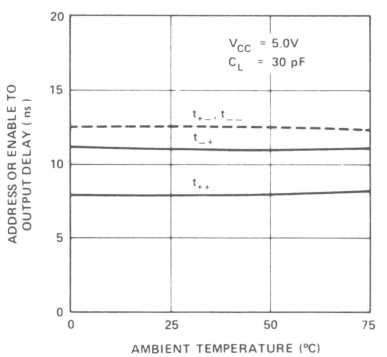
1. This parameter is periodically sampled and is not 100% tested.

TYPICAL CHARACTERISTICS

ADDRESS OR ENABLE TO OUTPUT DELAY VS. LOAD CAPACITANCE



ADDRESS OR ENABLE TO OUTPUT DELAY VS. AMBIENT TEMPERATURE



3404 6-BIT LATCH

SWITCHING CHARACTERISTICS

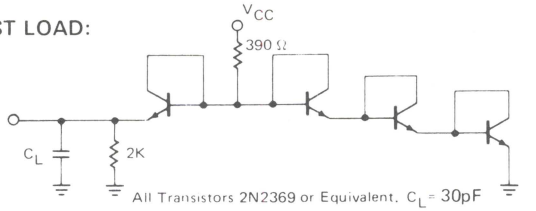
CONDITIONS OF TEST:

Input pulse amplitudes: 2.5V

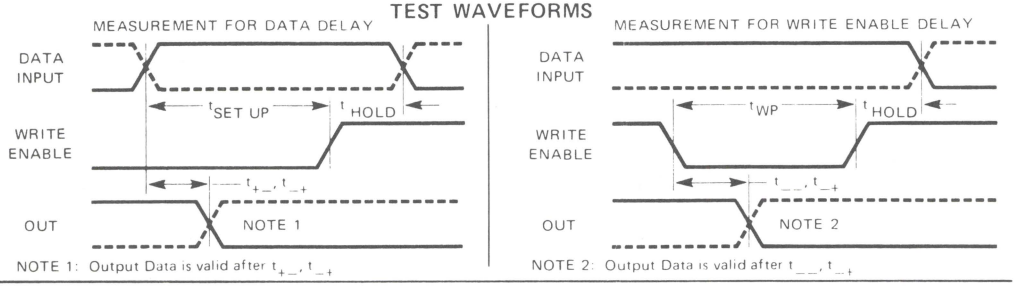
Input rise and fall times: 5 nsec between 1V and 2V

Measurements are made at 1.5V

TEST LOAD:



TEST WAVEFORMS



NOTE 1: Output Data is valid after t_{+-}, t_{-+}

NOTE 2: Output Data is valid after t_{--}, t_{-+}

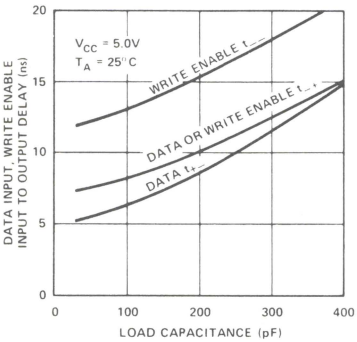
A.C. CHARACTERISTICS T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%; unless otherwise specified.

SYMBOL	PARAMETER		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
t_{+-}, t_{-+}	DATA TO OUTPUT DELAY				12	ns	
t_{--}, t_{-+}	WRITE ENABLE TO OUTPUT DELAY				17	ns	
$t_{SET\ UP}$	TIME DATA MUST BE PRESENT BEFORE RISING EDGE OF WRITE ENABLE		12			ns	
t_{HOLD}	TIME DATA MUST REMAIN AFTER RISING EDGE OF WRITE ENABLE		8			ns	
t_{WP}	WRITE ENABLE PULSE WIDTH		15			ns	
C_{IND}[3]	DATA INPUT CAPACITANCE	P3404		4		pF	f = 1 MHz, V_{CC} = 0V
		C3404		5		pF	V_{BIAS} = 2.0V, T_A = 25°C
C_{INW}[3]	WRITE ENABLE CAPACITANCE	P3404		7		pF	f = 1 MHz, V_{CC} = 0V
		C3404		8		pF	V_{BIAS} = 2.0V, T_A = 25°C

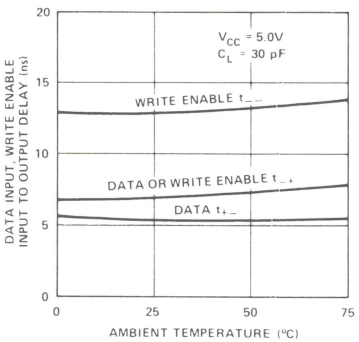
NOTE 3: This parameter is periodically sampled and is not 100% tested.

TYPICAL CHARACTERISTICS

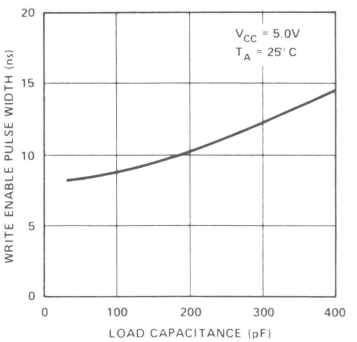
DATA INPUT, WRITE ENABLE TO OUTPUT DELAY VS. LOAD CAPACITANCE



DATA INPUT, WRITE ENABLE TO OUTPUT DELAY VS. AMBIENT TEMPERATURE



WRITE ENABLE PULSE WIDTH VS. LOAD CAPACITANCE



3207A
QUAD BIPOLAR-TO-MOS LEVEL SHIFTER AND DRIVER

- **High Speed, 45 nsec Max. — Delay + Transition Time Over Temperature with 200 pF Load**
- **TTL and DTL Compatible Inputs**
- **1103 and 1103A Memory Compatible at Output**
- **Simplifies Design — Replaces Discrete Components**
- **Easy to Use — Operates from Standard Bipolar and MOS Supplies**
- **Minimum Line Reflection — Input and Output Clamp Diodes**
- **High Input Breakdown Voltage — 19 Volts**
- **CerDIP Package — 16 Pin DIP**

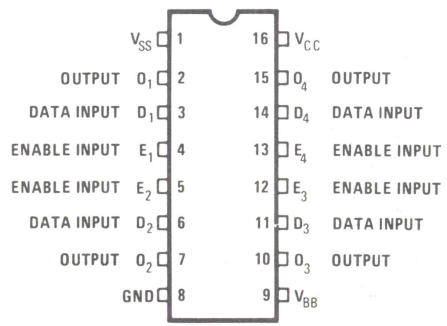
The 3207A is a Quad Bipolar-to-MOS level shifter and driver which accepts TTL and DTL input signals, and provides high output current and voltage suitable for driving MOS circuits. It is particularly suitable for driving the 1103 and 1103A memory chips. The circuit operates from a 5 volt TTL power supply, and V_{SS} and V_{BB} power supplies from the 1103 and 1103A.

The device features two common enable inputs per pair of devices which permits some logic to be done at their inputs, such as cenable and precharge decoding for the 1103 and 1103A.

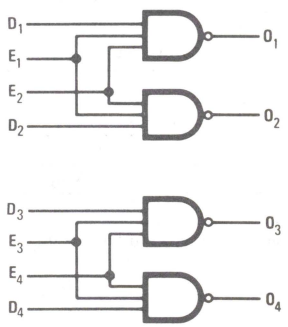
For the TTL inputs a logic "1" is V_{IH} and a logic "0" is V_{IL}. The 3207A outputs correspond to a logic "1" as V_{OL} and a logic "0" as V_{OH} for driving MOS inputs.

The 3207A is packaged in a hermetically sealed 16 pin ceramic dual-in-line package. The device performance is specified over the same temperature range as the 1103 and 1103A, i.e. from 0°C to +70°C.

PIN CONFIGURATION



LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... 0°C to +70°C
Storage Temperature..... −65°C to +160°C
All Input Voltages and V_{SS}..... −1.0 to +21V
Supply Voltage V_{CC} ..... −1.0 to +7V
All Outputs and Supply Voltage
V_{BB} with respect to GND ..... −1.0 to +25V
Power Dissipation at 25°C..... 2 Watts (1)

*COMMENT
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(1) Refer to the graph of Junction Temperature versus Total Power Dissipation on page 5-10 for other temperatures.

D.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 16V \pm 5\%$, $V_{BB} - V_{SS} = 3.0V$ to $4.0V$

SYMBOL	TEST	LIMIT MIN.	LIMIT MAX.	UNIT	CONDITIONS
I_{FD}	DATA INPUT LOAD CURRENT		−0.25	mA	$V_D = .45V$, $V_{CC} = 5.25V$, All Other Inputs at 5.25V, $V_{SS} = 16V$, $V_{BB} = 19V$
I_{FE}	ENABLE INPUT LOAD CURRENT		−0.50	mA	$V_E = .45V$, $V_{CC} = 5.25V$, All Other Inputs at 5.25V, $V_{SS} = 16V$, $V_{BB} = 19V$
I_{RD}	DATA INPUT LEAKAGE CURRENT		20	μA	$V_D = 19V$, $V_{CC} = 5.0V$, All Other Inputs Grounded, $V_{SS} = 16V$, $V_{BB} = 19V$
I_{RE}	ENABLE INPUT LEAKAGE CURRENT		20	μA	$V_E = 19V$, $V_{CC} = 5.0V$, All Other Inputs Grounded, $V_{SS} = 16V$, $V_{BB} = 19V$
V_{OL}	OUTPUT "LOW" VOLTAGE		.8 .7 .6	V(0°C) V(25°C) V(70°C)	$I_{OL} = 500\mu A$, $V_{CC} = 4.75V$ $V_{SS} = 16V$, $V_{BB} = 19V$ All Inputs at 2.0V
V_{OH} (MIN.)	OUTPUT "HIGH" VOLTAGE	$V_{SS} - .7$ $V_{SS} - .6$ $V_{SS} - .5$		V(0°C) V(25°C) V(70°C)	$I_{OH} = -500\mu A$, $V_{CC} = 5.0V$ $V_{SS} = 16V$, $V_{BB} = 19V$ All Inputs at 0.85V
V_{OH} (MAX.)			$V_{SS} + 1.0$	V	$I_{OH} = 5mA$, $V_{CC} = 5.0V$ $V_{SS} = 16V$, $V_{BB} = 19V$
I_{OL}	OUTPUT SINK CURRENT	100		mA	$V_O = 4V$, $V_{CC} = 5.0V$, $V_{SS} = 16V$, $V_{BB} = 19V$, $V_E = V_D = 2.0V$
I_{OH}	OUTPUT SOURCE CURRENT	−100		mA	$V_O = V_{SS} - 4V$, $V_{CC} = 5.0V$, $V_{SS} = 16V$ $V_{BB} = 19V$, $V_E = V_D = 0.85V$
V_{IL}	INPUT "LOW" VOLTAGE		1.0	V	$V_{CC} = 5.0V$, $V_{SS} = 16V$, $V_{BB} = 19V$
V_{IH}	INPUT "HIGH" VOLTAGE	2.0		V	$V_{CC} = 5.0V$, $V_{SS} = 16V$, $V_{BB} = 19V$
C_{IN}	INPUT CAPACITANCE	8(Typical)		pF	$V_{BIAS} = 2.0V$, $V_{CC} = 0V$

POWER SUPPLY CURRENT DRAIN:
All Outputs "Low"

Symbol	Parameter	Min.	Max.	Unit	Conditions
I_{CC}	Current from V_{CC}		83	mA	$V_{CC} = 5.25V$, $V_{SS} = 16.8V$, $V_{BB} = 20.8V$ All Inputs Open
I_{SS}	Current from V_{SS}		250	μA	
I_{BB}	Current from V_{BB}		21	mA	
P_{TOTAL}	Total Power Dissipation		900	mW	

All Outputs "High"

I_{CC}	Current from V_{CC}		33	mA	$V_{CC} = 5.25V$, $V_{SS} = 16.8V$, $V_{BB} = 20.8V$ All Inputs Grounded
I_{SS}	Current from V_{SS}		250	μA	
I_{BB}	Current from V_{BB}		3	mA	
P_{TOTAL}	Total Power Dissipation		250	mW	

Standby Condition with $V_{CC} = 0V$, $V_{SS} = V_{BB}$

I_{CC}	Current from V_{CC}		0	mA	$V_{CC} = 0V$, $V_{SS} = 16.8V$, $V_{BB} = 16.8V$
I_{SS}	Current from V_{SS}		250	μA	
I_{BB}	Current from V_{BB}		250	μA	
P_{TOTAL}	Total Power Dissipation		10	mW	

SWITCHING CHARACTERISTICS

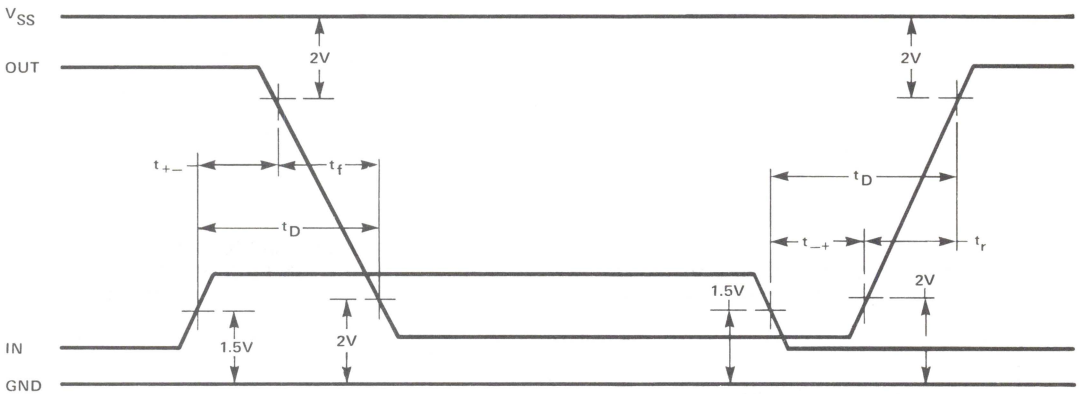
A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ±5%, V_{SS} = 16V ±5%, V_{BB} = V_{SS} +3 to 4V, f = 2 MHz, 50% Duty Cycle

SYMBOL	TEST	LIMITS (ns)				
		C_L = 100 pF		C_L = 200 pF		DELAY DIFFERENTIAL[1] C_L = 200 pF
		MIN.	MAX.	MIN.	MAX.	MAX.
t_{+-}	INPUT TO OUTPUT DELAY	5	15	5	15	5
t_{-+}	INPUT TO OUTPUT DELAY	5	25	5	25	10
t_r	OUTPUT RISE TIME	5	20	5	30	10
t_f	OUTPUT FALL TIME	5	20	10	30	10
t_D	DELAY + RISE OR FALL TIME	10	35	20	45	10

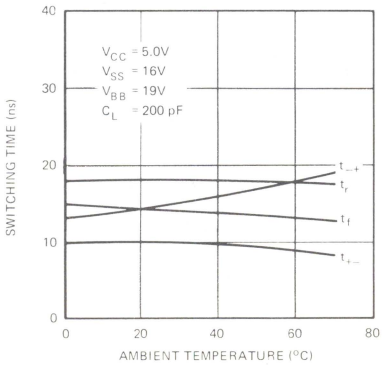
(1) This is defined as the maximum skew between any output in the same package, eg., all the input to output delays for the t_{-+} parameter are within a maximum of 10 nsec of each other in the same package.

WAVEFORMS

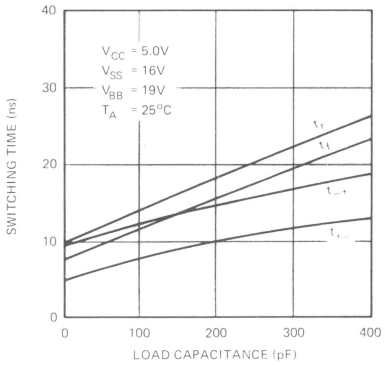


TYPICAL CHARACTERISTICS

SWITCHING TIME VS. AMBIENT TEMPERATURE

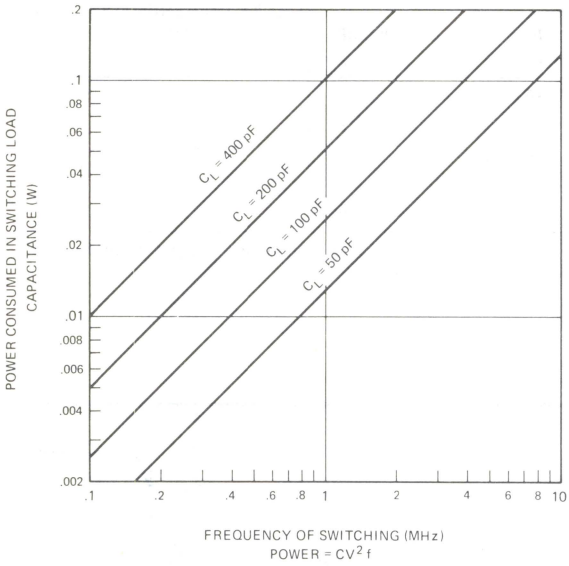


SWITCHING TIME VS. LOAD CAPACITANCE

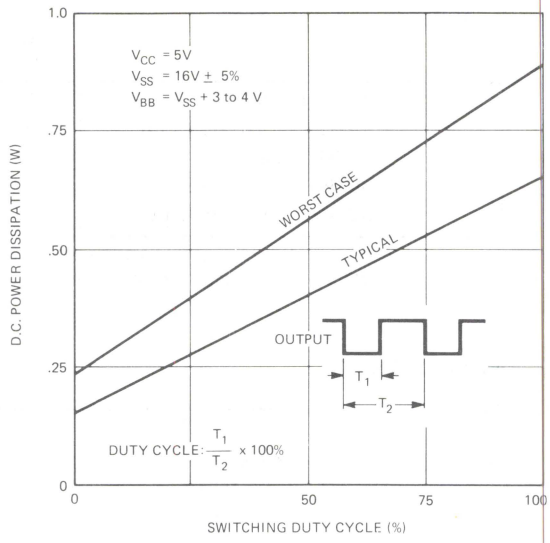


POWER AND SWITCHING CHARACTERISTICS

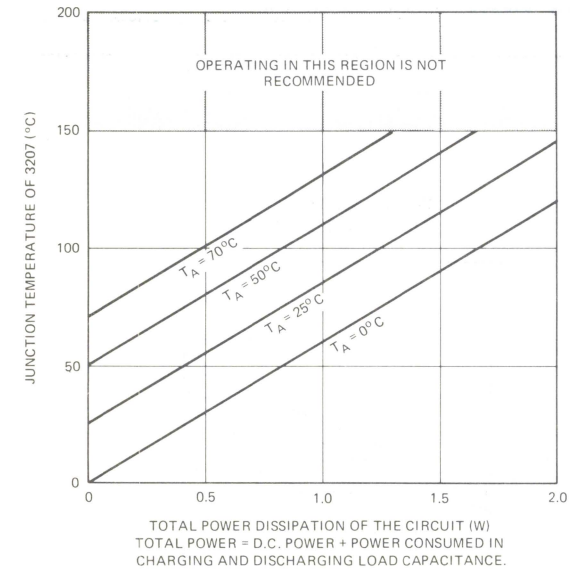
POWER CONSUMED IN CHARGING AND DISCHARGING LOAD CAPACITANCE OVER 0V TO 16V INTERVAL



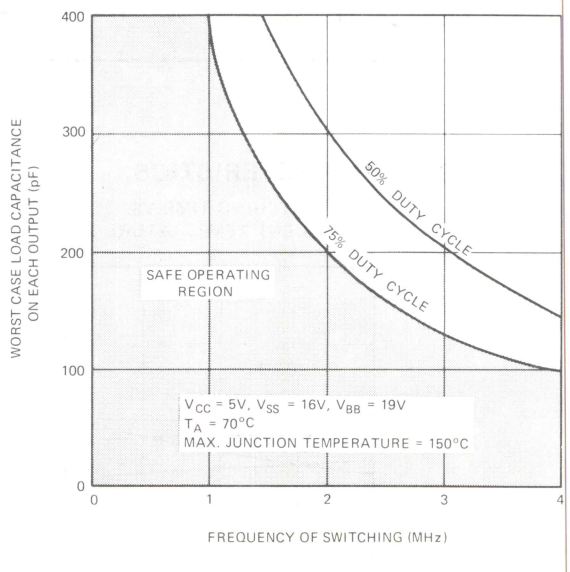
NO LOAD D.C. POWER DISSIPATION VS. OPERATING DUTY CYCLE



JUNCTION TEMPERATURE VS. TOTAL POWER DISSIPATION OF THE CIRCUIT



WORST CASELOAD CAPACITANCE ON EACH OUTPUT VS. FREQUENCY OF SWITCHING

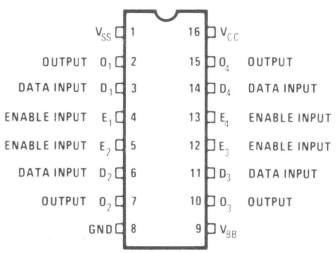


3207A-1
QUAD BIPOLAR-TO-MOS LEVEL SHIFTER AND DRIVER

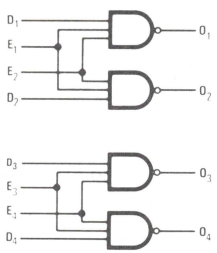
- **Power Supply Voltage Compatible with the High Voltage 1103-1**
- **1103-1 Memory Compatible at Output**

The Intel 3207A-1 is the high voltage version of the standard 3207A, and is compatible with the 1103-1. The 3207A-1 has all the same features as the standard 3207A. The absolute maximum ratings and pin configuration are repeated below for convenience, while the DC and AC characteristics appear below and on the next page.

PIN CONFIGURATION



LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . 0°C to +55°C
Storage Temperature . . . . . −65°C to +160°C
All Input Voltages . . . . . −1.0 to +21 Volts
Supply Voltage V_{CC} . . . . . −1.0 to +7.0 Volts
All Outputs and Supply Voltages V_{BB} and V_{SS} with respect to GND . . . . . −1.0 to +25 Volts
Power Dissipation at 25°C . . . . . 2 Watts

COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MEMORY SUPPORT

D.C. CHARACTERISTICS $T_A = 0°C$ to $55°C, V_{CC} = 5V \pm 5\%, V_{SS} = 19V \pm 5\%, V_{BB} - V_{SS} = 3.0V$ to $4.0V$

SYMBOL	TEST	LIMIT MIN.	LIMIT MAX.	UNIT	CONDITIONS
I_{FD}	DATA INPUT LOAD CURRENT		−0.25	mA	$V_D = .45V, V_{CC} = 5.25V$, All Other Inputs at 5.25V, $V_{SS} = 19V, V_{BB} = 23V$
I_{FE}	ENABLE INPUT LOAD CURRENT		−0.50	mA	$V_E = .45V, V_{CC} = 5.25V$, All Other Inputs at 5.25V, $V_{SS} = 19V, V_{BB} = 23V$
I_{RD}	DATA INPUT LEAKAGE CURRENT		20	μA	$V_D = 19V, V_{CC} = 5.0V$, All Other Inputs Grounded, $V_{SS} = 19V, V_{BB} = 23V$
I_{RE}	ENABLE INPUT LEAKAGE CURRENT		20	μA	$V_E = 19V, V_{CC} = 5.0V$, All Other Inputs Grounded, $V_{SS} = 19V, V_{BB} = 23V$
V_{OL}	OUTPUT "LOW" VOLTAGE		0.8 0.7 0.6	V(0°C) V(25°C) V(55°C)	$I_{OL} = 500\mu A, V_{CC} = 4.75V$ $V_{SS} = 19V, V_{BB} = 23V$ All Inputs at 2.0V
V_{OH} (MIN.)	OUTPUT "HIGH" VOLTAGE	$V_{SS} - 0.7$ $V_{SS} - 0.6$ $V_{SS} - 0.5$		V(0°C) V(25°C) V(55°C)	$I_{OH} = -500\mu A, V_{CC} = 5.0V$ $V_{SS} = 19V, V_{BB} = 23V$ All Inputs at 0.85V
V_{OH} (MAX.)			$V_{SS} + 1.0$	V	$I_{OH} = 5mA, V_{CC} = 5.0V$ $V_{SS} = 19V, V_{BB} = 23V$
I_{OL}	OUTPUT SINK CURRENT	100		mA	$V_O = 4V, V_{CC} = 5.0V, V_{SS} = 19V$, $V_{BB} = 23V, V_E = V_D = 2.0V$
I_{OH}	OUTPUT SOURCE CURRENT	−100		mA	$V_O = V_{SS} - 4V, V_{CC} = 5.0V, V_{SS} = 19V$ $V_{BB} = 23V, V_E = V_D = 0.85V$
V_{IL}	INPUT "LOW" VOLTAGE		1.0	V	$V_{CC} = 5.0V, V_{SS} = 19V, V_{BB} = 23V$
V_{IH}	INPUT "HIGH" VOLTAGE	2.0		V	$V_{CC} = 5.0V, V_{SS} = 19V, V_{BB} = 23V$
C_{IN}	INPUT CAPACITANCE		8(Typical)	pF	$V_{BIAS} = 2.0V, V_{CC} = 0V$

D.C. CHARACTERISTICS (Cont'd) $T_A = 0°C$ to $+55°C$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 19V \pm 5\%$, $V_{BB} - V_{SS} = 3.0V$ to $4.0V$

POWER SUPPLY CURRENT DRAIN:
All Outputs "Low"

Symbol	Parameter	Min.	Max.	Unit	Conditions
I_{CC}	Current from V_{CC}		83	mA	$V_{CC} = 5.25V$, $V_{SS} = 20V$, $V_{BB} = 24V$ All Inputs Open
I_{SS}	Current from V_{SS}		250	μA	
I_{BB}	Current from V_{BB}		25	mA	
P_{TOTAL}	Total Power Dissipation		1040	mW	

All Outputs "High"

I_{CC}	Current from V_{CC}		33	mA	$V_{CC} = 5.25V$, $V_{SS} = 20V$, $V_{BB} = 24V$ All Inputs Grounded
I_{SS}	Current from V_{SS}		250	μA	
I_{BB}	Current from V_{BB}		5	mA	
P_{TOTAL}	Total Power Dissipation		297	mW	

Standby Condition with $V_{CC} = 0V$, $V_{SS} = V_{BB}$

I_{CC}	Current from V_{CC}		0	mA	$V_{CC} = 0V$, $V_{SS} = 20V$, $V_{BB} = 20V$
I_{SS}	Current from V_{SS}		500	μA	
I_{BB}	Current from V_{BB}		500	μA	
P_{TOTAL}	Total Power Dissipation		15	mW	

MEMORY SUPPORT

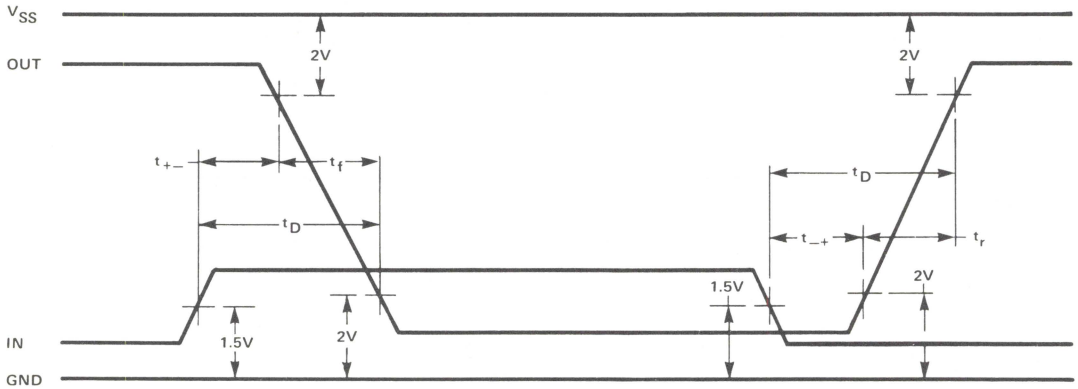
A.C. CHARACTERISTICS

$T_A = 0°C$ to $55°C$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 19V \pm 5\%$, $V_{BB} = V_{SS} + 3$ to $4V$, $f = 2$ MHz, 50% Duty Cycle

SYMBOL	TEST	LIMITS (ns)				
		$C_L = 100$ pF		$C_L = 200$ pF		DELAY DIFFERENTIAL (1) $C_L = 200$ pF
		MIN.	MAX.	MIN.	MAX.	MAX.
t_{+-}	INPUT TO OUTPUT DELAY	5	15	5	15	5
t_{-+}	INPUT TO OUTPUT DELAY	5	25	5	25	10
t_r	OUTPUT RISE TIME	5	20	5	30	10
t_f	OUTPUT FALL TIME	5	25	10	35	10
t_D	DELAY + RISE OR FALL TIME	10	35	20	45	10

(1) This is defined as the maximum skew between any output in the same package, eg., all the input to output delays for the t_{-+} parameter are within a maximum of 10 nsec of each other in the same package.

WAVEFORMS



3208A, 3408A
HEX BIPOLAR SENSE AMPLIFIERS FOR MOS CIRCUITS
3208A HEX SENSE AMPLIFIER
3408A HEX SENSE AMPLIFIER WITH LATCHES

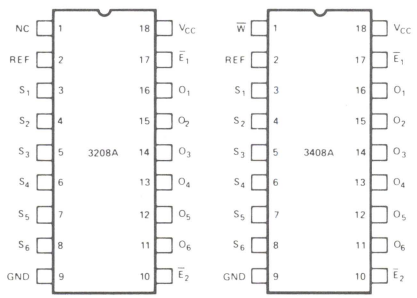
- **High Speed — 20nsec Max.**
- **Wire-OR Capability — Open Collector Output: 3208A Three-State Output: 3408A**
- **Single 5V Power Supply**
- **Input Level Compatible with 1103 Output**
- **Two Enable Inputs**
- **Minimum Line Reflection: Low Voltage Diode Input Clamp**
- **Plastic 18 Pin Dual In-Line Package**
- **Schottky TTL**

The Intel 3208A is a high speed hex sense amplifier designed to sense the output signals of the 1103 memory. The device features two separate enable inputs each controlling the output state of three sense amplifiers, and a common voltage reference input. OR-tie capability is available with the 3208A open collector TTL compatible output.

The 3408A is a hex sense amplifier with a latch circuit connected to each amplifier. The sensed data may be stored in the latches through application of a write pulse. The 3408A has three-state TTL outputs, hence in the non-enabled state the outputs float allowing wire-OR memory expansion. The latches may be bypassed by grounding the write input pin. Under this condition, the 3408A functions as a hex sense amplifier.

The 3208A and 3408A operate from a single +5 volt power supply. Device performance is specified over the complete ambient temperature range of 0°C to 70°C and over a V_{CC} supply voltage range of 5 volts ±5%. The 3208A and 3408A are packaged in an 18 pin plastic dual in-line package.

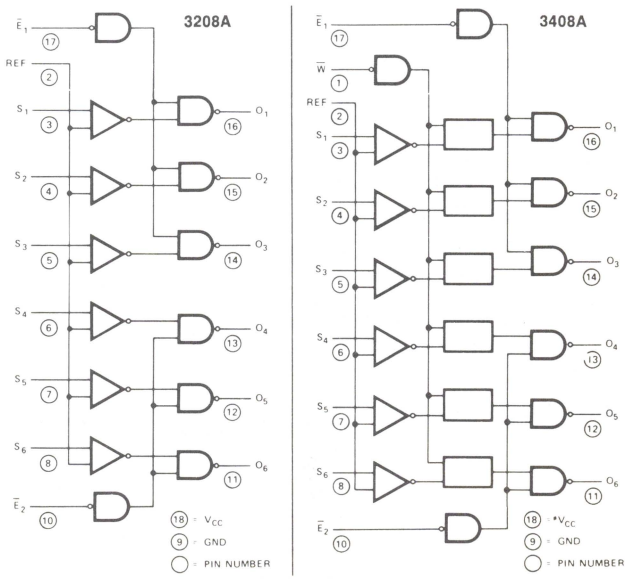
PIN CONFIGURATIONS



PIN NAMES

$S_1, S_2, S_3, S_4, S_5, S_6$	SENSE AMP INPUTS
$\bar{E}_1, \bar{E}_2$	ENABLE INPUTS
REF	REFERENCE INPUT
$O_1, O_2, O_3, O_4, O_5, O_6$	OUTPUTS (Non-inverting)
$\bar{W}$	WRITE INPUT (3408A only)

BLOCK DIAGRAMS



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	−55°C to +125°C
Storage Temperature	−65°C to +160°C
All Outputs or Supply Voltage	−0.5 to +7 Volts
All TTL Input Voltages	−1 to +5.5 Volts
All Sense Input Voltages	−1 to +1 Volt
Output Currents Total	300 mA
Input Current	125 mA

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at this or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS FOR 3208A T_A = 0°C to 70°C, V_{CC} = 5V ±5%

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
I_{FE}	INPUT LOAD CURRENT ON ENABLE INPUT			−0.25	mA	V_{CC} = 5.25V V_F = 0.45V
I_{RE}	INPUT LEAKAGE CURRENT ON ENABLE INPUT			20	μA	V_{CC} = 4.75V V_R = 5.25V
V_{IH}	INPUT "HIGH" VOLTAGE ON ENABLE INPUT	2.0			V	V_{CC} = 5.0V
V_{IL}	INPUT "LOW" VOLTAGE ON ENABLE INPUT			0.85	V	V_{CC} = 5.0V
V_{OL}	OUTPUT "LOW" VOLTAGE			0.45	V	V_{CC} = 4.75V I_{OL} = 10mA
I_{CEX}	OUTPUT LEAKAGE CURRENT			100	μA	V_{CC} = 5.25V V_{CEX} = 5.25V
I_{REF}	INPUT CURRENT ON REFERENCE INPUT			−150	μA	V_{CC} = 5.25V V_{REF} = 100mV
I_S	INPUT CURRENT ON SENSE AMP INPUT			−25	μA	V_{CC} = 5.25V V_S = 100mV
V_{SH}	INPUT "HIGH" VOLTAGE FOR SENSE AMP INPUT	V_{REF}			mV	V_{CC} = 4.75 to 5.25V V_{REF} = 100 to 200mV
V_{SL}	INPUT "LOW" VOLTAGE FOR SENSE AMP INPUT			V_{REF} −50	mV	V_{CC} = 4.75 to 5.25V V_{REF} = 100 to 200mV
V_{REF}	OPERATING RANGE OF REFERENCE VOLTAGE	100		200	mV	V_{CC} = 4.75 to 5.25V
I_{CC}	POWER SUPPLY CURRENT			120	mA	V_{CC} = 5.25V
V_C	INPUT CLAMP VOLTAGE ON ALL INPUTS			−1.0	V	V_{CC} = 4.75V I_C = −5.0mA
V_{SD}	SENSE INPUT CLAMP DIODE VOLTAGE			1.0	V	V_{CC} = 5.0V I_D = 5.0mA

3208A TRUTH TABLE

INPUTS		OUTPUT
Sense Amp	Enable	
$<V_{REF}$ −50mV	L	L
$>V_{REF}$	L	H
X	H	H

X = Don't care

D. C. Characteristics for 3408A $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
I_{FE}	INPUT LOAD CURRENT ON ENABLE INPUT			−0.25	mA	$V_{CC} = 5.25V$ $V_F = 0.45V$
I_{RE}	INPUT LEAKAGE CURRENT ON ENABLE INPUT			20	μA	$V_{CC} = 4.75V$ $V_R = 5.25V$
I_{FW}	INPUT LOAD CURRENT ON WRITE INPUT			−0.25	mA	$V_{CC} = 5.25V$ $V_F = 0.45V$
I_{RW}	INPUT LEAKAGE CURRENT ON WRITE INPUT			20	μA	$V_{CC} = 4.75V$ $V_R = 5.25V$
V_{IH}	INPUT "HIGH" VOLTAGE ON ENABLE AND WRITE INPUT	2.0			V	$V_{CC} = 5.0V$
V_{IL}	INPUT "LOW" VOLTAGE ON ENABLE AND WRITE INPUT			0.85	V	$V_{CC} = 5.0V$
V_{OL}	OUTPUT "LOW" VOLTAGE			0.45	V	$V_{CC} = 4.75V$ $I_{OL} = 10mA$
V_{OH}	OUTPUT "HIGH" VOLTAGE	2.4			V	$V_{CC} = 4.75V$ $I_{OH} = -1.5mA$
$\lvert I_O \rvert$	OUTPUT LEAKAGE CURRENT FOR HIGH IMPEDANCE STATE			100	μA	$V_{CC} = 5.25V$ $V_O = 0.45V/5.25V$
I_{SC}	OUTPUT SHORT CIRCUIT CURRENT	−40		−100	mA	$V_{CC} = 5.0V$ $V_O = 0V$
I_{REF}	INPUT CURRENT ON REFERENCE INPUT			−150	μA	$V_{CC} = 5.25V$ $V_{REF} = 100mV$
I_S	INPUT CURRENT ON SENSE INPUT			−25	μA	$V_{CC} = 5.25V$ $V_S = 100mV$
V_{SH}	INPUT "HIGH" VOLTAGE FOR SENSE AMP INPUT	V_{REF}			mV	$V_{CC} = 4.75$ to $5.25V$ $V_{REF} = 100$ to $200mV$
V_{SL}	INPUT "LOW" VOLTAGE FOR SENSE AMP INPUT			V_{REF} −60	mV	$V_{CC} = 4.75$ to $5.25V$ $V_{REF} = 100$ to $200mV$
V_{REF}	OPERATING RANGE OF REFERENCE VOLTAGE	100		200	mV	$V_{CC} = 4.75$ to $5.25V$
I_{CC}	POWER SUPPLY CURRENT			125	mA	$V_{CC} = 5.25V$
V_C	INPUT CLAMP VOLTAGE ON ALL INPUTS			−1.0	V	$V_{CC} = 4.75V$ $I_C = -5.0V$
V_{SD}	SENSE INPUT CLAMP DIODE VOLTAGE			1.0	V	$V_{CC} = 5.0V$ $I_D = 5.0mA$

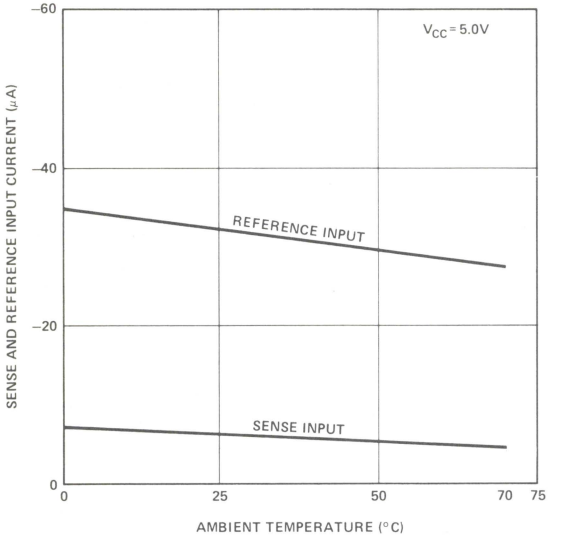
3408A TRUTH TABLE

INPUTS			OUTPUT
Sense Amp	Enable	Write	
$< V_{REF} - 60mV$	L	L	L
$> V_{REF}$	L	L	H
X	L	H	Previous Data Stored
X	H	X	High Z*

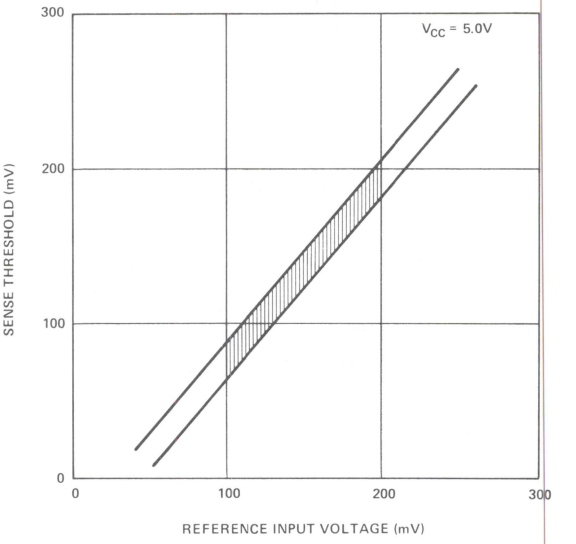
X = Don't care
*The output of the 3408A is three-state, hence when not enabled the output is a high impedance.

TYPICAL D.C. CHARACTERISTICS FOR 3208A/3408A

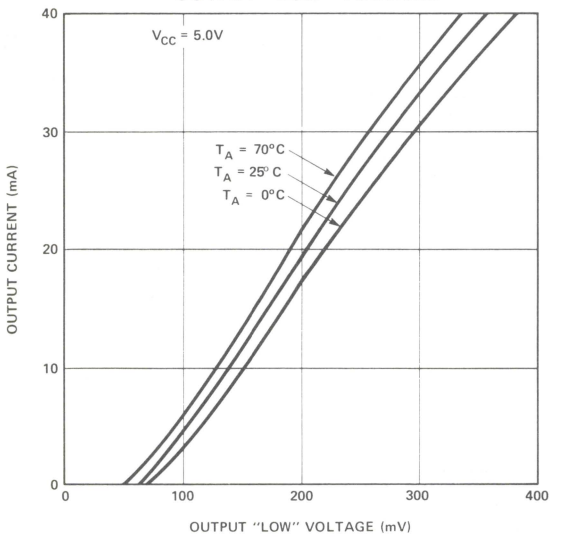
SENSE AND REFERENCE INPUT CURRENT VS. AMBIENT TEMPERATURE



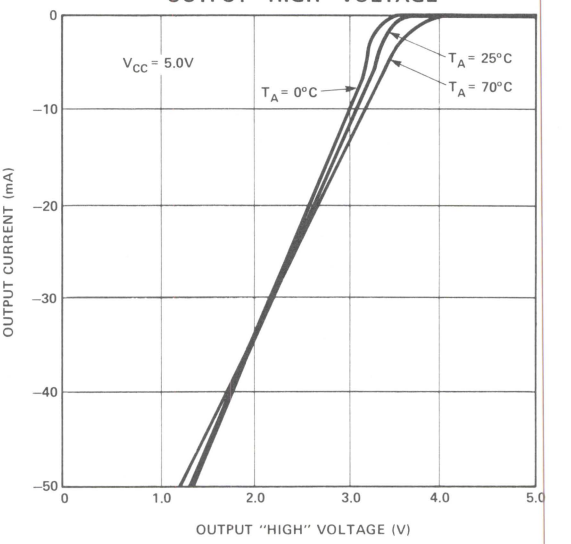
SENSE THRESHOLD VS. REFERENCE INPUT VOLTAGE



OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE



OUTPUT CURRENT VS. OUTPUT "HIGH" VOLTAGE



A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

3208A

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
t_{S-}	SENSE AMP INPUT TO OUTPUT DELAY			20	ns	D.C. LOAD = 10mA C_L = 30pF
t_{E-}	ENABLE INPUT TO OUTPUT DELAY			20	ns	D.C. LOAD = 10mA C_L = 30pF
t_{E+}				25		

3408A

t_{WP}	WRITE PULSE WIDTH	30			ns	D.C. LOAD = 10mA C_L = 30pF
t_{S-}	SENSE AMP INPUT TO OUTPUT DELAY			25	ns	D.C. LOAD = 10mA C_L = 30pF
t_{E-}	ENABLE INPUT TO OUTPUT DELAY, LATCH STORES "LOW"			20	ns	D.C. LOAD = 10mA C_L = 30pF
t_{E+}	ENABLE INPUT TO OUTPUT DELAY, LATCH STORES "HIGH"			25	ns	D.C. LOAD = 10mA C_L = 30 pF

CAPACITANCE (1) $T_A = 25°C$, f = 1 MHz

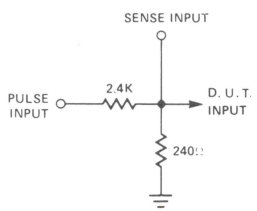
SYMBOL	TEST	LIMITS TYP.	LIMITS MAX.
C_O	V_{CC} = 0V, V_{BIAS} = 2.0V	8	12
C_{INE}	ENABLE INPUT V_{CC} = 0V, V_{BIAS} = 2.0V	6	10
C_{INS}	SENSE INPUT V_{CC} = 0V, V_{BIAS} = 0V	6	10

(1) This parameter is periodically sampled and is not 100% tested.

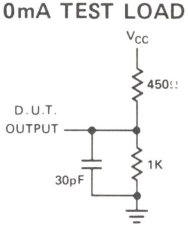
SWITCHING CHARACTERISTICS

CONDITIONS OF TEST

- Input Pulse amplitude: 2.5V for all TTL compatible inputs and 2.5V through a resistor network as shown below for sense input.
- Input Pulse rise and fall times: 5ns.
- Speed measurements are made at 1.5V for all TTL compatible inputs and outputs, and for sense input, see network and waveforms below. V_{REF} is set at 150mV.

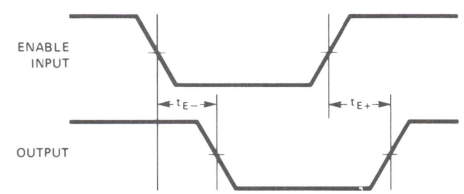


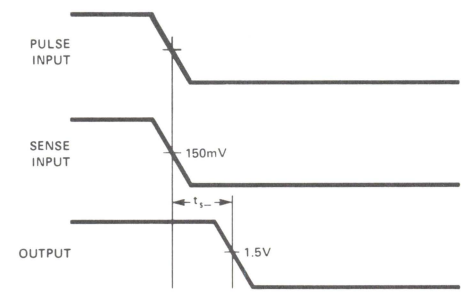
10mA TEST LOAD



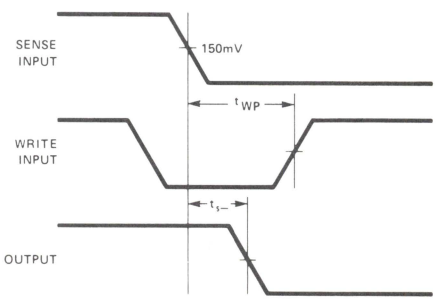
WAVEFORMS

3208A/3408A





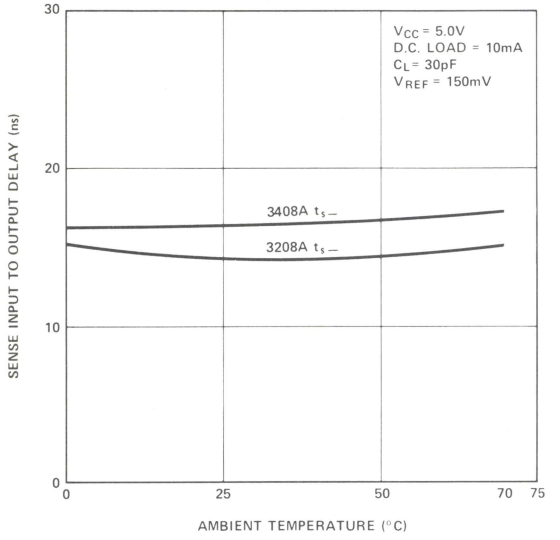
3408A ONLY



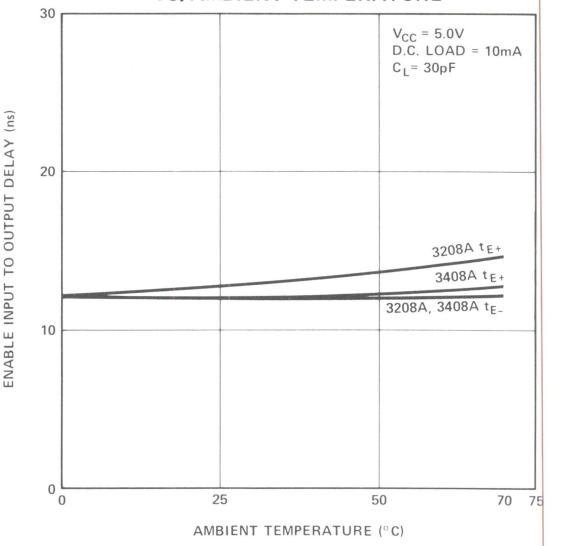
MEMORY SUPPORT

TYPICAL A.C. CHARACTERISTICS

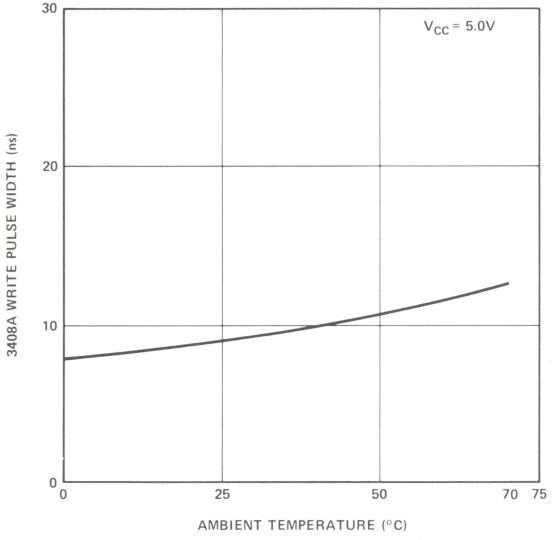
SENSE INPUT TO OUTPUT DELAY VS. AMBIENT TEMPERATURE



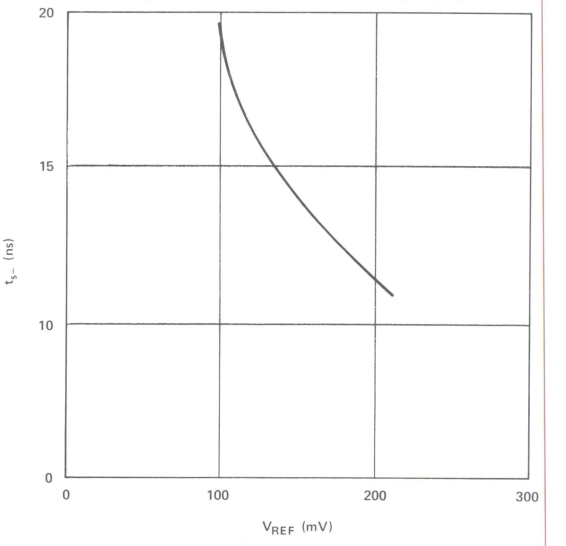
ENABLE INPUT TO OUTPUT DELAY VS. AMBIENT TEMPERATURE



3408A WRITE PULSE WIDTH VS. AMBIENT TEMPERATURE



SENSE INPUT TO OUTPUT DELAY VS. REFERENCE INPUT VOLTAGE



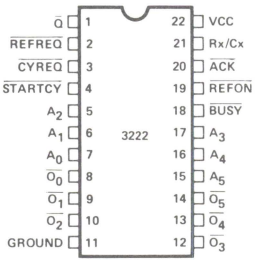
3222
REFRESH CONTROLLER FOR 4K DYNAMIC RANDOM ACCESS MEMORIES

- **Ideal for use in 2107A, 2107C Systems**
- **Simplifies System Design**
- **Reduces Package Count**
- **Standard 22-Pin DIP**
- **Adjustable Refresh Timing Oscillator**
- **6-Bit Address Multiplexer**
- **6-Bit Refresh Address Counter**
- **Refresh Cycle Controller**

The Intel® 3222 is a refresh controller for dynamic RAMs requiring refresh of up to 6 input addresses (or 4K bits for 64 x 64 organization). The device contains an accurate refresh timer (whose frequency can be set by an external resistor and capacitor), plus all necessary control and I/O circuitry to provide for the refresh requirements of dynamic RAMs. The chip's high performance makes it especially suitable for use with high speed N-channel RAMs like the Intel® 2107C. The 3222 is well suited for asynchronous dynamic memory systems.

The 3222 operates from a single +5 volt power supply and is specified for operation over a 0°C to 75°C ambient temperature range. It is fabricated by means of Intel's highly reliable Schottky bipolar process.

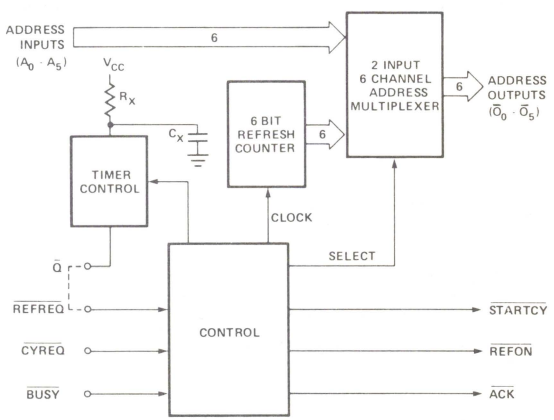
PIN CONFIGURATION



PIN NAMES

$A_0 - A_5$	ADDRESS INPUTS	$\bar{O}_0 - \bar{O}_5$	ADDRESS OUTPUTS
$\overline{ACK}$	ACKNOWLEDGE OUTPUT	$\bar{Q}$	INTERNAL REFRESH REQUEST LATCH OUTPUT
$\overline{BUSY}$	BUSY INPUT	$\overline{REFON}$	REFRESH ON OUTPUT
$\overline{CYREQ}$	CYCLE REQUEST INPUT	$\overline{REFREQ}$	REFRESH REQUEST INPUT
		RxCx	RC TIE POINT
		$\overline{STARTCY}$	START CYCLE OUTPUT
		V_{CC}	+5V SUPPLY

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . -65° to +125°C
Storage Temperature . . . . . -65° to +160°C
All Input, Output or Supply Voltages . . . . -0.5V to +7V
All Input Voltages . . . . . -1.0V to +5.5V
Output Currents . . . . . 100 mA
Power Dissipation . . . . . 1 W

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS All Limits Apply for V_{CC} = +5.0V ±5%, T_A = 0°C to +75°C.

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[1]	Max.		
I_{FB}	Input Load Current $\overline{BUSY}$		0.40	1	mA	V_{IN} = 0.45V
I_{FO}	Input Load Current All Other Inputs		0.05	0.25	mA	V_{IN} = 0.45V
I_{RB}	Input Leakage Current $\overline{BUSY}$		<1	50	μA	V_{IN} = V_{CC}
I_{RO}	Input Leakage Current All Other Inputs		<1	20	μA	V_{IN} = 5.25V
V_{CLAMP}	Input Clamp Voltage		-0.76	-1	V	I_C = -5.0mA
V_{IL}	Input "Low" Voltage			0.8	V	
V_{IH}	Input "High" Voltage	2.0			V	
I_{CC}	Power Supply Current		91	120	mA	V_{CC} = 5.25V
I_{SC}	Output High Short Circuit Current		-48	-70	mA	V_{OUT} = 0V V_{CC} = 5.25V
V_{OL}	Output Low Voltage		0.32	0.45	V	I_{OL} = 5mA
V_{OH}	Output High Voltage ($\overline{O}_0$-$\overline{O}_5$)	2.6	3.1		V	I_{OH} = -1mA V_{CC} = 4.75V
V_{OH1}	Output High Voltage (All Other Outputs)	2.4	3.0		V	I_{OH} = -1mA V_{CC} = 4.75V

Note 1: Typical values are for T_A = 25°C and nominal power supply voltages.

Capacitance[2], T_A = 25°C

Symbol	Test	Limits (pF)		Conditions
		Typ.	Max.	
C_{IN} (Address)	Input Capacitance	5	10	V_{bias} = 2.0V
C_{IN} ($\overline{CYREQ}$)	Input Capacitance	6	10	V_{CC} = 0V
C_{IN} ($\overline{BUSY}$)	Input Capacitance	20	30	f = 1MHz

Note 2: This parameter is periodically sampled and is not 100% tested.

A.C. Characteristics

All Limits Apply for V_{CC} = +5.0V ±5%, T_A = 0°C to +75°C. Load = 1 TTL, C_L = 15pF.
Conditions of Test: Input pulse amplitude: 3V, Input rise and fall times: 5ns between 1V and 2V. Measurements are made at 1.5V.

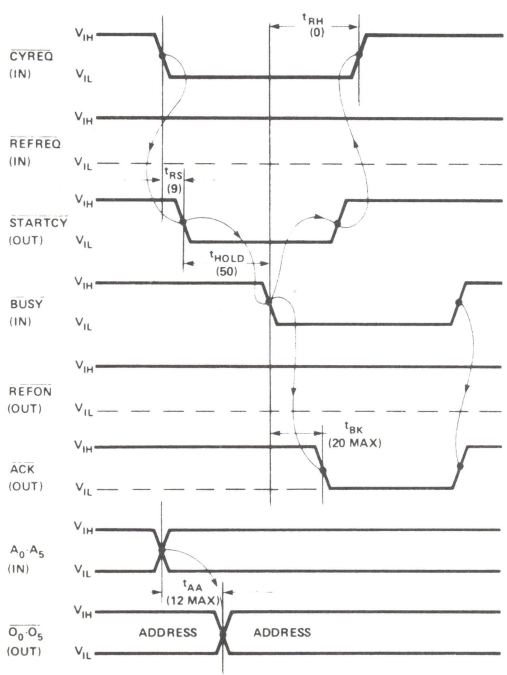
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Conditions
t_{AA}	Address In to Address Out		7	12	ns	$\overline{BUSY}$ = V_{IH}
t_{BAM}	$\overline{BUSY}$ In to Address Out		21	28	ns	
t_{BAR}	$\overline{BUSY}$ In to Counter Out		18	27	ns	
t_{BK}	$\overline{BUSY}$ In to $\overline{ACK}$ Out		14	20	ns	$\overline{REFREQ}$ = V_{IH}, $\overline{CYREQ}$ = V_{IL}
t_{BR}	$\overline{BUSY}$ In to $\overline{REFON}$ Out		15	24	ns	
t_{BS}	$\overline{BUSY}$ In to $\overline{STARTCY}$ Out	4	7	14	ns	$\overline{CYREQ}$ = V_{IL}
t_{HOLD}	$\overline{BUSY}$ Hold Time	50			ns	External Delay between $\overline{STARTCY}$ and $\overline{BUSY}$
t_{RH}	$\overline{CYREQ}$ or $\overline{REFREQ}$ Hold Time	0			ns	External Delay after $\overline{BUSY}$
t_{RR}	$\overline{REFREQ}$ to $\overline{REFON}$		18	26	ns	$\overline{CYREQ}$ and $\overline{BUSY}$ = V_{IH}, No priority contention between $\overline{REFREQ}$ and $\overline{CYREQ}$
t_{RRC}	$\overline{REFREQ}$ to $\overline{REFON}$		33	45	ns	$\overline{BUSY}$ = V_{IH}
t_{RS}	$\overline{CYREQ}$ or $\overline{REFREQ}$ In to $\overline{STARTCY}$ Out	9	14	21	ns	$\overline{BUSY}$ = V_{IH}
t_{Setup}	$\overline{BUSY}$ Setup Time	120			ns	$\overline{BUSY}$ = V_{IL} During Refresh

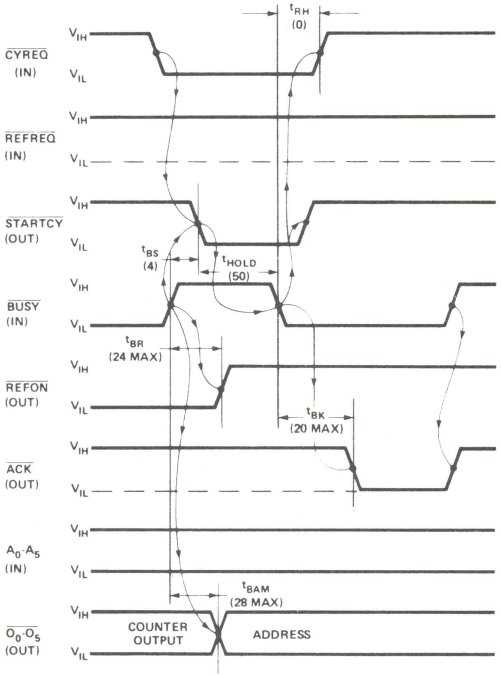
Note 1: Typical values are for T_A = 25°C and nominal power supply voltages.

A. SYSTEM MEMORY CYCLE WITH MEMORY NOT BUSY

B. SYSTEM MEMORY CYCLE WITH MEMORY BUSY (FOLLOWING REFRESH CYCLE)

(Numbers in parentheses are minimum values in ns unless otherwise specified.)



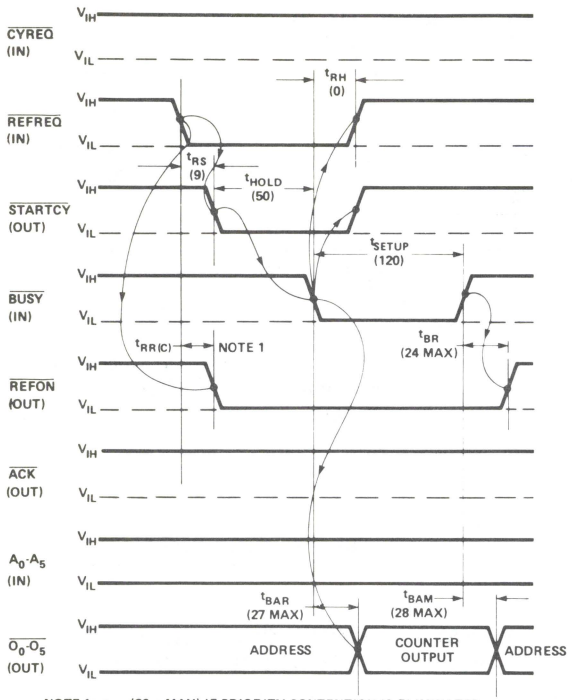


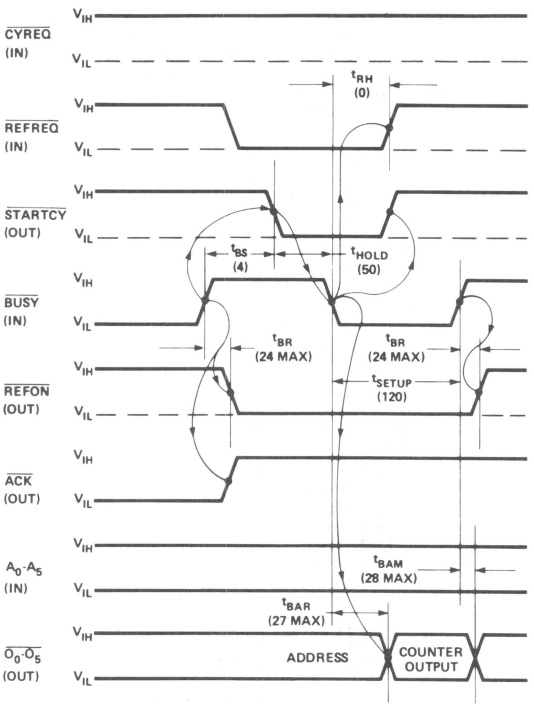
MEMORY SUPPORT

C. REFRESH MEMORY CYCLE WITH MEMORY NOT BUSY

D. REFRESH MEMORY CYCLE WITH MEMORY BUSY (FOLLOWING SYSTEM CYCLE)

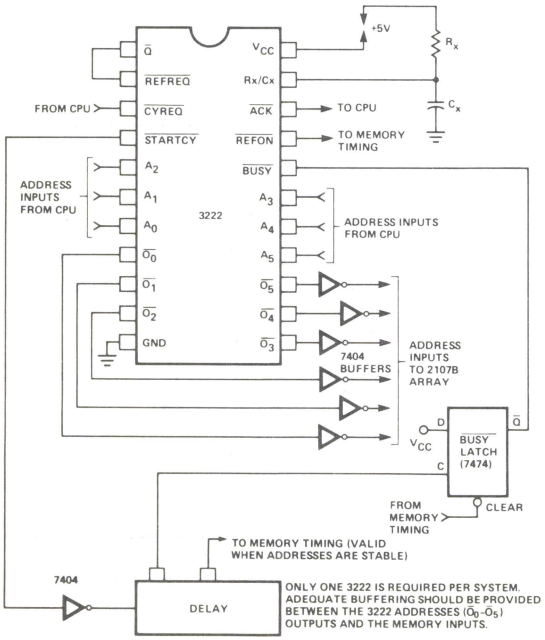
(Numbers in parentheses are minimum values in ns unless otherwise specified.)



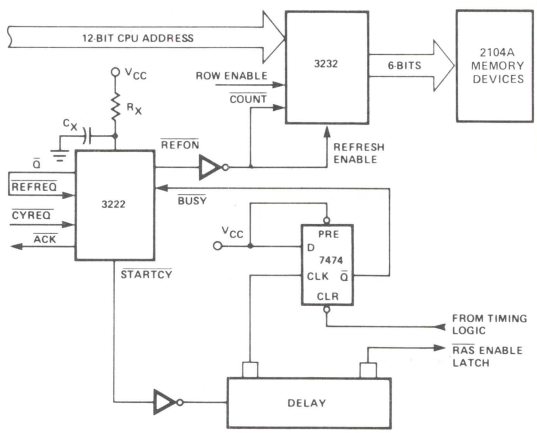


NOTE 1: t_{RR} (26ns MAX) IF PRIORITY CONTENTION IS ELIMINATED; t_{RRC}

E. TYPICAL APPLICATION OF 3222 REFRESH CONTROLLER IN A 2107C SYSTEM



F. USE OF 3222 FOR REFRESH TIMING AND CONTROL IN A 2104A SYSTEM



PIN NAMES AND FUNCTIONS

Pin No.	Pin Name	Function
1	$\overline{Q}$	Output of the internal Refresh Request latch. This pin may be connected to the Refresh Request input ($\overline{REFREQ}$) directly for asynchronous sequential mode refresh or indirectly through control logic for burst mode or synchronous mode refresh (see text).
2	$\overline{REFREQ}$	Refresh Request input (active when low). The request is honored only if the memory is not presently executing a cycle ($\overline{BUSY}$ high) and if a system cycle request did not occur first.
3	$\overline{CYREQ}$	System Memory Cycle Request input (active when low). The request is honored only if the memory is not presently executing a cycle ($\overline{BUSY}$ high) and if a refresh request did not occur first.
4	$\overline{STARTCY}$	Output signal indicating to external circuitry that a memory cycle (system or refresh) is to begin. See text for timing considerations for a refresh cycle.
5-7 15-17	A_0-A_5	Low order system address inputs. These addresses are multiplexed to the address output pins ($\overline{O}_0$-$\overline{O}_5$) during a system cycle.
8-10	$\overline{O}_0$-$\overline{O}_5$	Low order memory address outputs. During a system cycle these outputs give the low order (A_0-A_5) address of a memory access. During a refresh cycle these outputs give the refresh address (generated internal to the 3222).
11	GROUND	Ground.
18	$\overline{BUSY}$	An externally generated signal which the 3222 monitors to determine memory system status. If $\overline{BUSY}$ is high the memory is not busy and a system or refresh cycle may begin. If $\overline{BUSY}$ is low the memory is being accessed for a data I/O or refresh cycle and no other cycle may begin.
19	$\overline{REFON}$	The 3222 output which when low indicates the memory system is either ready to begin or is in a refresh cycle (Refresh On).
20	$\overline{ACK}$	The 3222 output which when low indicates the memory system is either ready to begin or is in a system cycle (system cycle request accepted and acknowledged).
21	RX/CX	Connection point for the RC network which determines the refresh period for sequential refresh mode. (See Refresh Control section).
22	V_{CC}	+5 volt supply.

FUNCTIONAL DESCRIPTION

The Intel® 3222 performs the four basic functions of a refresh controller by:

1. Providing a refresh timing oscillator.
2. Generating six bit refresh addresses.
3. Multiplexing refresh and system addresses to the six low order address inputs ($\overline{O}_0$-$\overline{O}_5$).
4. Providing control signals for both refresh and memory cycle accesses.

As shown in the pin configuration figure, the 3222 has as inputs the six low order (A_0-A_5) system addresses. These addresses are internally multiplexed with six internally generated refresh addresses. The output of these multiplexers provide the six low order addresses to the memory array.

The block diagram shows the four main circuit categories of the 3222. An explanation of the workings of each of these categories is given in the Device Operation section from a users point of view.

DEVICE OPERATION

Operation of the Intel® 3222 Refresh Controller is most easily explained by considering five conditions presented by the three input control lines Cycle Request ($\overline{CYREQ}$), Refresh Request ($\overline{REFREQ}$), and System Busy ($\overline{BUSY}$). These conditions are:

1. System memory cycle request — memory not busy ($\overline{BUSY}$ = High)
2. System memory cycle request — memory busy ($\overline{BUSY}$ =Low)
3. Refresh cycle request — memory not busy ($\overline{BUSY}$ = High)
4. Refresh cycle request — memory busy ($\overline{BUSY}$ =Low)
5. Simultaneous system memory cycle and refresh cycle requests.

Condition 5 is actually a subset of the four previous conditions and is included for completeness.

As is implied in the five conditions, the response of the 3222 to both refresh and memory cycles is dependent on the state of the $\overline{BUSY}$ input. The $\overline{BUSY}$ signal is generated externally to the 3222 and, when low, defines the time when the memory is performing a cycle (refresh or memory access). It is important to assure that $\overline{BUSY}$ is low for the *entire* memory cycle time. Interference may occur in asynchronous memory systems if the $\overline{BUSY}$ input goes high prematurely. (An asynchronous memory system is one in which the refresh and memory cycle requests occur independent of each other.)

System Memory Cycle Request — Memory Not Busy

This section details operation of the 3222 when the memory is not busy and a request for a system memory cycle is made (See Figure A for timing sequences). The request for a memory cycle is made by the $\overline{CYREQ}$ input going low. The Start Cycle output $\overline{STARTCY}$ goes low at t_{RS} after $\overline{CYREQ}$. $\overline{STARTCY}$ is used for two purposes:

1. To set the external $\overline{BUSY}$ latch. (See Figure E.)
2. To initiate memory system timing (after appropriate delay).

The required delay time depends on system configuration and associated delay paths for both Chip Enable (2107B input signal) and system addresses.

The low going $\overline{BUSY}$ input causes the internally generated Start Cycle output to go high and the Acknowledge output $\overline{ACK}$ to go low (after t_{BK} time). The Acknowledge output confirms that the requested system memory cycle has been accepted by the 3222. Note that the cycle request input may be returned to the high state when the $\overline{BUSY}$ input goes low. However, at the designer's discretion, the cycle request line may remain low until "just prior" to $\overline{BUSY}$ returning high. (If $\overline{BUSY}$ goes high before $\overline{CYREQ}$ goes high, another memory access may inadvertently be started.)

When the memory is not busy and a cycle request has been made, the low order system address delay through the 3222 is t_{AA} nsec. When the 3222 is not busy, the low order system addresses (A_0-A_5) are gated through to the output ($\overline{O}_0$-$\overline{O}_5$) independent of any other input.

System Memory Cycle Request — Memory Busy

The major differences between a system memory cycle request when the system is busy and when it is not busy (as previously described) are:

1. The Start Cycle output $\overline{STARTCY}$ does not go low until t_{BS} after the rising edge of the $\overline{BUSY}$ input. (Even though the $\overline{CYREQ}$ input is low.)
2. Output addresses $\overline{O}_0$-$\overline{O}_5$ change at or before t_{AA} time if the previous cycle was a system cycle request and change at or before t_{BAM} if the previous cycle was a Refresh Cycle request. (Note that the longer delay is after a refresh cycle.) See Figure B for definition of terms.

Note that for a system memory cycle following a refresh cycle, the refresh on output $\overline{REFON}$ goes high at or before t_{BR} relative to $\overline{BUSY}$ going high. Since the Acknowledge output $\overline{ACK}$ can not go low until after t_{HOLD} there is no ambiguity between $\overline{REFON}$ and $\overline{ACK}$. The memory is always defined as being in a refresh cycle, system cycle or no cycle.

Refresh Cycle — Memory Not Busy

Operation of the 3222 for a refresh request with the memory not busy (see Figure C) is similar to a system cycle request under the same condition. A refresh cycle is initiated by the Refresh Request input ($\overline{REFREQ}$) going low. This low going input causes both the Start Cycle output, $\overline{STARTCY}$, and Refresh On output, $\overline{REFON}$, to go low at t and t_{RRC} (or t_{RR}) time respectively. The low going edge of $\overline{STARTCY}$ is used to set the external $\overline{BUSY}$ latch low. As in the previous two cases, the $\overline{BUSY}$ input must remain low for the entire cycle required by the memory. As in the previous two cases, the low going $\overline{BUSY}$ drives the $\overline{STARTCY}$ output high.

Refresh Cycle — Memory Busy

For this condition, it is assumed that the previous cycle was a system access cycle. Timing conditions for this operation are shown in Figure D. Here, the $\overline{STARTCY}$ input goes low t_{BS} after $\overline{BUSY}$ returns high from the previous cycle. As before, $\overline{REFON}$ goes low t_{BR} after $\overline{BUSY}$ goes high. After t_{HOLD}, relative to $\overline{STARTCY}$, $\overline{BUSY}$ again goes low and places the low order refresh addresses on the address outputs ($\overline{O}_0$-$\overline{O}_5$) after t_{BAR} time. Internal refresh timing is performed in a manner identical to that described in Refresh Cycle-Memory Not Busy section.

Simultaneous Refresh and Memory System Cycle Request

The simultaneous request for a refresh and memory system access is almost a certainty in asynchronous systems. It is, therefore, necessary to have circuitry in any refresh controller capable of resolving the attendent ambiguity with minimum additional delay. The Intel® 3222 Refresh Controller has just such a circuit. (All timing parameters specified for asynchronous operation assume that a refresh and memory system request can occur at the same time.) A latch internal to the 3222 decides which signal ($\overline{CYREQ}$ or $\overline{REFREQ}$) it will accept if both occur simultaneously, and conditions the other control circuits appropriately. If a refresh cycle was accepted, $\overline{REFON}$ will go low at the appropriate time. If a memory system access was accepted then $\overline{ACK}$ will go low at the appropriate time.

Refresh Control

The 3222 controls both burst and distributed refresh modes. The burst refresh mode requires that $\overline{REFREQ}$ be generated externally to the 3222 since refresh is completed in 64 consecutive cycles every 2ms. A system requiring distributed refresh timing, however can be controlled either by the 3222 or by external circuitry. If refresh timing is to be controlled by the 3222 the output $\overline{Q}$ is tied to the $\overline{REFREQ}$ input. Timing is controlled by an oscillator internal to the 3222. The desired refresh timing interval is determined by:

1. $\frac{t_{REF}}{r} = .63\ R_xC_x$

   Where:

   t_{REF} = the total time between refreshes (e.g. 2msec) in msec.

   r = the number of rows to be refreshed on the memory device (for the 2107C r = 64).

   R_X = external timing resistance in KΩ (3K to 10K)

   C_x = external timing capacitance in μf. (0.005μf to 0.02μf)

The 3222's oscillator stability is guaranteed to be ±2% for a given part and ±6% from part to part, both over the ranges $0°C \leq T_A \leq 75°C$ and $V_{CC} = 5.0V \pm 5\%$.

Figure F shows how the 3222 may be used to control refresh in a 2104A system.

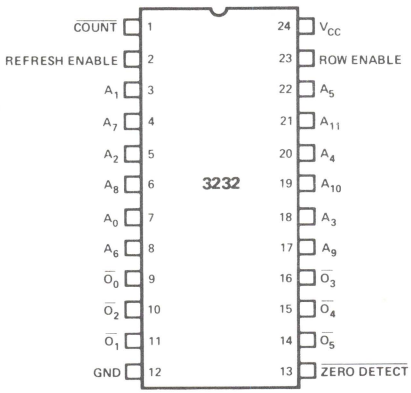
3232
ADDRESS MULTIPLEXER AND REFRESH COUNTER FOR 4K DYNAMIC RAMs

- **Ideal for 2104A**
- **Simplifies System Design**
- **Reduces Package Count**
- **Standard 24-Pin DIP**
- **Address Input to Output Delay: 9ns Maximum Driving 15pF, 25ns Maximum Driving 250pF**
- **Suitable for Either Distributed or Burst Refresh**
- **Single Power Supply: +5 Volts ±10%**

The Intel® 3232 contains an address multiplexer and refresh counter for multiplexed address dynamic RAMs requiring refresh of up to 6 input addresses (or 4K bits for 64 x 64 organization). It multiplexes twelve bits of system supplied address to six output address pins. The device also contains a 6 bit refresh counter which is externally controlled so that either distributed or burst refresh may be used. The high performance of the 3232 makes it especially suitable for use with high speed N-channel RAMs like the 2104A.

The 3232 operates from a single +5 volt power supply and is specified for operation over a 0 to +75°C ambient temperature range.

PIN CONFIGURATION



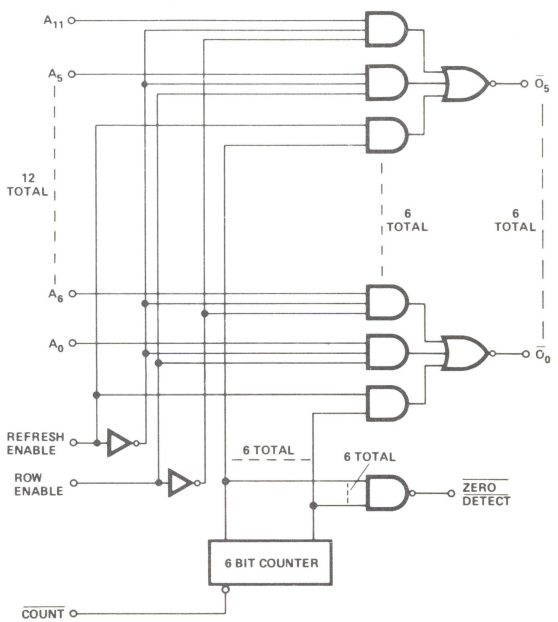
NOTE: A_0 THROUGH A_5 ARE ROW ADDRESSES.
A_6 THROUGH A_{11} ARE COLUMN ADDRESSES.

TRUTH TABLE AND DEFINITIONS:

REFRESH ENABLE	ROW ENABLE	OUTPUT
H	X	REFRESH ADDRESS (FROM INTERNAL COUNTER)
L	H	ROW ADDRESS (A_0 THROUGH A_5)
L	L	COLUMN ADDRESS (A_6 THROUGH A_{11})

$\overline{\text{COUNT}}$ – ADVANCES INTERNAL REFRESH COUNTER.
$\overline{\text{ZERO DETECT}}$ – INDICATES A ZERO IN THE REFRESH ADDRESS (USED IN BURST REFRESH MODE).

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -65° to +125°C
Storage Temperature ..... -65° to +160°C
All Input, Output, or
Supply Voltages .....-0.5V to +7 Volts
Output Currents 100mA
Power Dissipation 1W

COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

All Limits Apply for V_{CC} = 5.0V ±10%, T_A = 0°C to + 75°C

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.(1)	MAX.		
I_F	Input Load Current		-0.04	-0.25	mA	V_{IN} = 0.45V
I_R	Input Leakage Current		0	10	μA	V_{IN} = 5.5V
V_{IH}	Input High Voltage	2.0			V	
V_{IL}	Input Low Voltage			0.8	V	
V_{OL}	Output Low Voltage		0.25	0.40	V	I_{OL} = 5mA
V_{OH}	Output High Voltage ($\overline{O}_0$-$\overline{O}_5$)	2.8	4.0		V	I_{OH} = −1mA
V_{OH1}	Output High Voltage ($\overline{Zero\ Detect}$)	2.4	3.3		V	I_{OH} = −1mA
I_{CC}	Power Supply Current		100	150	mA	V_{CC} = 5.5V

Note 1. Typical values are for T_A = 25°C and V_{CC} = 5.0V.

A.C. CHARACTERISTICS

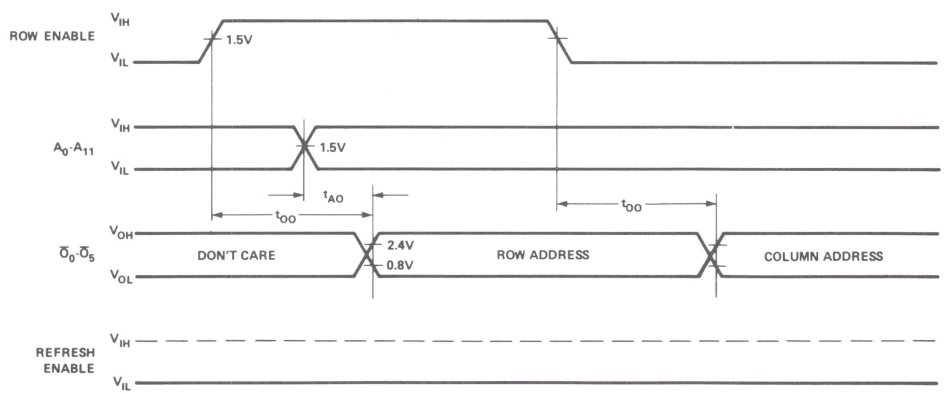
All Limits Apply for V_{CC} = +5.0V ±10%, T_A = 0°C to 75°C, Load = 1 TTL, C_L = 250pF, Unless Otherwise Specified.

SYMBOL	PARAMETER	MIN.	TYP.[1]	MAX.	UNIT	CONDITIONS
t_{AO}	Address Input to Output Delay		6	9	ns	Refresh Enable = Low[1] [2]
t_{AO1}	Address Input to Output Delay		16	25	ns	Refresh Enable = Low
t_{OO}	Row Enable to Output Delay	7	12	27	ns	Refresh Enable = Low[1] [2]
t_{OO1}	Row Enable to Output Delay	12	28	41	ns	Refresh Enable = Low
t_{EO}	Refresh Enable to Output Delay	7	14	27	ns	Note 1, 2
t_{EO1}	Refresh Enable to Output Delay	12	30	45	ns	
t_{CO}	$\overline{Count}$ to Output	15	40	60	ns	Refresh Enable = High[1] [2]
t_{CO1}	$\overline{Count}$ to Output	20	55	80	ns	Refresh Enable = High
f_C	Counting Frequency	5			MHz	
t_{CPW}	$\overline{Count}$ Pulse Width	35			ns	
t_{CZ}	$\overline{Count}$ to $\overline{Zero\ Detect}$	15		70	ns	Note 2

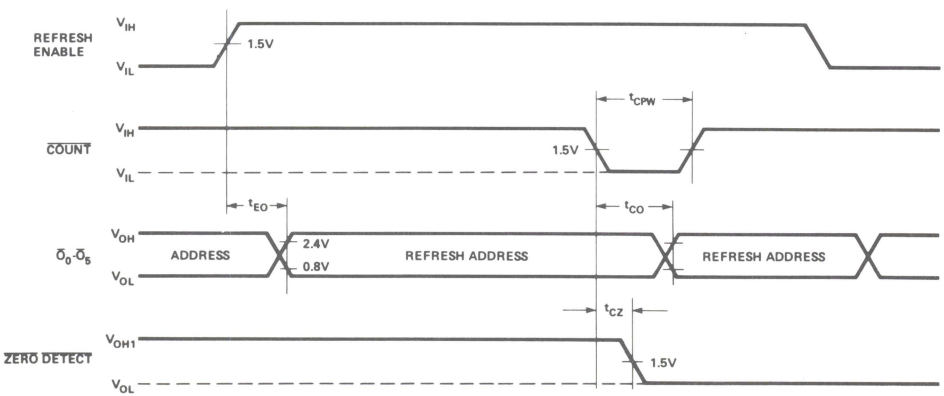
Note 1: V_{CC} = 5.0V, T_A = 25°C
2: C_L = 15pF

A.C. TIMING WAVEFORMS (Typically used with 2104A)

NORMAL CYCLE



REFRESH CYCLE



PIN NAMES AND FUNCTIONS

Pin. No.	Pin Name	Function
1	$\overline{\text{Count}}$ Input	Active low input increments internal six bit counter by one for each count pulse in.
2	Refresh Enable Input	Active high input which determines whether the 3232 is in refresh mode (H) or address enable (L).
7,3,5,18, 20,22	A_0-A_5 Inputs	Row Address inputs.
8,4,6,17, 19,21	A_6-A_{11} Inputs	Column address inputs.
9,11,10, 16,15,14	$\overline{O}_0$-$\overline{O}_5$ Outputs	Address outputs to memories. Inverted with respect to address inputs.
12	GND	Power supply ground.
13	$\overline{\text{Zero}}$ $\overline{\text{Detect}}$ Output	Active low output which senses that all six bits of refresh address in the counter are zero. Can be used in the burst mode to sense refresh completion.
23	Row Enable Input	High input selects row, low input selects column addresses of the driven memories.
24	V_{CC}	+5V power supply input.

DEVICE OPERATION

The Intel® 3232 Address Multiplexer/Refresh Counter performs the following functions:

1. Row, Column and Refresh Address multiplexing
2. Address counting for burst or distributed refresh.

These functions are controlled by two signals: Refresh Enable and Row Enable, both of which are active high TTL inputs. The truth table on page 1 shows the levels required to multiplex to the output:

1. Refresh addresses (from internal counter)
2. Row addresses (A_0 through A_5)
3. Column addresses (A_6 through A_{11})

Burst Refresh Mode

When refresh is requested, the refresh enable input is high. This input is ANDed with the 6 outputs of the internal 6 bit counter. At each $\overline{\text{Count}}$ pulse the counter increments by one, sequencing the outputs ($\overline{O}_0$-$\overline{O}_5$) through all 64 row addresses. When the counter sequences to all zeros, the $\overline{\text{Zero}}$ $\overline{\text{Detect}}$ output goes low signaling the end of the refresh sequence. Due to counter decoding spikes, the $\overline{\text{Zero}}$ $\overline{\text{Detect}}$ output is valid only after t_{CZ} following the low going edge of $\overline{\text{Count}}$.

Distributed Refresh Mode

In the distributed refresh mode, one row is selected for refresh each ($t_{REFRESH}/n$) time where n = number of rows in the device and $t_{REFRESH}$ is the specified refresh rate for the device. For the 2104A $t_{REFRESH}$ = 2msec and n = 64, therefore one row is refreshed each 31 μsec. Following the refresh cycle at row n_x, the Count input is pulsed, advancing the refresh address by one row so that the next refresh cycle will be performed on row n_{x+1}. The Count input may be pulsed following each refresh cycle or within the refresh cycle after the specified memory device address hold time.

Row and Column Address

All twelve system address lines are applied to the inputs of the 3232. When Refresh Enable is low and Row Enable is high, input addresses A_0-A_5 are gated to the outputs and applied to the driven memories. Conversely, when Row Enable is low (with Refresh Enable still low), input addresses A_6-A_{11} are gated to the outputs and applied to the driven memories.

Figure 1 shows a typical connection between the 3232 and the 2104A 4K dynamic RAM. When the memory devices are driven directly by the 3232, the address applied to the memory devices is the inverse of the address at the 3232 inputs due to the inverted outputs of the 3232. This should be remembered when checking out the memory system.

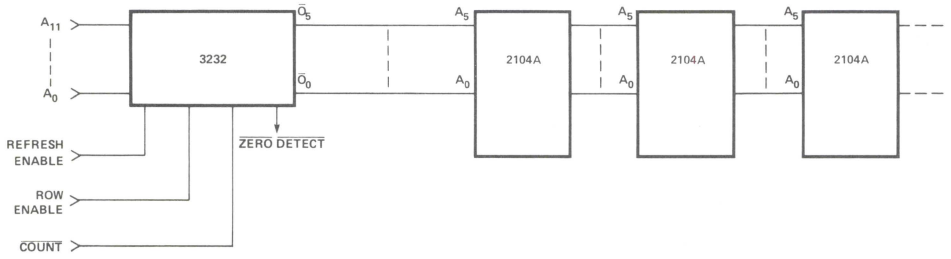


Figure 1. Typical Connection of 3232 and 2104 Memories.

3242
ADDRESS MULTIPLEXER AND REFRESH COUNTER FOR 16K DYNAMIC RAMs

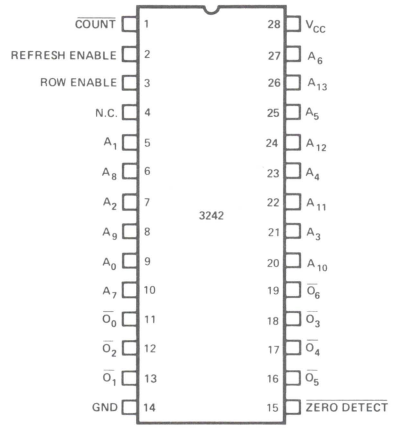
- **Ideal For 2116**
- **Simplifies System Design**
- **Reduces Package Count**
- **Standard 28-Pin DIP**
- **Suitable For Either Distributed Or Burst Refresh**
- **Single Power Supply: +5 Volts ±10%**
- **Address Input to Output Delay: 9ns Driving 15 pF, 25ns Driving 250pF**

The Intel® 3242 is an address multiplexer and refresh counter for multiplexed address dynamic RAMs requiring refresh of 64 or 128 cycles. It multiplexes 14 bits of system supplied address to 7 output address pins. The device also contains a 7 bit refresh counter which is externally controlled so that either distributed or burst refresh may be used. The high performance of the 3242 makes it especially suitable for use with high speed N-channel RAMs like the 2116.

The 3242 operates from a single +5 volt power supply and is specified for operation over a 0 to +75°C ambient temperature range. It is fabricated by means of Intel's highly reliable Schottky bipolar process and is packaged in a hermetically sealed 28 pin Type D package.

MEMORY SUPPORT

PIN CONFIGURATION



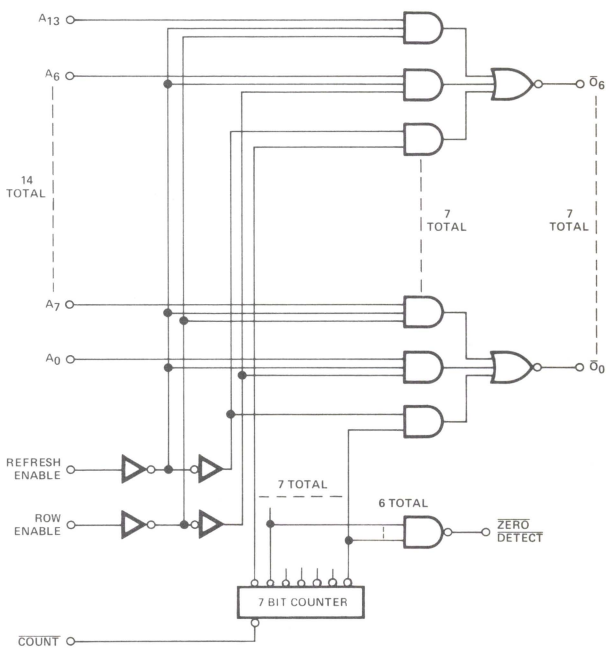
NOTE: A_0 THROUGH A_6 ARE ROW ADDRESSES.
A_7 THROUGH A_{13} ARE COLUMN ADDRESSES.

TRUTH TABLE AND DEFINITIONS:

REFRESH ENABLE	ROW ENABLE	OUTPUT
H	X	REFRESH ADDRESS (FROM INTERNAL COUNTER)
L	H	ROW ADDRESS (A_0 THROUGH A_6)
L	L	COLUMN ADDRESS (A_7 THROUGH A_{13})

$\overline{\text{COUNT}}$ – ADVANCES INTERNAL REFRESH COUNTER.
$\overline{\text{ZERO DETECT}}$ – INDICATES ZERO IN THE FIRST 6 SIGNIFICANT REFRESH COUNTER BITS (USED IN BURST REFRESH MODE)

LOGIC DIAGRAM



A.C. Characteristics

All Limits Apply for V_{CC} = +5.0V ±10%, T_A = 0°C to 75°C, Load = 1 TTL, C_L = 250pF, Unless Otherwise Specified.

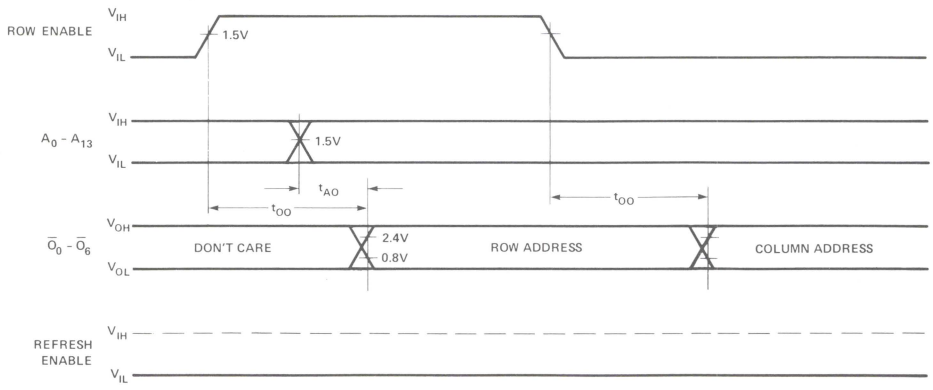
SYMBOL	PARAMETER	MIN.	TYP.(1)	MAX.	UNIT	CONDITIONS
t_{AO}	Address Input to Output Delay		6	9	ns	Refresh Enable = Low(2)(3)
t_{AOI}	Address Input to Output Delay		16	25	ns	Refresh Enable = Low
t_{OO}	Row Enable to Output Delay	7	12	27	ns	Refresh Enable = Low(2)(3)
t_{OOI}	Row Enable to Output Delay	12	28	41	ns	Refresh Enable = Low
t_{EO}	Refresh Enable to Output Delay	7	14	27	ns	Notes 2, 3
t_{EOI}	Refresh Enable to Output Delay	12	30	45	ns	
t_{CO}	$\overline{\text{Count}}$ to Output	15	40	60	ns	Refresh Enable = High(2)(3)
t_{COI}	$\overline{\text{Count}}$ to Output	20	55	80	ns	Refresh Enable = High
f_C	Counting Frequency			5	MHz	
t_{CPW}	$\overline{\text{Count}}$ Pulse Width	35			ns	
t_{CZ}	$\overline{\text{Count}}$ to $\overline{\text{Zero}}$ $\overline{\text{Detect}}$	15		70	ns	Note 3

Notes: 1. Typical values are for T_A = 25°C and V_{CC} = 5.0V.
2. T_A = 25°C, V_{CC} = 5.0V.
3. C_L = 15 pF.

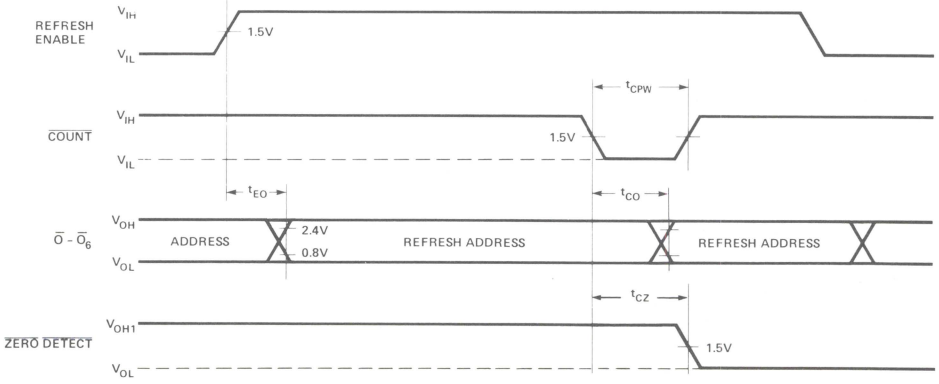
MEMORY SUPPORT

A.C. TIMING WAVEFORMS (Typically used with 2116)

NORMAL CYCLE



REFRESH CYCLE



Absolute Maximum Ratings*

Temperature Under Bias	-10° to +85°C
Storage Temperature	-65° to +150°C
All Input, Output, or Supply Voltages	-0.5V to +7 Volts
Output Currents	100mA
Power Dissipation	1W

*COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

All Limits Apply for V_{CC} = 5.0V ±10%, T_A = 0°C to + 75°C

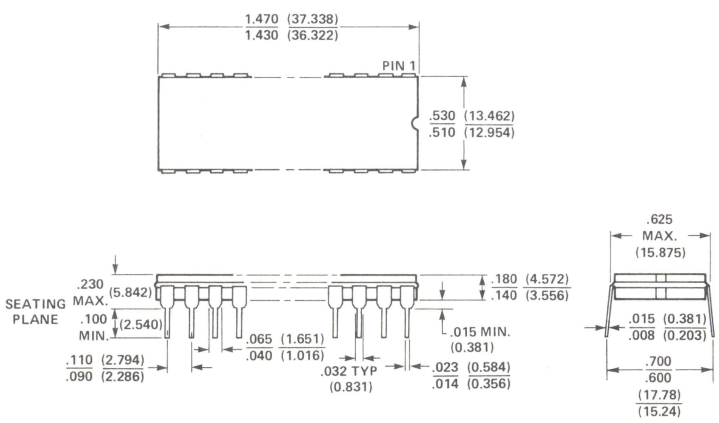
SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP. (1)	MAX.		
I_F	Input Load Current		-0.04	-0.25	mA	V_{IN} = 0.45V, Note 2
I_R	Input Leakage Current		0.01	10	μA	V_{IN} = 5.5V
V_{IH}	Input High Voltage	2.0			V	
V_{IL}	Input Low Voltage			0.8	V	
V_{OL}	Output Low Voltage		0.25	0.40	V	I_{OL} = 8mA
V_{OH}	Output High Voltage ($\overline{O_0}$-$\overline{O_6}$)	3.0	4.0		V	I_{OH} = −1mA
V_{OH1}	Output High Voltage ($\overline{Zero\ Detect}$)	2.4	3.3		V	I_{OH} = −1mA
I_{CC}	Power Supply Current		105	165	mA	V_{CC} = 5.5V

Notes: 1. Typical values are for T_A = 25°C and V_{CC} = 5.0V.

2. Inputs are high impedance, TTL compatible, and suitable for bus operation.

Packaging Information

28 LEAD HERMETIC DUAL IN-LINE PACKAGE
TYPE D



PIN NAMES AND FUNCTIONS

Pin No.	Pin Name	Function
1	$\overline{\text{Count}}$ Input*	Active low input increments internal 7-bit counter by one for each count pulse in.
2	Refresh Enable Input*	Active high input which determines whether the 3242 is in refresh mode (H) or address enable (L).
9,5,7,21, 23,25,27	A_0–A_6 Inputs*	Row address inputs.
10,6,8,20, 22,24,26	A_7–A_{13} Inputs*	Column address inputs.
11,13,12, 18,17,16, 19	$\overline{O}_0$–$\overline{O}_6$ Outputs	Address outputs to memories. Inverted with respect to address inputs.
14	GND	Power supply ground.
15	$\overline{\text{Zero}}$ $\overline{\text{Detect}}$ Output	Active low output which senses that the six low order bits of refresh address in the counter are zero. Can be used in the burst mode to sense refresh completion.
3	Row Enable Input*	High input selects row, low input selects column addresses of the driven memories.
28	V_{CC}	+5V power supply input.

*The inputs are high impedance, TTL compatible, and suitable for bus operation.

DEVICE OPERATION

The Intel® 3242 Address Multiplexer/Refresh Counter performs the following functions:

1. Row, Column and Refresh Address multiplexing.
2. Address Counting for burst or distributed refresh.

These functions are controlled by two signals: Refresh Enable and Row Enable, both of which are active high TTL inputs. The truth table on page 1 shows the levels required to multiplex to the output:

1. Refresh addresses (from internal counter).
2. Row addresses (A_0 through A_6).
3. Column addresses (A_7 through A_{13}).

Burst Refresh Mode

When refresh is requested, the refresh enable input is high. This input is ANDed with the seven outputs of the internal 7-bit counter. At each $\overline{\text{Count}}$ pulse the counter increments by one, sequencing the outputs ($\overline{O}_0$–$\overline{O}_6$) through 128 row addresses. When the first six significant bits of the counter sequence to all zeros, the $\overline{\text{Zero}}$ $\overline{\text{Detect}}$ output goes low, signaling the end of the refresh sequence. Due to counter decoding spikes, the $\overline{\text{Zero}}$ $\overline{\text{Detect}}$ output is valid only after t_{CZ} following the low-going edge of $\overline{\text{Count}}$. The $\overline{\text{Zero}}$ $\overline{\text{Detect}}$ output used in this manner signals the completion of 64 refresh cycles. To use the 128-cycle burst refresh mode, an external flip-flop must be driven by the $\overline{\text{Zero}}$ $\overline{\text{Detect}}$.

Distributed Refresh Mode

In the distributed refresh mode, one row is selected for refresh each ($t_{REFRESH}/n$) time where n = number of refresh cycles required for the device and $t_{REFRESH}$ is the specified refresh rate for the device. For the 2116 $t_{REFRESH}$ = 2 msec and n = 128 or 64, therefore, one row is refreshed each 15.5 or 31 μsec, respectively. Following the refresh cycle at row n_x, the $\overline{\text{Count}}$ input is pulsed, advancing the refresh address by one row so that the next refresh cycle will be performed on row n_{x+1}. The $\overline{\text{Count}}$ input may be pulsed following each refresh cycle or within the refresh cycle after the specified memory device address hold time.

Row and Column Address

All 14 system address lines are applied to the inputs of the 3242. When Refresh Enable is low and Row Enable is high, input addresses A_0–A_6 are gated to the outputs and applied to the driven memories. Conversely, when Row Enable is low (with Refresh Enable still low), input addresses A_7–A_{13} are gated to the outputs and applied to the driven memories.

Figure 1 shows a typical connection between the 3242 and the 2116 16K dynamic RAM. When the memory devices are driven directly by the 3242, the address applied to the memory devices is the inverse of the address at the 3242 inputs due to the inverted outputs of the 3242. This should be remembered when checking out the memory system.

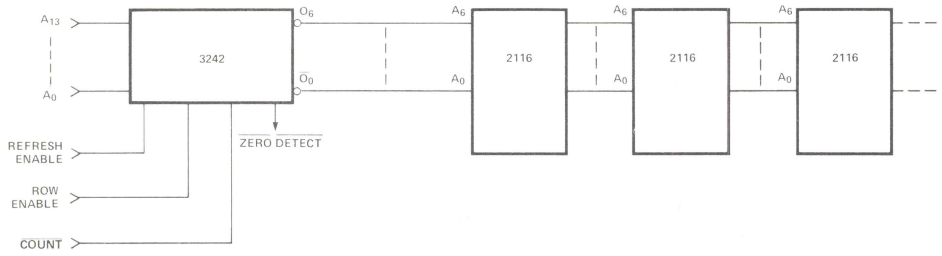


Figure 1. Typical Connection of 3242 and 2116 Memories.

3245
QUAD TTL-TO-MOS DRIVER
FOR 4K N-CHANNEL MOS RAMs

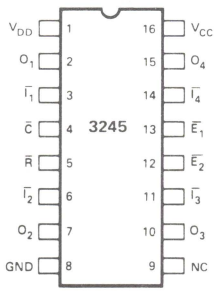
- **Fully Compatible with 4K RAMs Without Requiring Extra Supply or External Devices**
- **High Speed, 32 nsec Max. — Delay + Transition Time**
- **Low Power — 75mW Typical Per Channel**
- **High Density — Four Drivers in One Package**
- **TTL and DTL Compatible Inputs**
- **CerDIP Package — 16 Pin DIP**
- **Only +5 and +12 Volt Supplies Required**

The Intel® 3245 is a Quad Bipolar-to-MOS driver which accepts TTL and DTL input signals. It provides high output current and voltage suitable for driving the clock inputs of N-channel MOS memories such as the 2107B. The circuit operates from two power supplies which are 5 and 12 volts. Input and output clamp diodes minimize line reflections.

The device features two common enable inputs, a refresh select input, and a clock control input for simplified system designs. The internal gating structure of the 3245 eliminates gating delays and minimizes package count.

The 3245 is fabricated by means of Intel's highly reliable Schottky bipolar process and is specified for operation over a 0 to +75°C ambient temperature range.

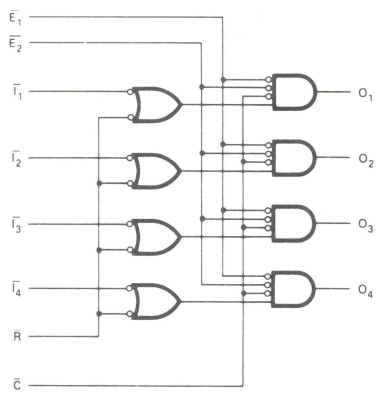
PIN CONFIGURATION



PIN NAMES

$\overline{I_1}$-$\overline{I_4}$	SELECT INPUTS	O_1-O_4	DRIVER OUTPUTS
$\overline{E_1}$, $\overline{E_2}$	ENABLE INPUTS	V_{CC}	+5V POWER SUPPLY
$\overline{R}$	REFRESH SELECT INPUT	V_{DD}	+12V POWER SUPPLY
$\overline{C}$	CLOCK CONTROL INPUT	NC	NOT CONNECTED

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . -10°C to 85°C
Storage Temperature. . . . . -65°C to +150°C
Supply Voltage, V_{CC} . . . . . -0.5 to +7V
Supply Voltage, V_{DD} . . . . . -0.5 to +14V
All Input Voltages . . . . . -1.0 to V_{DD}
Outputs for Clock Driver . . . . . -1.0 to V_{DD} +1V
Power Dissipation at 25°C 2W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to 75°C, V_{CC} = 5.0V ±5%, V_{DD} = 12V ±5%

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
I_{FD}	Input Load Current, $\overline{I}_1, \overline{I}_2, \overline{I}_3, \overline{I}_4$		-0.25	mA	V_F = 0.45V
I_{FE}	Input Load Current, $\overline{R}, \overline{C}, \overline{E}_1, \overline{E}_2$		-1.0	mA	V_F = 0.45V
I_{RD}	Data Input Leakage Current		10	µA	V_R = 5.0V
I_{RE}	Enable Input Leakage Current		40	µA	V_R = 5.0V
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 5mA, V_{IH} = 2V
		-1.0		V	I_{OL} = -5mA
V_{OH}	Output High Voltage	V_{DD}-0.50		V	I_{OH} = -1mA, V_{IL} = 0.8V
			V_{DD}+1.0	V	I_{OH} = 5mA
V_{IL}	Input Low Voltage, All Inputs		0.8	V	
V_{IH}	Input High Voltage, All Inputs	2		V	

POWER SUPPLY CURRENT DRAIN AND POWER DISSIPATION

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions — Input states to ensure the following output states:	Additional Test Conditions
I_{CC}	Current from V_{CC}	23	30	mA	High	
I_{DD}	Current from V_{DD}	19	26	mA		
P_{D1}	Power Dissipation	365	485	mW		
	Power Per Channel	91	121	mW		V_{CC} = 5.25V
I_{CC}	Current from V_{CC}	29	39	mA	Low	V_{DD} = 12.6V
I_{DD}	Current from V_{DD}	12	15	mA		
P_{D2}	Power Dissipation	300	388	mW		
	Power Per Channel	75	97	mW		

A.C. CHARACTERISTICS $T_A = 0°$ to $75°C$, $V_{CC} = 5.0V \pm 5\%$, $V_{DD} = 12V \pm 5\%$

Symbol	Parameter	Min.[1]	Typ.[2,4]	Max.[3]	Unit	Test Conditions
t_{-+}	Input to Output Delay	5	11		ns	$R_{SERIES} = 0$
t_{DR}	Delay Plus Rise Time		20	32	ns	$R_{SERIES} = 0$
t_{+-}	Input to Output Delay	3	7		ns	$R_{SERIES} = 0$
t_{DF}	Delay Plus Fall Time		18	32	ns	$R_{SERIES} = 0$
t_T	Output Transition Time	10	17	25	ns	$R_{SERIES} = 20\Omega$
t_{DR}	Delay Plus Rise Time		27	38	ns	$R_{SERIES} = 20\Omega$
t_{DF}	Delay Plus Fall Time		25	38	ns	$R_{SERIES} = 20\Omega$

NOTES: 1. $C_L = 150pF$
2. $C_L = 200pF$
3. $C_L = 250pF$

These values represent a range of total stray plus clock capacitance for nine 4K RAMs.

4. Typical values are measured at 25°C.

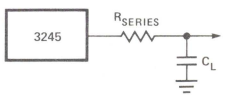
CAPACITANCE * $T_A = 25°C$

Symbol	Test	Typ.	Max.	Unit
C_{IN}	Input Capacitance, $\overline{I}_1, \overline{I}_2, \overline{I}_3, \overline{I}_4$	5	8	pF
C_{IN}	Input Capacitance, $\overline{R}, \overline{C}, \overline{E}_1, \overline{E}_2$	8	12	pF

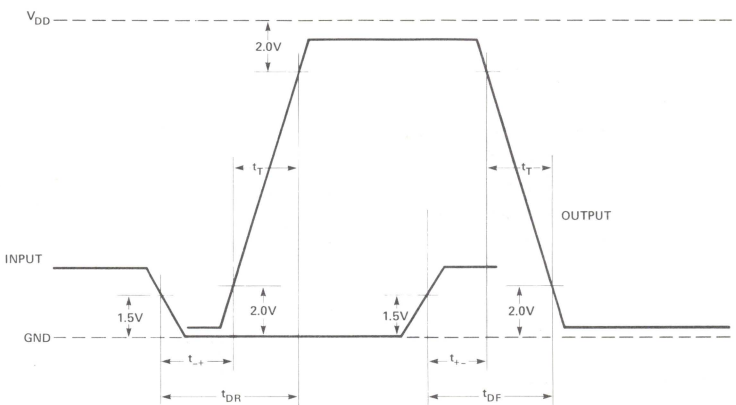
*This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, $V_{bias} = 2V$, $V_{CC} = 0V$, and $T_A = 25°C$.

A.C. CONDITIONS OF TEST

Input Pulse Amplitudes: 3.0V
Input Pulse Rise and Fall Times: 5 ns between 1 volt and 2 volts
Measurement Points: See Waveforms

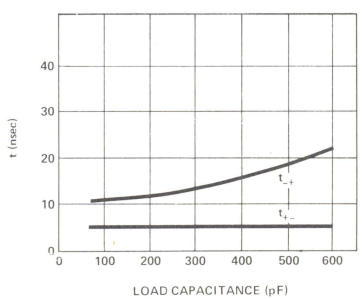


WAVEFORMS

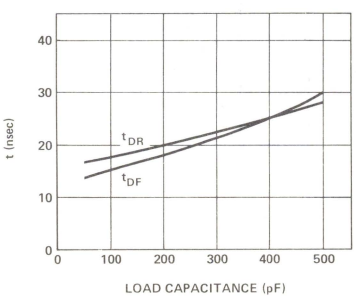


TYPICAL CHARACTERISTICS

INPUT TO OUTPUT DELAY VS. LOAD CAPACITANCE

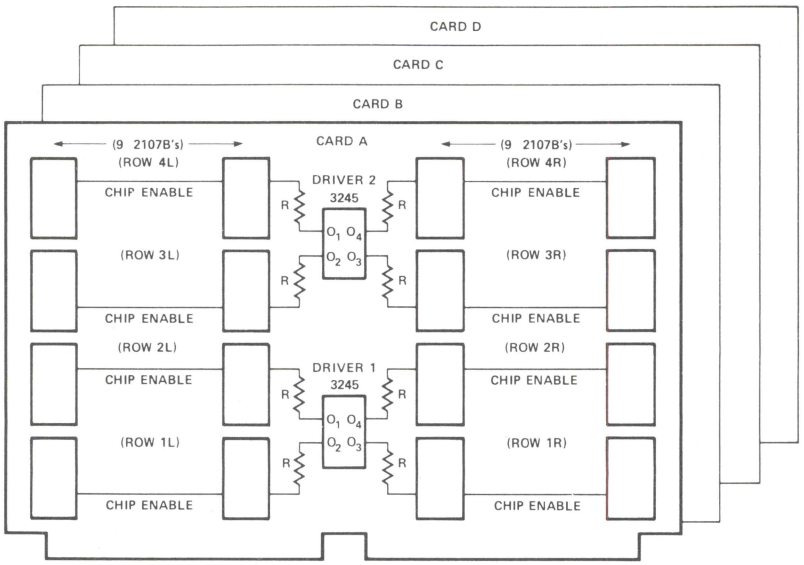


DELAY PLUS TRANSITION TIME VS. LOAD CAPACITANCE



Typical System

Below is an example of a 64K x 18 bit memory system (each card is 16K x 18) employing the 3245 quad high voltage driver for the chip enable inputs. A single 3245 package drives 16K x 9 bits. A_0 through A_{11} are 2107B addresses.



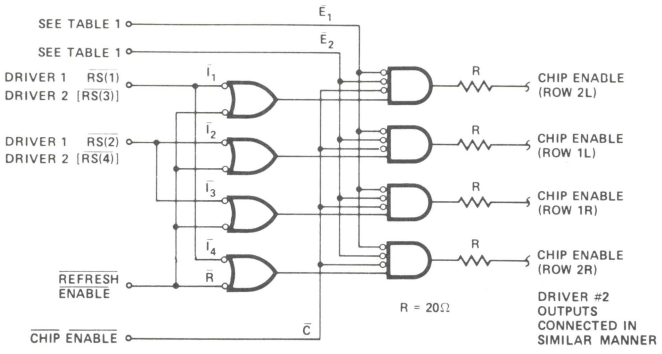
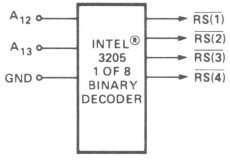
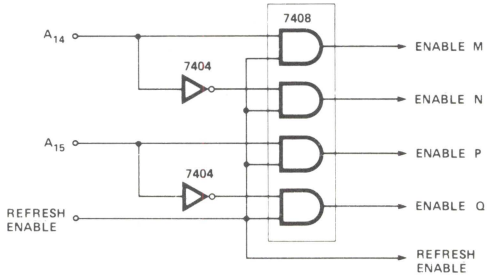


TABLE 1.

CARD	INPUTS $\overline{E_1}$	INPUTS $\overline{E_2}$
A	ENABLE M	ENABLE P
B	ENABLE M	ENABLE Q
C	ENABLE N	ENABLE P
D	ENABLE N	ENABLE Q





5235, 5235-1
QUAD TTL-TO-MOS DRIVER
FOR 4K N-CHANNEL MOS RAMs

- **CMOS Technology for Very Low Power: Suitable for Battery Backup**
- **High Density: Four Drivers in One Package**
- **Internal Gating Structure Minimizes Package Count**
- **TTL and DTL Compatible Inputs**
- **CerDIP Package: 16 Pin DIP**
- **Only One Power Supply Required, +12V (±10%)**

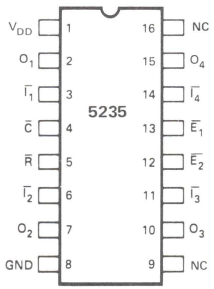
The Intel® 5235 and 5235-1 are Low Power Quad TTL-to-MOS drivers which accept TTL and DTL input levels. They provide high output current and voltage suitable for driving the clock inputs of N-channel MOS memories such as the 2107A or 2107C. The circuit operates from a single 12 volt power supply.

The device features two common enable inputs, a refresh select input, and a clock control input for simplified system design.

The 5235-1 is a selection of the 5235 and is guaranteed for 95ns maximum delay plus transition time while driving a 250pF load.

The Intel ion-implanted, silicon gate Complementary MOS (CMOS) process allows the design and production of very low power drivers.

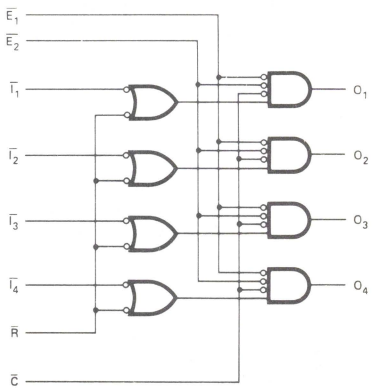
PIN CONFIGURATION



PIN NAMES

$\overline{I_1}$-$\overline{I_4}$	SELECT INPUTS	$\overline{C}$	CLOCK CONTROL INPUT
$\overline{E_1}$, $\overline{E_2}$	ENABLE INPUTS	O_1-O_4	DRIVER OUTPUTS
$\overline{R}$	REFRESH SELECT INPUT	V_{DD}	+12V POWER SUPPLY
		NC	NOT CONNECTED

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . -10°C to 80°C
Storage Temperature . . . . . -65°C to +150°C
Supply Voltage, V_{DD} . . . . . -0.5 to +14V
All Input Voltages . . . . . -0.5 to (V_{DD}+0.5V)
Outputs for Clock Driver . . . . . -0.5 to (V_{DD}+0.5V)
Power Dissipation at 25°C 1W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = 12V ±10%.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
$\|I_{LI}\|$	Input Load Current		0.1	10	µA	V_{IN} = ≤0.4V or ≥2.4V
V_{OL}	Output Low Voltage		0.15	0.4	V	I_{OL} = 5mA
		-1.0	-0.15		V	I_{OL} = -5mA
V_{OH}	Output High Voltage	V_{DD}-0.4	V_{DD}-0.15		V	I_{OH} = -5mA
			V_{DD}+0.15	V_{DD}+0.5	V	I_{OH} = 5mA
V_{IL}	Input Low Voltage, All Inputs			0.8	V	
V_{IH}	Input High Voltage, All Inputs	2.0			V	
I_{DD0}	Supply Current		1.0	2.0	mA	f = 0MHz; V_{DD}=13.2V, V_{IN}≤0.4V or V_{IN}≥2.4V, C_L = 0pf.
I_{DD1}	Supply Current		12	20	mA	f = 1MHz (See Figure 1); V_{DD}=13.2V, V_{IN}≤0.4V or V_{IN}≥2.4V, C_L = 0pf.

Note 1: Typical values are at 25°C and nominal voltage.

TYPICAL CHARACTERISTICS

Figure 1.
POWER SUPPLY CURRENT VS. FREQUENCY
(ALL 4 CHANNELS SWITCHING)

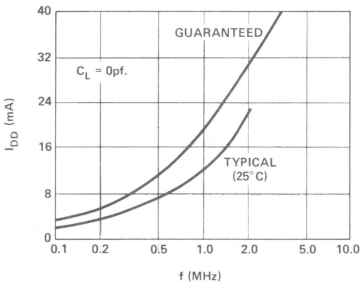


Figure 2.
DELAY PLUS TRANSITION TIME
VS. LOAD CAPACITANCE

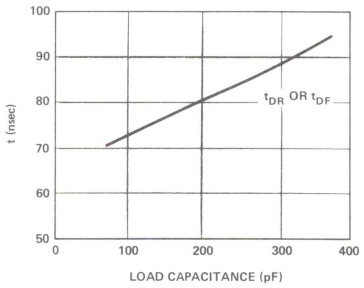


Figure 3.
DELAY PLUS TRANSITION TIME
VS. INPUT VOLTAGE

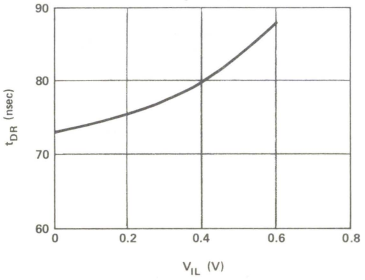
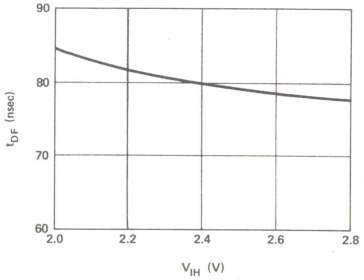


Figure 4.
DELAY PLUS TRANSITION TIME
VS. INPUT VOLTAGE



A.C. CHARACTERISTICS $T_A = 0°$ to $70°C$, $V_{DD} = 12V \pm 10\%$.

Symbol	Parameter	5235-1			5235			Unit
		Min.[1]	Typ.[2,4]	Max.[3]	Min.[1]	Typ.[2,4]	Max.[3]	
t_{-+}	Input to Output Delay	20	55		20	70		ns
t_{DR}	Delay Plus Rise Time		75	95		95	125	ns
t_{+-}	Input to Output Delay	20	55		20	70		ns
t_{DF}	Delay Plus Fall Time		75	95		95	125	ns
t_T	Transition Time	10	20	40	10	25	40	ns

NOTES: 1. $C_L = 150pF$ ┐
2. $C_L = 200pF$ ├ These values represent a range of total stray plus clock capacitance for nine 4K RAMs.
3. $C_L = 250pF$ ┘
4. Typical values are measured at 25°C, and nominal voltage.

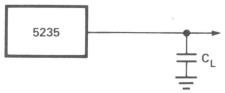
CAPACITANCE* $T_A = 25°C$

Symbol	Test	Typ.	Max.	Unit
C_{IN}	Input Capacitance	8	14	pF

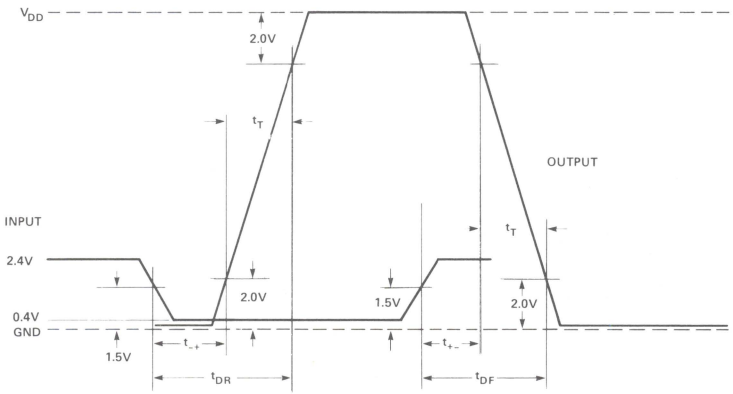
*This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, $V_{bias} = 2V$, $V_{CC} = 0V$, and $T_A = 25°C$.

A.C. CONDITIONS OF TEST

Input Pulse Amplitudes: 2.0V
Input Pulse Rise and Fall Times: 5ns between 0.9 volt and 1.9 volts
Measurement Points: See Waveforms



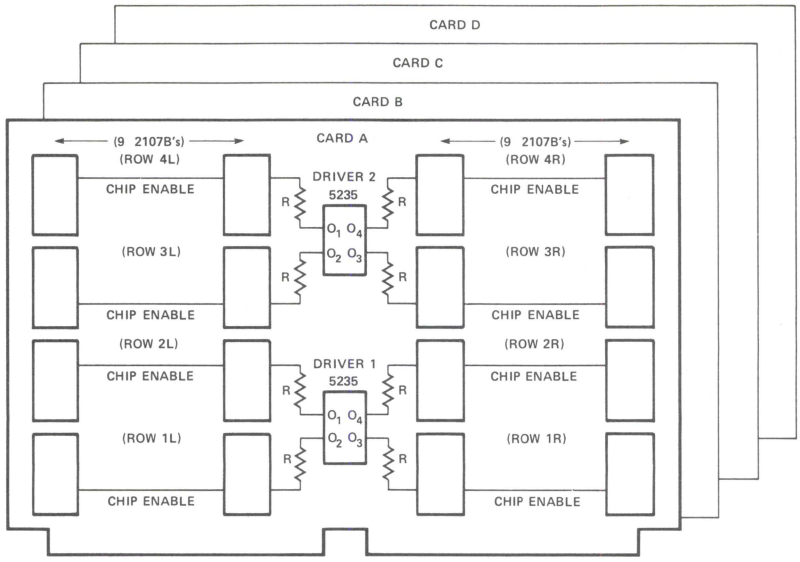
WAVEFORMS



MEMORY SUPPORT

Typical System

Below is an example of a 64K x 18 bit memory system (each card is 16K x 18) employing the 5235 quad high voltage driver for the chip enable inputs. A single 5235 package drives 16K x 9 bits. A_0 through A_{11} are 2107B addresses.



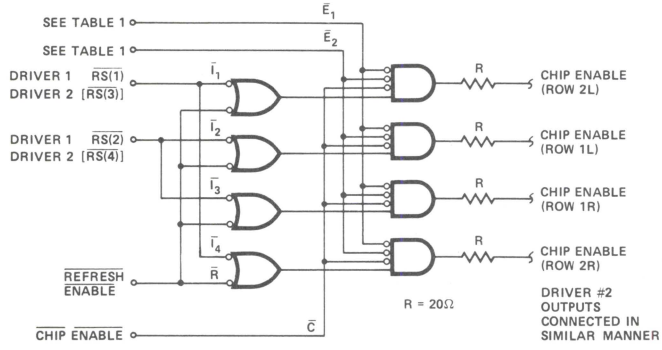


TABLE 1.

CARD	INPUTS $\overline{E}_1$	INPUTS $\overline{E}_2$
A	ENABLE M	ENABLE P
B	ENABLE M	ENABLE Q
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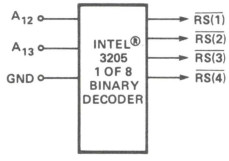
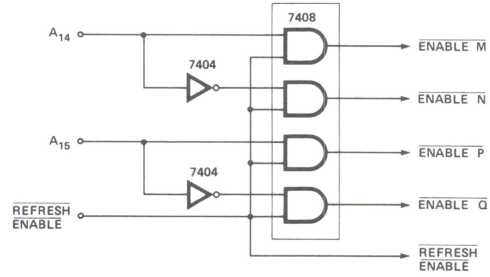
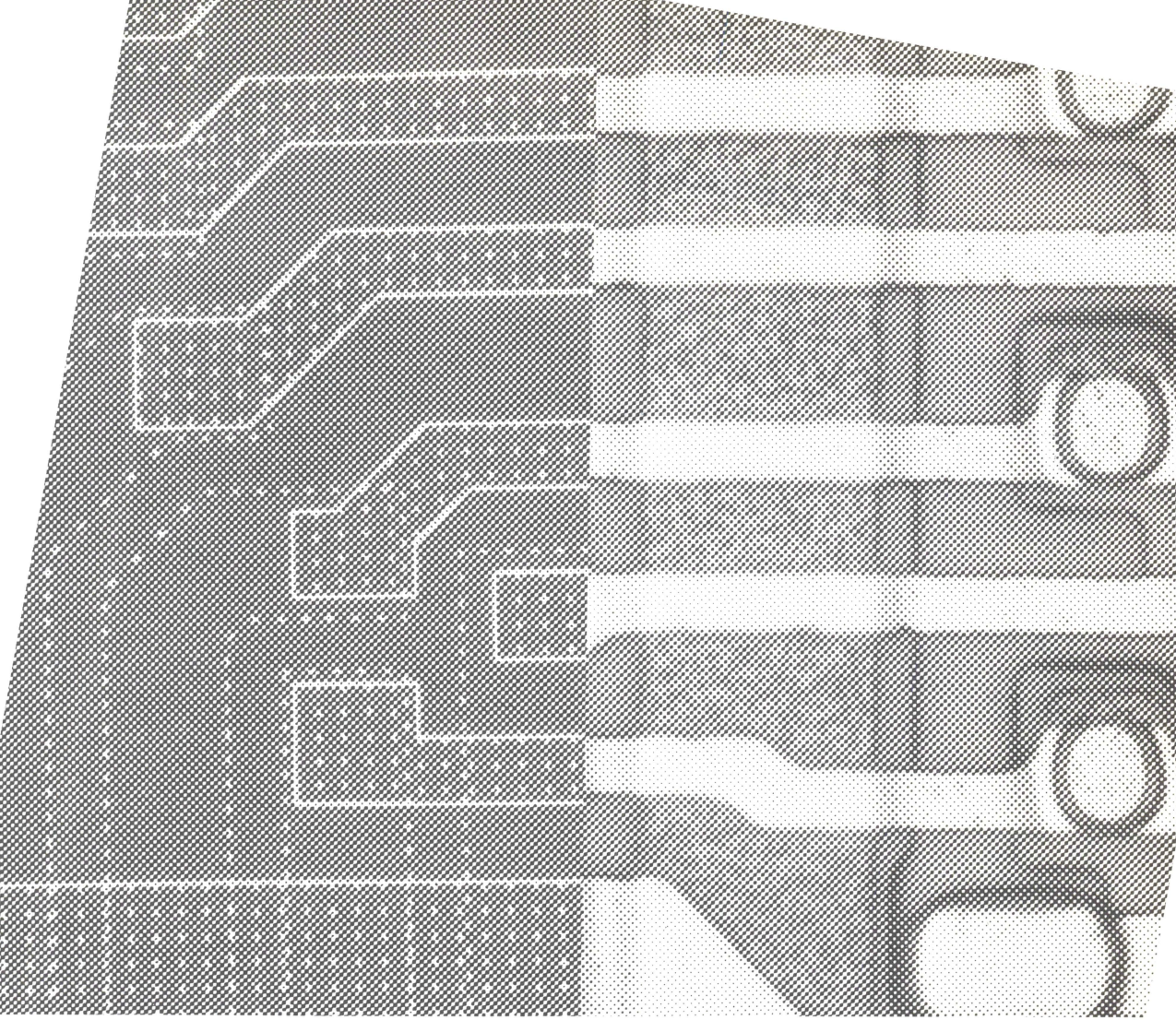
D	ENABLE N	ENABLE Q







7 Telecom

TELECOMMUNICATIONS

INTRODUCTION

The 2910 and 2911 Codecs (Coder-Decoder) are the first members of a family of advanced Telecommunication components. High density LSI fabrication techniques are used allowing sample and hold, digital to analog converter, and comparitors to be integrated on a single chip along with digital logic necessary to interface a full duplex PCM (Pulse Code Modulation) link. The primary applications are in telephone systems for the transmission, switching and concentration of voice communications in PCM systems.

TABLE OF CONTENTS

2910 PCM CODEC – μLAW 7-3
2911 PCM CODEC – A LAW 7-14

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

2910
PCM CODEC-μLAW
8 BIT COMPANDED A/D AND D/A CONVERTER

- **Per Channel, Single Chip Codec**
- **CCITT G711 & G733 Compatible. ATT T1 and T1/C Compatible with 8th Bit Signaling**
- **Microcomputer Interface with On-Chip Time-Slot Computation**
- **78db Dynamic Range, with Resolution Equivalent to 12-Bit Linear Conversion Around Zero**
- **$\pm$5% Power Supplies: +12V, +5V, -5V**
- **On-Chip Voltage Reference**
- **Low Power Consumption 300 mW. Standby Power 120 mW**
- **All Digital Inputs and Outputs TTL Compatible.**
- **Fabricated with Reliable N-Channel MOS Process**

The Intel® 2910 is a fully integrated PCM (Pulse Code Modulation) Codec (Coder-Decoder), fabricated with n-channel silicon gate technology. The high density of integration allows the sample and hold circuits, the digital-to-analog converter, the comparator and the successive approximation register to be integrated on the same chip, along with the logic necessary to interface a full duplex PCM link and provide in-band signaling.

The primary applications are in telephone systems:

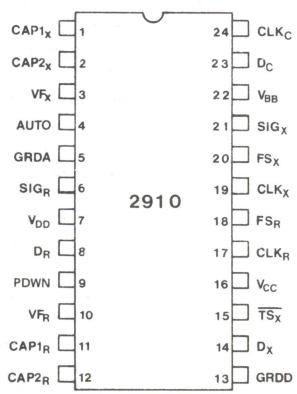
- Transmission — T1 Carrier (T1C compatible)
- Switching — Digital PBX's and Central Office Switching Systems
- Concentration — Subscriber Carrier/Concentrators

The wide dynamic range of the 2910 (78 dB) and the minimal conversion time (30 μsec minimum) make it an ideal product for other applications, like:

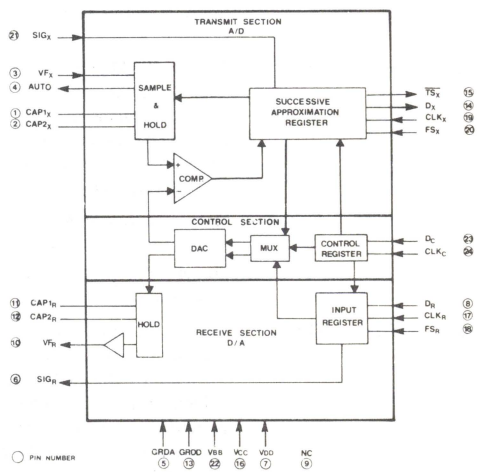
- Data Acquisition
- Telemetry
- Secure Communications Systems
- Signal Processing Systems

TELECOM

PIN CONFIGURATION



BLOCK DIAGRAM



PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

PIN DESCRIPTION

Pin No.	Symbol	Function	Description
1 2	$CAP1_X$ $CAP2_X$	Hold	Connections for the transmit holding capacitor. For an 8 kHz sampling system the capacitor should be 2000 pF, 20%, ceramic or polycarbonate.
3	VF_X	Input	Analog input to be encoded into a PCM word. The signal on this lead is sampled at the same rate as the transmit frame synchronization pulse FS_X, and the sample value is held in the external capacitor connected to the $CAP1_X$ and $CAP2_X$ leads until the encoding process is completed.
4	AUTO	Output	Most significant bit of the encoded PCM word (+5V for positive, –5V for negative value). Used as an internal ground offset correction, by integrating it through the input coupling capacitor. Refer to the Codec interface section.
5	GRDA	Ground	Analog return common to the transmit and receive analog circuits. Not connected to GRDD internally. The external connection to GRDD should have a very low impedance.
6	SIG_R	Output	Signaling output. SIG_R is updated with the 8th bit of the receive PCM word on signaling frames, and is latched between two signaling frames. TTL interface.
7	V_{DD}	Power	+12V, ±5%, referenced to GRDD or GRDA, depending upon system grounding considerations.
8	D_R	Input	Receive PCM highway (serial bus) interface. The Codec serially receives a PCM word (8 bits) through this lead at the proper time defined by FS_R, CLK_R, D_C, and CLK_C.
9	PDWN	Output	Normally low, this signal goes high while the Codec is in the power down mode. TTL interface, open drain output.
10	VF_R	Output	Analog output. The voltage present on VF_R is the decoded value of the PCM word received on lead D_R. This value is held constant between two conversions. For the dynamic range description, refer to the Codec operation section, decoding paragraph.
11 12	$CAP1_R$ $CAP2_R$	Hold	Connections for the receive holding capacitor. For an 8 kHz sampling system, the capacitor should be 600 pF, 20%, ceramic or polycarbonate.
13	GRDD	Ground	Ground return common to the DC power supplies, optionally V_{BB}, V_{CC}, and V_{DD}.
14	D_X	Output	Output of the transmit side onto the send PCM highway (serial bus). The 8-bit PCM word is serially sent out on this pin at the proper time defined by FS_X, CLK_X, D_C, and CLK_C. TTL three-state output.
15	$\overline{TS_X}$	Output	Normally high, this signal goes low while the Codec is transmitting an 8-bit PCM word on the D_X lead. (Time-slot information used for diagnostic purposes and also to gate the data on the D_X lead.) TTL interface, open drain output.
16	V_{CC}	Power	+5V, ±5%, referenced to GRDD.
17	CLK_R	Input	Master receive clock defining the bit rate on the receive PCM highway. Typically 1.544 Mbps for a T1 carrier system. Maximum rate 3.2 Mbps. 50% duty cycle. TTL compatible.
18	FS_R	Input	Frame synchronization pulse for the receive PCM highway. Maximum repetition rate 24 kHz. Also used to differentiate between non-signaling frames and signaling frames for the receive side. For functional description, refer to the Codec operation section, Codec control and signaling paragraph. TTL interface.
19	CLK_X	Input	Master transmit clock defining the bit rate on the transmit PCM highway. Typically 1.544 Mbps for a T1 carrier system. Maximum rate 3.2 Mbps. 50% duty cycle. TTL interface.

PRELIMINARY
Numerical parameters are not guaranteed but may change. Some

Pin No.	Symbol	Function	Description
20	FS_X	Input	Frame synchronization pulse for the transmit PCM highway. Maximum repetition rate 24 kHz. Also used to differentiate between non-signaling frames and signaling frames on the transmit side. For functional description, refer to the Codec operation section, Codec control and signaling paragraphs. TTL interface.
21	SIG_X	Input	Signaling input. This digital input is transmitted as the 8th bit of the PCM word on the D_X lead, on signaling frames. TTL interface.
22	V_{BB}	Power	–5V, ±5%, referenced to GRDD or GRDA, depending upon system grounding considerations.
23	D_C	Input	Data input to program the Codec for the chosen mode of operation. For functional description, see the Codec operation section, Codec control paragraph. TTL interface.
24	CLK_C	Input	Clock input to clock in the data on the D_C lead in order to define the mode of operation of the Codec. Maximum rate 1.6 Mbps. For functional description, refer to the Codec operation section, Codec control paragraph. TTL interface.

FUNCTIONAL DESCRIPTION

The 2910 PCM Codec provides the analog-to-digital and the digital-to-analog conversions necessary to interface a full duplex (4 wires) voice telephone circuit with the PCM highways of a time division multiplexed (TDM) system.

In a typical telephone system the Codec is used between the PCM highways and the line filters.

The Codec provides two major functions:

- Encoding and decoding of analog signals (voice and call progress tones)
- Encoding and decoding of the signaling and supervision information

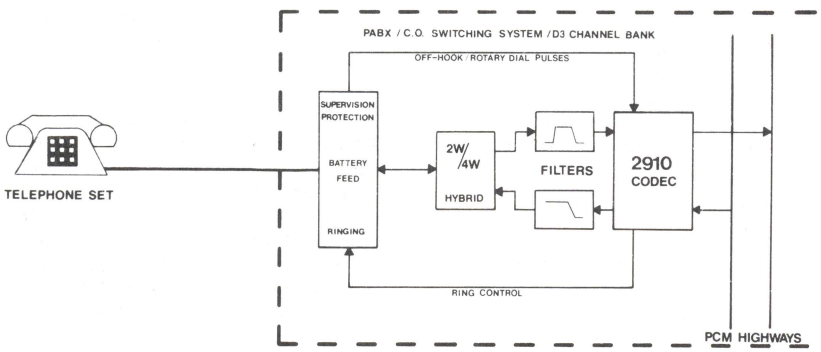
On a non-signaling frame, the Codec encodes the incoming analog signal at the frame rate (FS_X) into an 8-bit PCM word which is sent out on the D_X lead at the proper time. Similarly, on a non-signaling frame of the receive link, the Codec fetches an 8-bit PCM word from the receive highway (D_R lead) and decodes an analog value which will remain constant on lead VF_R until the next receive frame. Transmit and receive frames are independent. They can be asynchronous (transmission) or synchronous (switching) with each other.

On a signaling frame, the Codec transmit side will encode the incoming analog signal as previously described and substitute the signal present on lead SIG_X for the least significant bit of the encoded PCM word. Similarly, on a receive signaling frame, the Codec will decode the 7 most significant bits according to the CCITT G733 recommendation and will output the least significant bit value on the SIG_R lead until the next signaling frame. Signaling frames on the send and receive sides are independent of each other.

The 2910 Codec is intended to be used on line and trunk terminations. The call progress tones (dial tone, busy tone, ring-back tone, re-order tone), and the pre-recorded announcements, can be sent through the voice-path, while signaling (off hook and disconnect supervision, rotary dial pulses, ring control) is sent through the signaling path.

Circuitry is provided within the Codec to internally define the transmit and receive time-slots in order to minimize the common equipment. This feature can be bypassed and discrete time-slots sent to each Codec within a system.

In the power-down mode, most functions of the Codec are disabled to reduce power dissipation to a minimum.



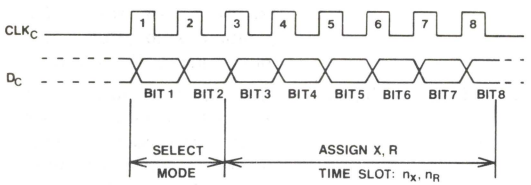
TYPICAL LINE TERMINATION

PRELIMINARY
Notices: This is not a final specification. Some parameter limits are subject to change.

CODEC OPERATION

Codec Control

The operation of the 2910 is defined by serially loading an 8-bit word through the D_C lead (data) and the CLK_C lead (clock). The loading is asynchronous with the other operations of the Codec, and takes place whenever transitions occur on the CLK_C lead. The D_C input is loaded in during the trailing edge of the CLK_C input.



The control word contains two fields:

Bit 1 and bit 2 define whether the subsequent 6 bits apply to both the transmit and receive side (00), the transmit side only (01), the receive side only (10) or whether the Codec should go into the standby, power-down mode (11). In the latter case (11), the following 6 bits are irrelevant.

The last 6 bits of the control word define the time-slot assignment, from 000000 (time-slot 1) to 111111 (time-slot 64).

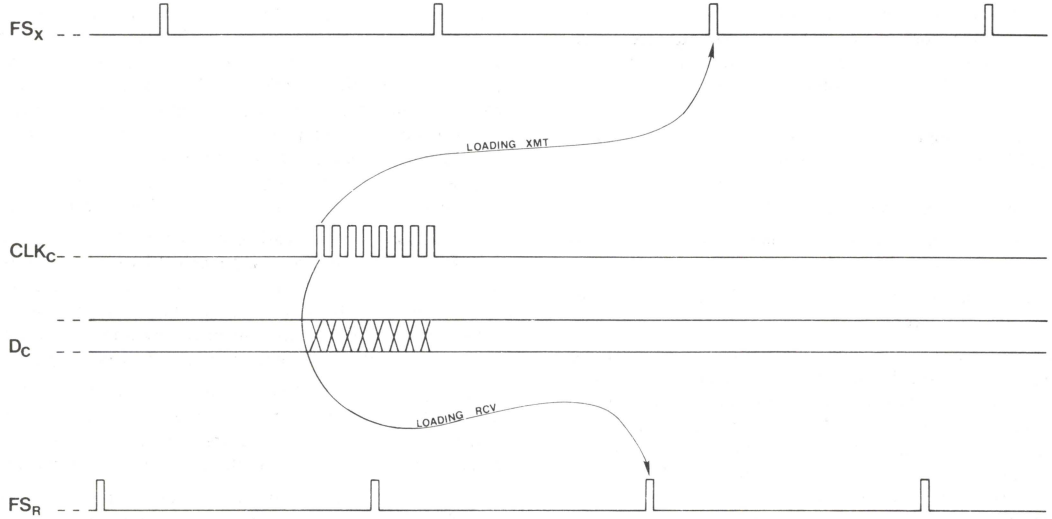
Bit 3 is the most significant bit and bit 8 the least significant and last into the Codec.

Bit 1	Bit 2	Mode
0	0	X & R
0	1	X
1	0	R
1	1	Standby

Bit 3 8	Time Slot
0 0 0 0 0 0	1
0 0 0 0 0 1	2
⋮	⋮
1 1 1 1 1 1	64

The Codec will retain the control word (or words) until a new word is loaded in or until power is lost. This feature allows to dynamically allocate the time-slots for switching applications.

The clocking of a full control word (8 bits) has to take place in less time than the frame duration (elapsed time between two FS_X or FS_R pulses). The Codec will load its transmit and/or receive time-slot control registers with the occurrence of the second FS (X or R) pulse following a transition on the CLK_C lead. The CLK_C should be deactivated during transmission time slots.



Time-Slots

A time-slot is a group of eight adjacent clock pulses (X or R) starting with a leading edge of the corresponding CLK (X or R). Time-slot 1 begins with the next leading CLK (X or R) edge following the leading edge of FS (X or R). The time-slots are adjacent (i.e., there is no gap between two consecutive time-slots).

There are two options to run the system timing:

1. Microcomputer Controlled Mode

   The same FS_X and FS_R pulses are sent to all Codecs in the system. Each Codec is programmed for a different time-slot. Each Codec computes its own time-slot, counting down the CLK (X or R) pulses until there is a match with the last 6 bits of the control word. The counts are reset by the FS (Xor R) pulse. Thus, there is no need for external generation of the time-slot.

2. Direct Control Mode

   Each Codec is programmed for time-slot 1 (code 00000000 for the control word). A different FS_X and FS_R pulse is sent to each Codec, staggered 8 clock pulses apart. Each Codec will consider its time-slot to be made of the 8 clock pulses beginning with the next leading CLK (X or R) edge following the leading edge of the FS (X or R) puise. In the direct mode, there is a need to externally generate a different FS_X and a different FS_R pulse for each Codec. The CLK_C lead is tied to CLK_X and the D_C lead is held low for normal operation, and high for power-down mode.

PRELIMINARY
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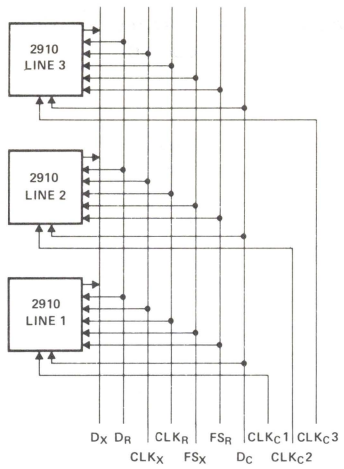
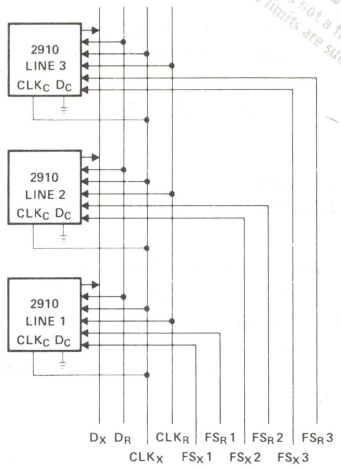
MICROCOMPUTER CONTROL MODE

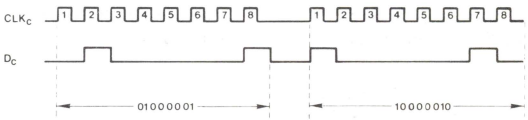


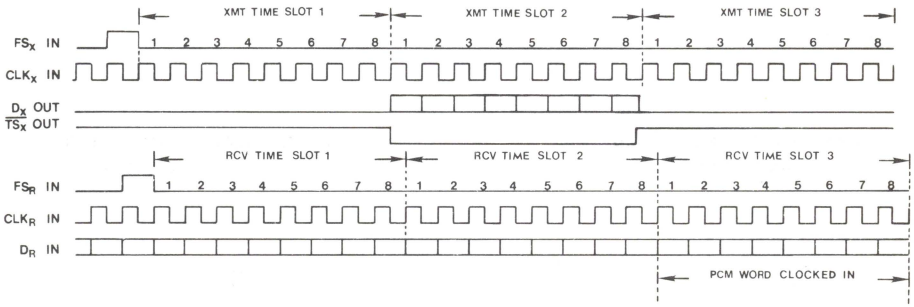
DIRECT MODE



Example

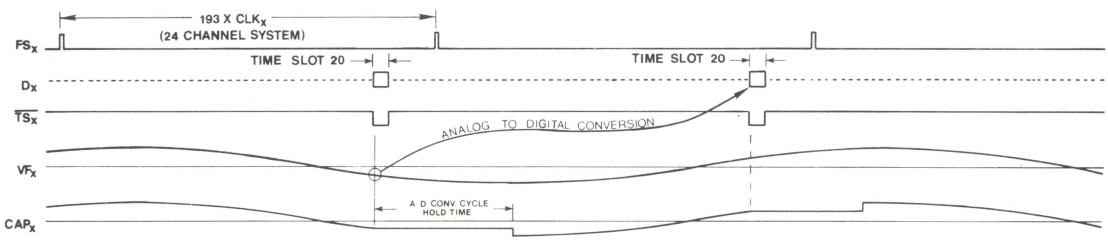
The two words 01000001 and 10000010 have been loaded into the Codec. The transmit side is now programmed for time-slot 2 and the receive side for time-slot 3. The Codec will output a PCM word on the transmit PCM highway (bus) during the time-slot 2 of the transmit frame, and will fetch a PCM word from the receive PCM highway during time-slot 3.





Encoding

The VF signal to be encoded is input on the VF_X lead. An internal switch samples the signal and the hold function is performed by the external capacitor connected to the $CAP1_X$ and $CAP2_X$ leads. The sampling is synchronized with the transmit time-slot and the conversion takes place during the following frame (worst case conversion time is 15 time-slots). The PCM word is then output on the D_X lead at the proper time-slot occurrence of the following frame as described earlier (see Codec control paragraph). The A/D converter saturates at 3.04 volts.



PRELIMINARY
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Conversion Law

The conversion law is commonly referred to as the μ Law or the $\mu = 255$ Law. Its mathematical expression is:

$$Y = \frac{\ln(1+\mu X)}{\ln(1+\mu)}$$

where X and Y are the normalized input and output of the encoder and decoder and $\mu = 255$.

The Codec approximates the μ Law through 15 segments. Each segment is made of 16 steps. In adjacent segments, the step sizes are in a ratio of two to one. Within each segment, the step size is constant with the exception of the first segment where the first step is half the size of the other steps in the segment.

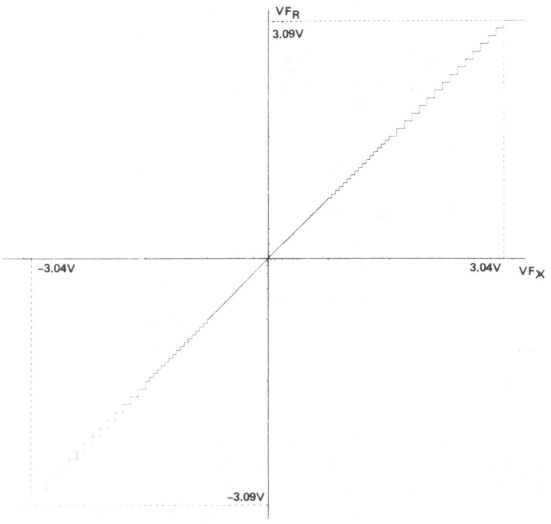
There are two transfer characteristics: the first one for 8-bit coding (non-signaling frame), the second one for 7-bit coding (signaling frame).

For 8-bit coding, the output levels are midway between the corresponding decision levels. The output levels Y_n are related to the input levels X_n by the expression:

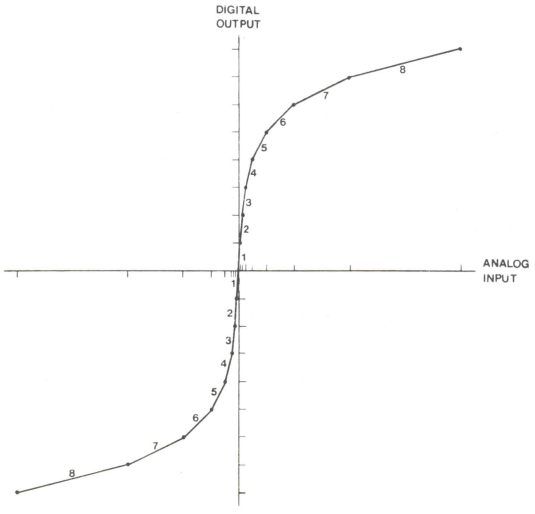
$$Y_n = \frac{X_n + X_{n+1}}{2} \qquad 0 < n \leqslant 127$$

$$Y_o = X_o = 0 \qquad n = 0$$

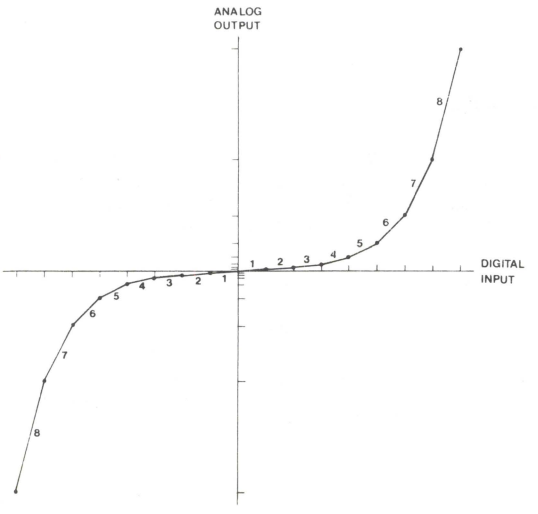
CODEC TRANSFER CHARACTERISTIC (8 BITS CODING)



CODER TRANSFER CHARACTERISTIC (A/D CONVERSION)



DECODER TRANSFER CHARACTERISTIC (D/A CONVERSION)



PRELIMINARY
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μ LAW – POSITIVE INPUT VALUES

(For Negative Input Values, Invert Bit 1)

1	2	3	4	5	6								7	8
Segment No.	No. of Steps × Step Size	Value at Segment End Points	Decision Value No. n	Decision Value X_n (1)	PCM Word Bit Number 1	2	3	4	5	6	7	8	Value at Decoder Output Y_n	Decoder Output Value No.
		8159 (3)	(128)	(8159)										
8	16 × 256		127	7903	1	0	0	0	0	0	0	0	8031	127
			⋮	⋮								(2)	⋮	⋮
			113	4319										
7	16 × 128	4063	112	4063	1	0	0	0	1	1	1	1	4191	112
			⋮	⋮								(2)	⋮	⋮
			97	2143										
6	16 × 64	2015	96	2015	1	0	0	1	1	1	1	1	2079	96
			⋮	⋮								(2)	⋮	⋮
			81	1055										
5	16 × 32	991	80	991	1	0	1	0	1	1	1	1	1023	80
			⋮	⋮								(2)	⋮	⋮
			65	511										
4	16 × 16	479	64	479	1	0	1	1	1	1	1	1	495	64
			⋮	⋮								(2)	⋮	⋮
			49	239										
3	16 × 8	223	48	223	1	1	0	0	1	1	1	1	231	48
			⋮	⋮								(2)	⋮	⋮
			33	103										
2	16 × 4	95	32	95	1	1	0	1	1	1	1	1	99	32
			⋮	⋮								(2)	⋮	⋮
			17	35										
1	15 × 2	31	16	31	1	1	1	0	1	1	1	1	33	16
			⋮	⋮								(2)	⋮	⋮
			2	3										
			1	1	1	1	1	1	1	1	1	0	2	1
	1 × 1		0	0	1	1	1	1	1	1	1	1	0	0

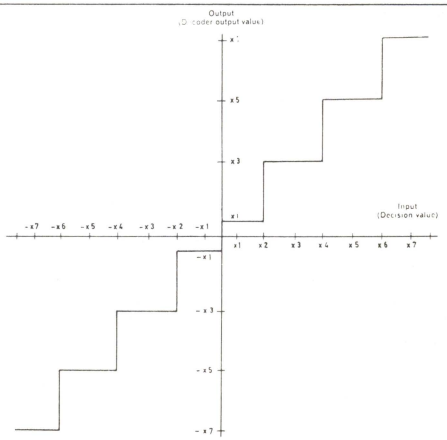
NOTES: (1) 8159 normalized value units correspond to VF_X max = 3.17 dBmO or 3.14 volts.

(2) The PCM word corresponding to positive input values between two successive decision values numbered n and n+1 (see column 4) is (255-n) expressed as a binary number.

(3) X_{128} is a virtual decision value.

For 7-bit coding on signaling frames, the 8th bit is not used for coding but is used to transmit signaling information. The transfer characteristic is shifted upwards by half a step and alternate decoding levels are eliminated owing to the lower resolution of the 7-bit code; except for the level next to zero, the output level is again half way between two decision levels.

$$Y_n = X_{2n-1} \qquad 1 < n < 63$$



PRELIMINARY
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Decoding

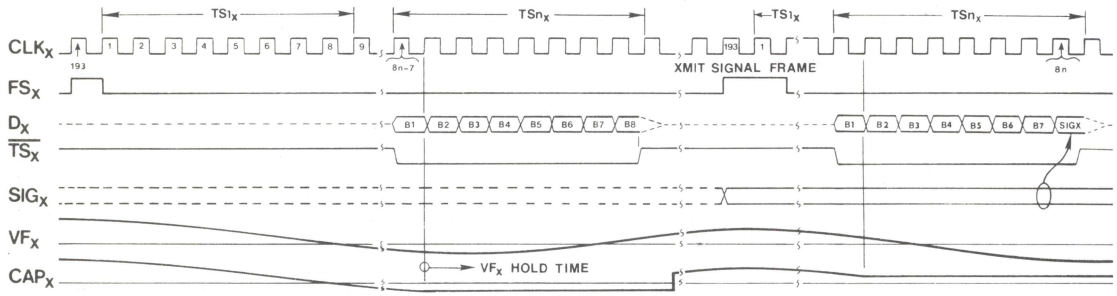
The PCM word fetched from the receive PCM highway is decoded as described in the previous paragraph. The decoded value is held in the external capacitor connected to the $CAP1_R$ and $CAP2_R$ leads. The output signal on lead VF_R has a dynamic range of ±3.09 volts for 8 bits coding, and ±3.04 volts for 7 bits coding; it is held constant between two successive decode operations.

Signaling

The duration of the FS_X and FS_R pulses defines whether a frame is an information frame or a signaling frame:

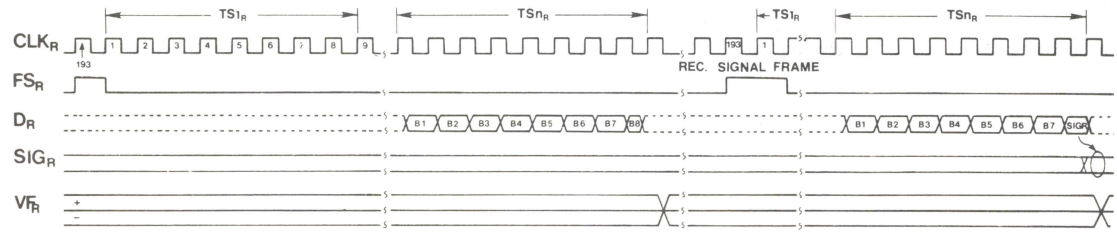
- A pulse with a full clock period (CLK_X for FS_X, CLK_R for FS_R) in duration means a non-signaling frame.
- A pulse having a two full clock (CLK_X for FS_X, CLK_R for FS_R) periods duration means a signaling frame.

When the FS_X pulse is widened, the 8th bit of the PCM word will be replaced by the value on the SIG_X input at the time when the 8th bit is output on the D_X lead.



On the decoding side, when the FS_R pulse is widened, the 8th bit of the PCM word is detected and transmitted on the SIG_R lead. That output is latched until the next receiving signaling frame.

The remaining 7 bits are decoded according to the value given in the conversion law section (CCITT G733 recommendation).



PRELIMINARY
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Standby Mode – Power Down

To minimize power consumption and dissipation in large systems, a standby mode is provided by loading a control word (D_C) with a "1" in bits 1 and 2 locations. Most of the Codec functions thereby become disabled, with the exception of the interface to the D_C and CLK_C leads, to allow the Codec to be reactivated.

The power consumption in the standby mode is less than 120 mW.

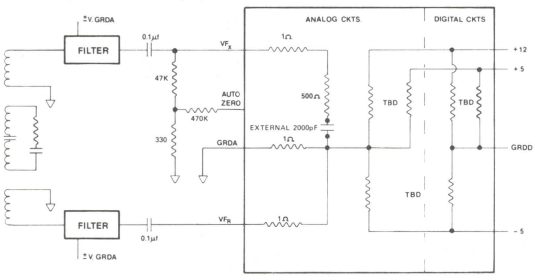
VOLTAGE REFERENCE FOR THE D/A CONVERSION

The voltage reference is generated on-board the chip and is calibrated during the manufacturing process. The dynamic range of the digital-to-analog converter is ±3.09 volts.

APPLICATION – LINE INTERFACE

Grounding

Digital grounding is connected to the GRDD lead. It is the common return for the digital signals.



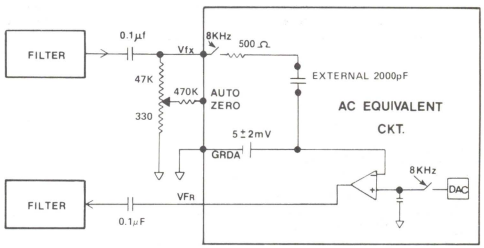
Analog grounding is connected to the GRDA lead. The GRDA and GRDD lead are not connected inside the 2910. An external connection is thus necessary outside the Codec to tie all the analog ground lines to the common return of the system GRDD. That external connection has to have a minimal impedance to avoid a DC offset in the Codec.

Auto Zero

The auto zero output (most significant bit or sign bit of the A/D conversion) integrated over a long time constant will compensate for the DC offset inside the Codec (voltage difference between the bottom of the DAC and GRDA). The above drawing shows a possible connection between the VF_X and Auto leads.

Filters Interface

Attached is the schematic of the equivalent circuits of the input and output of the Codec. Note that the output pulse stream is of the non-return to zero type.



TELECOM

PRELIMINARY
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ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . −40°C to +80°C
Storage Temperature . . . . . −65°C to +150°C
Supply Voltage with Respect to V_{SS} . . . . . −0.5V to +14V
All Input Voltages . . . . . −0.5V to (V_{DD} + 1V)
Outputs . . . . . −1V to (V_{DD} + 1V)
Power Dissipation 1.35W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC AND OPERATING CHARACTERISTICS

T_A = 0°C to +70°C, V_{DD} = +12V, V_{CC} = 5V, V_{BB} = −5V

DIGITAL INTERFACE

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
I_{IL}	Low Level Input Current			10	μA	$V_{IN} < V_{IL}$
I_{IH}	High Level Input Current			10	μA	$V_{IN} > V_{IH}$
V_{IL}	Input Low Voltage			+0.8	V	
V_{IH}	Input High Voltage	+2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 10 mA on D_X, 2.0 mA on SIG_R, 6.4 mA on $\overline{TS_X}$
V_{OH}	Output High Voltage	2.4			V	I_{OH} = 0.6 mA on SIG_R, 30 mA on D_X

ANALOG INTERFACE

A_{IL}	Input Leakage when Sampling			1	μA	−3.1V < V_{IN} < 3.1V
A_{IZ}	Input Impedance when Sampling			500	Ω	In series with CAP_X to GRD
A_{OZ}	Output Impedance	1.8	2.0	2.2	kΩ	User provided VF_R pull-down to V_{BB}
A_{OR}	Dynamic Range	−3.09		+3.09	V	

POWER DISSIPATION

I_{DDO}	Standby Current		TBD		mA	
I_{CCO}	Standby Current		TBD		mA	V_{DD} = +12, +10%
I_{BBO}	Standby Current		TBD		mA	V_{CC} = 5.0, +10%
						V_{BB} = −5.0, −10%
I_{DDI}	Operating Current			14	mA	Clocking Frequency
I_{CCI}	Operating Current			18	mA	X & R = 1.544 Mbps
I_{BBI}	Operating Current			5	mA	

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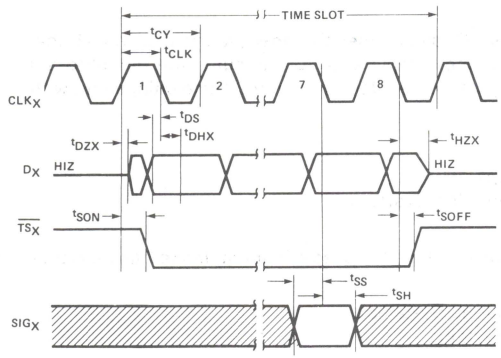
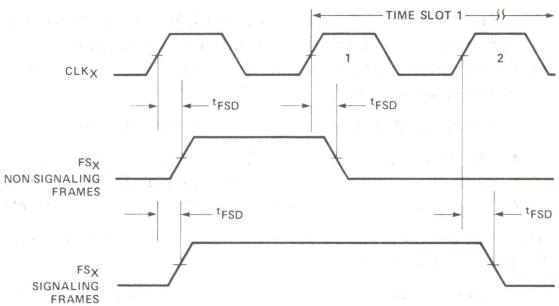
TIMING SPECIFICATION

TRANSMIT SECTION

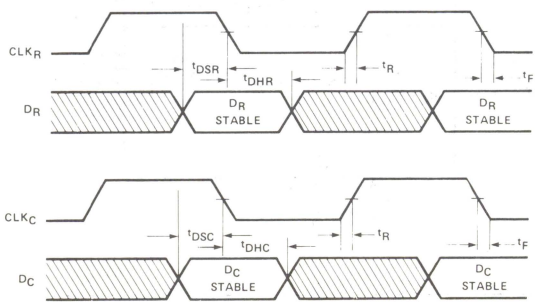
Symbol	Parameter	Min	Max	Unit	Comments
t_{CY}	Clock Period (2.048 MHz Systems)	485		ns	
t_r, t_f	Clock Rise and Fall Time		30	ns	
t_{CLK}	Clock Pulse Width	230		ns	Nominal 50% duty cycle
t_{DS}	New Data Setup	25		ns	Increase by 0.1 ms/pF below 500 pF
t_{DHX}	Data Hold Time	75		ns	
t_{HZX}	Data Float on TS Exit	75	205	ns	
t_{SOFF}	Time Slot X to Disable	70	185	ns	
t_{DZX}	Data Enabled on TS Entry	35		ns	
t_{SON}	Time Slot X to Enable	30	120	ns	
t_{SS}	Signal Setup Time	100		ns	
t_{SH}	Signal Hold Time	100		ns	
t_{FSD}	Frame Sync Delay	10	100	ns	

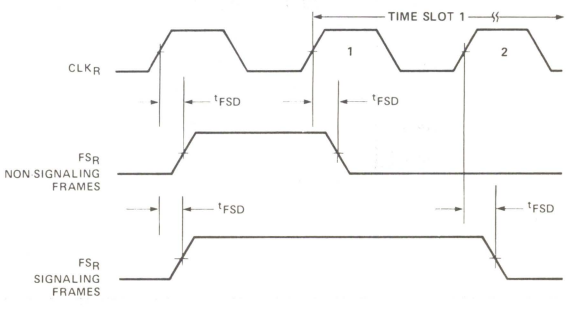




RECEIVE AND CONTROL SECTIONS

Symbol	Parameter	Min	Max	Unit	Comments
t_{VFR}	Analog Output Update		5	Time Slot	From the trailing edge of the channel time slot
t_{SIG_R}	SIG_R Update		300	ns	From the trailing edge of the channel time slot
t_{DSR}	Receive Data Setup	20		ns	
t_{DHR}	Receive Data Hold	50		ns	
t_{DSC}	Control Data Setup	50		ns	
t_{DHC}	Control Data Hold	50		ns	
t_{FSD}	Frame Sync Delay		100	ns	





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PRELIMINARY
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2911
PCM CODEC — A LAW
8-BIT COMPANDED A/D AND D/A CONVERTER

- **Per Channel, Single Chip Codec**
- **CCITT G711 and G732 Compatible. Even Order Bits Inversion Included**
- **Microcomputer Interface with On-Chip Time-Slot Computation**
- **66dB Dynamic Range, with Resolution Equivalent to 11-Bit Linear Conversion Around Zero**
- **±5% Power Supplies: +12V, +5V, -5V**
- **On-Chip Voltage Reference**
- **Low Power Consumption: 250 mW. Standby Power: 90 mW**
- **All Digital Inputs and Outputs TTL Compatible**
- **Fabricated with Reliable N-Channel MOS Process**

The Intel® 2911 is a fully integrated PCM (Pulse Code Modulation) Codec (Coder-Decoder), fabricated with N-channel silicon gate technology. The high density of integration allows the sample and hold circuits, the digital-to-analog converter, the comparator and the successive approximation register to be integrated on the same chip, along with the logic necessary to interface a full duplex PCM link.

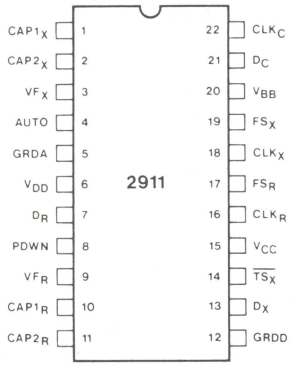
The primary applications are in telephone systems:

- Transmission — 30/32 Channel Systems at 2.048 Mbps
- Switching — Digital PBX's and Central Office Switching Systems
- Concentration — Subscriber Carrier/Concentrators

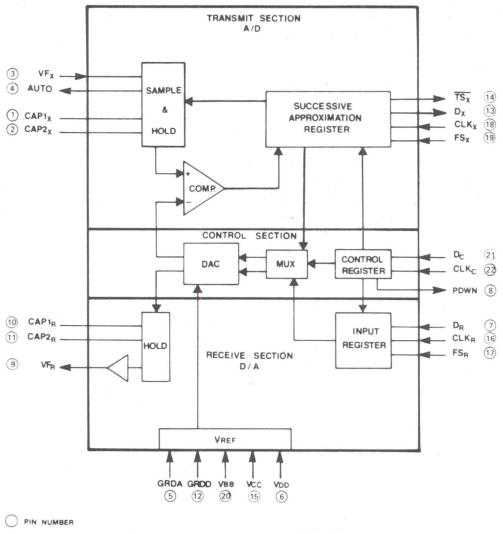
The wide dynamic range of the 2911 (66 dB) and the minimal conversion time (40 μsec minimum) make it an ideal product for other applications, like:

- Data Acquisition
- Telemetry
- Secure Communications Systems
- Signal Processing Systems

PIN CONFIGURATION



BLOCK DIAGRAM



PRELIMINARY

PIN DESCRIPTION

Pin No.	Symbol	Function	Description
1 2	$CAP1_X$ $CAP2_X$	Hold	Connections for the transmit holding capacitor. For an 8 kHz sampling system the capacitor should be 2000 pF, 20%.
3	VF_X	Input	Analog input to be encoded into a PCM word. The signal on this lead is sampled at the same rate as the transmit frame synchronization pulse FS_X, and the sample value is held in the external capacitor connected to the $CAP1_X$ and $CAP2_X$ leads until the encoding process is completed.
4	AUTO	Output	Most significant bit of the encoded PCM word (+5V for positive, -5V for negative value). Used as an internal ground offset correction, by integrating it through the input coupling capacitor. Refer to the Codec interface section.
5	GRDA	Ground	Analog return common to the transmit and receive analog circuits. Not connected to GRDD internally. The external connection to GRDD should have a very low impedance.
6	V_{DD}	Power	+12V, ±5%, referenced to GRDD or GRDA, depending upon system grounding considerations.
7	D_R	Input	Receive PCM highway (serial bus) interface. The Codec serially receives a PCM word (8-bits) through this lead at the proper time defined by FS_R, CLK_R, D_C, and CLK_C.
8	PDWN	Output	Normally low, this signal goes high while the Codec is in the power down mode. TTL interface, open drain output.
9	VF_R	Output	Analog output. The voltage present on VF_R is the decoded value of the PCM word received on lead D_R. This value is held constant between two conversions. For the dynamic range description, refer to the Codec operation section, decoding paragraph.
10 11	$CAP1_R$ $CAP2_R$	Hold	Connections for the receive holding capacitor. For an 8 kHz sampling system, the capacitor should be 400 pF, 20%.
12	GRDD	Ground	Ground return common to the DC power supplies, optionally V_{BB}, V_{CC}, and V_{DD}.
13	D_X	Output	Output of the transmit side onto the send PCM highway (serial bus). The 8-bit PCM word is serially sent out on this pin at the proper time defined by FS_X, CLK_X, D_C, and CLK_C. TTL three-state output.
14	$\overline{TS_X}$	Output	Normally high, this signal goes low while the Codec is transmitting an 8-bit PCM word on the D_X lead. (Time-slot information used for diagnostic purposes and also to gate the data on the D_X lead.) TTL interface, open drain output.
15	V_{CC}	Power	+5V, ±5%, referenced to GRDD.
16	CLK_R	Input	Master receive clock defining the bit rate on the receive PCM highway. Typically 2.048 Mbps for a carrier system. Maximum rate 2.1 Mbps. 50% duty cycle. TTL compatible.
17	FS_R	Input	Frame synchronization pulse for the receive PCM highway. Maximum repetition rate 16 kHz. For functional description, refer to the Codec operation section, Codec control paragraph. TTL interface.
18	CLK_X	Input	Master transmit clock defining the bit rate on the transmit PCM highway. Typically 2.048 Mbps for a carrier system. Maximum rate 2.1 Mbps. 50% duty cycle. TTL interface.
19	FS_X	Input	Frame synchronization pulse for the transmit PCM highway. Maximum repetition rate 16 kHz. For functional description, refer to the Codec operation section, Codec control paragraph. TTL interface.

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

Pin No.	Symbol	Function	Description
20	V_{BB}	Power	-5V, ±5%, referenced to GRDD or GRDA, depend-upon system grounding considerations.
21	D_C	Input	Data input to program the Codec for the chosen mode of operation. For functional description, see the Codec operation section, Codec control paragraph. TTL interface.
22	CLK_C	Input	Clock input to clock in the data on the D_C lead in order to define the mode of operation of the Codec. Maximum rate 2.1 Mbps. For functional description, refer to the Codec operation section, Codec control paragraph. TTL interface.

FUNCTIONAL DESCRIPTION

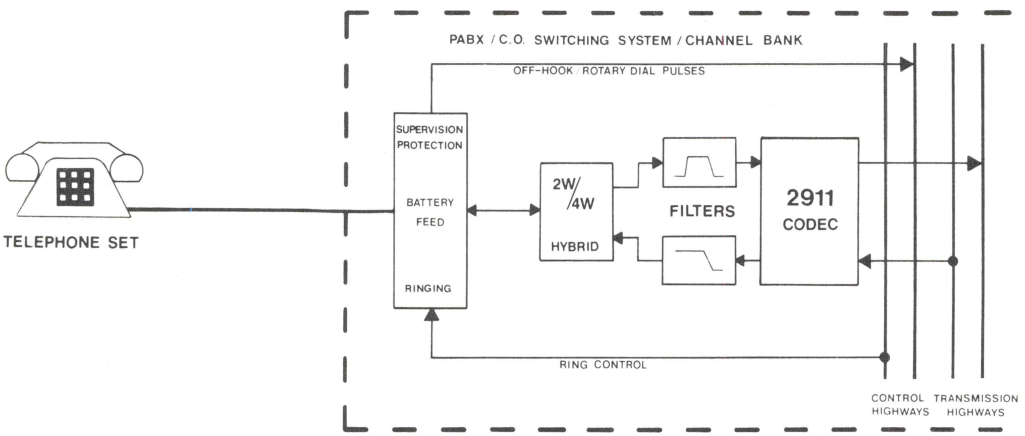
The 2911 PCM Codec provides the analog-to-digital and the digital-to-analog conversions necessary to interface a full duplex (4 wires) voice telephone circuit with the PCM highways of a time division multiplexed (TDM) system. The Codec is intended to be used on line and trunk terminations.

In a typical telephone system the Codec is located between the PCM highways and the channel filters.

The Codec encodes the incoming analog signal at the frame rate (FS_X) into an 8-bit PCM word which is sent out on the D_X lead at the proper time. Similarly, on the receive link, the Codec fetches an 8-bit PCM word from the receive highway (D_R lead) and decodes an analog value which will remain constant on lead VF_R until the next receive frame. Transmit and receive frames are independent. They can be asynchronous (transmission) or synchronous (switching) with each other.

Circuitry is provided within the Codec to internally define the transmit and receive time-slots in order to minimize the common equipment. This feature can be bypassed and discrete time-slots sent to each Codec within a system.

In the power-down mode, most functions of the Codec are disabled to reduce power dissipation to a minimum.



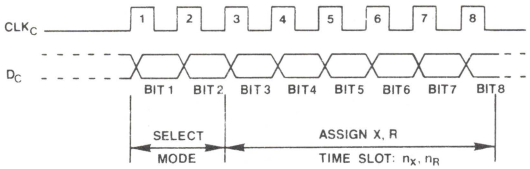
TYPICAL LINE TERMINATION

PRELIMINARY
Notice: This is not a final specification. Some parameter limits are subject to change.

CODEC OPERATION

Codec Control

The operation of the 2911 is defined by serially loading an 8-bit word through the D_C lead (data) and the CLK_C lead (clock). The loading is asynchronous with the other operations of the Codec, and takes place whenever transitions occur on the CLK_C lead. The D_C input is loaded in during the trailing edge of the CLK_C input.



The control word contains two fields:

Bit 1 and bit 2 define whether the subsequent 6 bits apply to both the transmit and receive side (00), the transmit side only (01), the receive side only (10) or whether the Codec should go into the standby, power-down mode (11).

When coming out of the power down mode, double programming is required with the two 8-bit bursts separated by at least two frames.

The last 6 bits of the control word define the time-slot assignment, from 000000 (time-slot 1) to 111111 time-slot 64).

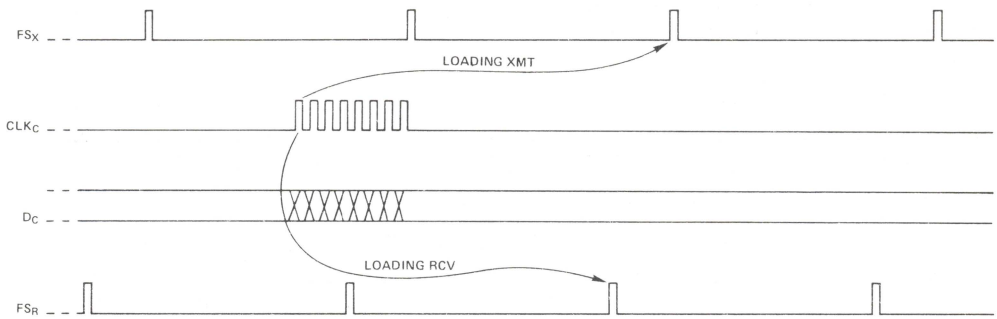
Bit 3 is the most significant bit and bit 8 the least significant and last into the Codec.

Bit 1	Bit 2	Mode
0	0	X & R
0	1	X
1	0	R
1	1	Standby

Bit 3 8	Time Slot
0 0 0 0 0 0	1
0 0 0 0 0 1	2
.	.
.	.
.	.
1 1 1 1 1 1	64

The Codec will retain the control word (or words) until a new word is loaded in or until power is lost. This feature allows dynamic allocation of the time-slots for switching applications.

The clocking of a full control word (8 bits) has to take place in less time than the frame duration (elapsed time between two FS_X or FS_R pulses). The Codec will load its transmit and/or receive time-slot control registers upon the occurrence of the second FS (X or R) pulse following a transition on the CLK_C lead. The CLK_C should be deactivated during transmission time slots.



Time-Slots

A time-slot is a group of eight adjacent clock pulses (X or R) starting with a leading edge of the corresponding CLK (X or R). Time-slot 1 begins with the next leading CLK (X or R) edge following the leading edge of FS (X or R). The time-slots are adjacent (i.e., there is no gap between two consecutive time-slots).

There are two options to run the system timing:

1. Microcomputer Controlled Mode

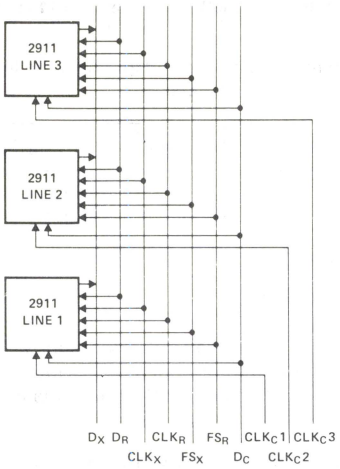
The same FS_X pulse is sent to all Codecs in the system. Similarily, each Codec receives the same FS_R pulse. Each Codec is programmed for a different time-slot. Each Codec computes its own time-slot, counting down the CLK (X or R) pulses until there is a match with the last 6 bits of the control word. The counts are reset by the FS (X or R) pulse. Thus, there is no need for external generation of the individual time-slot pulses.

2. Direct Control Mode

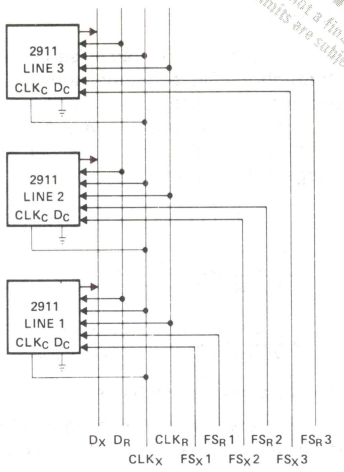
Each Codec is programmed for time-slot 1 (code 00000000 for the control word). A different FS_X and FS_R pulse is sent to each Codec, staggered 8 clock pulses apart from Codec to Codec. Each Codec will consider its time-slot to be made of the 8 clock pulses beginning with the next leading CLK (X or R) edge following the leading edge of the FS (X or R) pulses. In the direct mode, there is a need to externally generate a different FS_X and a different FS_R pulse for each Codec.

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MICROCOMPUTER CONTROL MODE

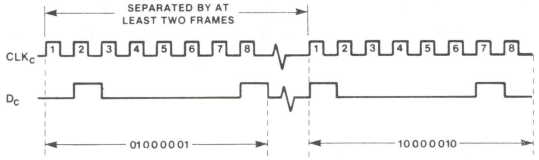


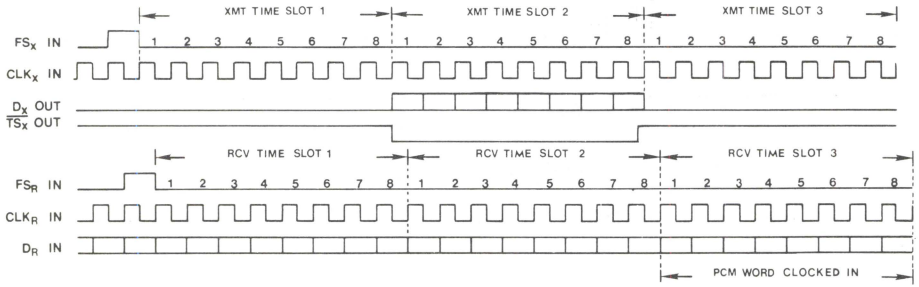
DIRECT MODE



Example:

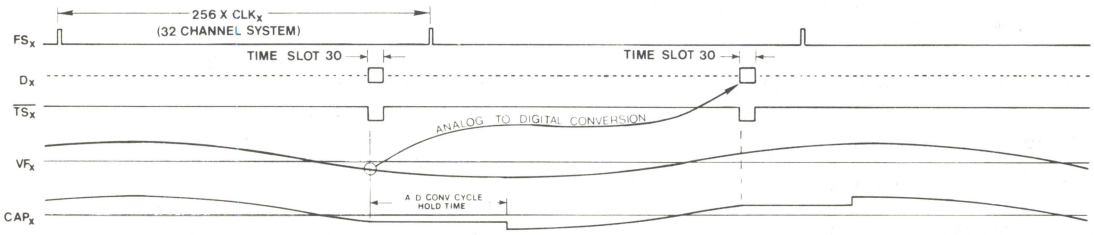
The two words 01000001 and 10000010 have been loaded into the Codec. The transmit side is now programmed for time-slot 2 and the receive side for time-slot 3. The Codec will output a PCM word on the transmit PCM highway (bus) during the time-slot 2 of the transmit frame, and will fetch a PCM word from the receive PCM highway during time-slot 3.





Encoding

The VF signal to be encoded is input on the VF_X lead. An internal switch samples the signal and the hold function is performed by the external capacitor connected to the $CAP1_X$ and $CAP2_X$ leads. The sampling is synchronized with the transmit time-slot and the conversion takes place during the following frame (worst case conversion time is 16 time-slots). The PCM word is then output on the D_X lead at the proper time-slot occurrence of the following frame as described earlier (see Codec control paragraph). The A/D converter saturates at 3.05 volts.



PRELIMINARY
Notice: This is not a final specification. Some parameter limits are subject to change.

Conversion Law

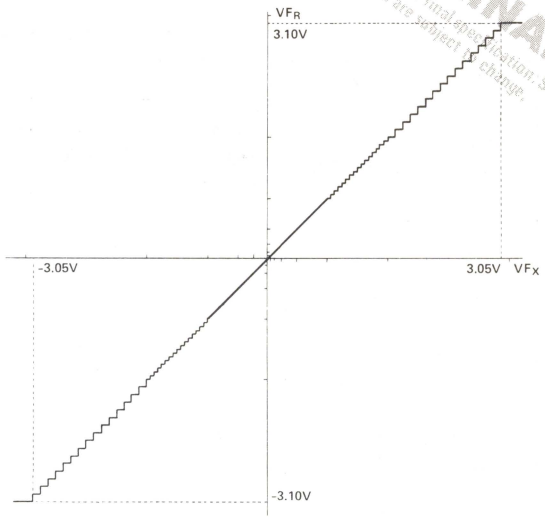
The conversion law is commonly referred to as the A Law.

The Codec provides a piecewise linear approximation of the logrithmic law through 13 segments. Each segment is made of 16 steps with the exception of the first segment which has 32 steps. In adjacent segments the step sizes are in a ratio of two to one. Within each segment, the step size is constant.

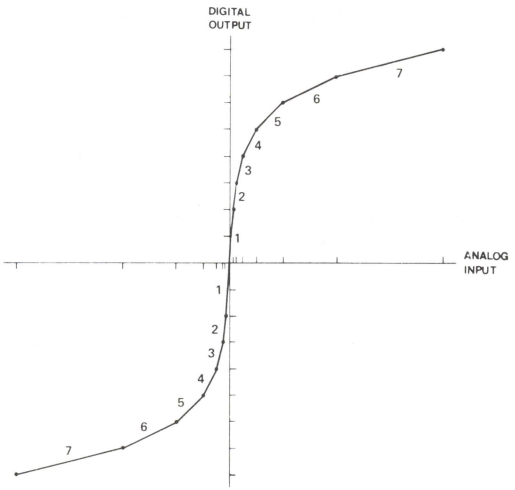
The output levels are midway between the corresponding decision levels. The output levels Y_n are related to the input levels X_n by the expression:

$$Y_n = \frac{X_{n-1} + X_n}{2} \qquad 0 < n \leq 128$$

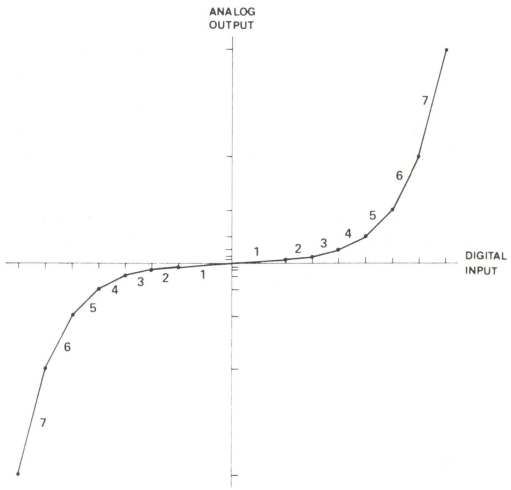
CODEC TRANSFER CHARACTERISTIC



CODER TRANSFER CHARACTERISTIC
(A/D CONVERSION)



DECODER TRANSFER CHARACTERISTIC
(D/A CONVERSION)



TELECOM

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

A LAW – POSITIVE INPUT VALUES

(For Negative Input Values, Invert Bit 1)

1	2	3	4	5	6								7	8
Segment No.	No. of Steps x Step Size	Value at Segment End Points	Decision Value No. n	Decision Value X_n (1)	PCM Word(4) Bit Number 1	2	3	4	5	6	7	8	Normalized Value at Decoder Output Y_n (5)	Decoder Output Value No.
		4096(3)	(128)	(4096)	1	1	1	1	1	1	1	1	4032	128
7	16 x 128		127 ⋮ 113	3968 ⋮ 2176							(2)		⋮	⋮
		2048	112	2048	1	1	1	1	0	0	0	0	2112	113
6	16 x 64		⋮ 97	⋮ 1088							(2)		⋮	⋮
		1024	96	1024	1	1	1	0	0	0	0	0	1056	97
5	16 x 32		⋮ 81	⋮ 544							(2)		⋮	⋮
		512	80	512	1	1	0	1	0	0	0	0	528	81
4	16 x 16		⋮ 65	⋮ 272							(2)		⋮	⋮
		256	64	256	1	1	0	0	0	0	0	0	264	65
3	16 x 8		⋮ 49	⋮ 136							(2)		⋮	⋮
		128	48	128	1	0	1	1	0	0	0	0	132	49
2	16 x 4		⋮ 33	⋮ 68							(2)		⋮	⋮
		64	32	64	1	0	1	0	0	0	0	0	66	33
1	32 x 2		⋮ 1	⋮ 2							(2)		⋮	⋮
			0	0	1	0	0	0	0	0	0	0	1	1

NOTES:

(1) 4096 normalized value units correspond to VF_X max = 3.14 dBmO or 3.15 volts.

(2) The PCM word corresponding to positive input values between two successive decision values numbered n and n+1 (see column 4) is (128+n) expressed as a binary number.

(3) X_{128} is a virtual decision value.

(4) The PCM word on the highways is the same as the one shown in column 6, with the even order bits inverted. The 2911 provides for the inversion of the even order bits on both the send and receive sections. The sign bit is inverted on the encoder side only.

(5) The voltage output on the VF_R lead is equal to the normalized value given in the table, augmented by an offset. The offset value is approximately 15mV.

Decoding

The PCM word fetched from the receive PCM highway is decoded as described in the previous paragraph. The decoded value is held in the external capacitor connected to the $CAP1_R$ and $CAP2_R$ leads. The output signal on lead VF_R has a dynamic range of ±3.10 volts; it is held constant between two successive decode operations. The VF_R output is updated within the fifth time-slot following the receive time-slot in which the channel is operating.

PRELIMINARY
Notice: This is not a final specification. Some parameter limits are subject to change.

Standby Mode — Power Down

To minimize power consumption and dissipation in large systems, a standby mode is provided by loading a control word (D_C) with a "1" in bits 1 and 2 locations. Most of the Codec functions thereby become disabled, with the exception of the interface to the D_C and CLK_C leads, to allow the Codec to be reactivated.

The power consumption in the standby mode is less than 90 mW.

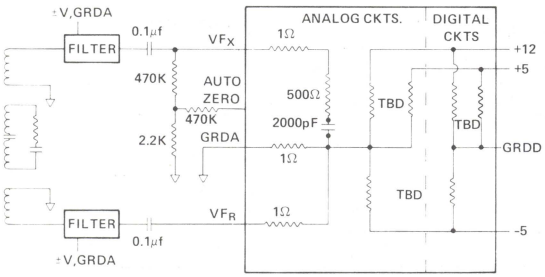
VOLTAGE REFERENCE FOR THE D/A CONVERSION

The voltage reference is generated on-board the chip and is calibrated during the manufacturing process. The tolerance is ±20mV. The dynamic range of the digital-to-analog converter is ±3.10 volts.

APPLICATION — LINE INTERFACE

Grounding

Digital grounding is connected to the GRDD lead. It is the common return for the digital signals.



Analog grounding is connected to the GRDA lead. The GRDA and GRDD lead are not connected inside the 2911. An external connection is thus necessary outside the Codec to tie all the analog ground lines to the common return of the system GRDD. That external connection has to have a minimal impedance to avoid a DC offset in the Codec.

Auto Zero

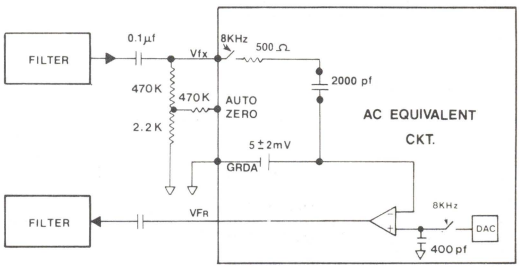
The auto zero output (most significant bit or sign bit of the A/D conversion) integrated over a long time constant will compensate for the DC offset inside the Codec (voltage difference between the bottom of the DAC and GRDA).

The above drawing shows a possible connection between the VF_X and Auto leads.

While improving DC offset, the use of Auto Zero may raise idle channel noise due to biasing near zero with resultant encoder "hunting" of the least significant bit.

Filters Interface

Attached is the schematic of the equivalent circuits of the input and output of the Codec. Note that the output pulse stream is of the non-return to zero type.



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . -40°C to +80°C
Storage Temperature . . . . . -65°C to +150°C
Supply Voltage with Respect to V_{SS} . . . . . -0.5V to +14V
All Input Voltages . . . . . -0.5V to (V_{DD} + 1V)
Outputs . . . . . -1V to (V_{DD} + 1V)
Power Dissipation 1.35W

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

DC AND OPERATING CHARACTERISTICS

$T_A = 0°C$ to $+70°C$, $V_{DD} = +12V$, $V_{CC} = 5V$, $V_{BB} = -5V$

POWER DISSIPATION

Symbol	Parameter	Limits Min.	Typ.	Max.	Unit	Test Conditions
I_{DDO}	Standby Current		TBD		mA	
I_{CCO}	Standby Current		TBD		mA	V_{DD} = +12, +10%
I_{BBO}	Standby Current		TBD		mA	V_{CC} = 5.0, +10%
						V_{BB} = -5.0, -10%
I_{DDI}	Operating Current		TBD		mA	Clocking Frequency
I_{CCI}	Operating Current		TBD		mA	X & R = 2.048 Mbps
I_{BBI}	Operating Current		TBD		mA	

DIGITAL INTERFACE

Symbol	Parameter	Limits Min.	Typ.	Max.	Unit	Test Conditions
I_{IL}	Low Level Input Current			10	μA	$V_{IN} < V_{IL}$
I_{IH}	High Level Input Current			10	μA	$V_{IN} > V_{IH}$
V_{IL}	Input Low Voltage			+0.8	V	
V_{IH}	Input High Voltage	+2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 10 mA on D_X 6.4 mA on $\overline{TS_X}$
V_{OH}	Output High Voltage	2.4			V	I_{OH} = 30 mA on D_X

ANALOG INTERFACE

Symbol	Parameter	Limits Min.	Typ.	Max.	Unit	Test Conditions
A_{IL}	Input Leakage when Sampling			1	μA	$-3.1V < V_{IN} < 3.1V$
A_{IZ}	Input Impedance when Sampling			500	Ω	In series with CAP_X to GRD
A_{OZ}	Output Impedance	1.8	2.0	2.2	kΩ	
A_{OR}	Dynamic Range (VF_R)	-3.1		+3.1	V	±10 mV

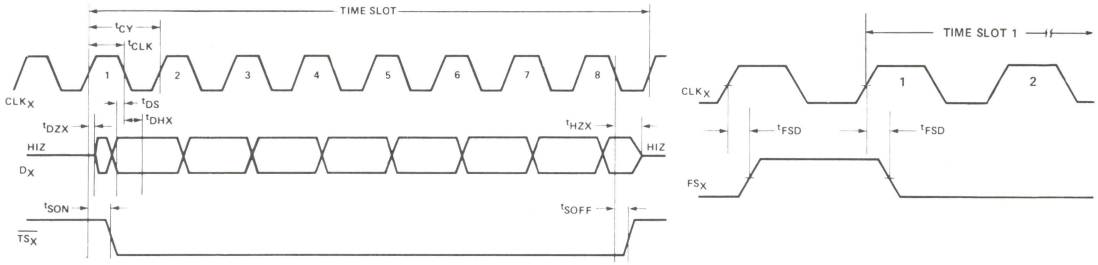
N_{IC}	Idle Channel Noise			-72	dBmOp	
ΔG	Gain Tracking Deviation from Gain at 0dBmO			±0.3	dB	Signal Level +3dBmO to -40dBmO
				±0.6	dB	Signal Level -40dBmO to -50dBmO
				±2.0	dB	Signal Level -50dBmO to -55dBmO
S/D	Signal to Total Distortion Ratio			35	dB	Signal Level 0dBmO to -30dBmO
				29	dB	Signal Level -40dBmO to -45dBmO
				24	dB	Signal Level -45dBmO

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

TIMING SPECIFICATION

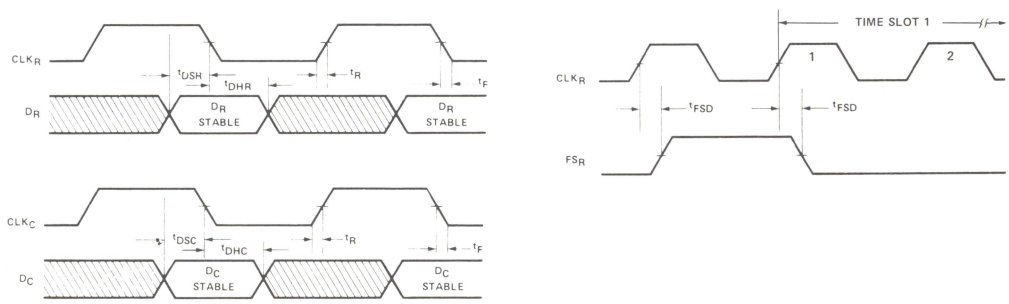
TRANSMIT SECTION

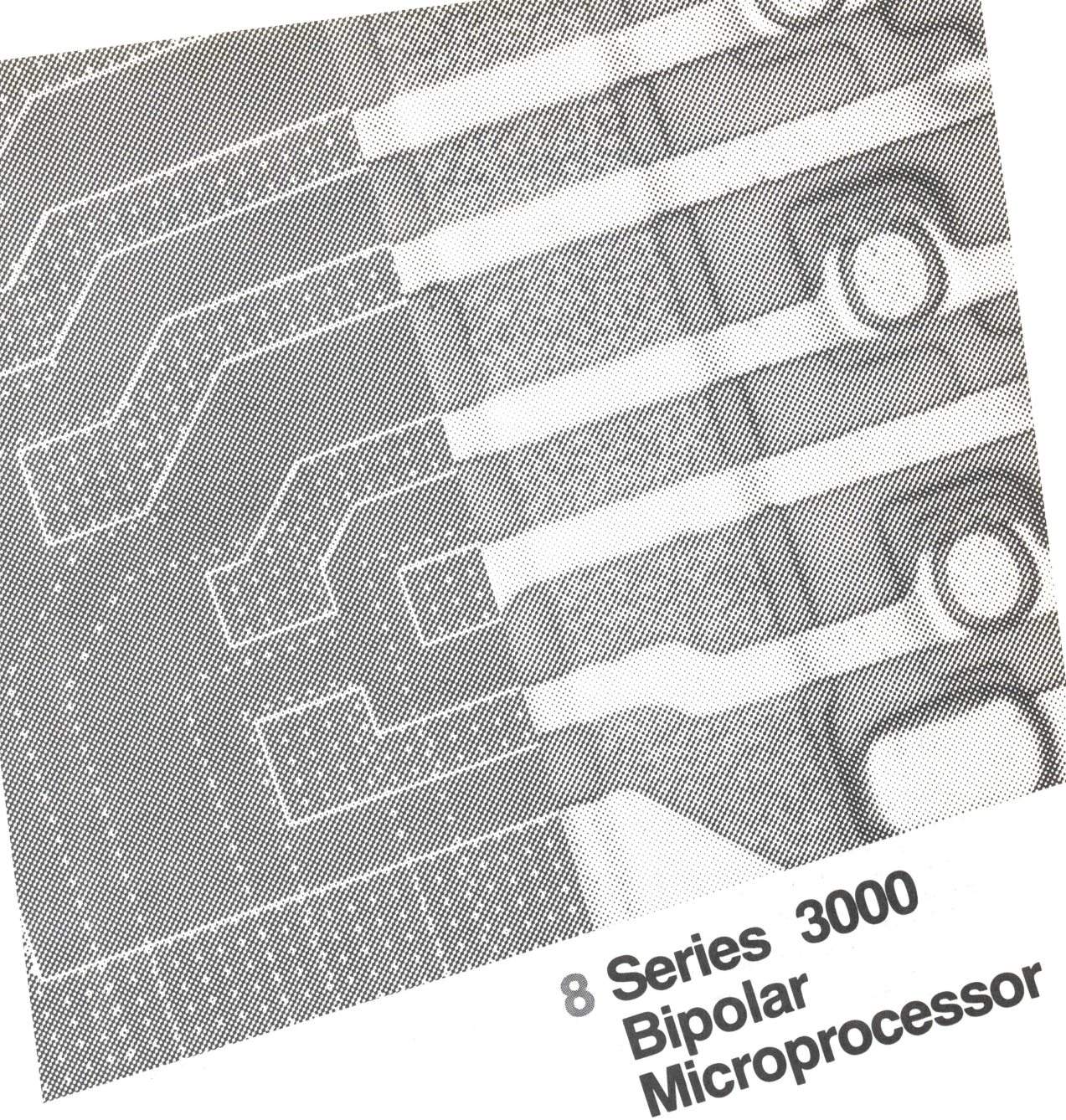
Symbol	Parameter	Limits		Units	Comments
		Min	Max		
t_{CY}	Clock Period (2.048 MHz Systems)	485		ns	
t_r, t_f	Clock Rise and Fall Time		30	ns	
t_{CLK}	Clock Pulse Width	230		ns	Nominal 50% duty cycle
t_{DS}	New Data Setup	50		ns	Increase by 0.1 ns/pF below 500 pF
t_{DHX}	Data Hold Time	75		ns	
t_{HZX}	Data Float on TS Exit	75	205	ns	
t_{SOFF}	Time Slot X to Disable	70	185	ns	
t_{DZX}	Data Enabled on TS Entry	35		ns	
t_{SON}	Time Slot X to Enable	30	180	ns	
t_{FSD}	Frame Sync Delay	10	100	ns	



RECEIVE AND CONTROL SECTIONS

Symbol	Parameter	Limits		Unit	Comments
		Min	Max		
t_{VFR}	Analog Output Update		7	Time Slot	From the trailing edge of the channel time slot
t_{DSR}	Receive Data Setup	20		ns	
t_{DHR}	Receive Data Hold	50		ns	
t_{DSC}	Control Data Setup	50		ns	
t_{DHC}	Control Data Hold	50		ns	
t_{FSD}	Frame Sync Delay	10	100	ns	





8 Series 3000 Bipolar Microprocessor

SERIES 3000 BIPOLAR MICROPROCESSOR

INTRODUCTION

Since its introduction, the Series 3000 family of computing elements has found acceptance in a wide range of high performance applications from disk controllers to airborne central processors. The Series 3000 offers the flexibility, performance, and system integration necessary for an effective system solution for both high speed controllers and central processors.

The entire 3000 family is available in commercial and military temperature range versions. In addition to the components, Intel has also developed a comprehensive support system to assist the user in writing microprograms, debugging hardware and microcode, and programming PROMs for both prototype and production systems.

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*Partial data sheets are shown here. For complete specifications, contact Intel Literature Department, Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051.

3001

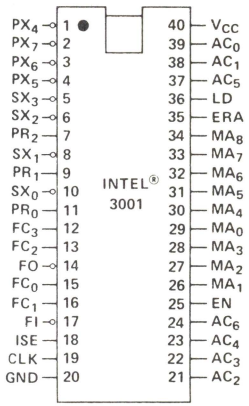
MICROPROGRAM CONTROL UNIT

The INTEL® 3001 Microprogram Control Unit (MCU) controls the sequence in which microinstructions are fetched from the microprogram memory. Its functions include the following:

- Maintenance of the microprogram address register.
- Selection of the next microinstruction based on the contents of the microprogram address register.
- Decoding and testing of data supplied via several input busses to determine the microinstruction execution sequence.
- Saving and testing of carry output data from the central processor (CP) array.
- Control of carry/shift input data to the CP array.
- Control of microprogram interrupts.

- High Performance – 85 ns Cycle Time
- TTL and DTL Compatible
- Fully Buffered Three-State and Open Collector Outputs
- Direct Addressing of Standard Bipolar PROM or ROM
- 512 Microinstruction Addressability
- Advanced Organization
  - 9-Bit Microprogram Address Register and Bus
  - 4-Bit Program Latch
  - Two Flag Registers
- Eleven Address Control Functions
  - Three Jump and Test Latch Functions
  - 16-way Jump and Test Instruction Bus Function
- Eight Flag Control Functions
  - Four Flag Input Functions
  - Four Flag Output Functions
- 40 Pin DIP

PACKAGE CONFIGURATION



SERIES 3000

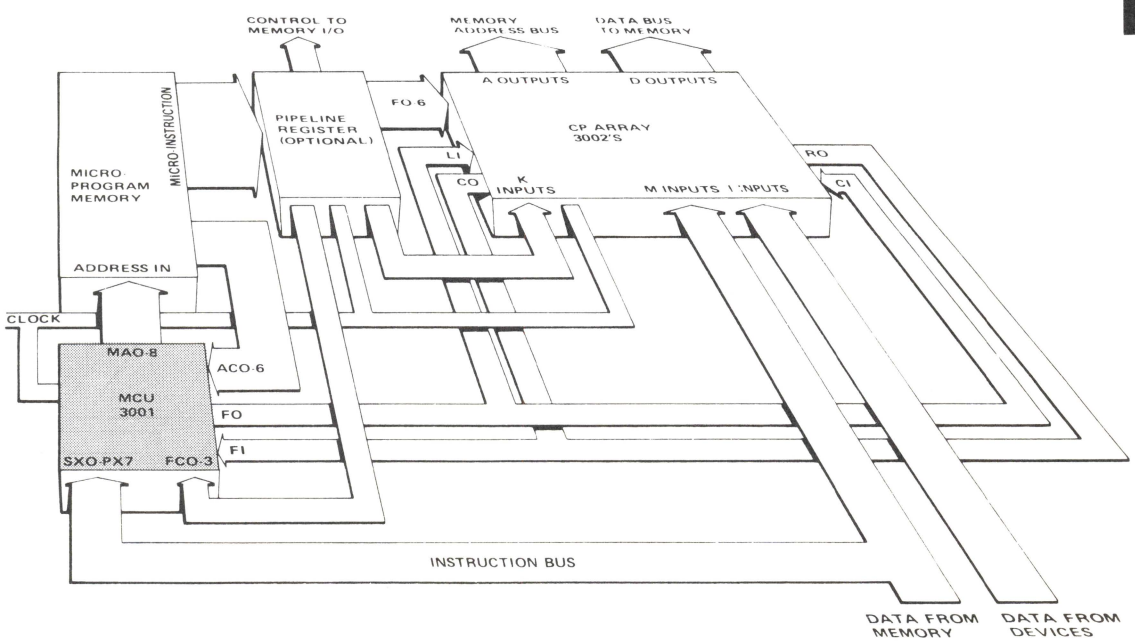


Figure 1. Block Diagram of a Typical System

3002

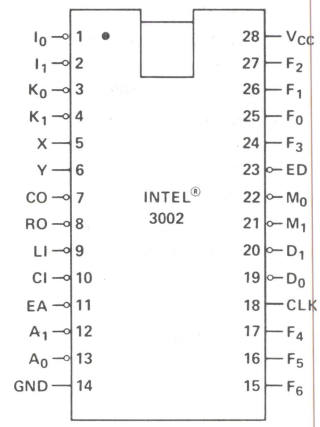
CENTRAL PROCESSING ELEMENT

The INTEL® 3002 Central Processing Element contains all of the circuits that represent a 2-bit wide slice through the data processing section of a digital computer. To construct a complete central processor for a given word width N, it is simply necessary to connect an array of N/2 CPE's together. When wired together in such an array, a set of CPE's provide the following capabilities:

- 2's complement arithmetic
- Logical AND, OR, NOT and exclusive-OR
- Incrementing and decrementing
- Shifting left or right
- Bit testing and zero detection
- Carry look-ahead generation
- Multiple data and address busses

- High Performance – 100 ns Cycle Time
- TTL and DTL Compatible
- N-Bit Word Expandable Multi-Bus Organization
  - 3 Input Data Busses
  - 2 Three-State Fully Buffered Output Data Busses
- 11 General Purpose Registers
- Full Function Accumulator
- Independent Memory Address Register
- Cascade Outputs for Full Carry Look-Ahead
- Versatile Functional Capability
  - 8 Function Groups
  - Over 40 Useful Functions
  - Zero Detect and Bit Test
- Single Clock
- 28 Pin DIP

PACKAGE CONFIGURATION



SERIES 3000

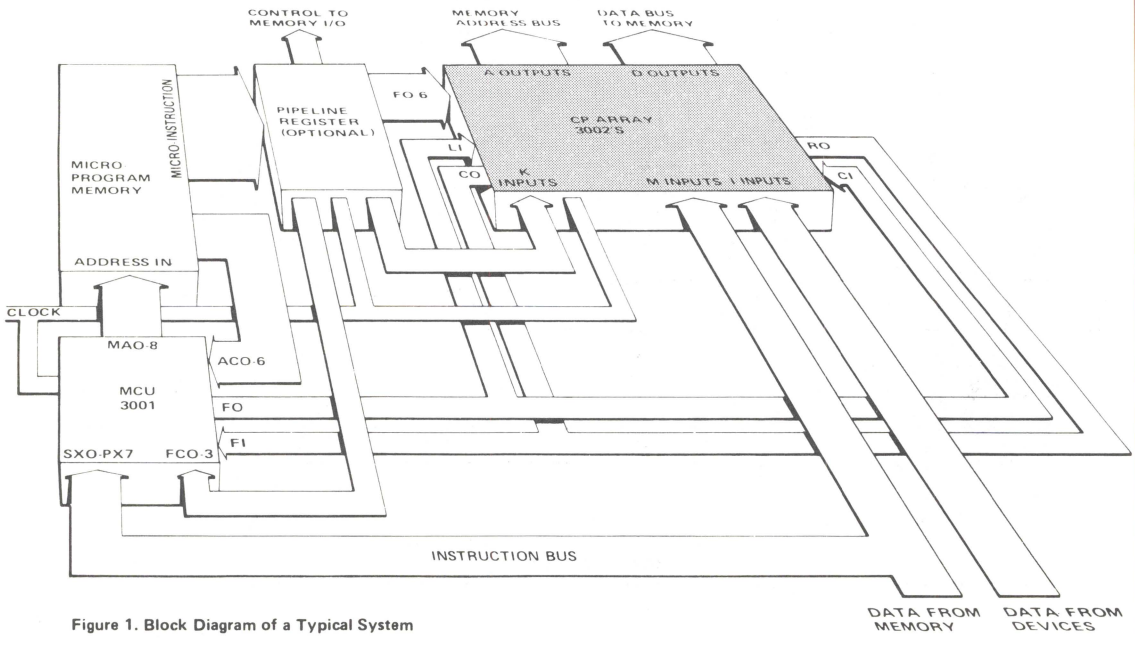


Figure 1. Block Diagram of a Typical System

3003

LOOK-AHEAD CARRY GENERATOR

The INTEL® 3003 Look-Ahead Carry Generator (LCG) is a high speed circuit capable of anticipating a carry across a full 16-bit 3002 Central Processing Element (CPE) array. When used with a larger 3002 CP array multiple 3003 carry generators provide high speed carry look-ahead capability for any word length.

The LCG accepts eight pairs of active high cascade inputs (X,Y) and an active low carry input and generates active low carries for up to eight groups of binary adders.

High Performance – 10 ns typical propagation delay

Compatible with INTEL 3001 MCU and 3002 CPE

DTL and TTL compatible

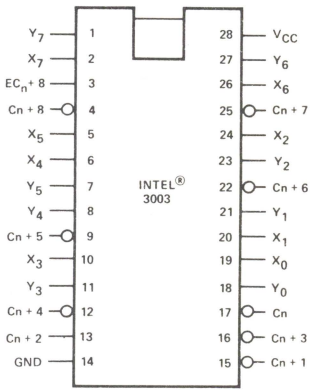
Full look-ahead across 8 adders

Low voltage diode input clamp

Expandable

28-pin DIP

PACKAGE CONFIGURATION



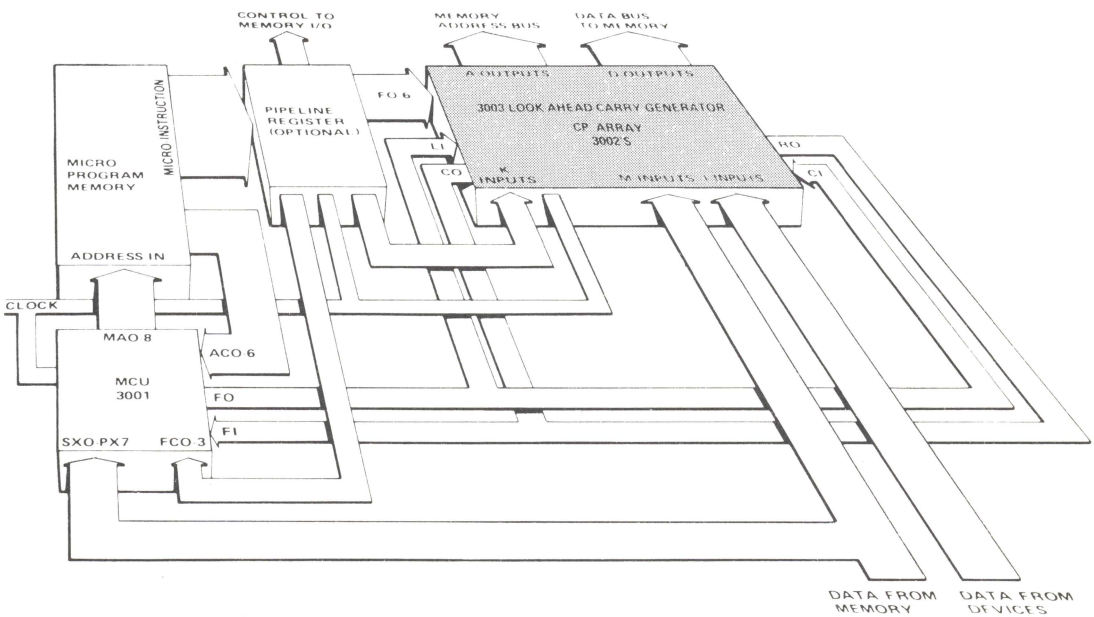
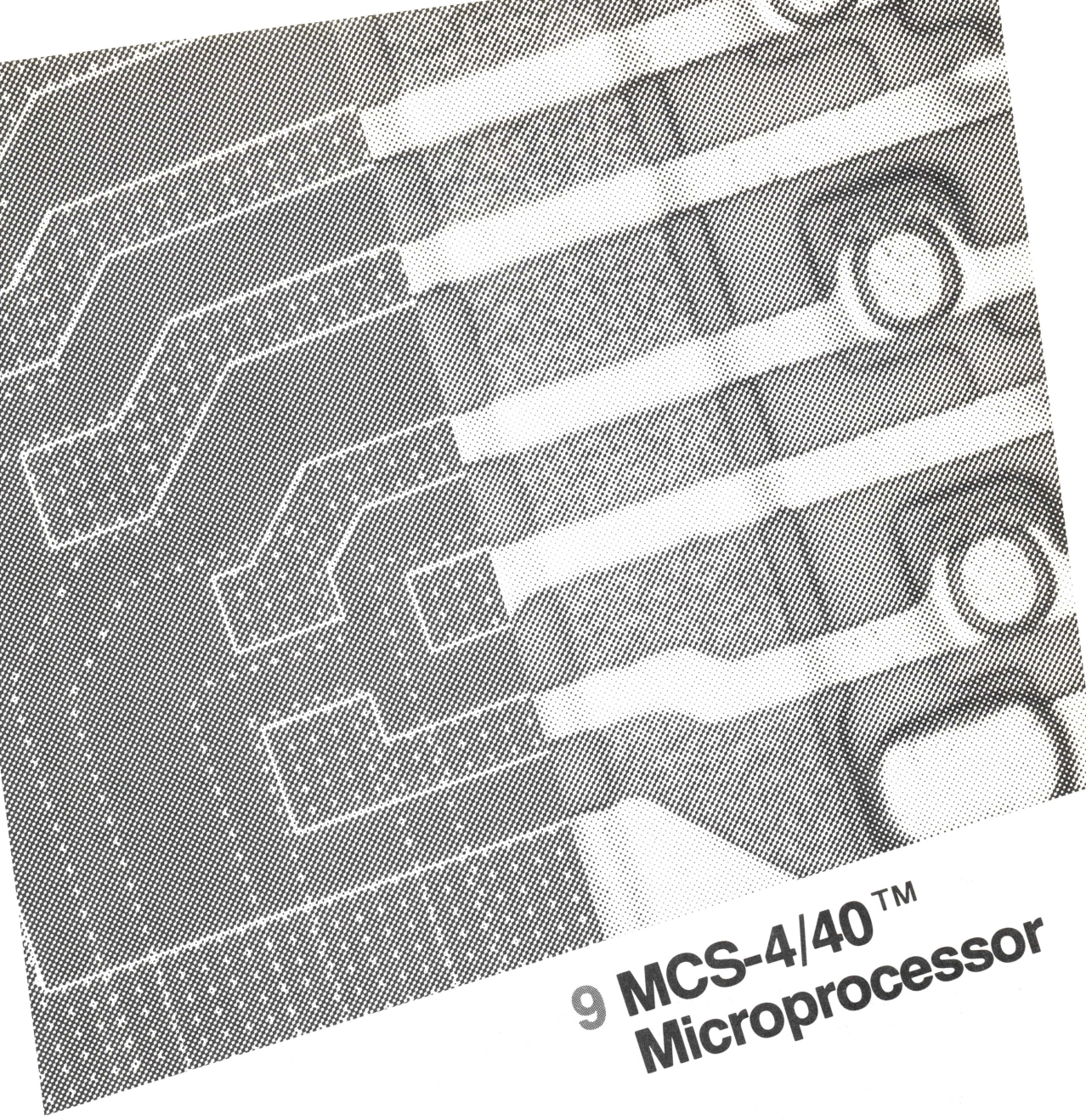


Diagram of a Typical System

SERIES 3000



9 MCS-4/40™ Microprocessor

MCS-4/40™ MICROPROCESSOR

INTRODUCTION

The MCS-4/40™ microprocessor family has been in use for a wide variety of computer and control applications since 1971. The 4004 and 4040 are complete 4-bit parallel central processing units (CPUs). The 4040 has a complete instruction set of 60 instructions, including arithmetic, interrupt, logical operations, I/O instructions, register instructions, ROM bank switching, register bank switching, interrupt disable, and enable. The 4004 has a total of 46 instructions all of which are part of the 4040 instruction set and are mutually compatible.

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*Partial data sheets are shown here. For complete specifications, contact Intel Literature Department, Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051.

4040

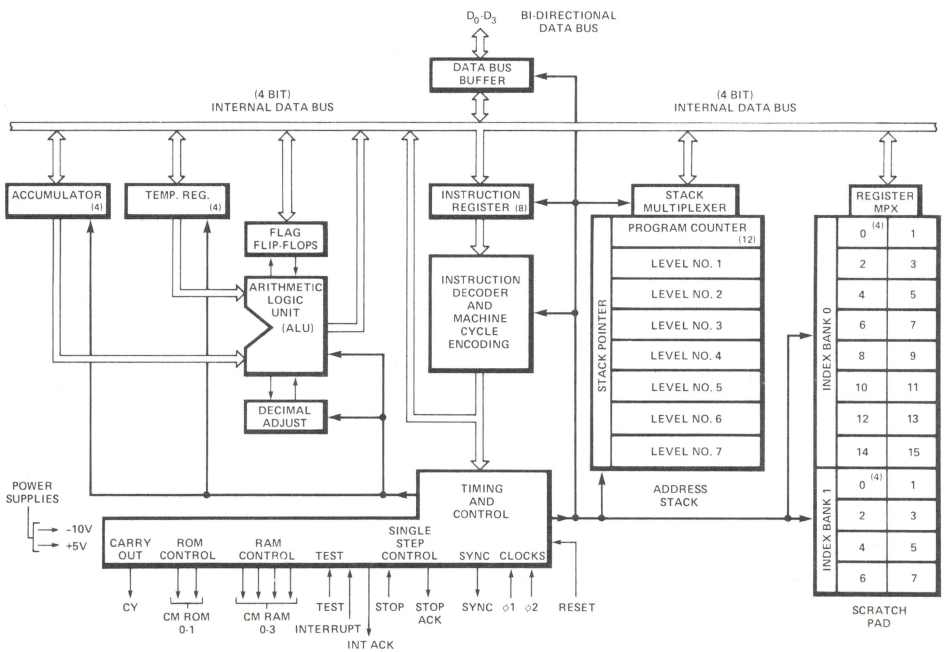
SINGLE CHIP 4-BIT P-CHANNEL MICROPROCESSOR

- **Functionally and Electrically Upward Compatible to 4004 CPU**
- **14 Additional Instructions (60 total) Including Logical Operations and Read Program Memory**
- **Interrupt Capability**
- **Single Step Operation**
- **8K Byte Memory Addressing Capability**
- **24 Index Registers**
- **Subroutine Nesting to 7 Levels**
- **Standard Operating Temperature Range of 0° to 70° C**
- **Also Available With -40° to +85° C Operating Range**

The Intel® 4040 is a complete 4-bit parallel central processing unit (CPU). The CPU can directly address 4K eight bit instruction words or 8K with a bank switch. Seven levels of subroutine nesting, including interrupt, and 24 randomly accessable index registers (24x4) are provided as convenient facilities for the designer. The index registers may be used for addressing or for scratch pad memory for storing computation results. The interrupt feature permits a normal program sequence to be interrupted, with normal program execution continuing after the interrupt service routine is completed. Provisions have also been made to permit single-stepping the CPU using the STOP and ACKNOWLEDGE signals.

The 4040 is an enhanced version of the 4004 and as such retains all the functional capability of that device. It will execute all the 4004 instructions, and is also electrically compatible with all components used with a 4004 CPU.

BLOCK DIAGRAM



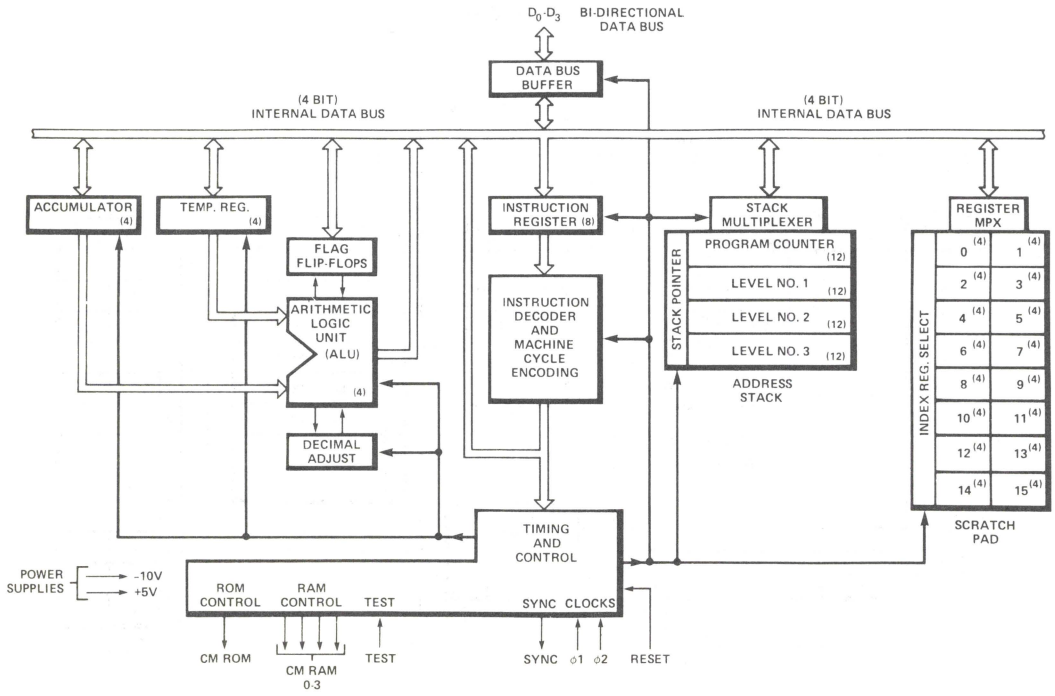
4004
SINGLE CHIP 4-BIT P-CHANNEL MICROPROCESSOR

- 4-Bit Parallel CPU With 46 Instructions
- Instruction Set Includes Conditional Branching, Jump to Subroutine and Indirect Fetching
- Binary and Decimal Arithmetic Modes
- 10.8 Microsecond Instruction Cycle
- CPU Directly Compatible With MCS-40 ROMs and RAMs
- Easy Expansion—One CPU can Directly Drive up to 32,768 Bits of ROM and up to 5120 Bits of RAM
- Standard Operating Temperature Range of 0° to 70°C
- Also Available With -40° to +85°C Operating Range

The Intel® 4004 is a complete 4-bit parallel central processing unit (CPU). The 4004 easily interfaces with keyboards, switches, displays, A-D converters, printers and other peripheral equipment.

The CPU can directly address 4K 8-bit instruction words of program memory and 5120 bits of data storage RAM. Sixteen index registers are provided for temporary data storage. Up to 16 4-bit input ports and 16 4-bit output ports may also be directly addressed.

The 4004 is fabricated with P-channel silicon gate MOS technology.



4003

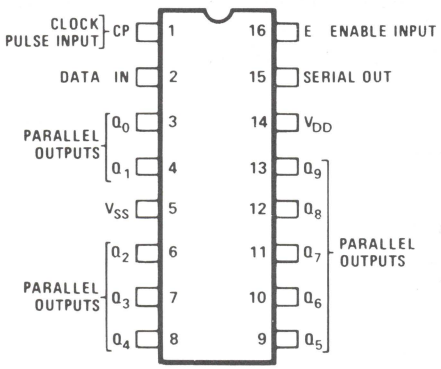
10-BIT SHIFT REGISTER/OUTPUT EXPANDER

- 10 Bit Serial-In/Parallel Out
- Serial-Out Capability for Additional I/O Expansion
- 16 Pin Dual-In-Line Package
- Easy Expansion of I/O Output Capability
- Enable Output Control
- Standard Operating Temperature Range of 0° to 70°C

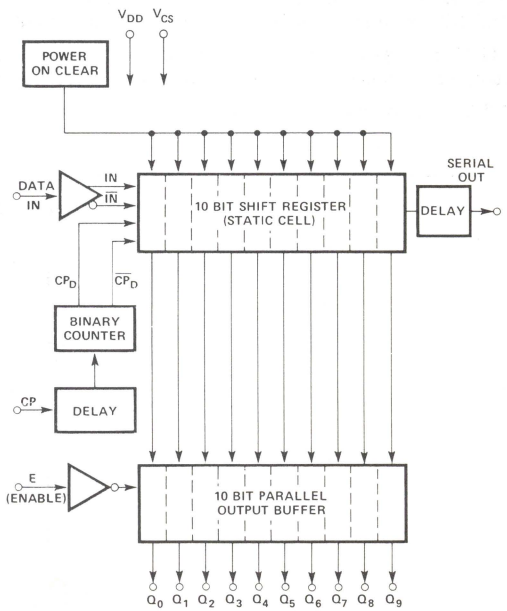
The 4003 is a 10 bit serial-in, parallel-out, serial-out shift register with enable logic. The 4003 is used to expand the number of ROM and RAM I/O ports to communicate with peripheral devices such as keyboards, printers, displays, readers, teletypewriters, etc.

The 4003 is a single phase static shift register; however, the clock pulse (CP) maximum width is limited to 10 msec. Data-in and CP can be simultaneous. To avoid race conditions, CP is internally delayed.

PIN CONFIGURATION



BLOCK DIAGRAM



4265
PROGRAMMABLE GENERAL PURPOSE I/O DEVICE

- Multi-Mode 14 Operating Modes
- 16 Lines of I/O Capability
- Bit Set/Reset
- Multiplexable Outputs
- Eight Bit Transfer Mode
- Interfaces to 8080 Peripherals
- Synchronous and Asynchronous Interface
- Strobed Buffer Inputs and Outputs
- TTL Interface
- Up to Eight 4265s Per System
- Interface to Standard RAMs
- 28 Pin Dual-In-Line Package
- Interface to Standard RAMs
- 28 Pin Dual-In-Line Package
- Standard Operating Temperature Range of 0° to 70°C
- Also Available with -40° to +85°C Operating Range

The 4265 is a general purpose I/O device designed to interface with the MCS-40™ microcomputer family. This device provides four software programmable 4-bit I/O ports which can be configured to allow any one of fourteen unique operating modes for interfacing to data memory or a variety of user peripheral devices.

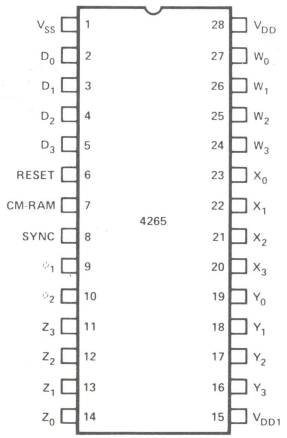
A single MCS-40 system can accomodate up to four 4265s (one per CM-RAM) without external logic or up to eight 4265s with one external decoder.

The 4265 resides on the MCS-40 data bus and uses the same selection procedure as 4002 RAM device. A valid compare selects the 4265 for MCS-40 I/O commands. As in the case of the 4002 or any MCS-40 peripheral circuit, selection occurs only when the proper SRC code and the CM signal are present simultaneously.

The 4265 provides an extremely flexible, general purpose I/O system capable of handling 4- or 8-bit input or output data. One of fourteen basic operating modes can be selected (software programmable) as described below.

Port Z is TTL compatible with any TTL device. Ports W, X, and Y are low-power TTL compatible.

PIN CONFIGURATION



4269
PROGRAMMABLE KEYBOARD DISPLAY DEVICE

Keyboard Features:

- Programmable to Interface to Encoded Keyboard (8-bit code), 64-Key Scanned Keyboard (expandable to 128 keys) or Sensor Matrix (64 sensors)
- 8 Character FIFO Character Buffer (or RAM in Sensor Mode)
- 2 Key Rollover and Key Debounce
- External Interrupt Line to Indicate When a Character Has Been Entered in Character Buffer

Display Features:

- Programmable to Interface to Individually Scanned Displays or Burrough's Self-Scan* Drive (16, 18, or 20 Characters)
- Two 16 x 4 Display Registers Recirculated Synchronously with Keyboard Scan Lines to Give Automatic Display Refresh
- Display Registers Loadable and Readable Selectively or Sequentially
- 40 Pin Dual In-Line Package
- Standard Operating Temperature Range of 0° to 70°C
- Also Available with -40°C to +85°C Operating Range

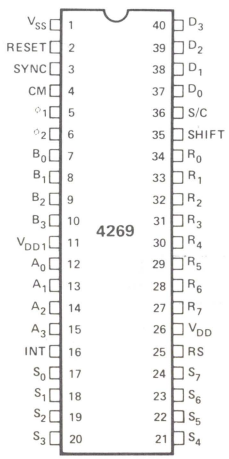
The 4269 has two separate and distinct sections: the keyboard section and the display section. The keyboard section can interface to a range of devices from a matrix of toggle or thumb switches such as found on an instrument panel up to a full typewriter style keyboard. The display section can interface to a range of devices from an array of individual LED indicators up to a gas discharge alphanumeric display.

The 4269 Programmable Keyboard Display (PKD) relieves the 4004 or 4040 CPU from continuously scanning a switch array or refreshing a display under software control. This greatly expands the CPU throughput. The 4269 can scan up to an 8 x 8 keyboard or sensor matrix (or a 2 x 8 x 8 keyboard with the use of the shift or control key input). The display portion can continuously refresh either a single 16 x 8 alphanumeric display; a single 8 x 8 alphanumeric display; a dual 16 x 4 digit display; a single 32 x 4 digit display; a 16 x 6, 18 x 6 or 20 x 6 alphanumeric gas discharge display such as the Burroughs Self-Scan*; or an array of 128 indicators.

*Self-Scan is a registered trademark of the Burroughs Corporation.

MCS-4/40

PIN CONFIGURATION



4201A

CLOCK GENERATOR

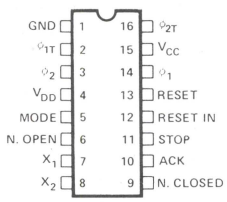
- **Complete Clock Requirements for MCS-40™ Systems**
- **Crystal Controlled Oscillator (XTAL External)**
- **MOS and TTL Level Clock Outputs**
- **Provides MCS-40 Reset Function Signal**
- **Standard Operating Temperature Range of 0° to 70°C**
- **Also Available with -40° to +85°C Operating Range**

The 4201A is a CMOS integrated circuit designed to fill the clock requirements of the MCS-40 microcomputer family. The 4201A contains a crystal controlled oscillator (XTAL external), clock generation circuitry, and both MOS and TTL level clock driver circuits.

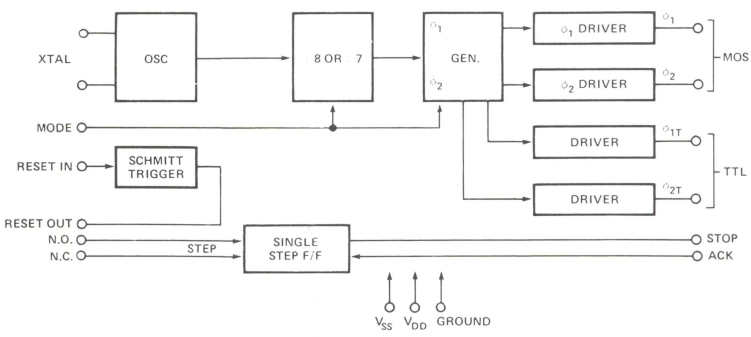
The 4201A also performs the power on reset function required by MCS-40 components and provides the logic necessary to implement the single-step function of the 4040 central processor unit.

PIN CONFIGURATION

4201A



BLOCK DIAGRAM



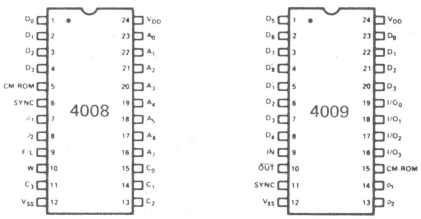
FOR NEW DESIGNS USE 4289

4008/4009
STANDARD MEMORY AND I/O INTERFACE SET

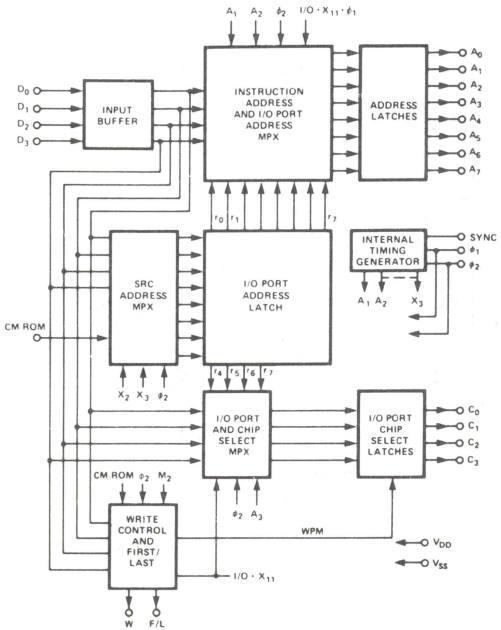
- **Direct Interface to Standard Memories**
- **Allows Write Program Memory**
- **24 Pin Dual In-Line Packages**
- **Standard Operating Temperature Range of 0° to 70 °C**

The standard memory and I/O interface set (4008/4009) provides the complete control functions performed by the 4001 or 4308 in MCS-40™ systems. The 4008/4009 are completely compatible with other members of the MCS-40 family. All activity is still under control of the CPU. One set of 4008/4009 and several TTL decoders is sufficient to interface to 4K words of program memory, sixteen four-bit input ports and sixteen four-bit output ports.

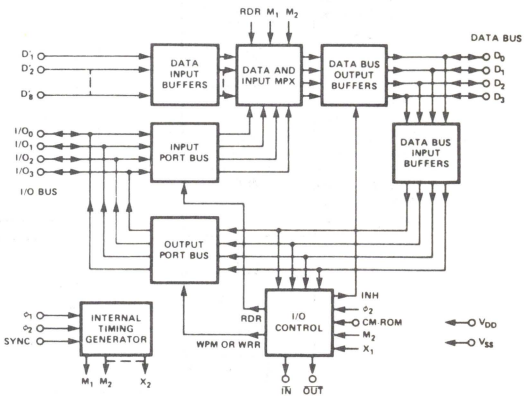
PIN CONFIGURATIONS



4008 BLOCK DIAGRAM



4009 BLOCK DIAGRAM



4289
STANDARD MEMORY INTERFACE

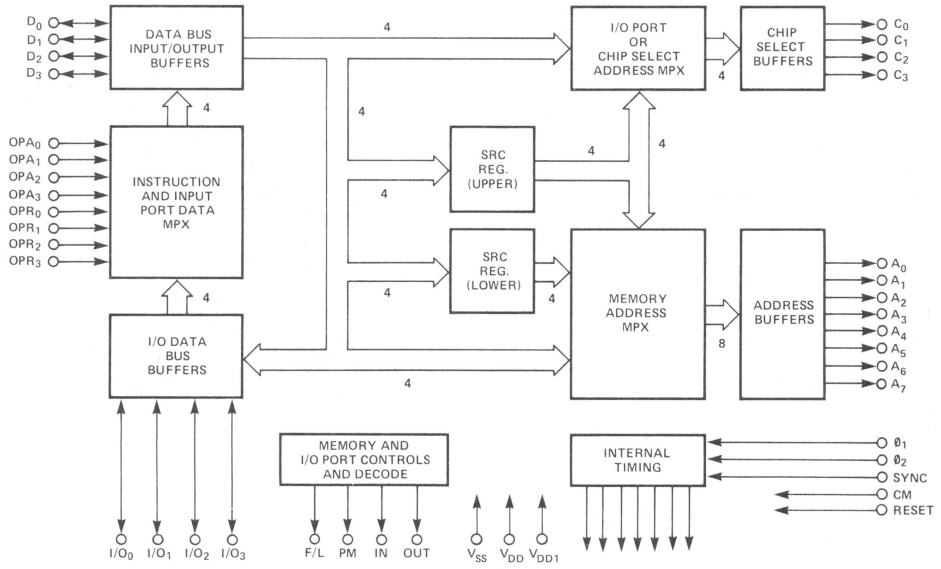
- **Direct Interface to all Standard Memories**
- **Allows Read and Write Program Memory**
- **Single Package Equivalent of 4008/4009**
- **TTL Compatible Address, Chip Select, Program Memory Data Lines**
- **40 Pin Dual In-Line Package**
- **Standard Operating Temperature Range of 0° to 70° C**
- **Also Available With -40° to +85° C Operating Range**

The 4289 standard memory interface and I/O interface enables the CPU devices to utilize standard memory components as program data memory. Notably, PROMs (4702A), RAMs (2102) and ROMs can be arranged in a memory array to facilitate system development. Programs generated using the 4289 interface can be committed to MCS-40™ ROMs (4308 and 4001) with no change to software.

The 4289 also contains a 4 bit bi-directional I/O port and necessary steering logic to multiplex a host of I/O sources to the CPU. The Read and Write Program Memory instruction allows the user to store data and modify program memory. The device directly addresses 4K of program memory. The address is obtained sequentially during A_1-A_3 states of an instruction cycle. The eight bit instruction is presented to the CPU during M_1 and M_2 states of the instruction cycle via the four bit data bus.

The 4289 stores the SRC instruction operand as an I/O address and responds to the ROM I/O instructions (WRR and RDR) by reading or writing data to and from the processor and 4289 I/O bus.

BLOCK DIAGRAM



4002

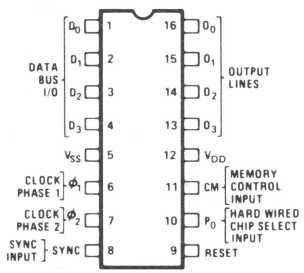
320-BIT RAM AND 4-BIT OUTPUT PORT

- **Four Registers of 20 4 Bit Characters**
- **Direct Interface to MCS-40™ 4 Bit Bus**
- **Output Port Low-Power TTL Compatible**
- **16 Pin Dual In-Line Package**
- **Standard Operating Temperature Range of 0° to 70°C**
- **Also Available With -40° to +85°C Operating Range**

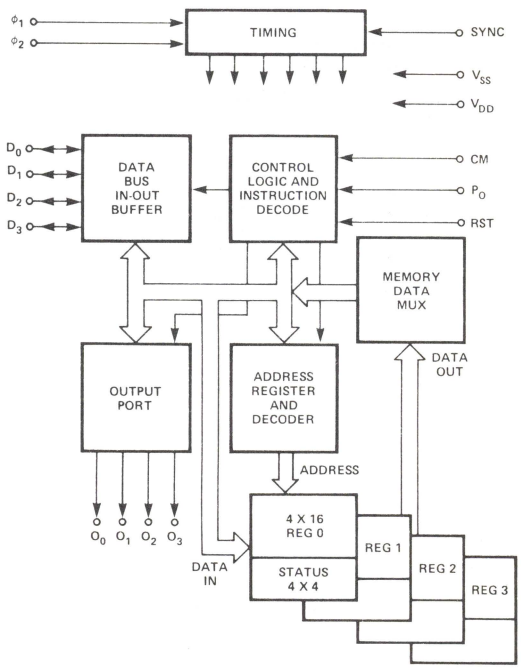
The 4002 performs two distinct functions. As a RAM it stores 320 bits arranged in 4 registers of twenty 4 bit characters each (16 main memory characters and 4 status characters). As a vehicle of communication with peripheral devices, it is provided with 4 output lines and associated control logic to perform output operations. The 4002 is a PMOS device and is compatible with all MCS-40™ components.

The 4002 is available in two options, the 4002-1 and 4002-2. Along with an external pin connected to either V_{DD} or V_{SS}, a two bit chip selection address is provided allowing a maximum of 1280 bits of 4002 RAM on a single MCS-40 CM-RAM line. Thus, the four CM-RAM lines give a maximum of 5120 bits of 4002 RAM in an MCS-40 system.

PIN CONFIGURATION



BLOCK DIAGRAM



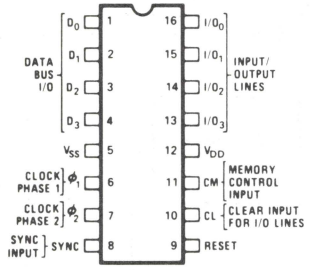
4001

256 x 8 MASK PROGRAMMABLE ROM AND 4-BIT I/O PORT

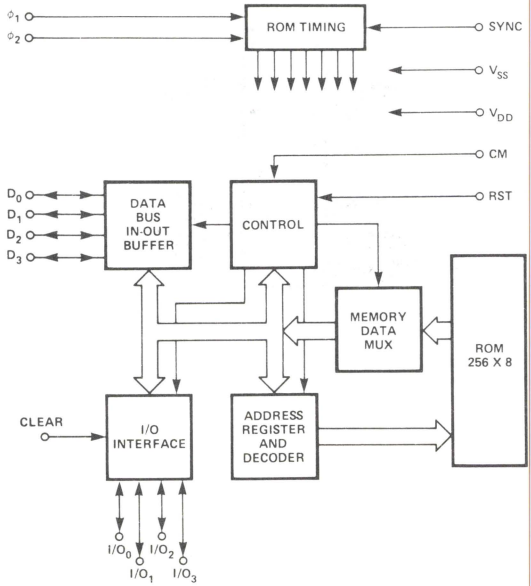
- **Direct Interface to MCS-40™ 4 Bit Data Bus**
- **I/O Port Low-Power TTL Compatible**
- **16 Pin Dual In-Line Package**
- **Standard Operating Temperature Range of 0° to 70° C**
- **Also Available With -40° to +85° C Operating Range**

The 4001 performs two basic and distinct functions. As a ROM it stores 256 x 8 words of program or data tables; as a vehicle of communication with peripheral devices it is provided with 4 I/O pins and associated control logic to perform input and output operations. The 4001 is a PMOS device, compatible with all other MCS-40™ devices.

PIN CONFIGURATION



BLOCK DIAGRAM



MCS-4/40

MCS® CUSTOM ROM ORDER FORM

4001 ROM

CUSTOMER_____

P.O. NUMBER_____

DATE_____

For Intel use only

S#_____ PPPP_____

STD_____ ZZ_____

_____ DD_____

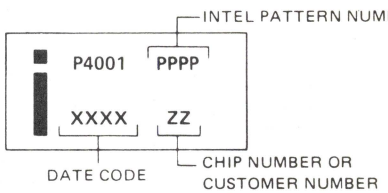
APP_____ DATE_____

All custom 4001 ROM orders must be submitted on this form. Programming information should be sent in the form of computer punched cards or punched paper tape per the formats designated on this order form. Additional forms are available from Intel.

MARKING

The marking as shown at the right must contain the Intel logo, the product type (P4001), the 4-digit Intel pattern number (PPPP), a date code (XXXX), and the 2-digit chip number (DD). An optional customer identification number may be substituted for the chip number (ZZ). Optional Customer Number (maximum 6 characters or spaces).

CUSTOMER NUMBER _____



MASK OPTION SPECIFICATIONS

A. CHIP NUMBER _____.
(Must be specified—any number from 0 through 15—DD).

B. I/O OPTION – Specify the connection numbers for each I/O pin (next page). Examples of some of the possible I/O options are shown below:

EXAMPLES – DESIRED OPTION/CONNECTIONS REQUIRED

1. Non-inverting output – 1 and 3 are connected.
2. Inverting output – 1 and 4 are connected.
3. Non-inverting input (no input resistor) – only 5 is connected.
4. Inverting input (input resistor to V_{SS}) – 2, 6, 7, and 9 are connected.
5. Non-inverting input (input resistor to V_{DD}) – 2, 7, 8, and 10 are connected.
6. If inputs and outputs are mixed on the same port, the pins used as the outputs must have the internal resistor connected to either V_{DD} or V_{SS} (8 and 9 or 8 and 10 must be connected). This is necessary for testing purposes. For example, if there are two inverting inputs (with no input resistor) and two non-inverting outputs, the connection would be made as follows:

   Inputs – 2 and 6 are connected
   Outputs – 1, 3, 8, and 9 are connected or
   1, 3, 8, and 10 are connected

   If the pins on a port are all inputs or all outputs, the internal resistors do not have to be connected.

C. 4001 CUSTOM ROM PATTERN – Programming information should be sent in the form of computer punched cards or punched paper tape. In either case, a printout of the truth table must accompany the order. In the BPNF format, the characters should be written as a "P" for a high level output = V_{SS} (negative logic "0") or an "N" for a low level output = V_{DD} (negative logic "1").

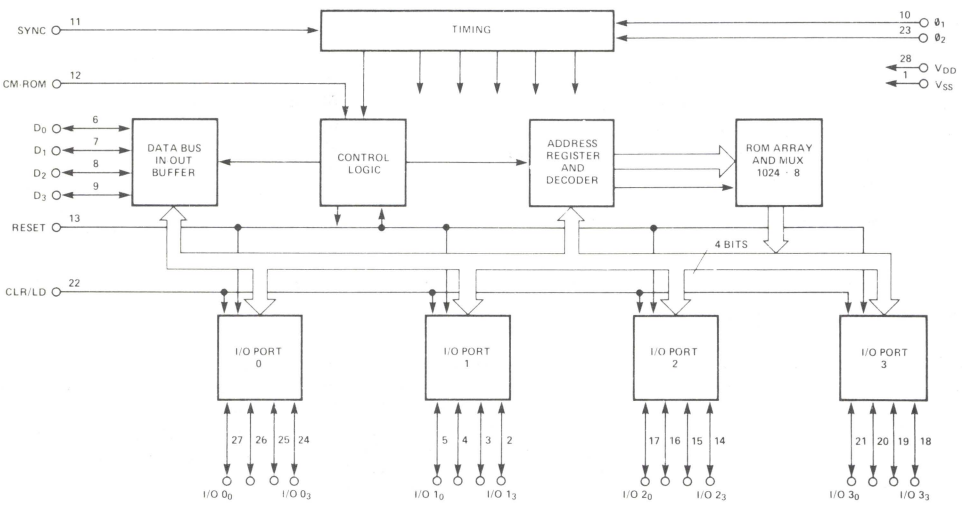
Hex input tapes for the 4001 and 4308 may also be generated by Intellec® Development Systems. These tapes are assumed to be negative logic. This means that a NOP instruction operation code (00000000), for example, would be coded as 00 in the HEX format. This would automatically result in the V_{IH} levels on the MCS 4/40 data bus. When the BPNF format is used, all logic representations must be inverted. Thus, a NOP would be represented as BPPPPPPPPF.

4308
1024 x 8 MASK PROGRAMMABLE ROM AND FOUR 4-BIT I/O PORTS

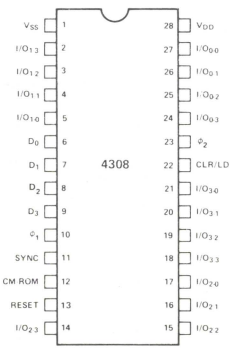
- **Direct Interface to MCS-40™ 4-Bit Data Bus**
- **Equivalent to Four 4001 ROMs**
- **Four Independent 4-Bit I/O Ports**
- **Input I/O Buffer Storage with an Optional Strobe**
- **I/O Ports Low-Power TTL Compatible**
- **28 Pin Dual In-Line Package**
- **Standard Operating Temperature Range of 0° to 70° C**
- **Also Available With -40° to +85° C Operating Range**

The 4308 is a 1024 x 8 bit word ROM memory with four I/O ports. It is designed for the MCS-40™ system and is operationally compatible with all existing MCS-40 elements. The 4308 is functionally identical to four 4001 chips. The 4308 has 16 I/O lines arranged in four groups of four lines.

BLOCK DIAGRAM



PIN CONFIGURATION



MCS® CUSTOM ROM ORDER FORM

4308 ROM

CUSTOMER _____

P.O. NUMBER _____

DATE _____

For Intel use only

S# _____ PPPP _____

STD _____ ZZ _____

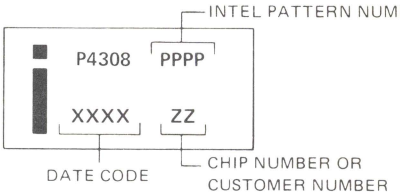
_____ DD _____

APP _____ DATE _____

All custom 4308 ROM orders must be submitted on this form. Programming information should be sent in the form of computer punched cards or punched paper tape per the formats designated on this order form. Additional forms are available from Intel.

MARKING

The marking as shown at the right must contain the Intel logo, the product type (P4308), the 4-digit Intel pattern number (PPPP), a date code (XXXX), and the 2-digit chip number (DD). An optional customer identification number may be substituted for the chip number (ZZ). Optional Customer Number (maximum 6 characters or spaces).



CUSTOMER NUMBER _____

MASK OPTION SPECIFICATION

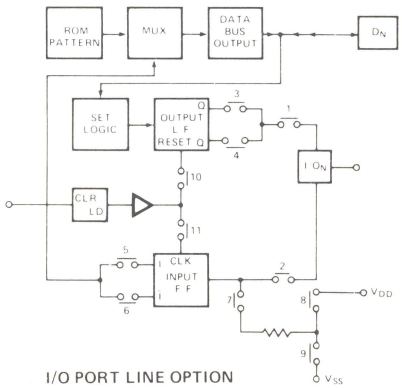
A. CHIP NUMBER _____ (Must be specified).

B. I/O OPTION – Specify the connection numbers for each I/O pin. See table below.

C. 4308 CUSTOM ROM PATTERN – Programming information should be sent in the form of computer punched cards or punched paper tape. In either case, a printout of the truth table must accompany the order. In the BPNF format, the characters should be written as a "P" for a high level output = V_{SS} (negative logic "0") or an "N" for a low level output = V_{DD} (negative logic "1").

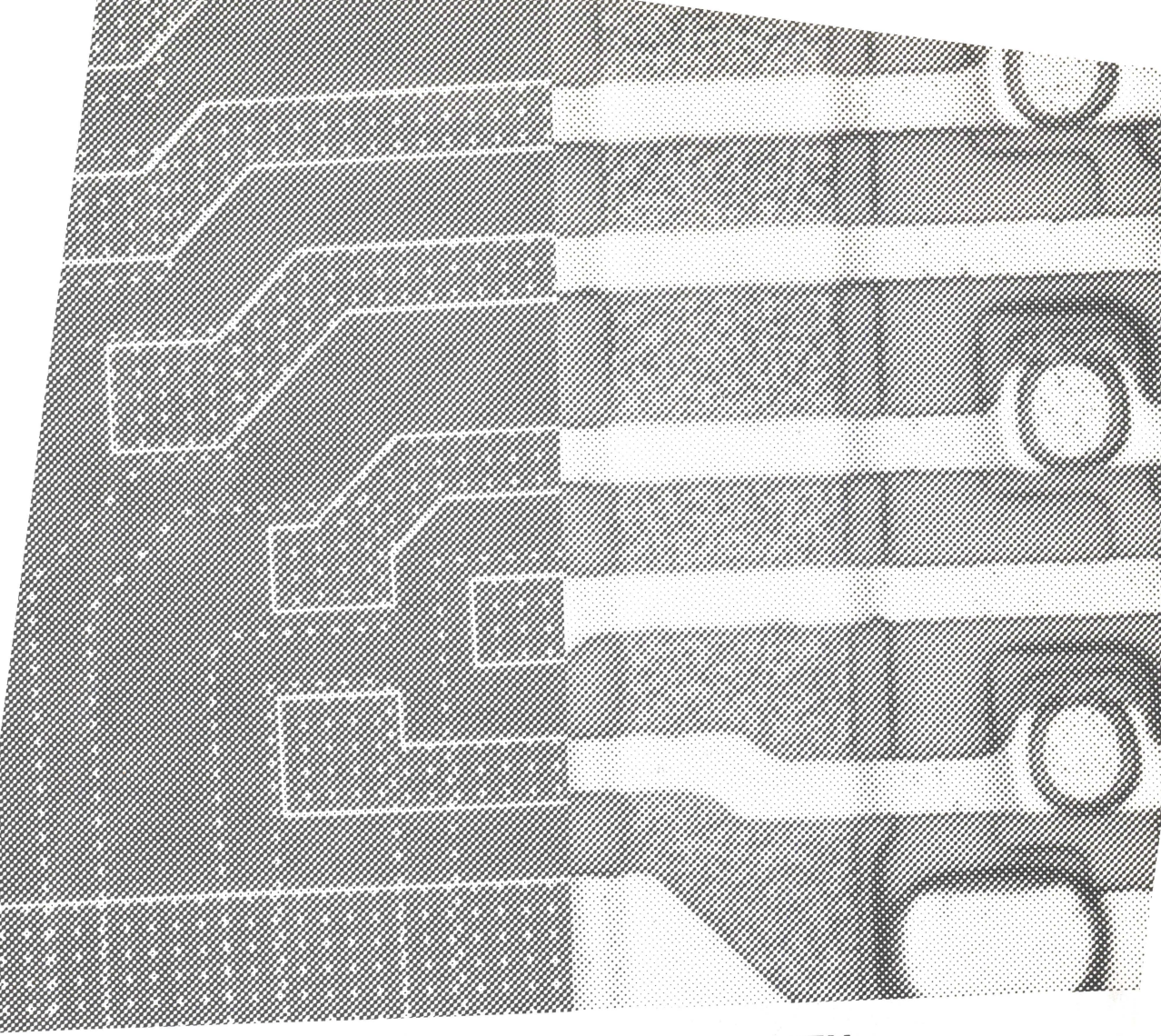
Hex input tapes for the 4001 and 4308 may also be generated by Intellec® Development Systems. These tapes are assumed to be negative logic. This means that a NOP instruction operation code (00000000), for example, would be coded as 00 in the HEX format. This would automatically result in the V_{IH} levels on the MCS 4/40 data bus. When the BPNF format is used, all logic representations must be inverted. Thus, a NOP would be represented as BPPPPPPPPF.

PIN		OPTION										
I/O 0_0	27	1	2	3	4	5	6	7	8	9	10	11
I/O 0_1	26	1	2	3	4	5	6	7	8	9	10	11
I/O 0_2	25	1	2	3	4	5	6	7	8	9	10	11
I/O 0_3	24	1	2	3	4	5	6	7	8	9	10	11
I/O 1_0	5	1	2	3	4	5	6	7	8	9	10	11
I/O 1_1	4	1	2	3	4	5	6	7	8	9	10	11
I/O 1_2	3	1	2	3	4	5	6	7	8	9	10	11
I/O 1_3	2	1	2	3	4	5	6	7	8	9	10	11
I/O 2_0	17	1	2	3	4	5	6	7	8	9	10	11
I/O 2_1	16	1	2	3	4	5	6	7	8	9	10	11
I/O 2_2	15	1	2	3	4	5	6	7	8	9	10	11
I/O 2_3	14	1	2	3	4	5	6	7	8	9	10	11
I/O 3_0	21	1	2	3	4	5	6	7	8	9	10	11
I/O 3_1	20	1	2	3	4	5	6	7	8	9	10	11
I/O 3_2	19	1	2	3	4	5	6	7	8	9	10	11
I/O 3_3	18	1	2	3	4	5	6	7	8	9	10	11



I/O PORT LINE OPTION

NOTE: Options 10 and 11 cannot both be specified.



10 MCS-48™ Microcomputers

MCS-48™ MICROCOMPUTERS

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INTRODUCTION

Recent advances in NMOS technology have allowed Intel for the first time to place enough capability on a single silicon die to create a true single chip microcomputer containing all the functions required in a digital processing system. This microcomputer, its variations, and its optional peripherals are collectively called the MCS-48 microcomputer family and are fully described in this manual.

The head of the family is the 8048 microcomputer which contains the following functions in a single 40-pin package:

8-Bit CPU
1K x 8 ROM program memory
64 x 8 RAM data memory
27 I/O lines
8-bit timer/event counter

A 2.5 or 5.0 microsecond cycle time and a repertoire of over 90 instructions each consisting of either one or two cycles makes the single chip 8048 the equal in performance of most presently available multi-chip NMOS microprocessors, yet the 8048 is a true "low-cost" microcomputer. A single 5V supply requirement for all MCS-48 components assures that "low cost" also applies to the power supply in your system.

Even with low component costs, however, a project may be jeopardized by high development and rework costs resulting from an inflexible production design. Intel has solved this problem by creating two pin-compatible versions of the 8048 microcomputer: the 8048 with mask programmable ROM program memory for low cost production and the 8748 with user programmable and erasable EPROM program memory for prototype development. The 8748 is essentially a single chip microcomputer "breadboard" which can be modified over and over again during development and pre-production, then simply replaced by the low cost 8048 ROM for volume production. The 8748 provides a very easy transition from development to production and also provides an easy vehicle for temporary field updates while new ROMs are being made.

To allow the MCS-48 to solve a wide range of problems and to provide for future expansion, all 8048 functions have been made externally expandable using either special expanders or standard memories and peripherals. An efficient low cost means of I/O expansion is provided by the 8243 Input/Output Expander which provides 16 I/O lines in a 24-pin package. For systems with large I/O requirements, multiple 8243s can be used.

For such applications as keyboards, displays, serial communication lines, etc., standard MCS-80 ™ (8080) peripheral circuits may be added. Program and data memory may be expanded using standard memories or the 8355 and 8155 memories that also include programmable I/O lines and timing functions.

The 8035 is an 8048 without internal program memory that allows the user to match his program memory requirements exactly by using a wide variety of external memories. The 8035 allows the user to select a minimum cost system no matter what his program memory requirements.

The 8048 was designed to be an efficient control processor as well as an arithmetic processor with an instruction set which allows the user to directly set and reset individual lines within its I/O ports as well as test individual bits within the accumulator. A large variety of branch and table look-up instructions make the 8048 very efficient in implementing standard logic functions. Special attention was also given to code efficiency with over 70% of the instructions being single byte and all others being only two bytes. This means many functions requiring 1.5K to 2.0K bytes in other processors may very well be compressed into the 1K words resident in the 8048.

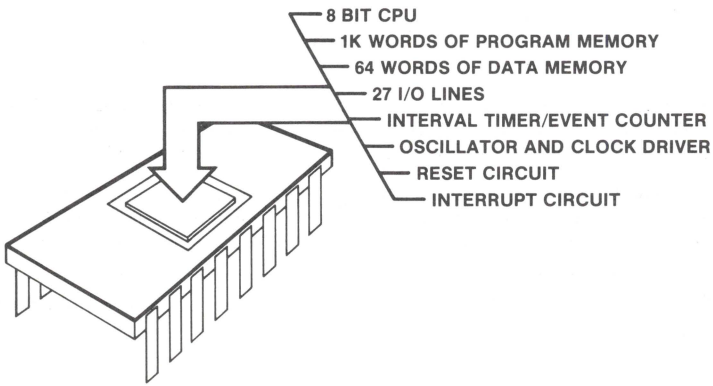


Figure 1. On Chip Features

SPECIAL FEATURES

- SINGLE 5V SUPPLY
- 40-PIN DIP
- PIN COMPATIBLE ROM AND EPROM
- 2.5 AND 5.0 μsec CYCLE VERSIONS
- ALL INSTRUCTIONS 1 OR 2 CYCLES
- SINGLE STEP
- 8-LEVEL STACK
- 2 WORKING REGISTER BANKS
- RC, XTAL, OR EXTERNAL FREQUENCY SOURCE
- CLOCK PER CYCLE AND OPTIONAL CLOCK PER STATE OUTPUT

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

8021
SINGLE COMPONENT 8-BIT MICROCOMPUTER

- 8-Bit CPU, ROM, RAM, I/O in Single 28-Pin Package
- Single 5V Supply (+4.5V to 6.5V)
- 10 μsec Cycle; All Instructions 1 or 2 Cycles
- Instructions —8748 Subset
- High Current Drive Capability—2 Pins
- 1K × 8 ROM
  64 × 8 RAM
  21 I/O Lines
- Interval Timer/Event Counter
- Clock Generated With Single Resistor or Inductor
- Zero-Cross Detection Capability
- Easily Expandable I/O

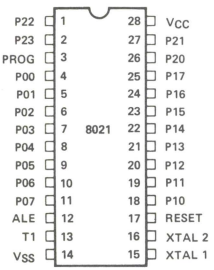
The Intel® 8021 is a totally self-sufficient 8-bit parallel computer fabricated on a single silicon chip using Intel's N-channel silicon gate MOS process. The features of the 8021 include a subset of the 8048 optimized for low cost, high volume applications, plus additional I/O flexibility and power.

The 8021 contains a 1K X 8 program memory, a 64 X 8 data memory, 21 I/O lines, and an 8-bit timer/event counter, in addition to on-board oscillator and clock circuits. For systems that require extra I/O capability, the 8021 can be expanded using the 8243 or discrete logic.

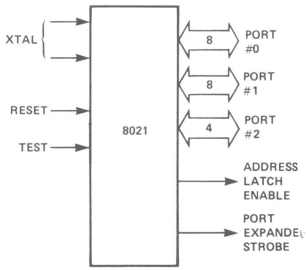
This microprocessor is designed to be an efficient controller as well as an arithmetic processor. The 8021 has bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single byte instructions and no instructions over two bytes in length.

To minimize development problems and maximize flexibility, an 8021 system can be easily designed using the 8021 emulation board, EMB-21. The EMB-21 contains a 40-pin socket which can accommodate either the 8748 shipped with the board or an ICE-48 plug. Also, the necessary discrete logic to reproduce the 8021's additional I/O features is included.

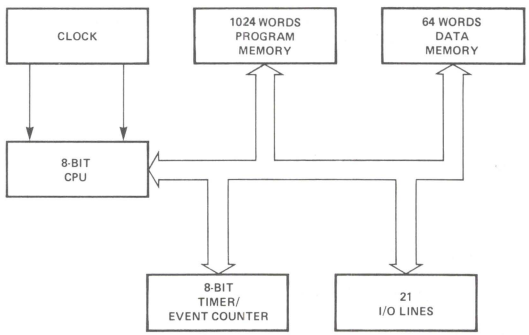
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



MCS-48

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

FUNCTIONAL SPECIFICATIONS

The following is a functional description of the major elements of the 8021.

Program Memory

The 8021 contains 1K X 8 of mask programmable ROM. No external ROM expansion capability is provided.

Data Memory

A 64 X 8 dynamic RAM is located on chip for data storage. All locations are indirectly addressable and eight designated locations are directly addressable. Also, included in the memory is the address stack, addressed by a 3-bit stack pointer.

Memory is organized as shown in Figure 1. The least significant 8 addresses, 0–7, are directly addressable by any of the 11 direct register instructions. The locations are readily accessible for a variety of operations with the least number of instruction bytes required for their manipulation.

Registers 0 and 1 have yet another function, in that they can be used to indirectly address all locations in memory, using the indirect register instructions. These indirect RAM address registers, IRAR's, are especially useful for repetitive-type operations on adjacent memory locations. The indirect register instruction specifies which IRAR to use, and the contents of the IRAR is used to address a location in RAM. The contents of the addressed location is used during the execution of the instruction, and may be modified. A value larger than 63 should not be preset in the IRAR when selected by an indirect register instruction. IRAR's may point to addresses 0–7, if desired.

Locations 8–23 may be used as the address stack. The address stack enables the processor to keep track of the return addresses generated from CALL instructions. A 3-bit stack pointer (SP) supplies the address of the locations to be loaded with the next return address generated. The SP to this pushdown stack is incremented by one after a return address is stored, and decremented by one before an address is fetched during a RET. A total of 8 levels of nesting is possible. The SP is initialized to location 8 upon RESET. Since each address is 10 bits long, two bytes must be used to store a single address. The SP is incremented and decremented by one, but each increment or decrement moves the address pointed to by two. Therefore, only even numbered addresses are pointed to.

If a particular application does not require 8 levels of nesting, the unused portion of the stack may be used as any other indirectly addressable scratchpad location. For example, if only 3 levels of subroutine nesting are used, then only locations 8–15 need be reserved for the address stack, and locations 16–63 can be used for data storage. The actual program counter address is not stored in the address stack. A separate register retains its value.

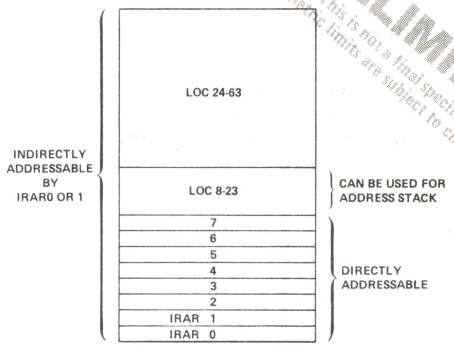


Figure 1. Internal RAM Organization

Oscillator and Clock

The 8021 contains its own onboard oscillator and clock circuit, requiring only an external timing control element. This control element can be a crystal, inductor, resistor, or clock in. The capacitor normally required in resistor or inductor timing control operation is integrated onto the 8021. All internal time slots are derived from the external element, and all outputs are a function of the oscillator frequency. Pins X1 and X2 are used to input the particular control element. An instruction cycle consists of 10 states, and each state is a time slot of 3 oscillator periods. Therefore, to obtain a 10 μsec instruction cycle, a 3 MHz crystal should be used.

Timer/Event Counter

An interval timer is available to enable the user to keep track of time elapsed or number of events occurred, during normal program execution and flow.

By a MOV T,A instruction, the contents of the accumulator are loaded to the timer. At the STRT T command an internal prescaler is zeroed and thereafter increments once each 30 input clocks (once each single cycle instruction, twice each double cycle instruction). The prescaler is a divide by 32. At the (11111) to (00000) transition the timer is incremented. The timer is 8 bits and an overflow (FFH) to (00H) timer flag is set. A conditional branch is available for testing this flag, the flag being reset each test. Total count capacity for the timer is $2^8 \times 2^5 = 8192$ or 81.9 msec at a 10 μsec cycle time. Contents of the timer are moved to the accumulator by the MOV A,T instruction without disturbing the counting process.

The timer may also be used as an event counter. After a STRT CNT command, the chip will respond to a high to low transition on the Test 1 pin by incrementing the timer. Transitions can occur no faster than one each three instruction cycles.

The timer and event functions are exclusive. Counting or timing may be started or stopped (STOP TCNT) at will.

Input/Output Capabilities

The 8021 I/O configurations are highly flexible. A number of different configurations are possible, tailoring an 8021 to a given task. Other than the power supply and dedicated pins, all other pins (20) can be used for input, output, or both, depending on the configuration.

P20—P23 and P10—P17 are quasi-bidirectional, and Test 1 is directly testable through program control. A simplified schematic of the quasi-bidirectional interface is shown in Figure 2. This configuration allows buffered outputs, and also allows external input. When writing a "0" or low value to these ports, the large pulldown device sinks an external TTL load. When writing a "1", a large current is supplied through the large pullup device to allow a fast data transfer. After a short time (less than one instruction cycle), the large device is shut off and the small pullup maintains the "1" level indefinitely. However, in this situtation, an input device capable of overriding the small amount of sustaining current supplied by the pullup device can be read. (Alternatively, the data written can be read). So, by writing a "1" to any particular pin, that pin can serve either as a true high-level latched output pin, or as just a pullup resistor on an input. This allows maximum user flexibility in selecting his input or latched output pins, with a minimum of external components.

Port 00—07 is also quasi-bidirectional, except there is no large pullup device. As outputs, this port is essentially open drain.

By mask option the small pullup devices on P00—P07 may be deleted on any pin providing a true open drain output. This is useful in driving analog circuits and certain loads, such as keyboards.

Also available is the 8243 I/O expander chip, which provides additional I/O capability with a limited number of overhead pins. This chip has 4 directly addressable 4-bit ports. It connects to the PROG pin, which provides a clock, and pins P20—P23, which provide address and data. These ports can be written with a MOVD P,A; ANLD P,A; and ORLD P,A for Ports 4—7. A high to low transition on PROG signifies that address and control are available on P20—P23. The previous data on P20—P23 before an output expander instruction is lost. Therefore, when using an output expander P20—P23 are not useful for general input/output. Reading is via the MOVD A,P. This circuit configuration is shown in Figure 3.

The Test 1 pin has a special bias input that allows zero-crossover sensing of slowly moving inputs. This is especially useful in SCR control of 60 Hz power and in developing time of day routines. As a ROM mask option there is a pullup resistor that is useful for switch contact input or standard TTL. See Figure 4.

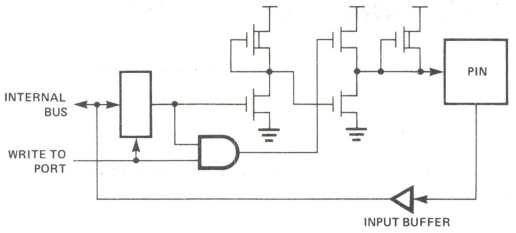


Figure 2. Quasi-Bidirectional Port Structure

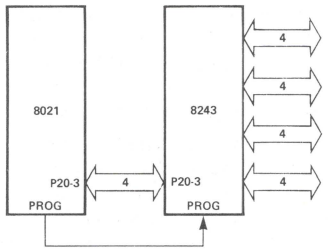


Figure 3. I/O Expander Interface

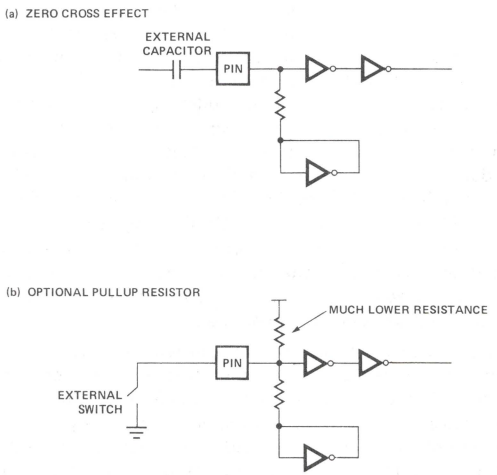


Figure 4. Test 1 Pin

CPU

The 8021 CPU has arithmetic and logical capability. A wide variety of arithmetic and logic instructions may be exercised, which affect the contents of the accumulator, and/or direct or indirect scratchpad locations. Provisions have been made for simplified BCD arithmetic capability through the use of the DAA, SWAP A, and XCHD instructions. In addition, MOVP A,@A allows table lookup for display formating and constants. Jump conditions such as zero, not zero refer to the accumulator contents at the time of the condition.

Reset

The 8021 may see poorly regulated and noisy power supplies. A useful feature is to sense when the power supply dips and do a reset to prevent continued operation with incorrect data. This feature may be implemented on the 8021 by connecting a diode between the RESET node and ground. See Figure 5.

A reset will then be forced if the supply drops approximately 1.5 volts and rapidly recovers. One instruction cycle will reset the 8021 to the initialized state.

By removing the diode and using only the capacitor, voltage drops in V_{CC} will not cause a RESET.

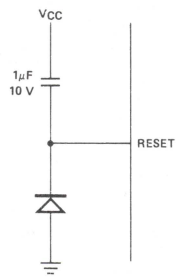


FIGURE 5. POWER ON RESET

Differences Between the 8021 and the 8748

Although the 8021 is basically an electrical and functional subset of the 8748, there are some differences:

1. *Pin Out* — As the 8021 is a 28-pin DIP, some form of adapter must be used to interface the 8021 socket to ICE-48. An emulation board, EMB-21, has been designed to perform this function. The EMB-21 also accounts for the increased flexibility of some 8021 I/O lines.
2. *Instruction Time* — The 8021 instruction cycle is 30 clock cycles long, the 8748 instruction cycle is 15 clocks long. Where exact timing is important the 8748 breadboard part should be operated at half the 8021 clock rate.
3. *Test 1* — To facilitate developing time of day routines from 60 Hz, and for SCR control, the Test 1 pin without the pullup resistor option will detect zero crossing of a capacitively coupled AC input.
4. *Quasi-Bidirectional Ports* — All 8021 ports are quasi-bidirectional to facilitate stand-alone use. Port 0 has open drain outputs and by mask option it may or may not have pullup resistors.
5. *Oscillator* — The 8021 has on-chip oscillator that is optimized for the single resistor mode. External connection will differ from the 8748.
6. *Dynamic RAM and Logic* — The 8021 utilizes dynamic RAM and some dynamic logic. Input clocking must be maintained above the minimum rate or improper operation may result.
7. *High Current Outputs* — Very high current drive is desirable for minimizing external parts required to do high power control. P10 and P11 have been designated high drive outputs capable of sinking 7 mA at V_{SS} +2.5 volts. (For clarity, this is 7 mA to V_{SS} with a 2.5 volt drop across the buffer.) These pins may, of course, be paralleled for 14 mA drive if the output logic states are always the same.
8. *Reset* — Reset has been modified on the 8021, as previously noted. A reset will be forced if the power supply drops approximately 1.5 volts and rapidly recovers, if a diode is used in the reset circuit. This prevents continued operation with incorrect data caused by a poorly regulated and/or noisy power supply.
9. *Instruction Set* — The following instructions, which are found in the 8748, have been deleted from the 8021 instruction set.

Data Moves	Registers	Branch	Timer	Control	Input/Output
MOV A,PSW	DEC R	JT0 addr	EN TCNTI	EN I	ANL P,#data
MOV PSW,A		JNT0 addr	DIS TCNTI	DIS I	ORL P,#data
MOVX A,@R	**Flags**	JF0 addr		SEL RB0	INS A,BUS *
MOVX @R,A	CLR F0	JF1 addr	**Subroutine**	SEL RB1	OUTL BUS,A *
MOVP3 A,@A	CPL F0	JNI addr	RETR	SEL MB0	ANL BUS,#data
	CLR F1	JBb addr		SEL MB1	ORL BUS,#data
	CPL F1			ENT0 CLK	

*These Instructions have been replaced in the 8021 by IN A,P0 and OUTL P0,A respectively.

PIN DESCRIPTION

Designation	Pin #	Function
V_{SS}	14	Circuit GND potential
V_{CC}	28	+5V power supply
PROG	3	Output strobe for 8243 I/O Expander
P00–P07 Port 0	4–11	8-bit quasi-bidirectional port
P10–P17 Port 1	18–25	8-bit quasi-bidirectional port
P20–P23 Port 2	26–27 1–2	4-bit quasi-bidirectional port P20–P23 also serve as a 4-bit I/O expander bus for 8243
T1	13	Input pin testable using the JT1 and JNT1 instructions. Can be designated the timer/event counter input using the STRT CNT instruction. Also allows zero-crossover sensing of slowly moving AC inputs.
RESET	17	Input used to initialize the processor by clearing status flip-flops and setting program counters to zero.
ALE	12	Address Latch Enable. Signal occuring once every 30 input clocks, used as an output clock.
XTAL1	15	One side of crystal, inductor, or resistor input for internal oscillator. Also input for external source. (Not TTL compatible.)
XTAL2	16	Other side of timing control element.

INSTRUCTION SET

	Mnemonic		Description	Bytes	Cycle
Accumulator	ADD	A,R	Add register to A	1	1
	ADD	A,@R	Add data memory to A	1	1
	ADD	A,#data	Add immediate to A	2	2
	ADDC	A,R	Add with carry	1	1
	ADDC	A,@R	Add with carry	1	1
	ADDC	A,#data	Add with carry	2	2
	ANL	A,R	And register to A	1	1
	ANL	A,@R	And data memory to A	1	1
	ANL	A,#data	And immediate to A	2	2
	ORL	A,R	Or register to A	1	1
	ORL	A,@R	Or data memory to A	1	1
	ORL	A,#data	Or immediate to A	2	2
	XRL	A,R	Exclusive Or register to A	1	1
	XRL	A,@R	Exclusive or data memory to A	1	1
	XRL	A,#data	Exclusive or immediate to A	2	2
	INC	A	Increment A	1	1
	DEC	A	Decrement A	1	1
	CLR	A	Clear A	1	1
	CPL	A	Complement A	1	1
	DA	A	Decimal Adjust A	1	1
	SWAP	A	Swap nibbles of A	1	1
	RL	A	Rotate A left	1	1
	RLC	A	Rotate A left through carry	1	1
	RR	A	Rotate A right	1	1
	RRC	A	Rotate A right through carry	1	1
Input/Output	IN	A,P	Input port to A	1	2
	OUTL	P,A	Output A to port	1	2
	MOVD	A,P	Input Expander port to A	1	2
	MOVD	P,A	Output A to Expander port	1	2
	ANLD	P,A	And A to Expander port	1	2
	ORLD	P,A	Or A to Expander port	1	2
Registers	INC	R	Increment register	1	1
	INC	@R	Increment data memory	1	1
Branch	JMP	addr	Jump unconditional	2	2
	JMPP	@A	Jump indirect	1	2
	DJNZ	R,addr	Decrement register and Jump on R not zero	2	2

	Mnemonic		Description	Bytes	Cycle
Branch	JC	addr	Jump on Carry = 1	2	2
	JNC	addr	Jump on Carry = 0	2	2
	JZ	addr	Jump on A Zero	2	2
	JNZ	addr	Jump on A not Zero	2	2
	JT1	addr	Jump on T1 = 1	2	2
	JNT1	addr	Jump on T1 = 0	2	2
	JTF	addr	Jump on timer flag	2	2
Subroutine	CALL		Jump to subroutine	2	2
	RET		Return	1	2
Flags	CLR	C	Clear Carry	1	1
	CPL	C	Complement Carry	1	1
Data Moves	MOV	A,R	Move register to A	1	1
	MOV	A,@R	Move data memory to A	1	1
	MOV	A,#data	Move immediate to A	2	2
	MOV	R,A	Move A to register	1	1
	MOV	@R,A	Move A to data memory	1	1
	MOV	R,#data	Move immediate to register	2	2
	MOV	@R,#data	Move immediate to data memory	2	2
	XCH	A,R	Exchange A and register	1	1
	XCH	A,@R	Exchange A and data memory	1	2
	XCHD	A,@R	Exchange nibble of A and register	1	1
	MOVP	A,@A	Move to A from current page	1	2
Timer/Counter	MOV	A,T	Read Timer/Counter	1	1
	MOV	T,A	Load Timer/Counter	1	1
	STRT	T	Start Timer	1	1
	STRT	CNT	Start Counter	1	1
	STOP	TCNT	Stop Timer/Counter	1	1
	NOP		No Operation	1	1

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . 0°C to 70°C
Storage Temperature . . . . . -65°C to +150°C
Voltage on Any Pin with
Respect to Ground . . . . . -0.5V to +7V
Power Dissipation . . . . . 1 W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = 5.5V \pm 1V$, $V_{SS} = 0V$

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
V_{IL}	Input Low Voltage (All except XTAL1, XTAL2)	-0.5		0.8	V	
V_{IH}	Input High Voltage (All except XTAL1, XTAL2)	2.0		V_{CC}	V	$V_{CC} = 5.0V \pm 10\%$
V_{IH_1}	Input High Voltage (All except XTAL1, XTAL2)	3.0		V_{CC}	V	$V_{CC} = 5.5V \pm 1V$
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 1.6$ mA
V_{OL_1}	Output Low Voltage (P10, P11)			2.5	V	$I_{OL} = 7$ mA
V_{OH}	Output High Voltage (All unless Open Drain)	2.4			V	$I_{OH} = 50\ \mu A$
I_{OL}	Output Leakage Current (Open Drain Option — Port 0)			-10	μA	$V_{CC} \geqslant V_{IN} \geqslant V_{SS} + 0.45$
I_{CC}	V_{CC} Supply Current			60	mA	

A.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = 5.5V \pm 1V$, $V_{SS} = 0V$

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{CY}	Cycle Time	10.0	50.0	μsec	3 MHz XTAL = 10 μsec
Δ_F	Oscillator Frequency Variation -Resistor Mode	-20	+20	%	F = 2.5 MHz

A.C. TEST CONDITIONS

Control Outputs: $C_L = 80$ pF, $R_L = 2.2K/4.3K$

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

8048/8748/8035
SINGLE COMPONENT 8-BIT MICROCOMPUTER

- 8048 Mask Programmable ROM
- 8748 User Programmable/Erasable EPROM
- 8035 External ROM or EPROM

- 8-Bit CPU, ROM, RAM, I/O in Single Package
- Interchangeable ROM and EPROM Versions
- Single 5V Supply
- 2.5 μsec and 5.0 μsec Cycle Versions: All Instructions 1 or 2 Cycles
- Over 90 Instructions: 70% Single Byte
- 1K x 8 ROM/EPROM
  64 x 8 RAM
  27 I/O Lines
- Interval Timer/Event Counter
- Easily Expandable Memory and I/O
- Compatible with 8000 Series Peripherals
- Single Level Interrupt

The Intel® 8048/8748/8035 is a totally self-sufficient 8-bit parallel computer fabricated on a single silicon chip using Intel's N-channel silicon gate MOS process.

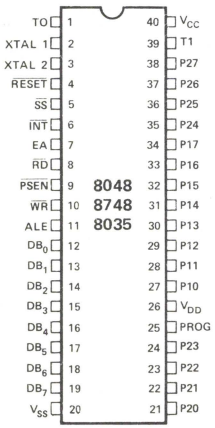
The 8048 contains a 1K x 8 program memory, a 64 x 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to onboard oscillator and clock circuits. For systems that require extra capability, the 8048 can be expanded using standard memories and MCS-80™ (8080A) peripherals. The 8035 is the equivalent of an 8048 without program memory. The 8035L has the RAM power down mode of the 8048 while the 8035 does not.

To reduce development problems to a minimum and provide maximum flexibility, three interchangeable pin-compatible versions of this single component microcomputer exist: the 8748 with user-programmable and erasable EPROM program memory for prototype and preproduction systems, the 8048 with factory-programmed mask ROM program memory for low cost, high volume production, and the 8035 without program memory for use with external program memories.

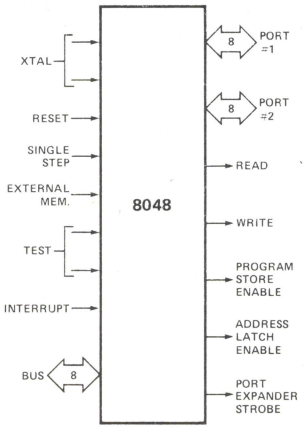
This microprocessor is designed to be an efficient controller as well as an arithmetic processor. The 8048 has extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single byte instructions and no instructions over 2 bytes in length.

MCS-48

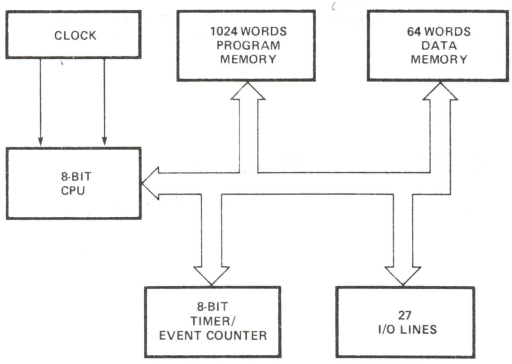
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

PIN DESCRIPTION

Designation	Pin #	Function
V_{SS}	20	Circuit GND potential
V_{DD}	26	Programming power supply; +25V during program, +5V during operation for both ROM and PROM. Low power standby pin in 8048 ROM version.
V_{CC}	40	Main power supply; +5V during operation and programming.
PROG	25	Program pulse (+25V) input pin during 8748 programming. Output strobe for 8243 I/O expander.
P10-P17 Port 1	27-34	8-bit quasi-bidirectional port.
P20-P27 Port 2	21-24 35-38	8-bit quasi-bidirectional port. P20-P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243.
DB_0-DB_7 BUS	12-19	True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of $\overline{PSEN}$. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.
T0	1	Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction. T0 is also used during programming.
T1	39	Input pin testable using the JT1, and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.
$\overline{INT}$	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low)

Designation	Pin #	Function
$\overline{RD}$	8	Output strobe activated during a BUS read. Can be used to enable data onto the bus from an external device. Used as a read strobe to external data memory. (Active low)
$\overline{RESET}$	4	Input which is used to initialize the processor. Also used during PROM programming verification, and power down. (Active low) (Non TTL V_{IH})
$\overline{WR}$	10	Output strobe during a bus write. (Active low) Used as write strobe to external data memory.
ALE	11	Address latch enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory.
$\overline{PSEN}$	9	Program store enable. This output occurs only during a fetch to external program memory. (Active low)
$\overline{SS}$	5	Single step input can be used in conjunction with ALE to "single step" the processor through each instruction. (Active low)
EA	7	External access input which forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification. (Active high)
XTAL1	2	One side of crystal input for internal oscillator. Also input for external source. (Non TTL V_{IH})
XTAL2	3	Other side of crystal input.

INSTRUCTION SET

	Mnemonic	Description	Bytes	Cycle
Accumulator	ADD A, R	Add register to A	1	1
	ADD A, @R	Add data memory to A	1	1
	ADD A, #data	Add immediate to A	2	2
	ADDC A, R	Add register with carry	1	1
	ADDC A, @R	Add data memory with carry	1	1
	ADDC A, #data	Add immediate with carry	2	2
	ANL A, R	And register to A	1	1
	ANL A, @R	And data memory to A	1	1
	ANL A, #data	And immediate to A	2	2
	ORL A, R	Or register to A	1	1
	ORL A, @R	Or data memory to A	1	1
	ORL A, #data	Or immediate to A	2	2
	XRL A, R	Exclusive or register to A	1	1
	XRL A, @R	Exclusive or data memory to A	1	1
	XRL A, #data	Exclusive or immediate to A	2	2
	INC A	Increment A	1	1
	DEC A	Decrement A	1	1
	CLR A	Clear A	1	1
	CPL A	Complement A	1	1
	DA A	Decimal adjust A	1	1
	SWAP A	Swap nibbles of A	1	1
	RL A	Rotate A left	1	1
	RLC A	Rotate A left through carry	1	1
	RR A	Rotate A right	1	1
	RRC A	Rotate A right through carry	1	1
Input/Output	IN A, P	Input port to A	1	2
	OUTL P, A	Output A to port	1	2
	ANL P, #data	And immediate to port	2	2
	ORL P, #data	Or immediate to port	2	2
	INS A, BUS	Input BUS to A	1	2
	OUTL BUS, A	Output A to BUS	1	2
	ANL BUS, #data	And immediate to BUS	2	2
	ORL BUS, #data	Or immediate to BUS	2	2
	MOVD A, P	Input expander port to A	1	2
	MOVD P, A	Output A to expander port	1	2
	ANLD P, A	And A to expander port	1	2
	ORLD P, A	Or A to expander port	1	2
Registers	INC R	Increment register	1	1
	INC @R	Increment data memory	1	1
	DEC R	Decrement register	1	1
Branch	JMP addr	Jump unconditional	2	2
	JMPP @A	Jump indirect	1	2
	DJNZ R, addr	Decrement register and skip	2	2
	JC addr	Jump on carry = 1	2	2
	JNC addr	Jump on carry = 0	2	2
	J Z addr	Jump on A zero	2	2
	JNZ addr	Jump on A not zero	2	2
	JT0 addr	Jump on T0 = 1	2	2
	JNT0 addr	Jump on T0 = 0	2	2
	JT1 addr	Jump on T1 = 1	2	2
	JNT1 addr	Jump on T1 = 0	2	2
	JF0 addr	Jump on F0 = 1	2	2
	JF1 addr	Jump on F1 = 1	2	2
	JTF addr	Jump on timer flag	2	2
	JNI addr	Jump on $\overline{INT}$ = 0	2	2
	JBb addr	Jump on accumulator bit	2	2

	Mnemonic	Description	Bytes	Cycles
Subroutine	CALL	Jump to subroutine	2	2
	RET	Return	1	2
	RETR	Return and restore status	1	2
Flags	CLR C	Clear carry	1	1
	CPL C	Complement carry	1	1
	CLR F0	Clear flag 0	1	1
	CPL F0	Complement flag 0	1	1
	CLR F1	Clear flag 1	1	1
	CPL F1	Complement flag 1	1	1
Data Moves	MOV A, R	Move register to A	1	1
	MOV A, @R	Move data memory to A	1	1
	MOV A, #data	Move immediate to A	2	2
	MOV R, A	Move A to register	1	1
	MOV @R, A	Move A to data memory	1	1
	MOV R, #data	Move immediate to register	2	2
	MOV @R, #data	Move immediate to data memory	2	2
	MOV A, PSW	Move PSW to A	1	1
	MOV PSW, A	Move A to PSW	1	1
	XCH A, R	Exchange A and register	1	1
	XCH A, @R	Exchange A and data memory	1	1
	XCHD A, @R	Exchange nibble of A and register	1	1
	MOVX A, @R	Move external data memory to A	1	2
	MOVX @R, A	Move A to external data memory	1	2
	MOVP A, @A	Move to A from current page	1	2
	MOVP3 A, @A	Move to A from page 3	1	2
Timer/Counter	MOV A, T	Read timer/counter	1	1
	MOV T, A	Load timer/counter	1	1
	STRT T	Start timer	1	1
	STRT CNT	Start counter	1	1
	STOP TCNT	Stop timer/counter	1	1
	EN TCNTI	Enable timer/counter interrupt	1	1
	DIS TCNTI	Disable timer/counter interrupt	1	1
Control	EN I	Enable external interrupt	1	1
	DIS I	Disable external interrupt	1	1
	SEL RB0	Select register bank 0	1	1
	SEL RB1	Select register bank 1	1	1
	SEL MB0	Select memory bank 0	1	1
	SEL MB1	Select memory bank 1	1	1
	ENT0 CLK	Enable clock output on T0	1	1
	NOP	No operation	1	1

Mnemonics copyright Intel Corporation 1976

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... -65°C to +150°C
Voltage On Any Pin With Respect to Ground ..... -0.5V to +7V
Power Dissipation ..... 1.5 Watt

*COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. AND OPERATING CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = V_{DD} = +5V ±10%*, V_{SS} = 0V

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
V_{IL}	Input Low Voltage (All Except XTAL1, XTAL2)	-.5		.8	V	
V_{IH}	Input High Voltage (All Except XTAL1,XTAL2,$\overline{RESET}$)	2.0		V_{CC}	V	
V_{IH1}	Input High Voltage ($\overline{RESET}$,XTAL1)	3.0		V_{CC}	V	
V_{OL}	Output Low Voltage (BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)			.45	V	I_{OL} = 2.0mA
V_{OL1}	Output Low Voltage (All Other Outputs Except PROG)			.45	V	I_{OL} = 1.6mA
V_{OL2}	Output Low Voltage (PROG)			.45	V	I_{OL} = 1.0mA
V_{OH}	Output High Voltage (BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	2.4			V	I_{OH} = 100μA
V_{OH1}	Output High Voltage (All Other Outputs)	2.4			V	I_{OH} = 50μA
I_{IL}	Input Leakage Current (T1, EA, $\overline{INT}$)			±10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
I_{OL}	Output Leakage Current (BUS, T0) (High Impedance State)			-10	μA	$V_{CC} \geq V_{IN} \geq V_{SS}$ +.45
I_{DD}	V_{DD} Supply Current		10	20	mA	
$I_{DD} + I_{CC}$	Total Supply Current		65	135	mA	

A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = V_{DD} = +5V ±10%*, V_{SS} = 0V

Symbol	Parameter	8048/8748 8035/8035L		8748-8 8035-8		Unit	Conditions (Note 1)
		Min.	Max.	Min.	Max.		
t_{LL}	ALE Pulse Width	400		600		ns	
t_{AL}	Address Setup to ALE	150		150		ns	
t_{LA}	Address Hold from ALE	80		80		ns	
t_{CC}	Control Pulse Width ($\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$)	900		1500		ns	
t_{DW}	Data Setup before $\overline{WR}$	500		640		ns	
t_{WD}	Data Hold After $\overline{WR}$	120		120		ns	C_L = 20pF
t_{CY}	Cycle Time	2.5	15.0	4.17	15.0	μs	6 MHz XTAL (3.6MHz XTAL for -8)
t_{DR}	Data Hold	0	200	0	200	ns	
t_{RD}	$\overline{PSEN}$, $\overline{RD}$ to Data In		500		750	ns	
t_{AW}	Address Setup to $\overline{WR}$	230		260		ns	
t_{AD}	Address Setup to Data In		950		1450	ns	
t_{AFC}	Address Float to $\overline{RD}$, $\overline{PSEN}$	0		0		ns	

*Standard 8748 and 8035 ±5%, ±10% available.

Note 1: Control Outputs: C_L = 80 pF
BUS Outputs: C_L = 150 pF, t_{CY} = 25μs

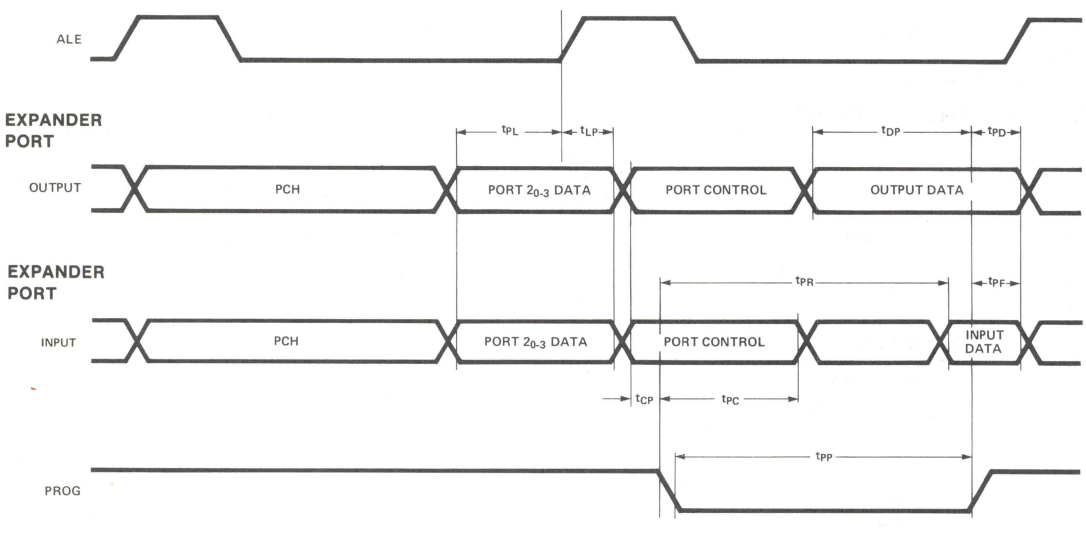
A.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{CP}	Port Control Setup Before Falling Edge of $\overline{PROG}$	110		ns	
t_{PC}	Port Control Hold After Falling Edge of $\overline{PROG}$	140		ns	
t_{PR}	PROG to Time P2 Input Must Be Valid	810		ns	
t_{DP}	Output Data Setup Time	220		ns	
t_{PD}	Output Data Hold Time	65		ns	
t_{PF}	Input Data Hold Time	110		ns	
t_{PP}	$\overline{PROG}$ Pulse Width	1510		ns	
t_{PL}	Port 2 I/O Data Setup	400		ns	
t_{LP}	Port 2 I/O Data Hold	150		ns	

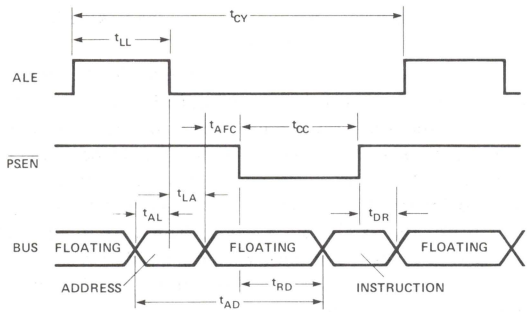
WAVEFORMS

PORT 2 TIMING

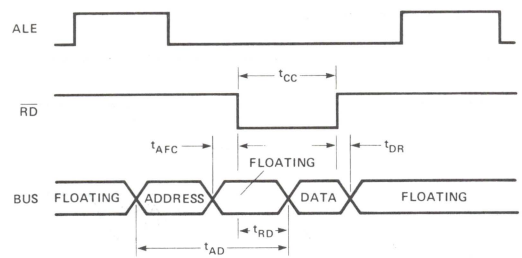


WAVEFORMS

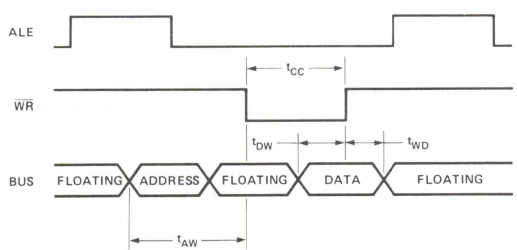
Instruction Fetch From External Program Memory



Read From External Data Memory



Write to External Data Memory



WARNING:

An attempt to program a missocketed 8748 will result in severe damage to the part. An indication of a properly socketed part is the appearance of the ALE clock output. The lack of this clock may be used to disable the programmer.

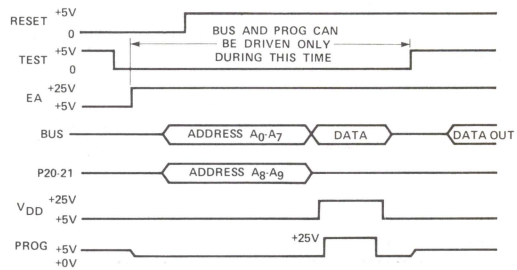
PROGRAMMING, VERIFYING, AND ERASING THE 8748 EPROM

Programming Verification

In brief, the programming process consists of: activating the program mode, applying an address, latching the address, applying data, and applying a programming pulse. Each word is programmed completely before moving on to the next and is followed by a verification step. The following is a list of the pins used for programming and a description of their functions:

Pin	Function
XTAL 1	Clock Input (1 to 6MHz)
Reset	Initialization and Address Latching
Test 0	Selection of Program of Verify Mode
EA	Activation of Program/Verify Modes
BUS	Address and Data Input Data Output During Verify
P20-1	Address Input
V_{DD}	Programming Power Supply
PROG	Program Pulse Input

Programming/Verification Sequence



The Program/Verify sequence is:

1. V_{DD} = 5v, Clock applied or internal oscillator operating, RESET = 0v, TEST 0 = 5v, EA = 5v, BUS and PROG floating.
2. Insert 8748 in programming socket
3. TEST 0 = 0v (select program mode)
4. EA = 25v (activate program mode)
5. Address applied to BUS and P20-1
6. RESET = 5v (latch address)
7. Data applied to BUS
8. V_{DD} = 25v (programming power)
9. PROG = 0v followed by one 50ms pulse to 25v
10. V_{DD} = 5v
11. TEST 0 = 5v (verify mode)
12. Read and verify data on BUS
13. TEST 0 = 0v
14. RESET = 0v and repeat from step 5
15. Programmer should be at conditions of step 1 when 8748 is removed from socket.

Programming Options

The 8748 EPROM can be programmed by either of two Intel products:

1. PROMPT-48 Microcomputer Design Aid, or
2. Universal PROM Programmer (UPP-101 or UPP-102) peripheral of the Intellec® Development System with a UPP-848 Personality Card.

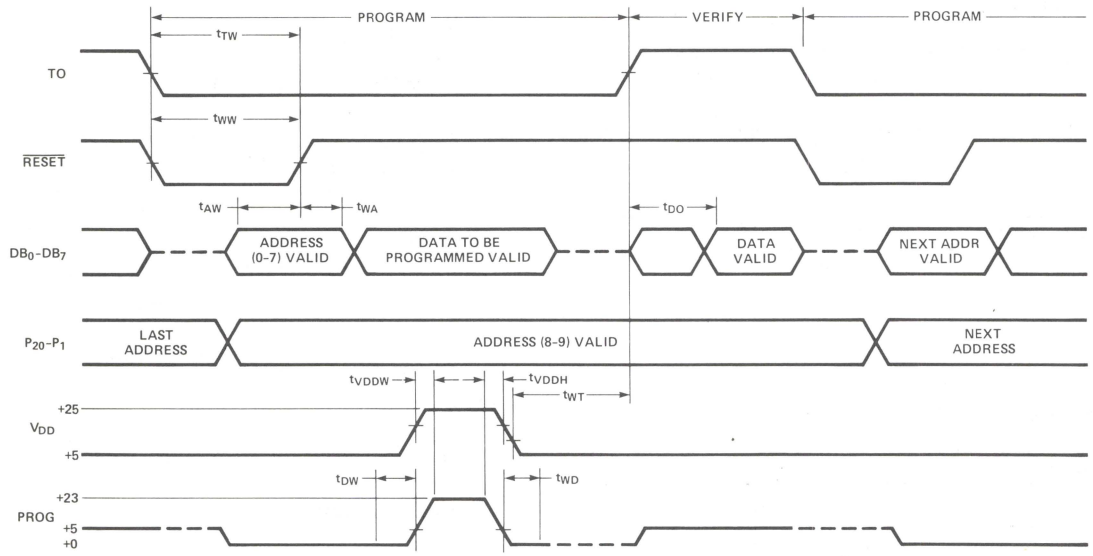
8748 Erasure Characteristics

The erasure characteristics of the 8748 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical 8748 in approximately 3 years while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the 8748 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 8748 window to prevent unintentional erasure.

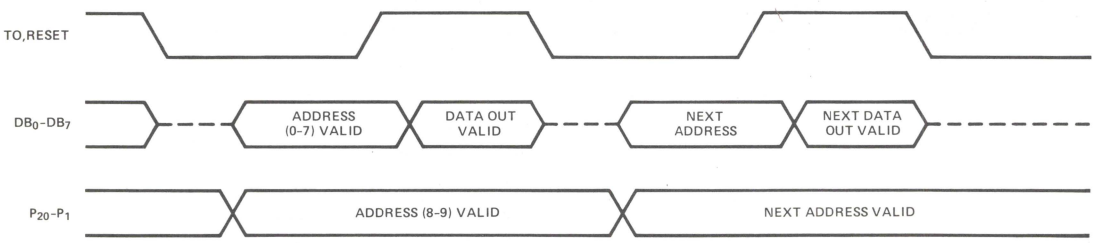
The recommended erasure procedure for the 8748 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000μW/cm^2 power rating. The 8748 should be placed within one inch from the lamp tubes during erasure. Some lamps have a filter on their tubes and this filter should be removed before erasure.

WAVEFORMS

Combination Program/Verify Mode (EPROM's Only)



Verify Mode (ROM/EPROM)



NOTES:
1. PROG MUST FLOAT IF EA IS LOW (i.e., ≠ 25V), OR IF T0 = 5V FOR THE 8741. FOR THE 8041 PROG MUST ALWAYS FLOAT.
2. V_{EAH} FOR 8041 = 11.4V MIN., 12.6V MAX.
3. THE FOLLOWING CONDITIONS MUST BE MET:
   $\overline{CS}$ = TTL '1'
   A0 = TTL '0'
   THIS CAN BE DONE USING 10K RESISTORS TO V_{CC}, V_{SS} RESPECTIVELY.
4. X_1 AND X_2 DRIVEN BY 3 MHz CLOCK WILL GIVE 5 μsec t_{CY}. THIS IS GOOD FOR -8 PARTS AS WELL AS NON -8 PARTS.

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

AC TIMING SPECIFICATION FOR PROGRAMMING

$T_A = 25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{DD} = 25V \pm 1V$

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{AW}	Address Setup Time to $\overline{RESET}$ ↑	4tcy			
t_{WA}	Address Hold Time After $\overline{RESET}$ ↑	4tcy			
t_{DW}	Data in Setup Time to PROG ↑	4tcy			
t_{WD}	Data in Hold Time After PROG ↓	4tcy			
t_{PH}	$\overline{RESET}$ Hold Time to Verify	4tcy			
t_{VDDW}	V_{DD}	4tcy			
t_{VDDH}	V_{DD} Hold Time After PROG ↓	0			
t_{PW}	Program Pulse Width	50	60	MS	
t_{TW}	Test 0 Setup Time for Program Mode	4tcy			
t_{WT}	Test 0 Hold Time After Program Mode	4tcy			
t_{DO}	Test 0 to Data Out Delay		4tcy		
t_{WW}	$\overline{RESET}$ Pulse Width to Latch Address	4tcy			
t_r, t_f	V_{DD} and PROG Rise and Fall Times	0.5	2.0	μs	
t_{CY}	CPU Operation Cycle Time	5.0		μs	
t_{RE}	$\overline{RESET}$ Setup Time Before EA ↑	4tcy			

Note: If Test 0 is high t_{DO} can be triggered by $\overline{RESET}$ ↑.

DC SPECIFICATION FOR PROGRAMMING

$T_A = 25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{DD} = 25V \pm 1V$

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{DOH}	V_{DD} Program Voltage High Level	24.0	26.0	V	
V_{DDL}	V_{DD} Voltage Low Level	4.75	5.25	V	
V_{PH}	PROG Program Voltage High Level	21.5	24.5	V	
V_{PL}	PROG Voltage Low Level		0.2	V	
V_{EAH}	EA Program or Verify Voltage High Level	21.5	24.5	V	
V_{EAL}	EA Voltage Low Level		5.25	V	
I_{DD}	V_{DD} High Voltage Supply Current		30.0	mA	
I_{PROG}	PROG High Voltage Supply Current		16.0	mA	
I_{EA}	EA High Voltage Supply Current		1.0	mA	

8748-4 / 8035-4
SINGLE COMPONENT 8-BIT MICROCOMPUTER

- **8748-4 User Programmable/Erasable EPROM**
- **8035-4 External ROM or EPROM**

- **8-Bit CPU, ROM, RAM, I/O in Single Package**
- **Interchangeable with 8048 ROM Version**
- **Single 5V Supply**
- **2.5 μsec Cycle. All Instructions 1 or 2 Cycles**
- **Over 90 Instructions: 70% Single Byte**
- **1K x 8 EPROM (8748-4)**
  64 x 8 RAM
  27 I/O Lines
- **Interval Timer/Event Counter**
- **Easily Expandable Memory and I/O**
- **Compatible with MCS-80™/MCS-85™ Peripherals**
- **Single Level Interrupt**

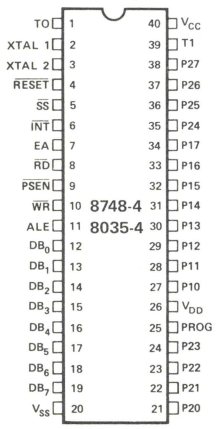
The Intel® 8748-4/8035-4 is a totally self-sufficient 8-bit parallel computer fabricated on a single silicon chip using Intel's N-channel silicon gate MOS process. The 8748-4 and the 8035-4 are the equivalent of the 8748 and 8035 except in their ability to interface to an 8243 I/O Expander device. The Standard 8748/8035 can input or output from the 8243. The 8748-8748-4/8035-4 can use the 8243 as an output expander only.

The 8748-4 contains a 1K x 8 program memory, a 64 x 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to on-board oscillator and clock circuits. For systems that require extra capability, the 8748-4 can be expanded using standard memories and MCS-80™ (8080A) peripherals. The 8035-4 is the equivalent of an 8748-4 without program memory.

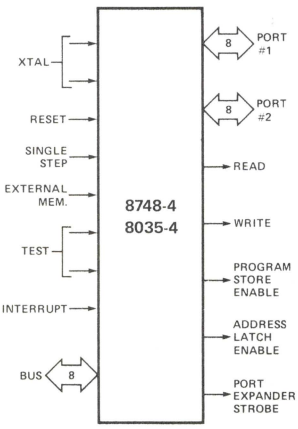
To reduce development problems to a minimum and provide maximum flexibility, three interchangeable pin-compatible versions of this single component microcomputer exist: the 8748-4 with user-programmable and eraseable EPROM program memory for prototype and preproduction systems, the 8048 with factory-programmed mask ROM program memory for low cost, high-volume production, and the 8035-4 without program memory for use with external program memories.

This microprocessor is designed to be an efficient controller as well as an arithmetic processor. The 8048 has extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single-byte instructions and no instructions over two bytes in length.

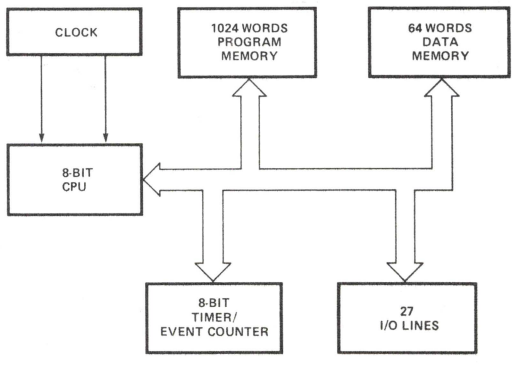
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN DESCRIPTION

Designation	Pin #	Function
V_{SS}	20	Circuit GND potential
V_{DD}	26	Programming power supply; +25V during program, +5V during operation for both ROM and PROM.
V_{CC}	40	Main power supply; +5V during operation and programming.
PROG	25	Program pulse (+25V) input pin during 8748 programming.
		Output strobe for 8243 I/O expander.
P10-P17 Port 1	27-34	8-bit quasi-bidirectional port.
P20-P27 Port 2	21-24 35-38	8-bit quasi-bidirectional port. P20-P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243.
D0-D7 BUS	12-19	True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of PSEN. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.
T0	1	Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction. T0 is also used during programming.
T1	39	Input pin testable using the JT1 and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.
$\overline{INT}$	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low)

Designation	Pin #	Function
$\overline{RD}$	8	Output strobe activated during a BUS read. Can be used to enable data onto the BUS from an external device. Used as a Read Strobe to External Data Memory. (Active low)
$\overline{RESET}$	4	Input which is used to initialize the processor. Also used during PROM programming verification, and power down. (Active low)
$\overline{WR}$	10	Output strobe during a BUS write. (Active low)(Non TTL V_{IH}) Used as write strobe to External Data Memory.
ALE	11	Address Latch Enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory.
$\overline{PSEN}$	9	Program Store Enable. This output occurs only during a fetch to external program memory. (Active low)
$\overline{SS}$	5	Single step input can be used in conjunction with ALE to "single step" the processor through each instruction. (Active low)
EA	7	External access input which forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification. (Active high)
XTAL1	2	One side of crystal input for internal oscillator. Also input for external source. (Not TTL Compatible)
XTAL2	2	Other side of crystal input.

INSTRUCTION SET

	Mnemonic	Description	Bytes	Cycle
Accumulator	ADD A, R	Add register to A	1	1
	ADD A, @R	Add data memory to A	1	1
	ADD A, #data	Add immediate to A	2	2
	ADDC A, R	Add register with carry	1	1
	ADDC A, @R	Add data memory with carry	1	1
	ADDC A, #data	Add immediate with carry	2	2
	ANL A, R	And register to A	1	1
	ANL A, @R	And data memory to A	1	1
	ANL A, #data	And immediate to A	2	2
	ORL A, R	Or register to A	1	1
	ORL A, @R	Or data memory to A	1	1
	ORL A, #data	Or immediate to A	2	2
	XRL A, R	Exclusive Or register to A	1	1
	XRL A, @R	Exclusive or data memory to A	1	1
	XRL A, #data	Exclusive or immediate to A	2	2
	INC A	Increment A	1	1
	DEC A	Decrement A	1	1
	CLR A	Clear A	1	1
	CPL A	Complement A	1	1
	DA A	Decimal adjust A	1	1
	SWAP A	Swap nibbles of A	1	1
	RL A	Rotate A left	1	1
	RLC A	Rotate A left through carry	1	1
	RR A	Rotate A right	1	1
	RRC A	Rotate A right through carry	1	1
Input/Output	IN A, P	Input port to A	1	2
	OUTL P, A	Output A to port	1	2
	ANL P, #data	And immediate to port	2	2
	ORL P, #data	Or immediate to port	2	2
	INS A, BUS	Input BUS to A	1	2
	OUTL BUS, A	Output A to BUS	1	2
	ANL BUS, #data	And immediate to BUS	2	2
	ORL BUS, #data	Or immediate to BUS	2	2
	MOVD P, A	Output A to expander port	1	2
	ANLD P, A	And A to expander port	1	2
	ORLD P, A	Or A to expander port	1	2
Registers	INC R	Increment register	1	1
	INC @R	Increment data memory	1	1
	DEC R	Decrement register	1	1
Branch	JMP addr	Jump unconditional	2	2
	JMPP @A	Jump indirect	1	2
	DJNZ R, addr	Decrement register and skip	2	2
	JC addr	Jump on carry = 1	2	2
	JNC addr	Jump on carry = 0	2	2
	J Z addr	Jump on A zero	2	2
	JNZ addr	Jump on A not zero	2	2
	JT0 addr	Jump on T0 = 1	2	2
	JNT0 addr	Jump on T0 = 0	2	2
	JT1 addr	Jump on T1 = 1	2	2
	JNT1 addr	Jump on T1 = 0	2	2
	JF0 addr	Jump on F0 = 1	2	2
	JF1 addr	Jump on F1 = 1	2	2
	JTF addr	Jump on timer flag	2	2
	JNI addr	Jump on $\overline{INT}$ = 0	2	2
	JBb addr	Jump on accumulator bit	2	2

	Mnemonic	Description	Bytes	Cycles
Subroutine	CALL	Jump to subroutine	2	2
	RET	Return	1	2
	RETR	Return and restore status	1	2
Flags	CLR C	Clear carry	1	1
	CPL C	Complement carry	1	1
	CLR F0	Clear flag 0	1	1
	CPL F0	Complement flag 0	1	1
	CLR F1	Clear flag 1	1	1
	CPL F1	Complement flag 1	1	1
Data Moves	MOV A, R	Move register to A	1	1
	MOV A, @R	Move data memory to A	1	1
	MOV A, #data	Move immediate to A	2	2
	MOV R, A	Move A to register	1	1
	MOV @R, A	Move A to data memory	1	1
	MOV R, #data	Move immediate to register	2	2
	MOV @R, #data	Move immediate to data memory	2	2
	MOV A, PSW	Move PSW to A	1	1
	MOV PSW, A	Move A to PSW	1	1
	XCH A, R	Exchange A and register	1	1
	XCH A, @R	Exchange A and data memory	1	1
	XCHD A, @R	Exchange nibble of A and register	1	1
	MOVX A, @R	Move external data memory to A	1	2
	MOVX @R, A	Move A to external data memory	1	2
	MOVP A, @A	Move to A from current page	1	2
	MOVP3 A, @A	Move to A from page 3	1	2
Timer/Counter	MOV A, T	Read timer/counter	1	1
	MOV T, A	Load timer/counter	1	1
	STRT T	Start timer	1	1
	STRT CNT	Start counter	1	1
	STOP TCNT	Stop timer/counter	1	1
	EN TCNTI	Enable timer/counter interrupt	1	1
	DIS TCNTI	Disable timer/counter interrupt	1	1
Control	EN I	Enable external interrupt	1	1
	DIS I	Disable external interrupt	1	1
	SEL RB0	Select register bank 0	1	1
	SEL RB1	Select register bank 1	1	1
	SEL MB0	Select memory bank 0	1	1
	SEL MB1	Select memory bank 1	1	1
	ENT0 CLK	Enable clock output on T0	1	1
	NOP	No operation	1	1

Mnemonics copyright Intel Corporation 1976, 1977

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... -65°C to +150°C
Voltage On Any Pin With Respect to Ground ..... -0.5V to +7V
Power Dissipation ..... 1.5 Watt

*COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. AND OPERATING CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = V_{DD} = +5V ±10%*, V_{SS} = 0V

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
V_{IL}	Input Low Voltage (All Except XTAL1, XTAL2)	-.5		.8	V	
V_{IH}	Input High Voltage (All Except XTAL1,XTAL2,$\overline{RESET}$)	2.0		V_{CC}	V	
V_{IH1}	Input High Voltage ($\overline{RESET}$,XTAL1)	3.0		V_{CC}	V	
V_{OL}	Output Low Voltage (BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)			.45	V	I_{OL} = 2.0mA
V_{OL1}	Output Low Voltage (All Other Outputs Except PROG)			.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage (BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	2.4			V	I_{OH} = 100μA
V_{OH1}	Output High Voltage (All Other Outputs)	2.4			V	I_{OH} = 50μA
I_{IL}	Input Leakage Current (T1, EA, $\overline{INT}$)			±10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
I_{OL}	Output Leakage Current (Bus, T0) (High Impedance State)			-10	μA	$V_{CC} \geq V_{IN} \geq V_{SS}$ +.45
I_{DD}	Power Down Supply Current		10	20	mA	T_A = 25°C
$I_{DD} + I_{CC}$	Total Supply Current		65	135	mA	T_A = 25°C

A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = V_{DD} = +5V ±5%*, V_{SS} = 0V

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{LL}	ALE Pulse Width	400		ns	
t_{AL}	Address Setup to ALE	150		ns	
t_{LA}	Address Hold from ALE	80		ns	
t_{CC}	Control Pulse Width ($\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$)	900		ns	
t_{DW}	Data Setup Before $\overline{WR}$	500		ns	
t_{WD}	Data Hold After $\overline{WR}$	120		ns	C_L = 20 pF
t_{CY}	Cycle Time	2.5	15.0	μs	6 MHz XTAL
t_{DR}	Data Hold	0	200	ns	
t_{RD}	$\overline{PSEN}$, $\overline{RD}$ to Data In		500	ns	
t_{AW}	Address Setup to $\overline{WR}$	230		ns	
t_{AD}	Address Setup to Data In		950	ns	
t_{AFC}	Address Float to $\overline{RD}$, $\overline{PSEN}$	0		ns	

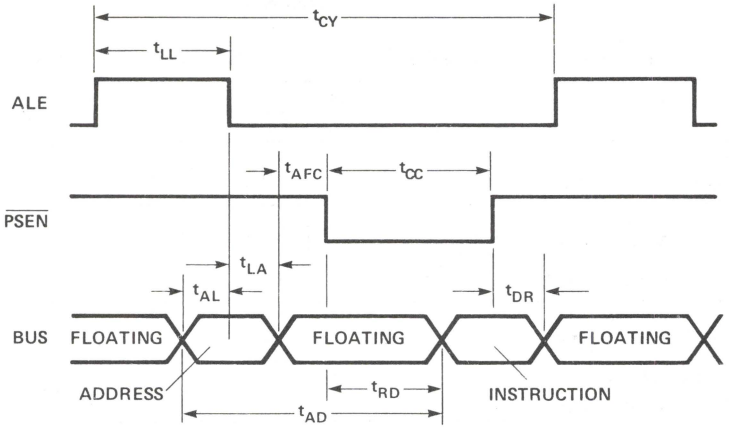
A.C. TEST CONDITIONS

Control Outputs: C_L = 80 pF
BUS Outputs: C_L = 150 pF
t_{CY} = 2.5μs

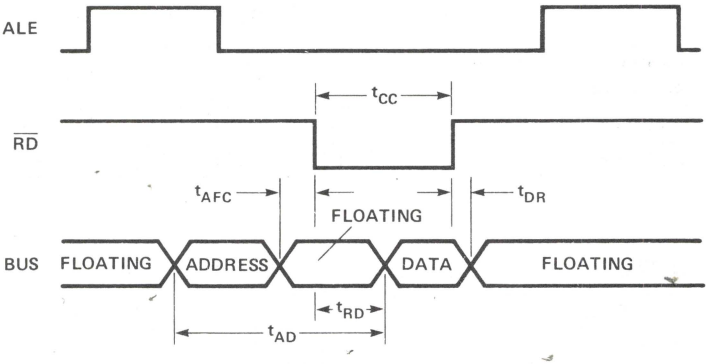
*Standard 8748 and 8035 ±5%, ±10% available.

WAVEFORMS

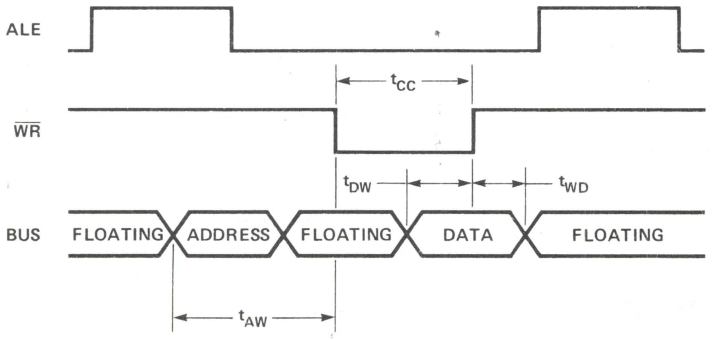
Instruction Fetch From External Program Memory



Read From External Data Memory



Write To External Data Memory



PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

8049/8039
SINGLE COMPONENT 8-BIT MICROCOMPUTER

• 8049 Mask Programmable ROM
• 8039 External ROM or EPROM

- **8-Bit CPU, ROM, RAM, I/O in Single Package**
- **Single 5V ±10% Supply**
- **2.5 μsec Cycle; All Instructions 1 or 2 Cycles**
- **Over 90 Instructions: 70% Single Byte**
- **Pin Compatible with 8048/8748**
- **2K x 8 ROM**
  128 x 8 RAM
  27 I/O Lines
- **Interval Timer/Event Counter**
- **Easily Expandable Memory and I/O**
- **Compatible with MCS-80/85™ Peripherals**
- **Single Level Interrupt**

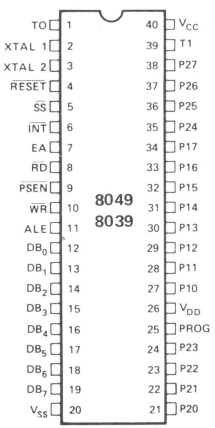
The Intel® 8049/8039 is a totally self-sufficient 8-bit parallel computer fabricated on a single silicon chip using Intel's N-channel silicon gate MOS process.

The 8049 contains a 2K x 8 program memory, a 128 x 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to on board oscillator and clock circuits. For systems that require extra capability, the 8049 can be expanded using standard memories and MCS-80™/MCS-85™ peripherals. The 8039 is the equivalent to an 8049 without program memory.

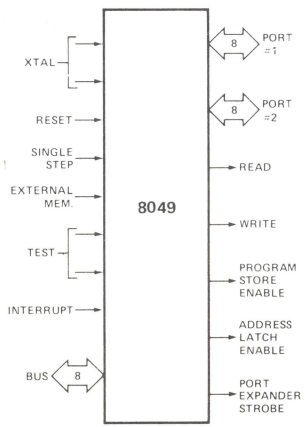
To reduce development problems to a minimum and provide maximum flexibility, two interchangeable pin-compatible versions of this single component microcomputer exist: the 8049 with factory-programmed mask ROM program memory for low-cost high volume production, and the 8039 without program memory for use with external program memories in prototype and preproduction systems.

This microprocessor is designed to be an efficient controller as well as an arithmetic processor. The 8049 has extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single byte instructions and no instructions over two bytes in length.

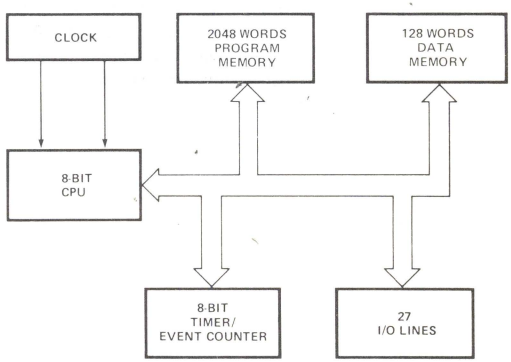
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



MCS-48

PIN DESCRIPTION

Designation	Pin #	Function
V_{SS}	20	Circuit GND potential.
V_{DD}	26	+5V during operation. Low power standby pin.
V_{CC}	40	Main power supply; +5V during operation.
PROG	25	Output strobe for 8243 I/O expander.
P10-P17 Port 1	27-34	8-bit quasi-bidirectional port.
P20-P27 Port 2	21-24 35-38	8-bit quasi-bidirectional port. P20-P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243.
D0-D7 BUS	12-19	True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of PSEN. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.
T0	1	Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction.
T1	39	Input pin testable using the JT1, and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.
$\overline{INT}$	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low)
$\overline{RD}$	8	Output strobe activated during a BUS read. Can be used to enable data onto the BUS from an external device. Used as a Read Strobe to External Data Memory. (Active low)
$\overline{RESET}$	4	Input which is used to initialize the processor. Also used during verification, and power down. (Active low)
$\overline{WR}$	10	Output strobe during a BUS write. (Active low)(Non TTL V_{IH}) Used as write strobe to External Data Memory.
ALE	11	Address Latch Enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory.
$\overline{PSEN}$	9	Program Store Enable. This output occurs only during a fetch to external program memory. (Active low)
$\overline{SS}$	5	Single step input can be used in conjunction with ALE to "single step" the processor through each instruction. (Active low)
EA	7	External Access input which forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification. (Active high)
XTAL1	2	One side of crystal input for internal oscillator. Also input for external source. (Not TTL Compatible)
XTAL2	3	Other side of crystal input.

INSTRUCTION SET

	Mnemonic	Description	Bytes	Cycle
Accumulator	ADD A, R	Add register to A	1	1
	ADD A, @R	Add data memory to A	1	1
	ADD A, #data	Add immediate to A	2	2
	ADDC A, R	Add register with carry	1	1
	ADDC A, @R	Add data memory with carry	1	1
	ADDC A, #data	Add immediate with carry	2	2
	ANL A, R	And register to A	1	1
	ANL A, @R	And data memory to A	1	1
	ANL A, #data	And immediate to A	2	2
	ORL A, R	Or register to A	1	1
	ORL A, @R	Or data memory to A	1	1
	ORL A, #data	Or immediate to A	2	2
	XRL A, R	Exclusive Or register to A	1	1
	XRL A, @R	Exclusive or data memory to A	1	1
	XRL A, #data	Exclusive or immediate to A	2	2
	INC A	Increment A	1	1
	DEC A	Decrement A	1	1
	CLR A	Clear A	1	1
	CPL A	Complement A	1	1
	DA A	Decimal Adjust A	1	1
	SWAP A	Swap nibbles of A	1	1
	RL A	Rotate A left	1	1
	RLC A	Rotate A left through carry	1	1
	RR A	Rotate A right	1	1
	RRC A	Rotate A right through carry	1	1
Input/Output	IN A, P	Input port to A	1	2
	OUTL P, A	Output A to port	1	2
	ANL P, #data	And immediate to port	2	2
	ORL P, #data	Or immediate to port	2	2
	INS A, BUS	Input BUS to A	1	2
	OUTL BUS, A	Output A to BUS	1	2
	ANL BUS, #data	And immediate to BUS	2	2
	ORL BUS, #data	Or immediate to BUS	2	2
	MOVD A, P	Input Expander port to A	1	2
	MOVD P, A	Output A to Expander port	1	2
	ANLD P, A	And A to Expander port	1	2
	ORLD P, A	Or A to Expander port	1	2
Registers	INC R	Increment register	1	1
	INC @R	Increment data memory	1	1
	DEC R	Decrement register	1	1
Branch	JMP addr	Jump unconditional	2	2
	JMPP @A	Jump indirect	1	2
	DJNZ R, addr	Decrement register and skip	2	2
	JC addr	Jump on Carry = 1	2	2
	JNC addr	Jump on Carry = 0	2	2
	J Z addr	Jump on A Zero	2	2
	JNZ addr	Jump on A not Zero	2	2
	JT0 addr	Jump on T0 = 1	2	2
	JNT0 addr	Jump on T0 = 0	2	2
	JT1 addr	Jump on T1 = 1	2	2
	JNT1 addr	Jump on T1 = 0	2	2
	JF0 addr	Jump on F0 = 1	2	2
	JF1 addr	Jump on F1 = 1	2	2
	JTF addr	Jump on timer flag	2	2
	JNI addr	Jump on $\overline{INT}$ = 0	2	2
	JBb addr	Jump on Accumulator Bit	2	2

	Mnemonic	Description	Bytes	Cycles
Subroutine	CALL	Jump to subroutine	2	2
	RET	Return	1	2
	RETR	Return and restore status	1	2
Flags	CLR C	Clear Carry	1	1
	CPL C	Complement Carry	1	1
	CLR F0	Clear Flag 0	1	1
	CPL F0	Complement Flag 0	1	1
	CLR F1	Clear Flag 1	1	1
	CPL F1	Complement Flag 1	1	1
Data Moves	MOV A, R	Move register to A	1	1
	MOV A, @R	Move data memory to A	1	1
	MOV A, #data	Move immediate to A	2	2
	MOV R, A	Move A to register	1	1
	MOV @R, A	Move A to data memory	1	1
	MOV R, #data	Move immediate to register	2	2
	MOV @R, #data	Move immediate to data memory	2	2
	MOV A, PSW	Move PSW to A	1	1
	MOV PSW, A	Move A to PSW	1	1
	XCH A, R	Exchange A and register	1	1
	XCH A, @R	Exchange A and data memory	1	1
	XCHD A, @R	Exchange nibble of A and register	1	1
	MOVX A, @R	Move external data memory to A	1	2
	MOVX @R, A	Move A to external data memory	1	2
	MOVP A, @A	Move to A from current page	1	2
	MOVP3 A, @A	Move to A from Page 3	1	2
Timer/Counter	MOV A, T	Read Timer/Counter	1	1
	MOV T, A	Load Timer/Counter	1	1
	STRT T	Start Timer	1	1
	STRT CNT	Start Counter	1	1
	STOP TCNT	Stop Timer/Counter	1	1
	EN TCNTI	Enable Timer/Counter Interrupt	1	1
	DIS TCNTI	Disable Timer/Counter Interrupt	1	1
Control	EN I	Enable external interrupt	1	1
	DIS I	Disable external interrupt	1	1
	SEL RB0	Select register bank 0	1	1
	SEL RB1	Select register bank 1	1	1
	SEL MB0	Select memory bank 0	1	1
	SEL MB1	Select memory bank 1	1	1
	ENT0 CLK	Enable Clock output on T0	1	1
	NOP	No Operation	1	1

Mnemonics copyright Intel Corporation 1976, 1977

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin With Respect to Ground ..... -0.5V to +7V
Power Dissipation ..... 1.5 Watt

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = V_{DD} = +5V \pm 10\%$, $V_{SS} = 0V$

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
V_{IL}	Input Low Voltage (All Except XTAL1, XTAL2)	-0.5		0.8	V	
V_{IH}	Input High Voltage (All Except XTAL1, XTAL2, $\overline{RESET}$)	2.0		V_{CC}	V	
V_{IH1}	Input High Voltage ($\overline{RESET}$, XTAL1)	3.0		V_{CC}	V	
V_{OL}	Output Low Voltage (BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)			0.45	V	$I_{OL} = 2.0mA$
V_{OL1}	Output Low Voltage (All Other Outputs Except PROG)			0.45	V	$I_{OL} = 1.6mA$
V_{OH}	Output High Voltage (BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	2.4			V	$I_{OH} = 100\mu A$
V_{OH1}	Output High Voltage (All Other Outputs)	2.4			V	$I_{OH} = 50\mu A$
I_{IL}	Input Leakage Current (T1, EA, $\overline{INT}$)			±10	μA	$V_{SS} \leqslant V_{IN} \leqslant V_{CC}$
I_{OL}	Output Leakage Current (Bus, T0) (High Impedance State)			-10	μA	$V_{CC} \geqslant V_{IN} \geqslant V_{SS} + 0.45$
I_{DD}	Power Down Supply Current		20	50	mA	$T_A = 25°C$
$I_{DD}+I_{CC}$	Total Supply Current		75	140	mA	$T_A = 25°C$

A.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = V_{DD} = +5V \pm 10\%$, $V_{SS} = 0V$

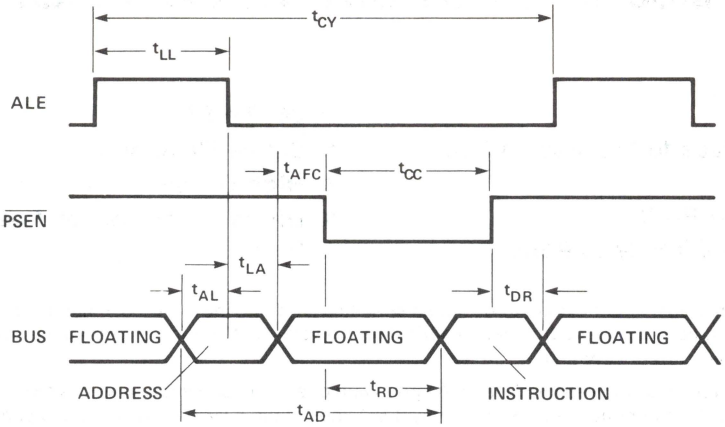
Symbol	Parameter	8049/8039		Unit	Conditions
		Min.	Max.		
t_{LL}	ALE Pulse Width	400		ns	
t_{AL}	Address Setup to ALE	150		ns	
t_{LA}	Address Hold from ALE	80		ns	
t_{CC}	Control Pulse Width ($\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$)	900		ns	
t_{DW}	Data Set-Up Before $\overline{WR}$	500		ns	
t_{WD}	Data Hold After $\overline{WR}$	120		ns	$C_L = 20$ pF
t_{CY}	Cycle Time	2.5	15.0	μs	6 MHz XTAL
t_{DR}	Data Hold	0	200	ns	
t_{RD}	$\overline{PSEN}$, $\overline{RD}$ to Data In		500	ns	
t_{AW}	Address Setup to $\overline{WR}$	230		ns	
t_{AD}	Address Setup to Data In		950	ns	
t_{AFC}	Address Float to $\overline{RD}$, $\overline{PSEN}$	0		ns	

A.C. TEST CONDITIONS

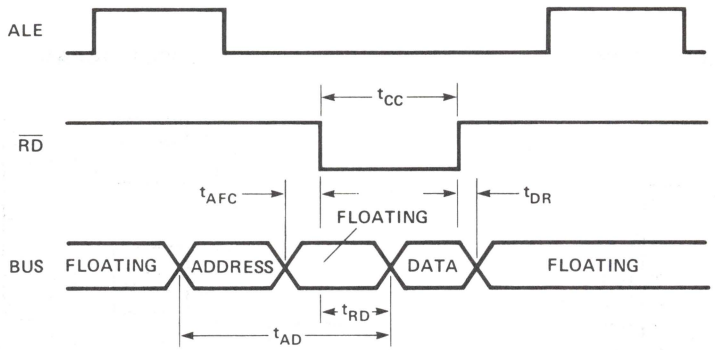
Control Outputs: $C_L = 80$ pF BUS Outputs: $C_L = 150$ pF $t_{CY} = 2.5\mu s$

WAVEFORMS

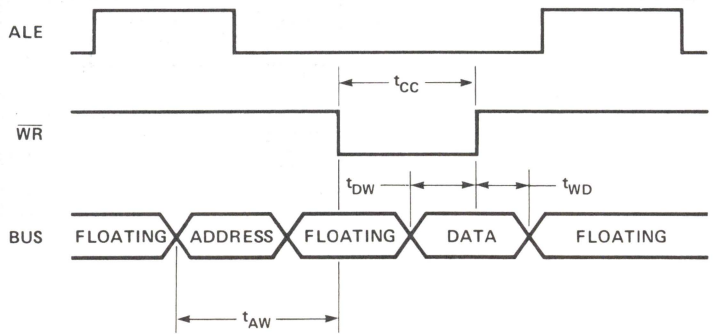
Instruction Fetch From External Program Memory



Read From External Data Memory



Write To External Data Memory



PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

8243
MCS-48™ INPUT/OUTPUT EXPANDER

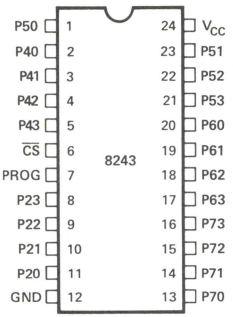
- **Low Cost**
- **Simple Interface to MCS-48™ Microcomputers**
- **Four 4-Bit I/O Ports**
- **AND and OR Directly to Ports**
- **24-Pin DIP**
- **Single 5V Supply**
- **High Output Drive**
- **Direct Extension of Resident 8048 I/O Ports**

The Intel® 8243 is an input/output expander designed specifically to provide a low cost means of I/O expansion for the MCS-48™ family of single chip microcomputers. Fabricated in 5 volts NMOS, the 8243 combines low cost, single supply voltage and high drive current capability.

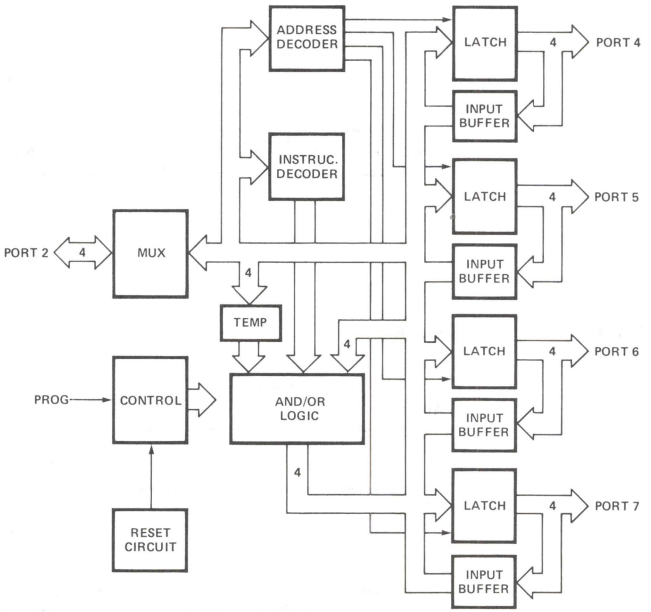
The 8243 consists of four 4-bit bidirectional static I/O ports and one 4-bit port which serves as an interface to the MCS-48 microcomputers. The 4-bit interface requires that only 4 I/O lines of the 8048 be used for I/O expansion, and also allows multiple 8243's to be added to the same bus.

The I/O ports of the 8243 serve as a direct extension of the resident I/O facilities of the MCS-48 microcomputers and are accessed by their own MOV, ANL, and ORL instructions.

PIN CONFIGURATION



BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

General Operation

The 8243 contains four 4-bit I/O ports which serve as an extension of the on-chip I/O and are addressed as ports 4-7. The following operations may be performed on these ports:

- Transfer Accumulator to Port.
- Transfer Port to Accumulator.
- AND Accumulator to Port.
- OR Accumulator to Port.

All communication between the 8048 and the 8243 occurs over Port 2 (P20-P23) with timing provided by an output pulse on the PROG pin of the processor. Each transfer consists of two 4-bit nibbles:

The first containing the "op code" and port address and the second containing the actual 4-bits of data.

A high to low transition of the PROG line indicates that address is present while a low to high transition indicates the presence of data. Additional 8243's may be added to the 4-bit bus and chip selected using additional output lines from the 8048/8748/8035.

Power On Initialization

Initial application of power to the device forces input/output ports 4, 5, 6, and 7 to the tri-state and port 2 to the input mode. The PROG pin may be either high or low when power is applied. The first high to low transition of PROG causes device to exit power on mode. The power on sequence is initiated if V_{CC} drops below 1V.

P21	P20	Address Code	P23	P22	Instruction Code
0	0	Port 4	0	0	Read
0	1	Port 5	0	1	Write
1	0	Port 6	1	0	ORLD
1	1	Port 7	1	1	ANLD

Write Modes

The device has three write modes. MOVD Pi, A directly writes new data into the selected port and old data is lost. ORLD Pi,A takes new data, OR's it with the old data and then writes it to the port. ANLD Pi,A takes new data AND's it with the old data and then writes it to the port. Operation code and port address are latched from the input port 2 on the high to low transition of the PROG pin. On the low to high transition of PROG data on port 2 is transferred to the logic block of the specified output port.

After the logic manipulation is performed, the data is latched and outputed. The old data remains latched until new valid outputs are entered.

Read Mode

The device has one read mode. The operation code and port address are latched from the input port 2 on the high to low transition of the PROG pin. As soon as the read operation and port address are decoded, the appropriate outputs are tri-stated, and the input buffers switched on. The read operation is terminated by a low to high transition of the PROG pin. The port (4, 5, 6 or 7) that was selected is switched to the tri-stated mode while port 2 is returned to the input mode.

Normally, a port will be in an output (write mode) or input (read mode). If modes are changed during operation, the first read following a write should be ignored; all following reads are valid. This is to allow the external driver on the port to settle after the first read instruction removes the low impedance drive from the 8243 output. A read of any port will leave that port in a high impedance state.

Sink Capability

The 8243 can sink 5 mA @ .4V on each of its 16 I/O lines simultaneously. If, however, all lines are not sinking simultaneously or all lines are not fully loaded, the drive capability of any individual line increases as is shown by the accompanying curve.

For example, if only 5 of the 16 lines are to sink current at one time, the curve shows that each of those 5 lines is capable of sinking 10 mA @ .4V (if any lines are to sink 10 mA the total I_{OL} must not exceed 50 mA or five 10 mA loads).

Example: How many pins can drive 5 TTL loads (1.6 mA) assuming remaining pins are unloaded?

I_{OL} = 5 x 1.6 mA = 8 mA
ϵI_{OL} = 70 mA from curve
pins = 70 mA ÷ 8 mA/pin = 8.75 = 8

In this case, 8 lines can sink 8 mA for a total of 64 mA. This leaves 6 mA sink current capability which can be divided in any way among the remaining 8 I/O lines of the 8243.

Example: This example shows how the use of the 20 mA sink capability of Port 7 affects the sinking capability of the other I/O lines.

An 8243 will drive the following loads simultaneously.

2 loads — 20 mA @ 1V (port 7 only)
8 loads — 5 mA @ .4V
6 loads — 3.2 mA @ .4V
Is this within the specified limits?

ϵI_{OL} = (2 x 20) + (8 x 5) + (6 x 3.2) = 99.2 mA from the curve: for I_{OL} = 5 mA, ϵI_{OL} = 100 mA since 99.2 mA < 100 mA the loads are within specified limits.

Although the 20 mA @ 1V loads are used in calculating ϵI_{OL}, it is the largest current required @ .4V which determines the maximum allowable ϵI_{OL}.

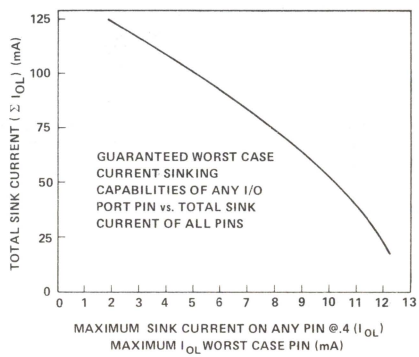


Figure 1. Sink Capability

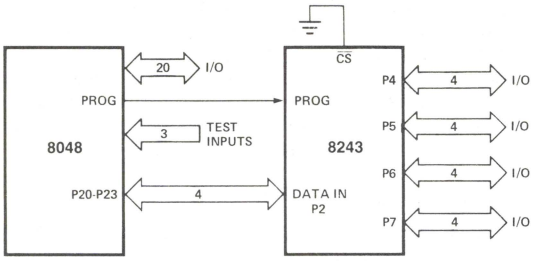


Figure 2. Expander Interface

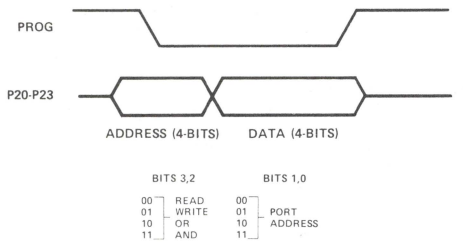


Figure 3. Output Expander Timing

PIN DESCRIPTION

Symbol	Pin No.	Function
PROG	7	Clock Input. A high to low transition on PROG signifies that address and control are available on P20-P23, and a low to high transition signifies that data is available on P20-23.
$\overline{CS}$	6	Chip Select Input. A high on CS inhibits any change of output or internal status.
P20-P23	11-8	Four-bit bidirectional port contains the address and control bits on a high to low transition of PROG. During a low to high transition contains the data for a selected output port if a write operation, or the data from a selected port before the low to high transition if a read operation.
GND	12	0V supply.
P40-P43 P50-P53 P60-P63 P70-P73	2-5 1,23-21 20-17 13-16	Four-bit bidirectional I/O ports. May be programmed to be input (during read), low impedance latched output (after write) or a tri-state (after read). Data on pins P20-23 may be directly written. ANDed or ORed with previous data.
V_{CC}	24	+5V supply.

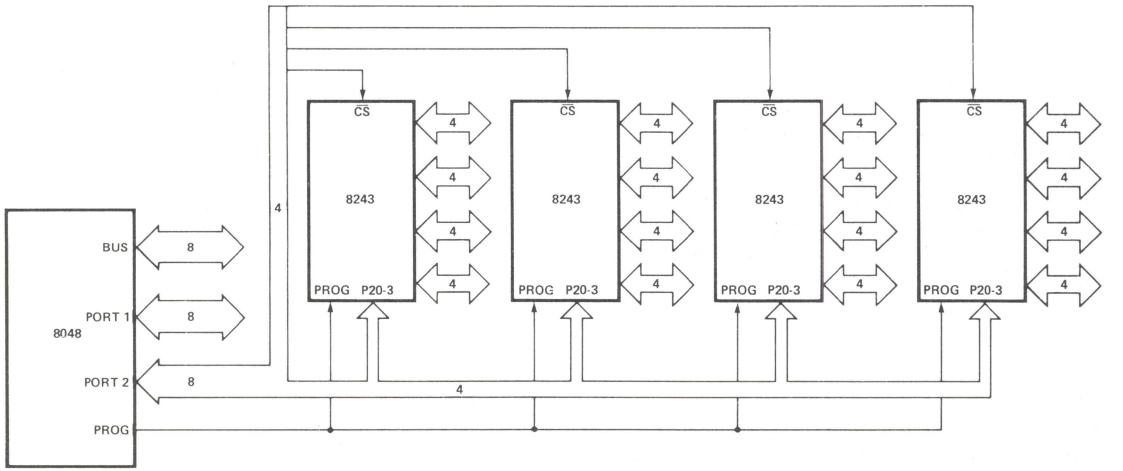


Figure 4. Using Multiple 8243's

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . 0°C to 70°C
Storage Temperature . . . . . –65°C to +150°C
Voltage on Any Pin
With Respect to Ground . . . . . –0.5V to +7V
Power Dissipation . . . . . 1 Watt

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}+0.5	V	
V_{OL1}	Output Low Voltage Ports 4-7			0.45	V	I_{OL} = 5 mA*
V_{OL2}	Output Low Voltage Port 7			1	V	I_{OL} = 20 mA
V_{OH1}	Output High Voltage Ports 4-7	2.4			V	I_{OH}= 240μA
I_{IL1}	Input Leakage Ports 4-7	-10		20	μA	V_{in} = V_{CC} to 0V
I_{IL2}	Input Leakage Port 2, CS, PROG	-10		10	μA	V_{in} = V_{CC} to 0V
V_{OL3}	Output Low Voltage Port 2			.45	V	I_{OL}= 0.6 mA
I_{CC}	V_{CC} Supply Current		10	20	mA	
V_{OH2}	Output Voltage Port 2	2.4				I_{OH}= 100μA
I_{OL}	Sum of all I_{OL} from 16 Outputs			100	mA	5 mA Each Pin

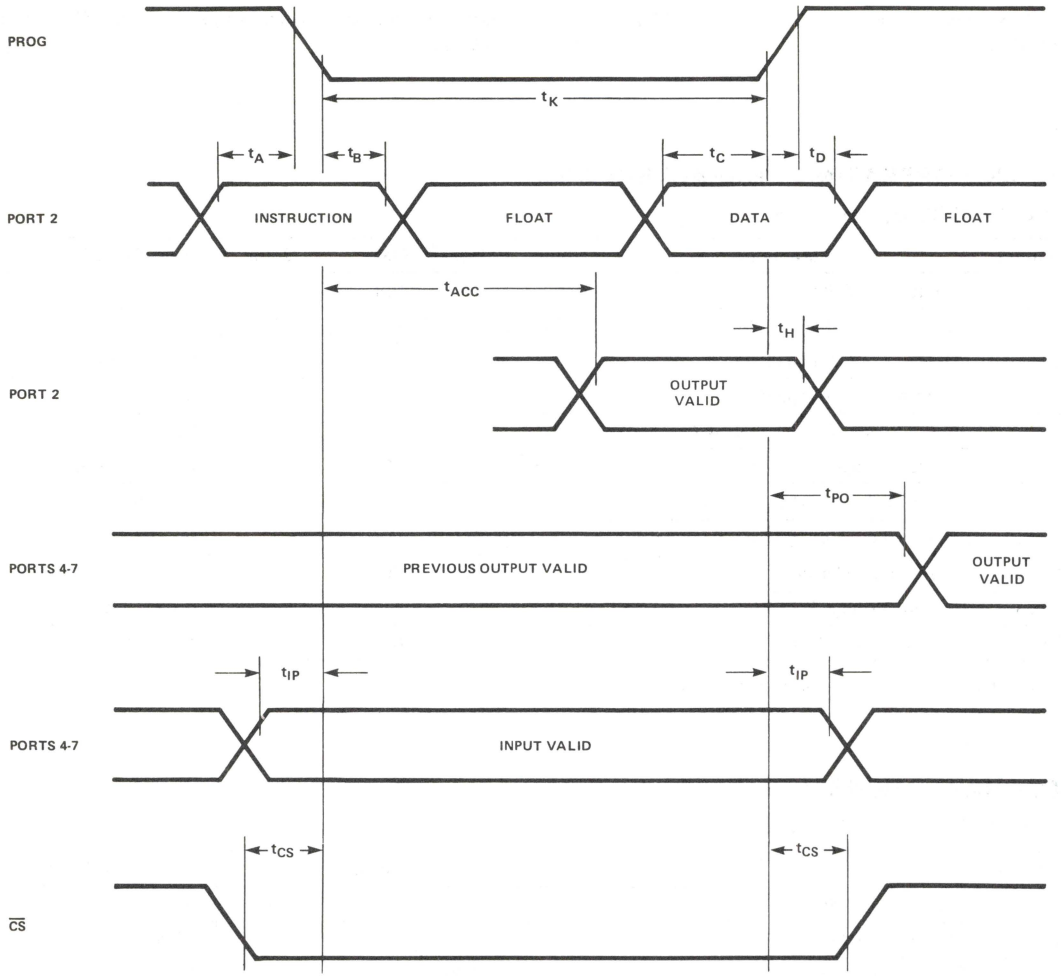
*See following graph for additional sink current capability.

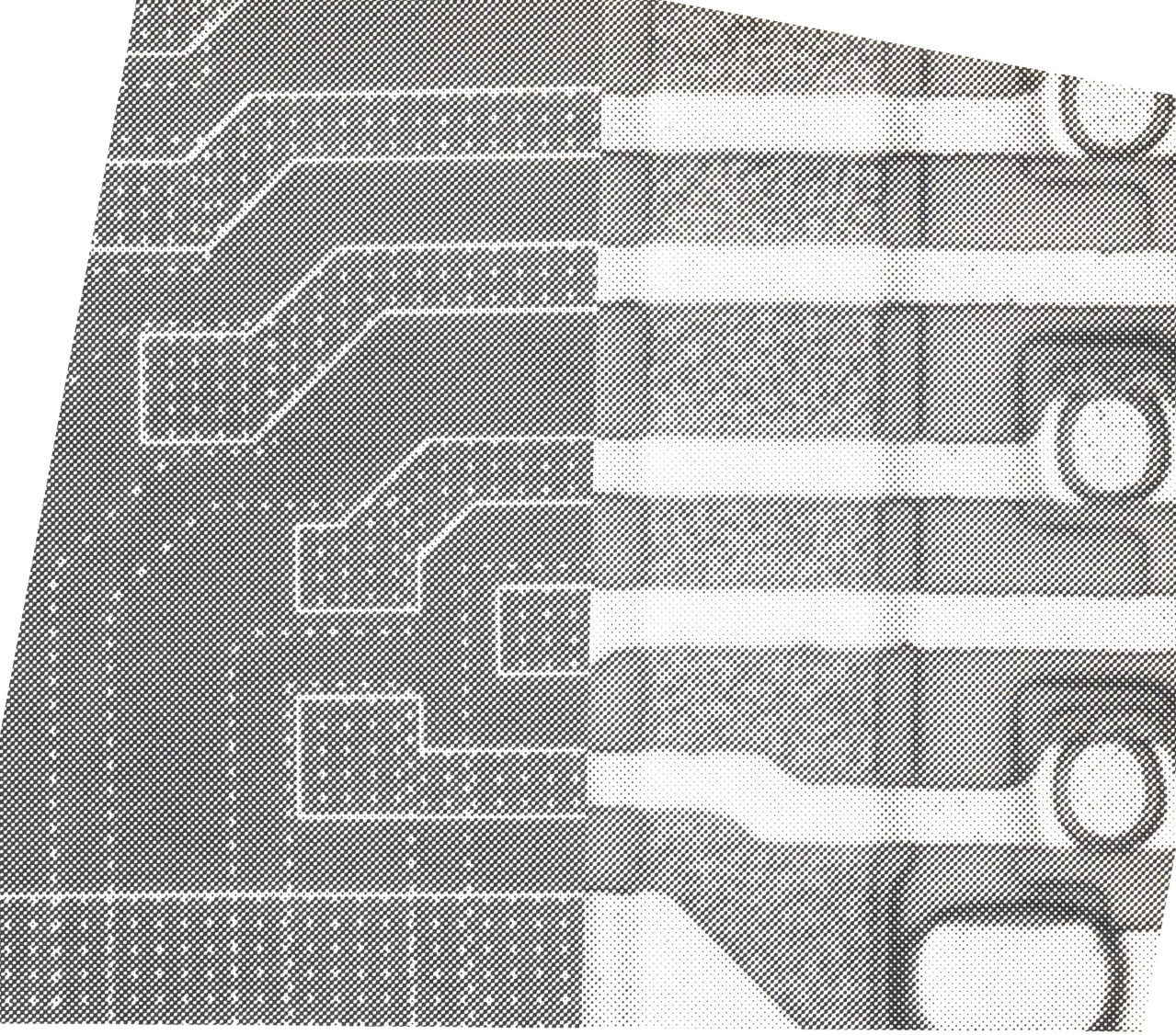
A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 10%

Symbol	Parameter	Min.	Max.	Units	Test Conditions
t_A	Code Valid Before PROG	100		ns	80 pF Load
t_B	Code Valid After PROG	60		ns	20 pF Load
t_C	Data Valid Before PROG	200		ns	80 pF Load
t_D	Data Valid After PROG	20		ns	20 pF Load
t_H	Floating After PROG	0	150	ns	20 pF Load
t_K	PROG Negative Pulse Width	900		ns	
t_{CS}	CS Valid Before/After PROG	50		ns	
t_{PO}	Ports 4-7 Valid After PROG		700	ns	100 pF Load
t_{LP1}	Ports 4-7 Valid Before/After PROG	100		ns	
t_{ACC}	Port 2 Valid After PROG		750	ns	80 pF Load

WAVEFORMS


PROG
t_K
t_A
t_B
t_C
t_D
PORT 2
INSTRUCTION
FLOAT
DATA
FLOAT
t_{ACC}
t_H
PORT 2
OUTPUT VALID
t_{PO}
PORTS 4-7
PREVIOUS OUTPUT VALID
OUTPUT VALID
t_{IP}
t_{IP}
PORTS 4-7
INPUT VALID
t_{CS}
t_{CS}
$\overline{CS}$



11 MCS-80/85™ Microprocessors

MCS-80/85™ MICROPROCESSORS

INTRODUCTION

The MCS-80 and MCS-85 have become the industry standard 8-bit microcomputer systems. Their wide usage is due to many factors, among them total system support in terms of the largest family of state-of-the-art processors, memories, and peripheral components. Many of these are described in the pages that follow. In addition, system designers using the 8080A and 8085A have the benefit of the world's largest and most usable set of microcomputer development tools (see section 13).

The MCS-85 components are of particular interest for new microcomputer designs. Systems designed around the 8085A and the new 8085A-2 offer the highest performance-to-cost ratios in the industry. Higher speed, single power supply requirement, and low component count while maintaining total MCS-80 software compatibility are key features of the MCS-85 system.

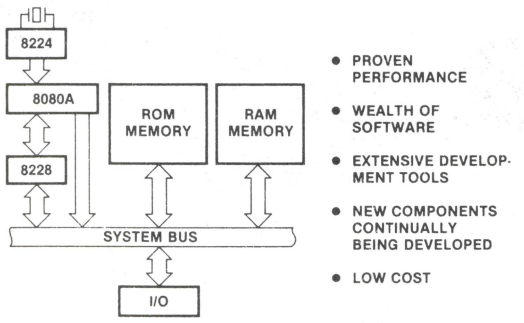


Figure 1. MCS-80™ — Foundation for MCS-85™

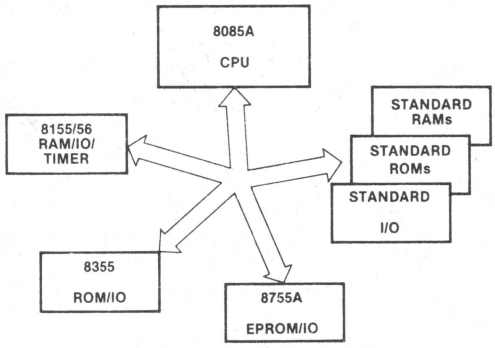


Figure 2. MCS-85™ — The New Industry Standard

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RECOMMENDED PRODUCTS FOR MCS-80/85 MICROCOMPUTER APPLICATIONS

Function	Part No.	Page No.	Description	T_{ACC} (ns)	8085	8080A	8008
Memory and I/O Expanders for MCS-85	8155/8156	11-63	RAM—I/O—TIMER		X		
	8355	11-77	ROM—I/O		X		
	8755A	11-84	EPROM—I/O		X		
	8202	11-76	Dynamic RAM Controller		X	X	
RAMs (Static)	8101A-4	3-26	256 x 4	450	X	X	X
	8102A-4	3-30	1K x 1	450	X	X	X
	8111A-4	3-85	256 x 4	450	X	X	X
	5101	3-153	256 x 4 CMOS	450	X	X	X
	2114	3-94	1K x 4	450	X	X	X
	2142	3-133	1K x 4	450	X	X	X
RAMs (Dynamic)	2104A-4	3-36	4K x 1	300	X	X	
	2107C	3-60	4K x 1	270	X	X	
	2117-4	3-117	16K x 1	250	X	X	
RAM Support Circuits	3222	6-19	Refresh controller		X	X	
	3232	6-25	Refresh counter/multiplexer		X	X	
	3242	6-29	Refresh counter/multiplexer		X	X	
ROMs	2308	4-18	1K x 8	450	X	X	X
	8308	4-18	1K x 8	450	X	X	X
	8316A	4-22	2K x 8	850	X	X	X
	2316E	4-25	2K x 8	450	X	X	X
EPROMs	1702A-2	4-5	256 x 8	650		X	X
	2704	4-38	512 x 8	450	X	X	X
	8708	Blank	1K x 8	450	X	X	X
	2708	4-38	1K x 8	450	X	X	X
	2708L	4-38	1K x 8	450	X	X	X
	2708-1	4-38	1K x	350	X	X	X
	2716	4-44	2K x 8	450	X	X	X
Peripherals	8205	12-11	1-8 decoder		X	X	X
	8212	12-17	8-bit latch		X	X	X
	8214	12-31	Priority unit		X	X	X
	8216	12-38	4-bit bus driver		X	X	X
	8224	12-24	Clock generator			X	
	8226	12-38	4-bit bus driver		X	X	X
	8228	11-34	System controller			X	
	8238	11-34	System controller			X	
	8251A	12-46	USART		X	X	X
	8253	12-65	Interval timer		X	X	X
	8255A	12-76	PPI		X	X	X
	8257	12-98	DMA		X	X	
	8259	12-111	Interrupt		X	X	
	8041/8741	12-3	Universal peripheral interface		X	X	
	8271	12-123	Floppy disk		X	X	
	8273	12-142	SDLC		X	X	
	8275	12-165	CRT		X	X	
	8278	12-188	KYBD/display		X	X	
	8279	12-198	KYBD/display		X	X	X
	8294	12-209	Data encryption		X	X	

8008/8008-1
8-BIT MICROPROCESSOR

- **Instruction Cycle Time — 1.25 μs with 8008-1 or 20 μs with 8008**
- **Directly Addresses 16K x 8 Bits of Memory (RAM, ROM, or S.R.)**
- **Interrupt Capability**
- **48 Instructions, Data Oriented**
- **Address Stack Contains 8 14-Bit Registers (Including Program Counter) Which Permit Nesting of Subroutines Up to 7 Levels**

The Intel® 8008 is a single chip MOS 8-bit parallel central processor unit (CPU) for the MCS-8 microcomputer system.

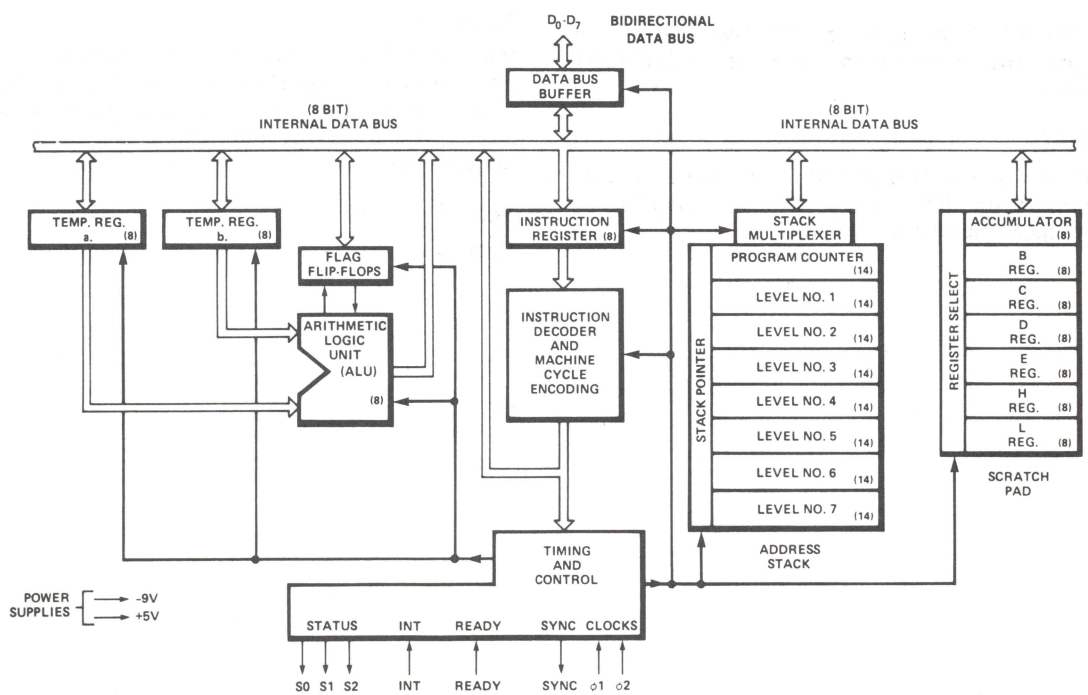
This CPU contains 6 8-bit data registers, an 8-bit accumulator, 2 8-bit temporary registers, 4 flag bits (carry, zero, sign, parity), and an 8-bit parallel binary arithmetic unit which implements addition, subtraction, and logical operations. A memory stack containing a 14-bit program counter and 7 14-bit words is used internally to store program and subroutine addresses. The 14-bit address permits the direct addressing of 16K words of memory (any mix of RAM, ROM, or S.R.).

The instruction set of the 8008 consists of 48 instructions including data manipulation, binary arithmetic, and jump to subroutine.

The normal program flow of the 8008 may be interrupted through the use of the interrupt control line. This allows the servicing of slow I/O peripheral devices while also executing the main program.

The ready command line synchronizes the 8008 to the memory cycle allowing any type or speed of semiconductor memory to be used.

BLOCK DIAGRAM



PIN DESCRIPTION

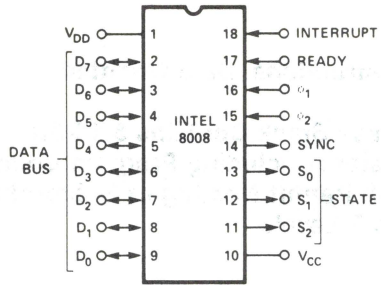


Figure 1. Pin Configuration

D_0-D_7

BI-DIRECTIONAL DATA BUS. All address and data communication between the processor and the program memory, data memory, and I/O devices occurs on these 8 lines. Cycle control information is also available.

INT

INTERRUPT input. A logic "1" level at this input causes the processor to enter the INTERRUPT mode.

READY

READY input. This command line is used to synchronize the 8008 to the memory cycle allowing any speed memory to be used.

SYNC

SYNC output. Synchronization signal generated by the processor. It indicates the beginning of a machine cycle.

ϕ_1, ϕ_2

Two phase clock inputs.

S_0, S_1, S_2

MACHINE STATE OUTPUTS. The processor controls the use of the data bus and determines whether it will be sending or receiving data. State signals S_0, S_1, and S_2, along with SYNC inform the peripheral circuitry of the state of the processor.

V_{CC} +5V ±5%

V_{DD} -9V ±5%

INSTRUCTION SET

Data and Instruction Formats

Data in the 8008 is stored in the form of 8-bit binary integers. All data transfers to the system data bus will be in the same format.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

DATA WORD

The program instructions may be one, two, or three bytes in length. Multiple byte instructions must be stored in successive words in program memory. The instruction formats then depend on the particular operation executed.

		TYPICAL INSTRUCTIONS
One Byte Instructions		
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OP CODE	Register to register, memory reference, I/O arithmetic or logical, rotate or return instructions
Two Byte Instructions		
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OP CODE	
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OPERAND	Immediate mode instructions
Three Byte Instructions		
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OP CODE	
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	LOW ADDRESS	JUMP or CALL instructions
X X D_5 D_4 D_3 D_2 D_1 D_0	HIGH ADDRESS*	*For the third byte of this instruction, D_6 and D_7 are "don't care" bits.

For the MCS-8™ a logic "1" is defined as a high level and a logic "0" is defined as a low level.

Index Register Instructions

The load instructions do not affect the flag flip-flops. The increment and decrement instructions affect all flip-flops except the carry.

MNEMONIC	MINIMUM STATES REQUIRED	INSTRUCTION CODE D_7 D_6	D_5 D_4 D_3	D_2 D_1 D_0	DESCRIPTION OF OPERATION
(1) MOV r_1, r_2	(5)	1 1	D D D	S S S	Load index register r_1 with the content of index register r_2.
(2) MOV r, M	(8)	1 1	D D D	1 1 1	Load index register r with the content of memory register M.
MOV M, r	(7)	1 1	1 1 1	S S S	Load memory register M with the content of index register r.
(3) MVI r	(8)	0 0 B B	D D D B B B	1 1 0 B B B	Load index register r with data B . . . B.
MVI M	(9)	0 0 B B	1 1 1 B B B	1 1 0 B B B	Load memory register M with data B . . . B.
INR r	(5)	0 0	D D D	0 0 0	Increment the content of index register r (r ≠ A).
DCR r	(5)	0 0	D D D	0 0 1	Decrement the content of index register r (r ≠ A).

Accumulator Group Instructions

The result of the ALU instructions affect all of the flag flip-flops. The rotate instructions affect only the carry flip-flop.

ADD r	(5)	1 0	0 0 0	S S S	Add the content of index register r, memory register M, or data B . . . B to the accumulator. An overflow (carry) sets the carry flip-flop.
ADD M	(8)	1 0	0 0 0	1 1 1	
ADI	(8)	0 0 B B	0 0 0 B B B	1 0 0 B B B	
ADC r	(5)	1 0	0 0 1	S S S	Add the content of index register r, memory register M, or data B . . . B from the accumulator with carry. An overflow (carry) sets the carry flip-flop.
ADC M	(8)	1 0	0 0 1	1 1 1	
ACI	(8)	0 0 B B	0 0 1 B B B	1 0 0 B B B	
SUB r	(5)	1 0	0 1 0	S S S	Subtract the content of index register r, memory register M, or data B . . . B from the accumulator. An underflow (borrow) sets the carry flip-flop.
SUB M	(8)	1 0	0 1 0	1 1 1	
SUI	(8)	0 0 B B	0 1 0 B B B	1 0 0 B B B	
SBB r	(5)	1 0	0 1 1	S S S	Subtract the content of index register r, memory register M, or data data B . . . B from the accumulator with borrow. An underflow (borrow) sets the carry flip-flop.
SBB M	(8)	1 0	0 1 1	1 1 1	
SBI	(8)	0 0 B B	0 1 1 B B B	1 0 0 B B B	

MNEMONIC	MINIMUM STATES REQUIRED	INSTRUCTION CODE $D_7 D_6$	$D_5 D_4 D_3$	$D_2 D_1 D_0$	DESCRIPTION OF OPERATION
ANA r	(5)	1 0	1 0 0	S S S	Compute the logical AND of the content of index register r,
ANA M	(8)	1 0	1 0 0	1 1 1	memory register M, or data B . . . B with the accumulator.
ANI	(8)	0 0	1 0 0	1 0 0	
		B B	B B B	B B B	
XRA r	(5)	1 0	1 0 1	S S S	Compute the EXCLUSIVE OR of the content of index register
XRA M	(8)	1 0	1 0 1	1 1 1	r, memory register M, or data B . . . B with the accumulator.
XRI	(8)	0 0	1 0 1	1 0 0	
		B B	B B B	B B B	
ORA r	(5)	1 0	1 1 0	S S S	Compute the INCLUSIVE OR of the content of index register
ORA M	(8)	1 0	1 1 0	1 1 1	r, memory register m, or data B . . . B with the accumulator.
ORI	(8)	0 0	1 1 0	1 0 0	
		B B	B B B	B B B	
CMP r	(5)	1 0	1 1 1	S S S	Compare the content of index register r, memory register M,
CMP M	(8)	1 0	1 1 1	1 1 1	or data B . . . B with the accumulator. The content of the
CPI	(8)	0 0	1 1 1	1 0 0	accumulator is unchanged.
		B B	B B B	B B B	
RLC	(5)	0 0	0 0 0	0 1 0	Rotate the content of the accumulator left.
RRC	(5)	0 0	0 0 1	0 1 0	Rotate the content of the accumulator right.
RAL	(5)	0 0	0 1 0	0 1 0	Rotate the content of the accumulator left through the carry.
RAR	(5)	0 0	0 1 1	0 1 0	Rotate the content of the accumulator right through the carry.
Program Counter and Stack Control Instructions					
(4) JMP	(11)	0 1	X X X	1 0 0	Unconditionally jump to memory address $B_3 \ldots B_3 B_2 \ldots B_2$.
		B_2 B_2	B_2 B_2 B_2	B_2 B_2 B_2	
		X X	B_3 B_3 B_3	B_3 B_3 B_3	
(5) JNC, JNZ, JP, JPO	(9 or 11)	0 1	0 C_4 C_3	0 0 0	Jump to memory address $B_3 \ldots B_3 B_2 \ldots B_2$ if the condition
		B_2 B_2	B_2 B_2 B_2	B_2 B_2 B_2	flip-flop is false. Otherwise, execute the next instruction in sequence.
		X X	B_3 B_3 B_3	B_3 B_3 B_3	
JC, JZ JM, JPE	(9 or 11)	0 1	1 C_4 C_3	0 0 0	Jump to memory address $B_3 \ldots B_3 B_2 \ldots B_2$ if the condition
		B_2 B_2	B_2 B_2 B_2	B_2 B_2 B_2	flip-flop is true. Otherwise, execute the next instruction in sequence.
		X X	B_3 B_3 B_3	B_3 B_3 B_3	
CALL	(11)	0 1	X X X	1 1 0	Unconditionally call the subroutine at memory address $B_3 \ldots$
		B_2 B_2	B_2 B_2 B_2	B_2 B_2 B_2	$B_3 B_2 \ldots B_2$. Save the current address (up one level in the stack).
		X X	B_3 B_3 B_3	B_3 B_3 B_3	
CNC, CNZ, CP, CPO	(9 or 11)	0 1	0 C_4 C_3	0 1 0	Call the subroutine at memory address $B_3 \ldots B_3 B_2 \ldots B_2$ if the
		B_2 B_2	B_2 B_2 B_2	B_2 B_2 B_2	condition flip-flop is false, and save the current address (up one
		X X	B_3 B_3 B_3	B_3 B_3 B_3	level in the stack.) Otherwise, execute the next instruction in sequence.
CC, CZ, CM, CPE	(9 or 11)	0 1	1 C_4 C_3	0 1 0	Call the subroutine at memory address $B_3 \ldots B_3 B_2 \ldots B_2$ if the
		B_2 B_2	B_2 B_2 B_2	B_2 B_2 B_2	condition flip-flop is true, and save the current address (up one
		X X	B_3 B_3 B_3	B_3 B_3 B_3	level in the stack). Otherwise, execute the next instruction in sequence.
RET	(5)	0 0	X X X	1 1 1	Unconditionally return (down one level in the stack).
RNC, RNZ, RP, RPO	(3 or 5)	0 0	0 C_4 C_3	0 1 1	Return (down one level in the stack) if the condition flip-flop is false. Otherwise, execute the next instruction in sequence.
RC, RZ RM, RPE	(3 or 5)	0 0	1 C_4 C_3	0 1 1	Return (down one level in the stack) if the condition flip-flop is true. Otherwise, execute the next instruction in sequence.
RST	(5)	0 0	A A A	1 0 1	Call the subroutine at memory address AAA000 (up one level in the stack).
Input/Output Instructions					
IN	(8)	0 1	0 0 M	M M 1	Read the content of the selected input port (MMM) into the accumulator.
OUT	(6)	0 1	R R M	M M 1	Write the content of the accumulator into the selected output port (RRMMM, RR ≠ 00).
Machine Instruction					
HLT	(4)	0 0	0 0 0	0 0 X	Enter the STOPPED state and remain there until interrupted.
	(4)	1 1	1 1 1	1 1 1	

NOTES:

(1) SSS = Source Index Register, DDD = Destination Index Register — These registers, r_i, are designated A(accumulator—000), B(001), C(010), D(011), E(100), H(101), L(110).

(2) Memory registers are addressed by the contents of registers H & L.

(3) Additional bytes of instruction are designated by BBBBBBBB.

(4) X = "Don't Care".

(5) Flag flip-flops are defined by $C_4 C_3$: carry (00-overflow or underflow), zero (01-result is zero), sign (10-MSB of result is "1"), parity (11-parity is even).

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	−55°C to +150°C
Input Voltages and Supply Voltage With Respect to V_{CC}	+0.5 to −20V
Power Dissipation	1.0 W @ 25°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = −9V ±5% unless otherwise specified. Logic "1" is defined as the more positive level (V_{IH}, V_{OH}). Logic "0" is defined as the more negative level (V_{IL}, V_{OL}).

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
I_{DD}	AVERAGE SUPPLY CURRENT-OUTPUTS LOADED*		30	60	mA	T_A = 25°C
I_{LI}	INPUT LEAKAGE CURRENT			10	μA	V_{IN} = 0V
V_{IL}	INPUT LOW VOLTAGE (INCLUDING CLOCKS)	V_{DD}		V_{CC}−4.2	V	
V_{IH}	INPUT HIGH VOLTAGE (INCLUDING CLOCKS)	V_{CC}−1.5		V_{CC}+0.3	V	
V_{OL}	OUTPUT LOW VOLTAGE			0.4	V	I_{OL} = 0.44mA C_L = 200 pF
V_{OH}	OUTPUT HIGH VOLTAGE	V_{CC}−1.5			V	I_{OH} = 0.2mA

*Measurements are made while the 8008 is executing a typical sequence of instructions. The test load is selected such that at V_{OL} = 0.4V, I_{OL} = 0.44mA on each output.

A.C. CHARACTERISTICS

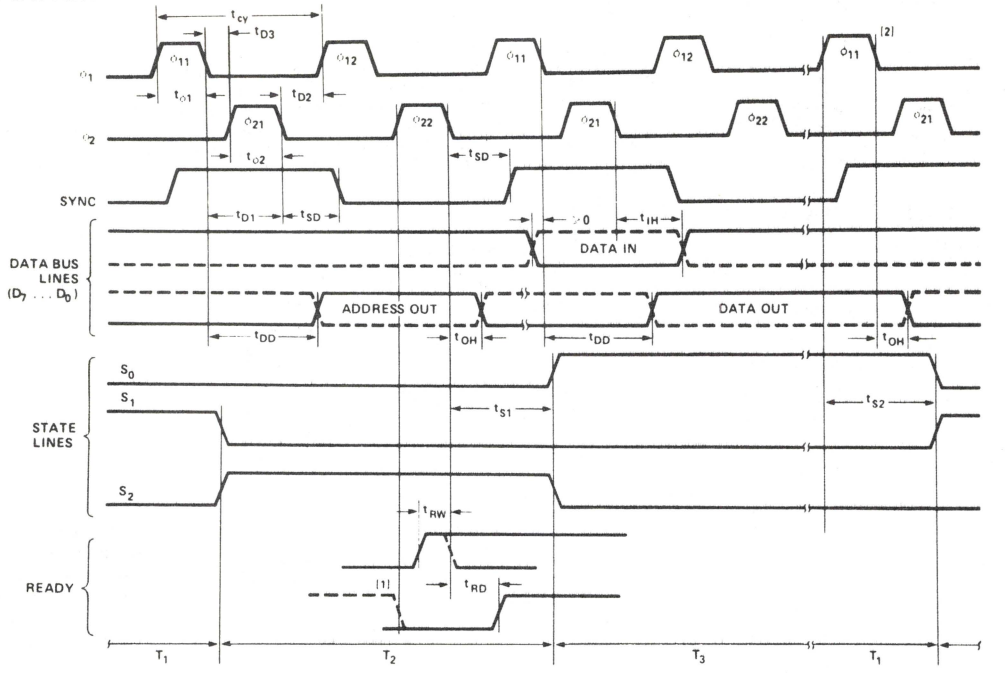
T_A = 0°C to 70°C; V_{CC} = +5V ±5%, V_{DD} = −9V ±5%. All measurements are referenced to 1.5V levels.

SYMBOL	PARAMETER	8008 LIMITS		8008-1 LIMITS		UNIT	TEST CONDITIONS
		MIN.	MAX.	MIN.	MAX.		
t_{CY}	CLOCK PERIOD	2	3	1.25	3	μs	t_R,t_F = 50ns
t_R,t_F	CLOCK RISE AND FALL TIMES		50		50	ns	
$t_{\phi 1}$	PULSE WIDTH OF ϕ_1	.70		.35		μs	
$t_{\phi 2}$	PULSE WIDTH OF ϕ_2	.55		.35		μs	
t_{D1}	CLOCK DELAY FROM FALLING EDGE OF ϕ_1 TO FALLING EDGE OF ϕ_2	.90	1.1		1.1	μs	
t_{D2}	CLOCK DELAY FROM ϕ_2 TO ϕ_1	.40		.35		μs	
t_{D3}	CLOCK DELAY FROM ϕ_1 TO ϕ_2	.20		.20		μs	
t_{DD}	DATA OUT DELAY		1.0		1.0	μs	C_L = 100pF
t_{OH}	HOLD TIME FOR DATA BUS OUT	.10		.10		μs	
t_{IH}	HOLD TIME FOR DATA IN	[1]		[1]		μs	
t_{SD}	SYNC OUT DELAY		.70		.70	μs	C_L = 100pF
t_{S1}	STATE OUT DELAY (ALL STATES EXCEPT T1 AND T1I) [2]		1.1		1.1	μs	C_L = 100pF
t_{S2}	STATE OUT DELAY (STATES T1 AND T1I)		1.0		1.0	μs	C_L = 100pF
t_{RW}	PULSE WIDTH OF READY DURING ϕ_{22} TO ENTER T3 STATE	.35		.35		μs	
t_{RD}	READY DELAY TO ENTER WAIT STATE	.20		.20		μs	

[1] t_{IH} MIN ≥ t_{SD}

[2] If the INTERRUPT is not used, all states have the same output delay, t_{S1}.

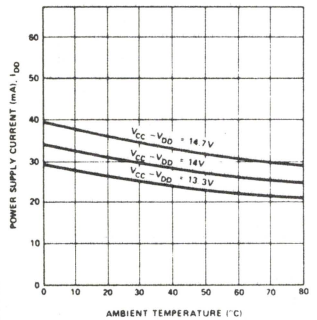
TIMING DIAGRAM



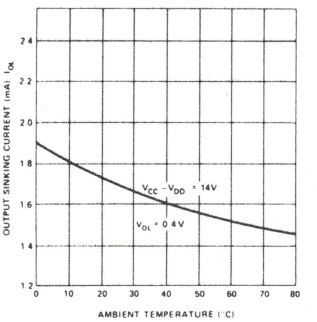
Notes: 1. READY line must be at "0" prior to ϕ_{22} of T_2 to guarantee entry into the WAIT state.
2. INTERRUPT line must not change levels within 200 ns (max.) of falling edge of ϕ_1.

TYPICAL D.C. CHARACTERISTICS

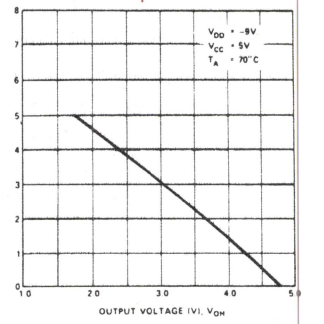
POWER SUPPLY CURRENT VS. TEMPERATURE



OUTPUT SINKING CURRENT VS. TEMPERATURE

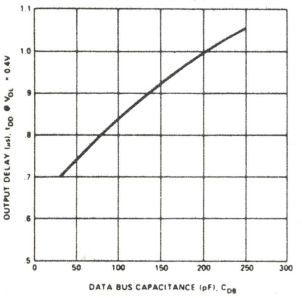


OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



TYPICAL A.C. CHARACTERISTICS

DATA OUT DELAY VS. OUTPUT LOAD CAPACITANCE



CAPACITANCE f = 1MHz; T_A = 25°C; Unmeasured Pins Grounded

SYMBOL	TEST	LIMIT (pF)	
		TYP.	MAX.
C_{IN}	INPUT CAPACITANCE	5	10
C_{DB}	DATA BUS I/O CAPACITANCE	5	10
C_{OUT}	OUTPUT CAPACITANCE	5	10

8080A/8080A-1/8080A-2
8-BIT N-CHANNEL MICROPROCESSOR

The 8080A is functionally and electrically compatible with the Intel® 8080.

- **TTL Drive Capability**
- **2 μs (– 1:1.3 μs, – 2:1.5 μs) Instruction Cycle**
- **Powerful Problem Solving Instruction Set**
- **6 General Purpose Registers and an Accumulator**
- **16-Bit Program Counter for Directly Addressing up to 64K Bytes of Memory**
- **16-Bit Stack Pointer and Stack Manipulation Instructions for Rapid Switching of the Program Environment**
- **Decimal, Binary, and Double Precision Arithmetic**
- **Ability to Provide Priority Vectored Interrupts**
- **512 Directly Addressed I/O Ports**

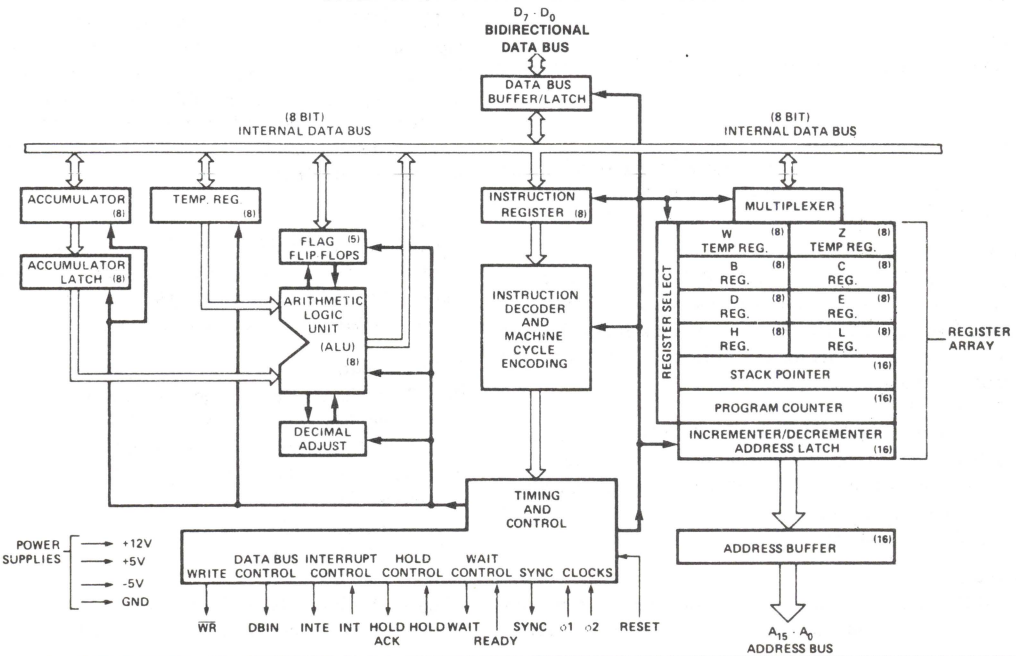
The Intel® 8080A is a complete 8-bit parallel central processing unit (CPU). It is fabricated on a single LSI chip using Intel's n-channel silicon gate MOS process. This offers the user a high performance solution to control and processing applications.

The 8080A contains 6 8-bit general purpose working registers and an accumulator. The 6 general purpose registers may be addressed individually or in pairs providing both single and double precision operators. Arithmetic and logical instructions set or reset 4 testable flags. A fifth flag provides decimal arithmetic operation.

The 8080A has an external stack feature wherein any portion of memory may be used as a last in/first out stack to store/retrieve the contents of the accumulator, flags, program counter, and all of the 6 general purpose registers. The 16-bit stack pointer controls the addressing of this external stack. This stack gives the 8080A the ability to easily handle multiple level priority interrupts by rapidly storing and restoring processor status. It also provides almost unlimited subroutine nesting.

This microprocessor has been designed to simplify systems design. Separate 16-line address and 8-line bidirectional data busses are used to facilitate easy interface to memory and I/O. Signals to control the interface to memory and I/O are provided directly by the 8080A. Ultimate control of the address and data busses resides with the HOLD signal. It provides the ability to suspend processor operation and force the address and data busses into a high impedance state. This permits OR-tying these busses with other controlling devices for (DMA) direct memory access or multiprocessor operation.

8080A CPU FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

The following describes the function of all of the 8080A I/O pins. Several of the descriptions refer to internal timing periods.

A_{15}-A_0 (output three-state)
ADDRESS BUS; the address bus provides the address to memory (up to 64K 8-bit words) or denotes the I/O device number for up to 256 input and 256 output devices. A_0 is the least significant address bit.

D_7-D_0 (input/output three-state)
DATA BUS; the data bus provides bi-directional communication between the CPU, memory, and I/O devices for instructions and data transfers. Also, during the first clock cycle of each machine cycle, the 8080A outputs a status word on the data bus that describes the current machine cycle. D_0 is the least significant bit.

SYNC (output)
SYNCHRONIZING SIGNAL; the SYNC pin provides a signal to indicate the beginning of each machine cycle.

DBIN (output)
DATA BUS IN; the DBIN signal indicates to external circuits that the data bus is in the input mode. This signal should be used to enable the gating of data onto the 8080A data bus from memory or I/O.

READY (input)
READY; the READY signal indicates to the 8080A that valid memory or input data is available on the 8080A data bus. This signal is used to synchronize the CPU with slower memory or I/O devices. If after sending an address out the 8080A does not receive a READY input, the 8080A will enter a WAIT state for as long as the READY line is low. READY can also be used to single step the CPU.

WAIT (output)
WAIT; the WAIT signal acknowledges that the CPU is in a WAIT state.

$\overline{WR}$ (output)
WRITE; the $\overline{WR}$ signal is used for memory WRITE or I/O output control. The data on the data bus is stable while the $\overline{WR}$ signal is active low ($\overline{WR}$ = 0).

HOLD (input)
HOLD; the HOLD signal requests the CPU to enter the HOLD state. The HOLD state allows an external device to gain control of the 8080A address and data bus as soon as the 8080A has completed its use of these buses for the current machine cycle. It is recognized under the following conditions:

- the CPU is in the HALT state.
- the CPU is in the T2 or TW state and the READY signal is active.

As a result of entering the HOLD state the CPU ADDRESS BUS (A_{15}-A_0) and DATA BUS (D_7-D_0) will be in their high impedance state. The CPU acknowledges its state with the HOLD ACKNOWLEDGE (HLDA) pin.

HLDA (output)
HOLD ACKNOWLEDGE; the HLDA signal appears in response to the HOLD signal and indicates that the data and address bus will go to the high impedance state. The HLDA signal begins at:

- T3 for READ memory or input.
- The Clock Period following T3 for WRITE memory or OUTPUT operation.

In either case, the HLDA signal appears after the rising edge of ϕ_1 and high impedance occurs after the rising edge of ϕ_2.

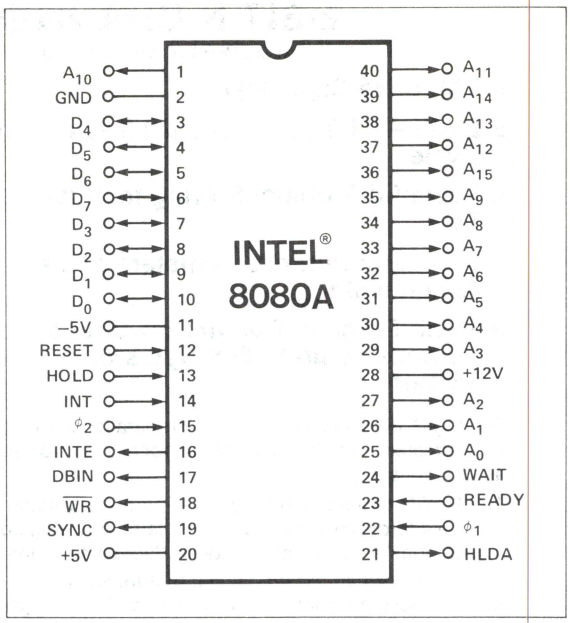


Figure 1. Pin Configuration

INTE (output)
INTERRUPT ENABLE; indicates the content of the internal interrupt enable flip/flop. This flip/flop may be set or reset by the Enable and Disable Interrupt instructions and inhibits interrupts from being accepted by the CPU when it is reset. It is automatically reset (disabling further interrupts) at time T1 of the instruction fetch cycle (M1) when an interrupt is accepted and is also reset by the RESET signal.

INT (input)
INTERRUPT REQUEST; the CPU recognizes an interrupt request on this line at the end of the current instruction or while halted. If the CPU is in the HOLD state or if the Interrupt Enable flip/flop is reset it will not honor the request.

RESET (input) [1]
RESET; while the RESET signal is activated, the content of the program counter is cleared. After RESET, the program will start at location 0 in memory. The INTE and HLDA flip/flops are also reset. Note that the flags, accumulator, stack pointer, and registers are not cleared.

V_{SS}	Ground Reference.
V_{DD}	+12 ± 5% Volts.
V_{CC}	+5 ± 5% Volts.
V_{BB}	-5 ±5% Volts (substrate bias).
ϕ_1, ϕ_2	2 externally supplied clock phases. (non TTL compatible)

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to +70° C
Storage Temperature	-65°C to +150°C
All Input or Output Voltages With Respect to V_{BB}	-0.3V to +20V
V_{CC}, V_{DD} and V_{SS} With Respect to V_{BB}	-0.3V to +20V
Power Dissipation	1.5W

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	V_{SS}−1		V_{SS}+0.8	V	
V_{IHC}	Clock Input High Voltage	9.0		V_{DD}+1	V	
V_{IL}	Input Low Voltage	V_{SS}−1		V_{SS}+0.8	V	
V_{IH}	Input High Voltage	3.3		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.9mA on all outputs, I_{OH} = -150μA.
V_{OH}	Output High Voltage	3.7			V	
$I_{DD\,(AV)}$	Avg. Power Supply Current (V_{DD})		40	70	mA	Operation T_{CY} = .48 μsec
$I_{CC\,(AV)}$	Avg. Power Supply Current (V_{CC})		60	80	mA	
$I_{BB\,(AV)}$	Avg. Power Supply Current (V_{BB})		.01	1	mA	
I_{IL}	Input Leakage			±10	μA	$V_{SS} \leqslant V_{IN} \leqslant V_{CC}$
I_{CL}	Clock Leakage			±10	μA	$V_{SS} \leqslant V_{CLOCK} \leqslant V_{DD}$
I_{DL} [2]	Data Bus Leakage in Input Mode			-100 -2.0	μA mA	$V_{SS} \leqslant V_{IN} \leqslant V_{SS}$ +0.8V V_{SS} +0.8V $\leqslant V_{IN} \leqslant V_{CC}$
I_{FL}	Address and Data Bus Leakage During HOLD			+10 -100	μA	$V_{ADDR/DATA} = V_{CC}$ $V_{ADDR/DATA} = V_{SS}$ + 0.45V

CAPACITANCE

T_A = 25°C $V_{CC} = V_{DD} = V_{SS}$ = 0V, V_{BB} = -5V

Symbol	Parameter	Typ.	Max.	Unit	Test Condition
C_ϕ	Clock Capacitance	17	25	pf	f_c = 1 MHz
C_{IN}	Input Capacitance	6	10	pf	Unmeasured Pins
C_{OUT}	Output Capacitance	10	20	pf	Returned to V_{SS}

NOTES:
1. The RESET signal must be active for a minimum of 3 clock cycles.
2. When DBIN is high and $V_{IN} > V_{IH}$ an internal active pull up will be switched onto the Data Bus.
3. ΔI supply / ΔT_A = -0.45%/°C.

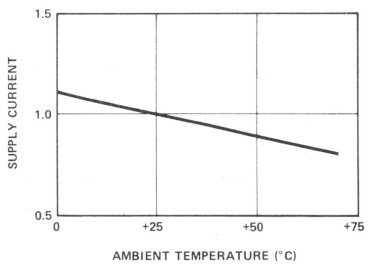


Figure 2. Typical Supply Current vs. Temperature, Normalized[3]

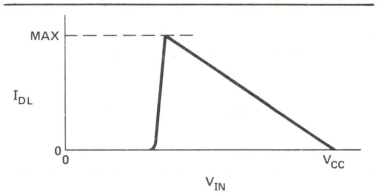


Figure 3. Data Bus Characteristic During DBIN

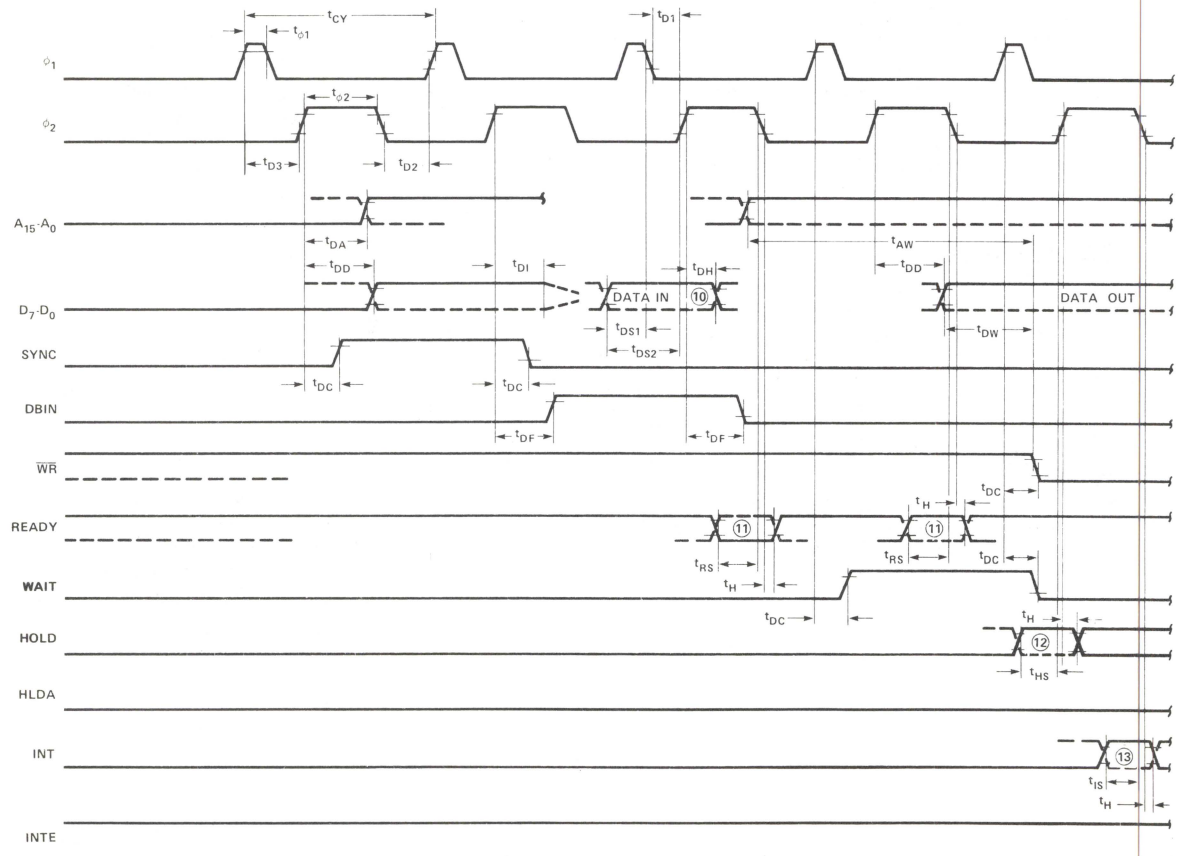
A.C. CHARACTERISTICS (8080A)

T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, V_{SS} = 0V, Unless Otherwise Noted

Symbol	Parameter	Min.	Max.	-1 Min.	-1 Max.	-2 Min.	-2 Max.	Unit	Test Condition
t_{CY}[3]	Clock Period	0.48	2.0	0.32	2.0	0.38	2.0	μsec	
t_r, t_f	Clock Rise and Fall Time	0	50	0	25	0	50	nsec	
$t_{\phi 1}$	ϕ_1 Pulse Width	60		50		60		nsec	
$t_{\phi 2}$	ϕ_2 Pulse Width	220		145		175		nsec	
t_{D1}	Delay ϕ_1 to ϕ_2	0		0		0		nsec	
t_{D2}	Delay ϕ_2 to ϕ_1	70		60		70		nsec	
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	80		60		70		nsec	
t_{DA}[2]	Address Output Delay From ϕ_2		200		150		175	nsec	C_L = 100 pF
t_{DD}[2]	Data Output Delay From ϕ_2		220		180		200	nsec	C_L = 100 pF
t_{DC}[2]	Signal Output Delay From ϕ_2 or ϕ_2 (SYNC, WR, WAIT, HLDA)		120		110		120	nsec	C_L = 50 pF
t_{DF}[2]	DBIN Delay From ϕ_2	25	140	25	130	25	140	nsec	C_L = 50 pF
t_{DI}[1]	Delay for Input Bus to Enter Input Mode		t_{DF}		t_{DF}		t_{DF}	nsec	
t_{DS1}	Data Setup Time During ϕ_1 and DBIN	30		10		20		nsec	

WAVEFORMS

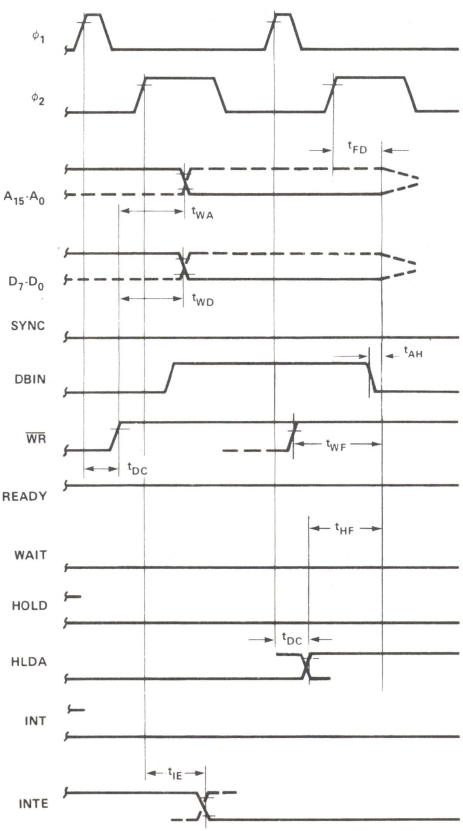
(Note: Timing measurements are made at the following reference voltages: CLOCK "1" = 8.0V "0" = 1.0V; INPUTS "1" = 3.3V, "0" = 0.8V; OUTPUTS "1" = 2.0V, "0" = 0.8V.)



A.C. CHARACTERISTICS (8080A)

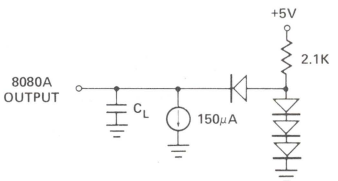
T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, V_{SS} = 0V, Unless Otherwise Noted

Symbol	Parameter	Min.	Max.	-1 Min.	-1 Max.	-2 Min.	-2 Max.	Unit	Test Condition
t_{DS2}	Data Setup Time to ϕ_2 During DBIN	150		120		130		nsec	
t_{DH}[1]	Data Holt time From ϕ_2 During DBIN	[1]		[1]		[1]		nsec	
t_{IE}[2]	INTE Output Delay From ϕ_2		200		200		200	nsec	C_L = 50 pF
t_{RS}	READY Setup Time During ϕ_2	120		90		90		nsec	
t_{HS}	HOLD Setup Time to ϕ_2	140		120		120		nsec	
t_{IS}	INT Setup Time During ϕ_2	120		100		100		nsec	
t_H	Hold Time From ϕ_2 (READY, INT, HOLD)	0		0		0		nsec	
t_{FD}	Delay to Float During Hold (Address and Data Bus)		120		120		120	nsec	
t_{AW}[2]	Address Stable Prior to WR	[5]		[5]		[5]		nsec	C_L = 100 pF: Address, Data C_L = 50 pF: $\overline{WR}$,HLDA,DBIN
t_{DW}[2]	Output Data Stable Prior to WR	[6]		[6]		[6]		nsec	
t_{WD}[2]	Output Data Stable From WR	[7]		[7]		[7]		nsec	
t_{WA}[2]	Address Stable From WR	[7]		[7]		[7]		nsec	
t_{HF}[2]	HLDA to Float Delay	[8]		[8]		[8]		nsec	
t_{WF}[2]	WR to Float Delay	[9]		[9]		[9]		nsec	
t_{AH}[2]	Address Hold Time After DBIN During HLDA	-20		-20		-20		nsec	



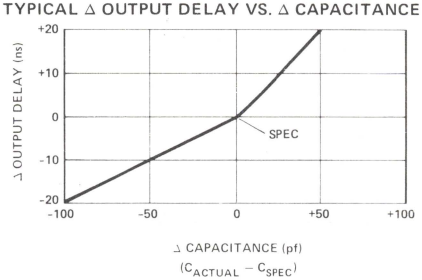
NOTES: (Parenthesis gives -1, -2 specifications, respectively)

1. Data input should be enabled with DBIN status. No bus conflict can then occur and data hold time is assured. t_{DH} = 50 ns or t_{DF}, whichever is less.
2. Load Circuit.



3. $t_{CY} = t_{D3} + t_{r\phi2} + t_{\phi2} + t_{f\phi2} + t_{D2} + t_{r\phi1} \geq 480$ ns (-1:320 ns, -2:380 ns).

TYPICAL Δ OUTPUT DELAY VS. Δ CAPACITANCE



4. The following are relevant when interfacing the 8080A to devices having V_{IH} = 3.3V:
   a) Maximum output rise time from .8V to 3.3V = 100ns @ C_L = SPEC.
   b) Output delay when measured to 3.0V = SPEC +60ns @ C_L = SPEC.
   c) If $C_L \neq$ SPEC, add .6ns/pF if $C_L > C_{SPEC}$, subtract .3ns/pF (from modified delay) if $C_L < C_{SPEC}$.
5. $t_{AW} = 2\,t_{CY} - t_{D3} - t_{r\phi2} - 140$ ns (-1:110 ns, -2:130 ns).
6. $t_{DW} = t_{CY} - t_{D3} - t_{r\phi2} - 170$ ns (-1:150 ns, -2:170 ns).
7. If not HLDA, $t_{WD} = t_{WA} = t_{D3} + t_{r\phi2} + 10$ns. If HLDA, $t_{WD} = t_{WA} = t_{WF}$.
8. $t_{HF} = t_{D3} + t_{r\phi2} - 50$ns.
9. $t_{WF} = t_{D3} + t_{r\phi2} - 10$ns
10. Data in must be stable for this period during DBIN · T_3. Both t_{DS1} and t_{DS2} must be satisfied.
11. Ready signal must be stable for this period during T_2 or T_W. (Must be externally synchronized.)
12. Hold signal must be stable for this period during T_2 or T_W when entering hold mode, and during T_3, T_4, T_5 and T_{WH} when in hold mode. (External synchronization is not required.)
13. Interrupt signal must be stable during this period of the last clock cycle of any instruction in order to be recognized on the following instruction. (External synchronization is not required.)
14. This timing diagram shows timing relationships only; it does not represent any specific machine cycle.

INSTRUCTION SET

The accumulator group instructions include arithmetic and logical operators with direct, indirect, and immediate addressing modes.

Move, load, and store instruction groups provide the ability to move either 8 or 16 bits of data between memory, the six working registers and the accumulator using direct, indirect, and immediate addressing modes.

The ability to branch to different portions of the program is provided with jump, jump conditional, and computed jumps. Also the ability to call to and return from subroutines is provided both conditionally and unconditionally. The RESTART (or single byte call instruction) is useful for interrupt vector operation.

Double precision operators such as stack manipulation and double add instructions extend both the arithmetic and interrupt handling capability of the 8080A. The ability to increment and decrement memory, the six general registers and the accumulator is provided as well as extended increment and decrement instructions to operate on the register pairs and stack pointer. Further capability is provided by the ability to rotate the accumulator left or right through or around the carry bit.

Input and output may be accomplished using memory addresses as I/O ports or the directly addressed I/O provided for in the 8080A instruction set.

The following special instruction group completes the 8080A instruction set: the NOP instruction, HALT to stop processor execution and the DAA instructions provide decimal arithmetic capability. STC allows the carry flag to be directly set, and the CMC instruction allows it to be complemented. CMA complements the contents of the accumulator and XCHG exchanges the contents of two 16-bit register pairs directly.

Data and Instruction Formats

Data in the 8080A is stored in the form of 8-bit binary integers. All data transfers to the system data bus will be in the same format.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

DATA WORD

The program instructions may be one, two, or three bytes in length. Multiple byte instructions must be stored in successive words in program memory. The instruction formats then depend on the particular operation executed.

One Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE

TYPICAL INSTRUCTIONS

Register to register, memory reference, arithmetic or logical, rotate, return, push, pop, enable or disable Interrupt instructions

Two Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OPERAND

Immediate mode or I/O instructions

Three Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	LOW ADDRESS OR OPERAND 1
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HIGH ADDRESS OR OPERAND 2

Jump, call or direct load and store instructions

For the 8080A a logic "1" is defined as a high level and a logic "0" is defined as a low level.

8080 INSTRUCTION SET

Summary of Processor Instructions

Mnemonic	Description	Instruction Code[1] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock[2] Cycles
MOVE, LOAD, AND STORE										
MOVr1,r2	Move register to register	0	1	D	D	D	S	S	S	5
MOV M,r	Move register to memory	0	1	1	1	0	S	S	S	7
MOV r,M	Move memory to register	0	1	D	D	D	1	1	0	7
MVI r	Move immediate register	0	0	D	D	D	1	1	0	7
MVI M	Move immediate memory	0	0	1	1	0	1	1	0	10
LXI B	Load immediate register Pair B & C	0	0	0	0	0	0	0	1	10
LXI D	Load immediate register Pair D & E	0	0	0	1	0	0	0	1	10
LXI H	Load immediate register Pair H & L	0	0	1	0	0	0	0	1	10
STAX B	Store A indirect	0	0	0	0	0	0	1	0	7
STAX D	Store A indirect	0	0	0	1	0	0	1	0	7
LDAX B	Load A indirect	0	0	0	0	1	0	1	0	7
LDAX D	Load A indirect	0	0	0	1	1	0	1	0	7
STA	Store A direct	0	0	1	1	0	0	1	0	13
LDA	Load A direct	0	0	1	1	1	0	1	0	13
SHLD	Store H & L direct	0	0	1	0	0	0	1	0	16
LHLD	Load H & L direct	0	0	1	0	1	0	1	0	16
XCHG	Exchange D & E, H & L Registers	1	1	1	0	1	0	1	1	4
STACK OPS										
PUSH B	Push register Pair B & C on stack	1	1	0	0	0	1	0	1	11
PUSH D	Push register Pair D & E on stack	1	1	0	1	0	1	0	1	11
PUSH H	Push register Pair H & L on stack	1	1	1	0	0	1	0	1	11
PUSH PSW	Push A and Flags on stack	1	1	1	1	0	1	0	1	11
POP B	Pop register Pair B & C off stack	1	1	0	0	0	0	0	1	10
POP D	Pop register Pair D & E off stack	1	1	0	1	0	0	0	1	10
POP H	Pop register Pair H & L off stack	1	1	1	0	0	0	0	1	10
POP PSW	Pop A and Flags off stack	1	1	1	1	0	0	0	1	10
XTHL	Exchange top of stack, H & L	1	1	1	0	0	0	1	1	18
SPHL	H & L to stack pointer	1	1	1	1	1	0	0	1	5
LXI SP	Load immediate stack pointer	0	0	1	1	0	0	0	1	10
INX SP	Increment stack pointer	0	0	1	1	0	0	1	1	5
DCX SP	Decrement stack pointer	0	0	1	1	1	0	1	1	5
JUMP										
JMP	Jump unconditional	1	1	0	0	0	0	1	1	10
JC	Jump on carry	1	1	0	1	1	0	1	0	10
JNC	Jump on no carry	1	1	0	1	0	0	1	0	10
JZ	Jump on zero	1	1	0	0	1	0	1	0	10
JNZ	Jump on no zero	1	1	0	0	0	0	1	0	10
JP	Jump on positive	1	1	1	1	0	0	1	0	10
JM	Jump on minus	1	1	1	1	1	0	1	0	10
JPE	Jump on parity even	1	1	1	0	1	0	1	0	10
JPO	Jump on parity odd	1	1	1	0	0	0	1	0	10
PCHL	H & L to program counter	1	1	1	0	1	0	0	1	5
CALL										
CALL	Call unconditional	1	1	0	0	1	1	0	1	17
CC	Call on carry	1	1	0	1	1	1	0	0	11/17
CNC	Call on no carry	1	1	0	1	0	1	0	0	11/17
CZ	Call on zero	1	1	0	0	1	1	0	0	11/17
CNZ	Call on no zero	1	1	0	0	0	1	0	0	11/17
CP	Call on positive	1	1	1	1	0	1	0	0	11/17
CM	Call on minus	1	1	1	1	1	1	0	0	11/17
CPE	Call on parity even	1	1	1	0	1	1	0	0	11/17
CPO	Call on parity odd	1	1	1	0	0	1	0	0	11/17
RETURN										
RET	Return	1	1	0	0	1	0	0	1	10
RC	Return on carry	1	1	0	1	1	0	0	0	5/11
RNC	Return on no carry	1	1	0	1	0	0	0	0	5/11
RZ	Return on zero	1	1	0	0	1	0	0	0	5/11
RNZ	Return on no zero	1	1	0	0	0	0	0	0	5/11
RP	Return on positive	1	1	1	1	0	0	0	0	5/11
RM	Return on minus	1	1	1	1	1	0	0	0	5/11
RPE	Return on parity even	1	1	1	0	1	0	0	0	5/11
RPO	Return on parity odd	1	1	1	0	0	0	0	0	5/11
RESTART										
RST	Restart	1	1	A	A	A	1	1	1	11
INCREMENT AND DECREMENT										
INR r	Increment register	0	0	D	D	D	1	0	0	5
DCR r	Decrement register	0	0	D	D	D	1	0	1	5
INR M	Increment memory	0	0	1	1	0	1	0	0	10
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10
INX B	Increment B & C registers	0	0	0	0	0	0	1	1	5
INX D	Increment D & E registers	0	0	0	1	0	0	1	1	5
INX H	Increment H & L registers	0	0	1	0	0	0	1	1	5
DCX B	Decrement B & C	0	0	0	0	1	0	1	1	5
DCX D	Decrement D & E	0	0	0	1	1	0	1	1	5
DCX H	Decrement H & L	0	0	1	0	1	0	1	1	5
ADD										
ADD r	Add register to A	1	0	0	0	0	S	S	S	4
ADC r	Add register to A with carry	1	0	0	0	1	S	S	S	4
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7
ADI	Add immediate to A	1	1	0	0	0	1	1	0	7
ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0	7
DAD B	Add B & C to H & L	0	0	0	0	1	0	0	1	10
DAD D	Add D & E to H & L	0	0	0	1	1	0	0	1	10
DAD H	Add H & L to H & L	0	0	1	0	1	0	0	1	10
DAD SP	Add stack pointer to H & L	0	0	1	1	1	0	0	1	10

NOTES: 1. DDD or SSS: B 000, C 001, D 010, E 011, H 100, L 101, Memory 110, A 111.
2. Two possible cycle times, (6/12) indicate instruction cycles dependent on condition flags.

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Summary of Processor Instructions (Cont.)

Mnemonic	Description	Instruction Code[1] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock[2] Cycles
SUBTRACT										
SUB r	Subtract register from A	1	0	0	1	0	S	S	S	4
SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S	4
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7
SUI	Subtract immediate from A	1	1	0	1	0	1	1	0	7
SBI	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7
LOGICAL										
ANA r	And register with A	1	0	1	0	0	S	S	S	4
XRA r	Exclusive Or register with A	1	0	1	0	1	S	S	S	4
ORA r	Or register with A	1	0	1	1	0	S	S	S	4
CMP r	Compare register with A	1	0	1	1	1	S	S	S	4
ANA M	And memory with A	1	0	1	0	0	1	1	0	7
XRA M	Exclusive Or memory with A	1	0	1	0	1	1	1	0	7
ORA M	Or memory with A	1	0	1	1	0	1	1	0	7
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7
ANI	And immediate with A	1	1	1	0	0	1	1	0	7
XRI	Exclusive Or immediate with A	1	1	1	0	1	1	1	0	7
ORI	Or immediate with A	1	1	1	1	0	1	1	0	7
CPI	Compare immediate with A	1	1	1	1	1	1	1	0	7
ROTATE										
RLC	Rotate A left	0	0	0	0	0	1	1	1	4
RRC	Rotate A right	0	0	0	0	1	1	1	1	4
RAL	Rotate A left through carry	0	0	0	1	0	1	1	1	4
RAR	Rotate A right through carry	0	0	0	1	1	1	1	1	4
SPECIALS										
CMA	Complement A	0	0	1	0	1	1	1	1	4
STC	Set carry	0	0	1	1	0	1	1	1	4
CMC	Complement carry	0	0	1	1	1	1	1	1	4
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4
INPUT/OUTPUT										
IN	Input	1	1	0	1	1	0	1	1	10
OUT	Output	1	1	0	1	0	0	1	1	10
CONTROL										
EI	Enable Interrupts	1	1	1	1	1	0	1	1	4
DI	Disable Interrupt	1	1	1	1	0	0	1	1	4
NOP	No-operation	0	0	0	0	0	0	0	0	4
HLT	Halt	0	1	1	1	0	1	1	0	7

NOTES: 1. DDD or SSS: B=000. C=001. D=010. E=011. H=100. L=101. Memory=110. A=111.
2. Two possible cycle times. (6/12) indicate instruction cycles dependent on condition flags.

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M8080A
8-BIT N-CHANNEL MIRCOPROCESSOR

The M8080A is functionally compatible with the Intel® 8080.

MILITARY TEMP.

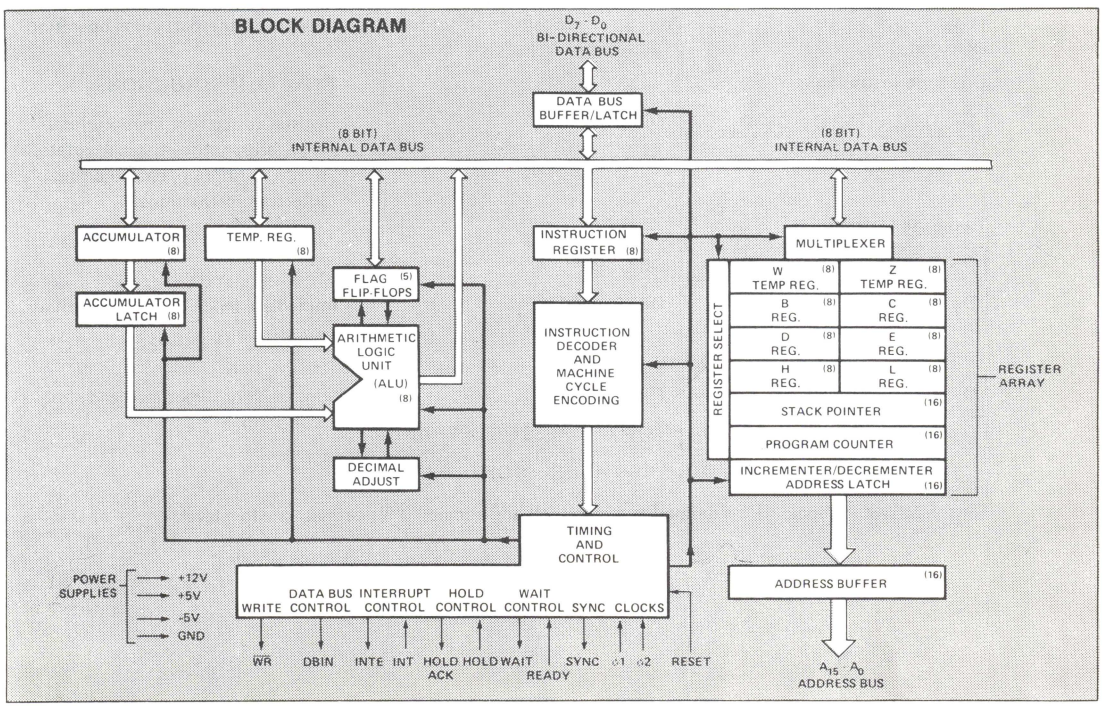
- **Fully Military Temperature Range −55°C to +125°C**
- **±10% Power Supply Tolerance**
- **2 μs Instruction Cycle**
- **Powerful Problem Solving Instruction Set**
- **6 General Purpose Registers and an Accumulator**
- **16-Bit Program Counter for Directly Addressing up to 64K Bytes of Memory**
- **16-Bit Stack Pointer and Stack Manipulation Instructions for Rapid Switching of the Program Environment**
- **Decimal, Binary, and Double Precision Arithmetic**
- **Ability to Provide Priority Vectored Interrupts**
- **512 Directly Addressed I/O Ports**
- **TTL Drive Capability**

The Intel® M8080A is a complete 8-bit parallel central processing unit (CPU). It is fabricated on a single LSI chip using Intel's n-channel silicon gate MOS process. This offers the user a high performance solution to control and processing applications.

The M8080A contains 6 8-bit general purpose working registers and an accumulator. The 6 general purpose registers may be addressed individually or in pairs providing both single and double precision operators. Arithmetic and logical instructions set or reset 4 testable flags. A fifth flag provides decimal arithmetic operation.

The M8080A has an external stack feature wherein any portion of memory may be used as a last in/first out stack to store /retrieve the contents of the accumulator, flags, program counter and all of the 6 general purpose registers. The 16-bit stack pointer controls the addressing of this external stack. This stack gives the M8080A the ability to easily handle multiple level priority interrupts by rapidly storing and restoring processor status. It also provides almost unlimited subroutine nesting.

This microprocessor has been designed to simplify systems design. Separate 16-line address and 8-line bidirectional data busses are used to facilitate easy interface to memory and I/O. SIgnals to control the interface to memory and I/O are provided directly by the M8080A. Ultimate control of the address and data busses resides with the hold signal. It provides the ability to suspend processor operation and force the address and data busses into a high impedance state. This permits OR-tying these busses with other controlling device for (DMA) direct memory access or multi-processor operation.



MILITARY TEMP.

INSTRUCTION SET

The accumulator group instructions include arithmetic and logical operators with direct, indirect, and immediate addressing modes.

Move, load, and store instruction groups provide the ability to move either 8 or 16 bits of data between memory, the six working registers and the accumulator using direct, indirect, and immediate addressing modes.

The ability to branch to different portions of the program is provided with jump, jump conditional, and computed jumps. Also the ability to call to and return from subroutines is provided both conditionally and unconditionally. The RESTART (or single byte call instruction) is useful for interrupt vector operation.

Double precision operators such as stack manipulation and double add instructions extend both the arithmetic and interrupt handling capability of the M8080A. The ability to increment and decrement memory, the six general registers and the accumulator is provided as well as extended increment and decrement instructions to operate on the register pairs and stack pointer. Further capability is provided by the ability to rotate the accumulator left or right through or around the carry bit.

Input and output may be accomplished using memory addresses as I/O ports or the directly addressed I/O provided for in the M8080A instruction set.

The following special instruction group completes the M8080A instruction set: the NOP instruction, HALT to stop processor execution and the DAA instructions provide decimal arithmetic capability. STC allows the carry flag to be directly set, and the CMC instruction allows it to be complemented. CMA complements the contents of the accumulator and XCHG exchanges the contents of two 16-bit register pairs directly.

Data and Instruction Formats

Data in the M8080A is stored in the form of 8-bit binary integers. All data transfers to the system data bus will be in the same format.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

DATA WORD

The program instructions may be one, two, or three bytes in length. Multiple byte instructions must be stored in successive words in program memory. The instruction formats then depend on the particular operation executed.

One Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE

TYPICAL INSTRUCTIONS

Register to register, memory reference, arithmetic or logical, rotate, return, push, pop, enable or disable Interrupt instructions

Two Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OPERAND

Immediate mode or I/O instructions

Three Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	LOW ADDRESS OR OPERAND 1
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HIGH ADDRESS OR OPERAND 2

Jump, call or direct load and store instructions

For the M8080A a logic "1" is defined as a high level and a logic "0" is defined as a low level.

MILITARY GRADE

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input or Output Voltages With Respect to V_{BB}	-0.3V to +20V
V_{CC}, V_{DD} and V_{SS} With Respect to V_{BB}	-0.3V to +20V
Power Dissipation	1.7W

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = -55°C to +125°C, V_{DD} = +12V ±10%, V_{CC} = +5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	V_{SS}-1		V_{SS}+0.8	V	
V_{IHC}	Clock Input High Voltage	8.5		V_{DD}+1	V	
V_{IL}	Input Low Voltage	V_{SS}-1		V_{SS}+0.8	V	
V_{IH}	Input High Voltage	3.0		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.9mA on all outputs,
V_{OH}	Output High Voltage	3.7			V	I_{OH} = 150μA.
$I_{DD\,(AV)}$	Avg. Power Supply Current (V_{DD})		50	80	mA	Operation
$I_{CC\,(AV)}$	Avg. Power Supply Current (V_{CC})		60	100	mA	T_{CY} = .48 μsec
$I_{BB\,(AV)}$	Avg. Power Supply Current (V_{BB})		.01	1	mA	
I_{IL}	Input Leakage			±10	μA	$V_{SS} \leqslant V_{IN} \leqslant V_{CC}$
I_{CL}	Clock Leakage			±10	μA	$V_{SS} \leqslant V_{CLOCK} \leqslant V_{DD}$
I_{DL} [2]	Data Bus Leakage in Input Mode			-100 -2.0	μA mA	$V_{SS} \leqslant V_{IN} \leqslant V_{SS}+0.8V$ $V_{SS}+0.8V \leqslant V_{IN} \leqslant V_{CC}$
I_{FL}	Address and Data Bus Leakage During HOLD			+10 -100	μA	$V_{ADDR/DATA} = V_{CC}$ $V_{ADDR/DATA} = V_{SS}$ + 0.45V

CAPACITANCE

T_A = 25°C $V_{CC} = V_{DD} = V_{SS}$ = 0V, V_{BB} = -5V

Symbol	Parameter	Typ.	Max.	Unit	Test Condition
C_ϕ	Clock Capacitance	17	25	pf	f_c = 1 MHz
C_{IN}	Input Capacitance	6	10	pf	Unmeasured Pins
C_{OUT}	Output Capacitance	10	20	pf	Returned to V_{SS}

NOTES:

1. The RESET signal must be active for a minimum of 3 clock cycles.
2. When DBIN is high and $V_{IN} > V_{IH}$ an internal active pull up will be switched onto the Data Bus.
3. ΔI supply / ΔT_A = -0.45%/°C.

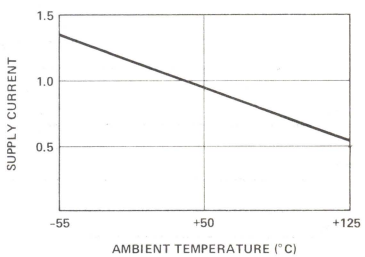


Figure 1. Typical Supply Current vs. Temperature, Normalized[3]

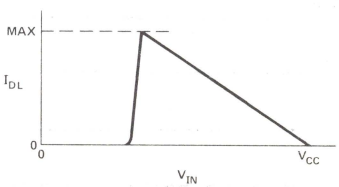


Figure 2. Data Bus Characteristic During DBIN

MILITARY TEMP.

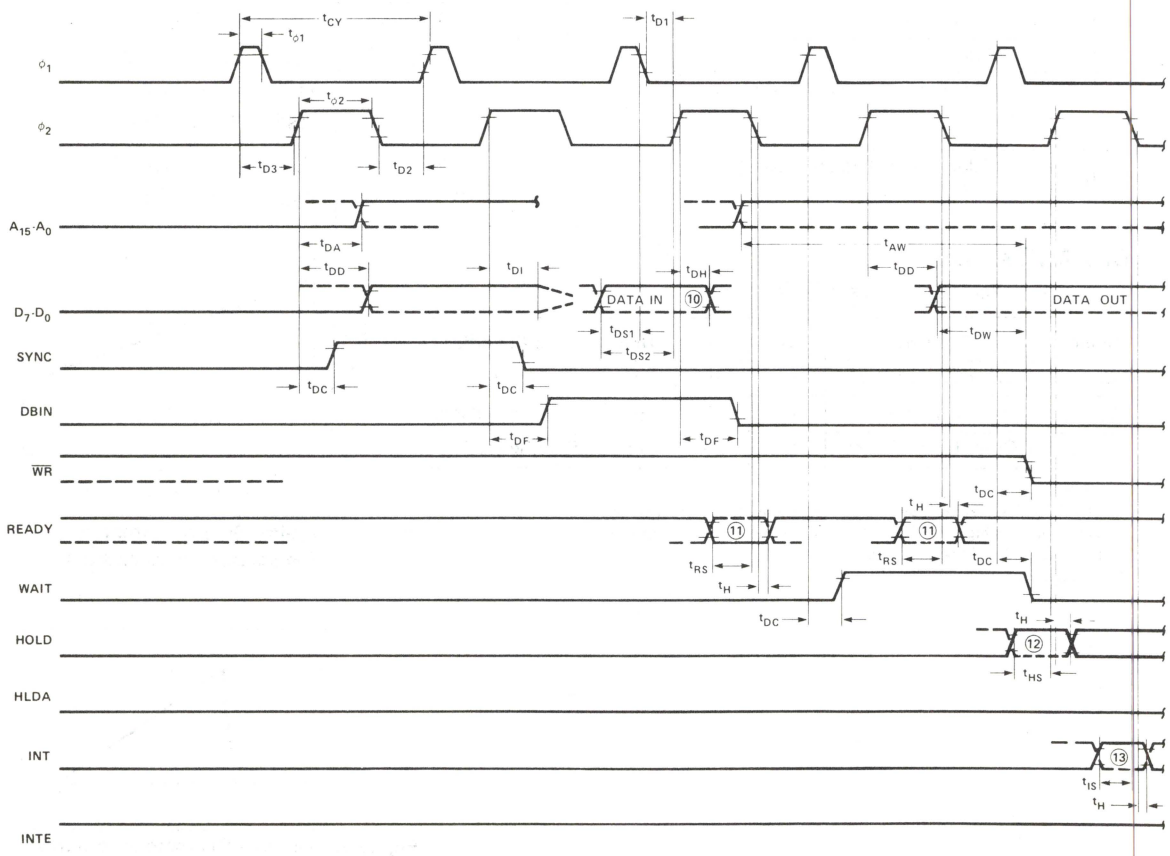
A.C. CHARACTERISTICS

T_A = -55°C to +125°C, V_{DD} = +12V ±10%, V_{CC} = +5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{CY}[3]	Clock Period	0.48	2.0	μsec	
t_r, t_f	Clock Rise and Fall Time	0	50	nsec	
$t_{\phi 1}$	ϕ_1 Pulse Width	60		nsec	
$t_{\phi 2}$	ϕ_2 Pulse Width	220		nsec	
t_{D1}	Delay ϕ_1 to ϕ_2	0		nsec	
t_{D2}	Delay ϕ_2 to ϕ_1	80		nsec	
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	80		nsec	
t_{DA}[2]	Address Output Delay From ϕ_2		200	nsec	C_L = 50pf
t_{DD}[2]	Data Output Delay From ϕ_2		220	nsec	
t_{DC}[2]	Signal Output Delay From ϕ_1, or ϕ_2 (SYNC, $\overline{WR}$, WAIT, HLDA)		140	nsec	
t_{DF}[2]	DBIN Delay From ϕ_2	25	150	nsec	
t_{DI}[1]	Delay for Input Bus to Enter Input Mode		t_{DF}	nsec	
t_{DS1}	Data Setup Time During ϕ_1 and DBIN	30		nsec	

WAVEFORMS[14]

(Note: Timing measurements are made at the following reference voltages: CLOCK "1" = 7.0V, "0" = 1.0V; INPUTS "1" = 3.0V, "0" = 0.8V; OUTPUTS "1" = 2.0V, "0" = 0.8V.)

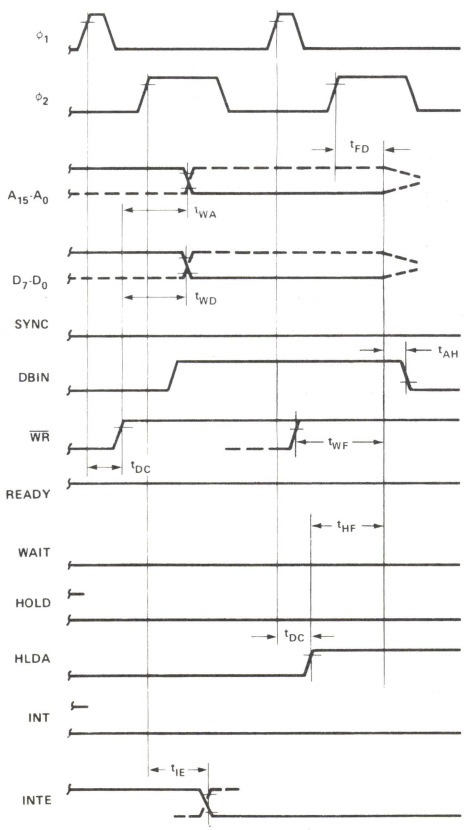


MILITARY TEMP.

A.C. CHARACTERISTICS (Continued)

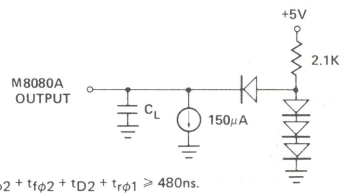
T_A = -55°C to +125°C, V_{DD} = +12V ±10%, V_{CC} = +5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{DS2}	Data Setup Time to ϕ_2 During DBIN	130		nsec	
t_{DH} [1]	Data Hold Time From ϕ_2 During DBIN	[1]		nsec	
t_{IE} [2]	INTE Output Delay From ϕ_2		200	nsec	C_L = 50pf
t_{RS}	READY Setup Time During ϕ_2	120		nsec	
t_{HS}	HOLD Setup Time to ϕ_2	140		nsec	
t_{IS}	INT Setup Time During ϕ_2	120		nsec	
t_H	Hold Time From ϕ_2 (READY, INT, HOLD)	0		nsec	
t_{FD}	Delay to Float During Hold (Address and Data Bus)		130	nsec	
t_{AW} [2]	Address Stable Prior to $\overline{WR}$	[5]		nsec	C_L = 50pf
t_{DW} [2]	Output Data Stable Prior to $\overline{WR}$	[6]		nsec	
t_{WD} [2]	Output Data Stable From $\overline{WR}$	[7]		nsec	
t_{WA} [2]	Address Stable From $\overline{WR}$	[7]		nsec	
t_{HF} [2]	HLDA to Float Delay	[8]		nsec	
t_{WF} [2]	$\overline{WR}$ to Float Delay	[9]		nsec	
t_{AH} [2]	Address Hold Time After DBIN During HLDA	-20		nsec	



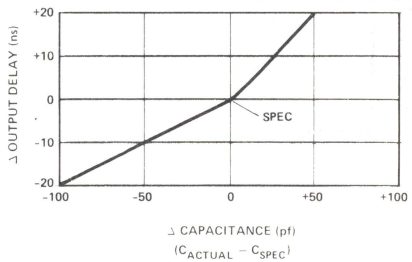
NOTES:

1. Data input should be enabled with DBIN status. No bus conflict can then occur and data hold time is assured. t_{DH} = 50 ns or t_{DF}, whichever is less.
2. Load Circuit.



3. $t_{CY} = t_{D3} + t_{r\phi2} + t_{\phi2} + t_{f\phi2} + t_{D2} + t_{r\phi1} \geq 480$ns.

TYPICAL Δ OUTPUT DELAY VS. Δ CAPACITANCE



4. The following are relevant when interfacing the M8080A to devices having V_{IH} = 3.3V:
   a) Maximum output rise time from .8V to 3.3V = 100ns @ C_L = SPEC.
   b) Output delay when measured to 3.0V = SPEC +60ns @ C_L = SPEC.
   c) If $C_L \neq$ SPEC, add .6ns/pF if $C_L > C_{SPEC}$, subtract .3ns/pF (from modified delay) if $C_L < C_{SPEC}$.
5. $t_{AW} = 2\,t_{CY} - t_{D3} - t_{r\phi2} - 140$nsec.
6. $t_{DW} = t_{CY} - t_{D3} - t_{r\phi2} - 170$nsec.
7. If not HLDA, $t_{WD} = t_{WA} = t_{D3} + t_{r\phi2} + 10$ns. If HLDA, $t_{WD} = t_{WA} = t_{WF}$.
8. $t_{HF} = t_{D3} + t_{r\phi2} - 50$ns.
9. $t_{WF} = t_{D3} + t_{r\phi2} - 10$ns
10. Data in must be stable for this period during DBIN · T_3. Both t_{DS1} and t_{DS2} must be satisfied.
11. Ready signal must be stable for this period during T_2 or T_W. (Must be externally synchronized.)
12. Hold signal must be stable for this period during T_2 or T_W when entering hold mode, and during T_3, T_4, T_5 and T_{WH} when in hold mode. (External synchronization is not required.)
13. Interrupt signal must be stable during this period of the last clock cycle of any instruction in order to be recognized on the following instruction. (External synchronization is not required.)
14. This timing diagram shows timing relationships only; it does not represent any specific machine cycle.

8224
CLOCK GENERATOR AND DRIVER FOR 8080A CPU

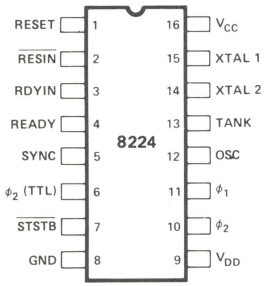
- **Single Chip Clock Generator/Driver for 8080A CPU**
- **Power-Up Reset for CPU**
- **Ready Synchronizing Flip-Flop**
- **Advanced Status Strobe**
- **Oscillator Output for External System Timing**
- **Crystal Controlled for Stable System Operation**
- **Reduces System Package Count**

The Intel® 8224 is a single chip clock generator/driver for the 8080A CPU. It is controlled by a crystal, selected by the designer to meet a variety of system speed requirements.

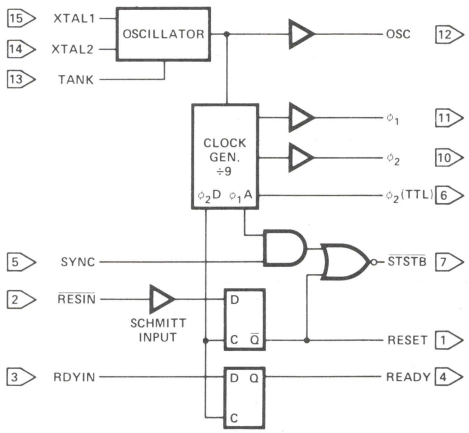
Also included are circuits to provide power-up reset, advance status strobe, and synchronization of ready.

The 8224 provides the designer with a significant reduction of packages used to generate clocks and timing for 8080A.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

RESIN	RESET INPUT
RESET	RESET OUTPUT
RDYIN	READY INPUT
READY	READY OUTPUT
SYNC	SYNC INPUT
STSTB	STATUS STB (ACTIVE LOW)
ϕ_1	8080 CLOCKS
ϕ_2	8080 CLOCKS

XTAL 1	CONNECTIONS FOR CRYSTAL
XTAL 2	CONNECTIONS FOR CRYSTAL
TANK	USED WITH OVERTONE XTAL
OSC	OSCILLATOR OUTPUT
ϕ_2 (TTL)	ϕ_2 CLK (TTL LEVEL)
V_{CC}	+5V
V_{DD}	+12V
GND	0V

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . −65°C to 150°C
Supply Voltage, V_{CC} . . . . . −0.5V to +7V
Supply Voltage, V_{DD} . . . . . −0.5V to +13.5V
Input Voltage . . . . . −1.5V to +7V
Output Current 100mA

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = 0°C to 70°C; V_{CC} = +5.0V ±5%; V_{DD} = +12V ±5%.

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Units	Test Conditions
I_F	Input Current Loading			-.25	mA	V_F = .45V
I_R	Input Leakage Current			10	μA	V_R = 5.25V
V_C	Input Forward Clamp Voltage			1.0	V	I_C = -5mA
V_{IL}	Input "Low" Voltage			.8	V	V_{CC} = 5.0V
V_{IH}	Input "High" Voltage	2.6 2.0			V	Reset Input All Other Inputs
V_{IH}-V_{IL}	RESIN Input Hysteresis	.25			V	V_{CC} = 5.0V
V_{OL}	Output "Low" Voltage			.45 .45	V V	(ϕ_1,ϕ_2), Ready, Reset, $\overline{STSTB}$ I_{OL} =2.5mA All Other Outputs I_{OL} = 15mA
V_{OH}	Output "High" Voltage ϕ_1 , ϕ_2 READY, RESET All Other Outputs	 9.4 3.6 2.4			 V V V	 I_{OH} = -100μA I_{OH} = -100μA I_{OH} = -1mA
I_{SC}[1]	Output Short Circuit Current (All Low Voltage Outputs Only)	-10		-60	mA	V_O = 0V V_{CC} = 5.0V
I_{CC}	Power Supply Current			115	mA	
I_{DD}	Power Supply Current			12	mA	

Note: 1. Caution, ϕ_1 and ϕ_2 output drivers do not have short circuit protection

Crystal Requirements

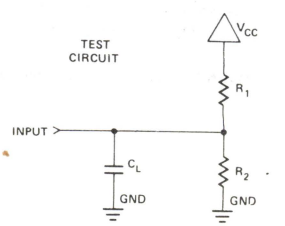
Tolerance: .005% at 0°C -70°C
Resonance: Series (Fundamental)*
Load Capacitance: 20-35pF
Equivalent Resistance: 75-20 ohms
Power Dissipation (Typ.) : 4mW

*With tank circuit use 3rd overtone mode.

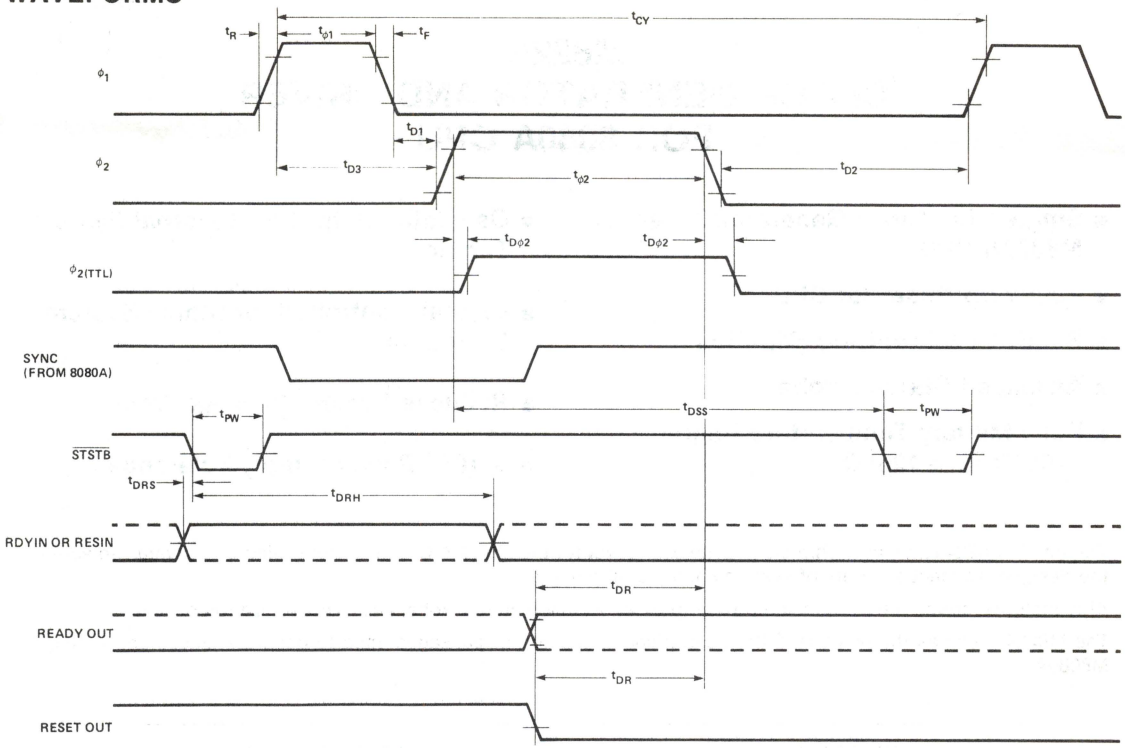
A.C. CHARACTERISTICS

V_{CC} = +5.0V ± 5%; V_{DD} = +12.0V ± 5%; T_A = 0°C to 70°C

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
$t_{\phi 1}$	ϕ_1 Pulse Width	$\frac{2tcy}{9}$ - 20ns			ns	C_L = 20pF to 50pF
$t_{\phi 2}$	ϕ_2 Pulse Width	$\frac{5tcy}{9}$ - 35ns				
t_{D1}	ϕ_1 to ϕ_2 Delay	0				
t_{D2}	ϕ_2 to ϕ_1 Delay	$\frac{2tcy}{9}$ - 14ns				
t_{D3}	ϕ_1 to ϕ_2 Delay	$\frac{2tcy}{9}$		$\frac{2tcy}{9}$ + 20ns		
t_R	ϕ_1 and ϕ_2 Rise Time			20		
t_F	ϕ_1 and ϕ_2 Fall Time			20		
$t_{D\phi 2}$	ϕ_2 to ϕ_2 (TTL) Delay	-5		+15	ns	ϕ_2TTL,CL=30 R_1=300Ω R_2=600Ω
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay	$\frac{6tcy}{9}$ - 30ns		$\frac{6tcy}{9}$		
t_{PW}	$\overline{STSTB}$ Pulse Width	$\frac{tcy}{9}$ - 15ns				$\overline{STSTB}$, CL=15pF R_1 = 2K R_2 = 4K
t_{DRS}	RDYIN Setup Time to Status Strobe	50ns - $\frac{4tcy}{9}$				
t_{DRH}	RDYIN Hold Time After $\overline{STSTB}$	$\frac{4tcy}{9}$				
t_{DR}	RDYIN or RESIN to ϕ_2 Delay	$\frac{4tcy}{9}$ - 25ns				Ready & Reset CL=10pF R_1=2K R_2=4K
t_{CLK}	CLK Period		$\frac{tcy}{9}$			
f_{max}	Maximum Oscillating Frequency			27	MHz	
C_{in}	Input Capacitance			8	pF	V_{CC}=+5.0V V_{DD}=+12V V_{BIAS}=2.5V f=1MHz



WAVEFORMS



VOLTAGE MEASUREMENT POINTS: ϕ_1, ϕ_2 Logic "0" = 1.0V, Logic "1" = 8.0V. All other signals measured at 1.5V.

EXAMPLE:

A.C. CHARACTERISTICS (For t_{CY} = 488.28 ns)

T_A = 0°C to 70°C; V_{DD} = +5V ±5%; V_{DD} = +12V ±5%.

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Units	Test Conditions
$t_{\phi 1}$	ϕ_1 Pulse Width	89			ns	t_{CY}=488.28ns
$t_{\phi 2}$	ϕ_2 Pulse Width	236			ns	
t_{D1}	Delay ϕ_1 to ϕ_2	0			ns	
t_{D2}	Delay ϕ_2 to ϕ_1	95			ns	ϕ_1 & ϕ_2 Loaded to C_L = 20 to 50pF
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	109		129	ns	
t_r	Output Rise Time			20	ns	
t_f	Output Fall Time			20	ns	
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay	296		326	ns	
$t_{D\phi 2}$	ϕ_2 to ϕ_2 (TTL) Delay	-5		+15	ns	
t_{PW}	Status Strobe Pulse Width	40			ns	Ready & Reset Loaded to 2mA/10pF
t_{DRS}	RDYIN Setup Time to $\overline{STSTB}$	-167			ns	
t_{DRH}	RDYIN Hold Time after $\overline{STSTB}$	217			ns	All measurements referenced to 1.5V unless specified otherwise.
t_{DR}	READY or RESET to ϕ_2 Delay	192			ns	
f_{MAX}	Oscillator Frequency			18.432	MHz	

MILITARY TEMP.

M8224
CLOCK GENERATOR AND DRIVER FOR 8080A CPU

- **Single Chip Clock Generator/Driver for M8080A CPU**
- **Power-Up Reset for CPU**
- **Ready Synchronizing Flip-Flop**
- **Advanced Status Strobe**
- **Fully Military Temperature Range −55°C to +125°C**
- **Oscillator Output for External System Timing**
- **Crystal Controlled for Stable System Operation**
- **Reduces System Package Count**
- **±10% Power Supply Tolerance**

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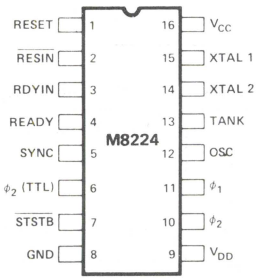
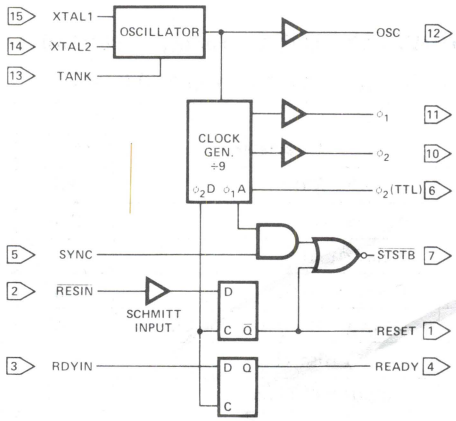
The M8224 provides the designer with a significant reduction of packages used to generate clocks and timing for M8080A.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

$\overline{\text{RESIN}}$	RESET INPUT
RESET	RESET OUTPUT
RDYIN	READY INPUT
READY	READY OUTPUT
SYNC	SYNC INPUT
$\overline{\text{STSTB}}$	STATUS STB (ACTIVE LOW)
ϕ_1	8080 CLOCKS
ϕ_2	

XTAL 1	CONNECTIONS FOR CRYSTAL
XTAL 2	
TANK	USED WITH OVERTONE XTAL
OSC	OSCILLATOR OUTPUT
ϕ_2 (TTL)	ϕ_2 CLK (TTL LEVEL)
V_{CC}	+5V
V_{DD}	+12V
GND	0V

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-55°C to 125°C
Storage Temperature	-65°C to 150°C
Supply Voltage, V_{CC}	-0.5V to +7V
Supply Voltage, V_{DD}	-0.5V to +13.5V
Input Voltage	-1.0V to +7V
Output Current	100mA

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = -55°C to 125°C; V_{CC} = +5.0V ±10%; V_{DD} = +12V ±10%.

Symbol	Parameter	Limits Min.	Typ.	Max.	Units	Test Conditions
I_F	Input Current Loading			-.25	mA	V_F = .45V
I_R	Input Leakage Current			10	μA	V_R = 5.5V
V_C	Input Forward Clamp Voltage			-1.2	V	I_C = -5mA
V_{IL}	Input "Low" Voltage			.8	V	V_{CC} = 5.0V
V_{IH}	Input "High" Voltage $\overline{RESIN}$ All Other Inputs	2.6 2.0			V	
V_{IH}-V_{IL}	$\overline{RESIN}$ Input Hysteresis	.25			V	V_{CC} = 5.0V
V_{OL}	Output "Low" Voltage OSC, φ2 (TTL)			.45	V	I_{OL} = 10mA
	All Other Outputs			.45	V	I_{OL} = 2.5mA
V_{OH}	Output "High" Voltage					
	ϕ_1 , ϕ_2	9.0			V	I_{OH} = -100μA
	READY, RESET	3.3			V	I_{OH} = -100μA
	OSC, φ2 (TTL), $\overline{STSTB}$	2.4			V	I_{OH} = -1mA
I_{OS}[1]	Output Short Circuit Current (All Low Voltage Outputs Only)	-10		-60	mA	V_O = 0V V_{CC} = 5.0V
I_{CC}	Power Supply Current			115	mA	
I_{DD}	Power Supply Current			12	mA	

Note: 1. Caution, ϕ_1 and ϕ_2 output drivers do not have short circuit protection

Crystal Requirements

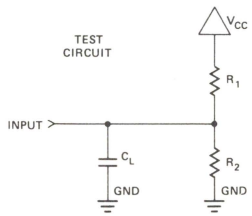
Tolerance: .005% at -55°C to 125°C
Resonance: Series (Fundamental)*
Load Capacitance: 20-35pF
Equivalent Resistance: 75-20 ohms
Power Dissipation (Min): 4mW

*With tank circuit use 3rd overtone mode.

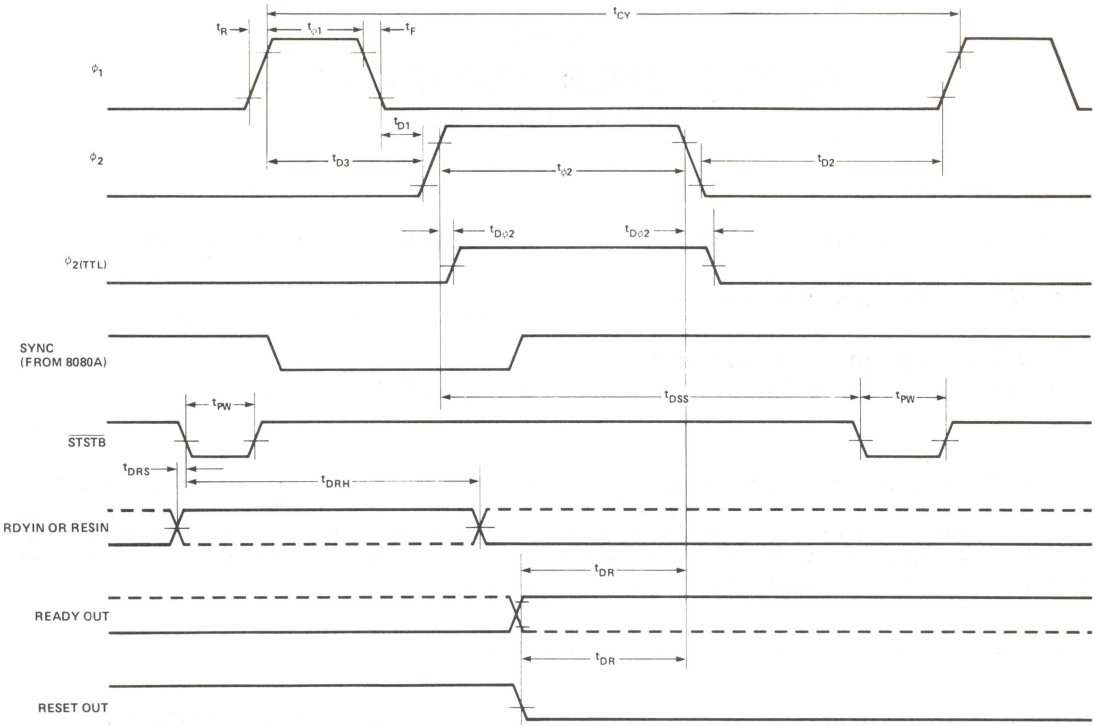
A.C. CHARACTERISTICS

V_{CC} = +5.0 ±10%; V_{DD} = +12.0V ±10%; T_A = -55°C to +125°C

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
$t_{\phi 1}$	ϕ_1 Pulse Width	$\frac{2tcy}{9}$ - 20ns			ns	C_L = 20pF to 50pF
$t_{\phi 2}$	ϕ_2 Pulse Width	$\frac{5tcy}{9}$ - 45ns				
t_{D1}	ϕ_1 to ϕ_2 Delay	0				
t_{D2}	ϕ_2 to ϕ_1 Delay	$\frac{2tcy}{9}$ - 25ns				
t_{D3}	ϕ_1 to ϕ_2 Delay	$\frac{2tcy}{9}$		$\frac{2tcy}{9}$ + 40ns		
t_R	ϕ_1 and ϕ_2 Rise Time			25		
t_F	ϕ_1 and ϕ_2 Fall Time			25		
$t_{D\phi 2}$	ϕ_2 to ϕ_2 (TTL) Delay	-5		+15	ns	ϕ_2TTL, CL=30pF R_1=300Ω R_2=600Ω
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay	$\frac{6tcy}{9}$ - 30ns		$\frac{6tcy}{9}$		$\overline{STSTB}$, CL=15pF R_1 = 2K R_2 = 4K
t_{PW}	$\overline{STSTB}$ Pulse Width	$\frac{tcy}{9}$ - 23ns				
t_{DRS}	RDYIN Setup Time to Status Strobe	50ns - $\frac{4tcy}{9}$				
t_{DRH}	RDYIN Hold Time After $\overline{STSTB}$	$\frac{4tcy}{9}$				
t_{DR}	READY or RESET to ϕ_2 Delay	$\frac{4tcy}{9}$ - 25ns				CL=10pF R_1=2K R_2=4K
t_{CLK}	CLK Period		$\frac{tcy}{9}$			
f_{max}	Maximum Oscillating Frequency	27			MHz	
C_{in}	Input Capacitance			8	pF	V_{CC}=+5.0V V_{DD}=+12V V_{BIAS}=2.5V f=1MHz



WAVEFORMS



VOLTAGE MEASUREMENT POINTS: ϕ_1, ϕ_2 Logic "0" = 1.0V, Logic "1" = 7.0V. READY, RESET Logic "0" = 0.8V, Logic "1" = 3.0V. All other signals measured at 1.5V.

Example:

A.C. CHARACTERISTICS (For t_{CY} = 488.28 ns.)

T_A = -55°C to 125°C; V_{DD} = +5V ±10%; V_{DD} = +12V ±10%.

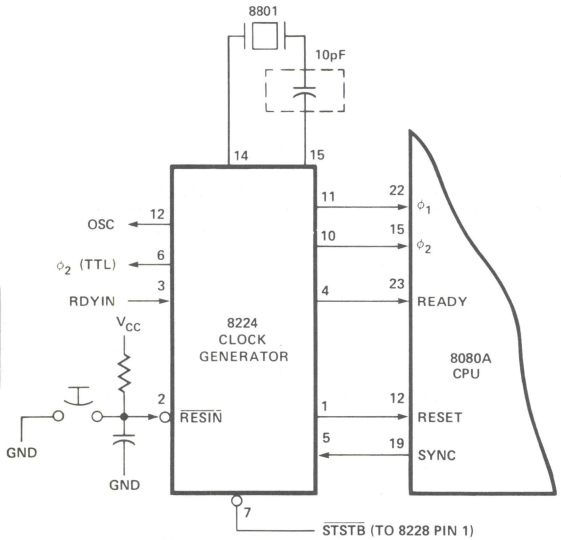
Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Units	Test Conditions
$t_{\phi 1}$	ϕ_1 Pulse Width	89			ns	t_{CY}=488.28ns
$t_{\phi 2}$	ϕ_2 Pulse Width	226			ns	
t_{D1}	Delay ϕ_1 to ϕ_2	0			ns	
t_{D2}	Delay ϕ_2 to ϕ_1	84			ns	ϕ_1 & ϕ_2 Loaded to C_L = 20 to 50pF
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	109		149	ns	
t_r	Output Rise Time			25	ns	
t_f	Output Fall Time			25	ns	
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay	296		326	ns	
$t_{D\phi 2}$	ϕ_2 to ϕ_2 (TTL) Delay	-5		+15	ns	
t_{PW}	Status Strobe Pulse Width	31			ns	Ready & Reset Loaded to 2mA/10pF
t_{DRS}	RDYIN Setup Time to $\overline{STSTB}$	-167			ns	
t_{DRH}	RDYIN Hold Time after $\overline{STSTB}$	217			ns	All measurements referenced to 1.5V unless specified otherwise.
t_{DR}	READY or RESET to ϕ_2 Delay	192			ns	

8801
CLOCK GENERATOR CRYSTAL FOR 8224/8080A

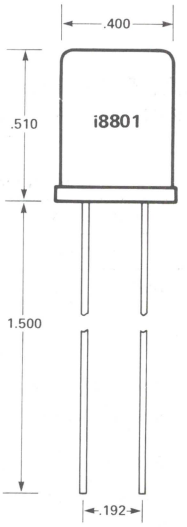
- **Specifically Selected for Intel® 8224**
- **18.432 MHz for 1.95 μs 8080A Cycle**
- **Simple Generation of all Standard Communication Baud Rates**
- **Frequency Deviation ±0.005%**
- **Fundamental Frequency Mode**
- **0°C to 70°C Operating Temperature**

The Intel® 8801 is a quartz crystal specifically selected to operate with the 8224 clock generator and the 8080A CPU. It resonates in the fundamental frequency mode at 18.432 MHz. This frequency allows the 8080A at full speed (T_{CY} = 488 ns) to have a cycle of 1.95 μs and also simplifies the generation of all standard communication baud rates. The 8801 crystal is exactly matched to the requirements of the 8080A/8224 and provides both high performance and system flexibility for the microcomputer designer.

8801 INTERFACE



PACKAGING INFORMATION



APPLICATIONS

The selection of 18.432 MHz provides the 8080A with clocks whose period is 488ns. This allows the 8080A to operate at very close to its maximum specified speed (480 ns). The 8224, when used with the 8801, outputs a signal on its OSC pin that is an approximately symetrical square wave at a frequency of 18.432 MHz. This frequency signal can be easily divided down to generate an accurate, stable baud rate clock that can be connected directly to the transmitter or receiver clocks of the 8251 USART. This feature allows the designer to support most standard communication interfaces with a minimum of extra hardware.

The chart below (Fig. 1) shows the equivalent baud rates that are generated with the corresponding dividers.

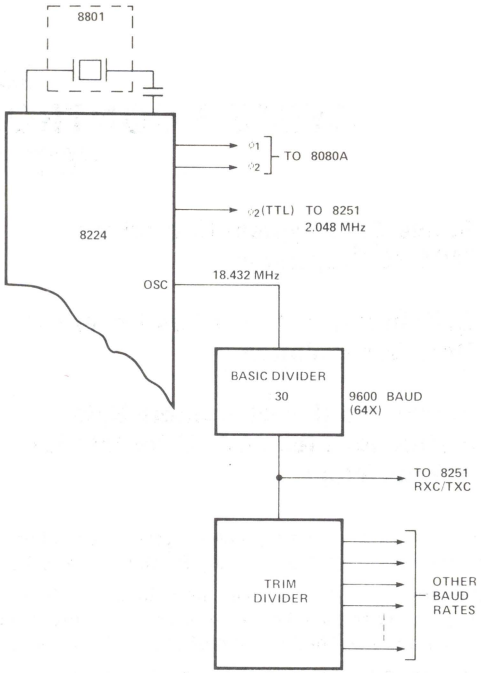


Figure 1. Block Diagram

BAUD RATE 64x	BAUD RATE 16x	FREQUENCY	BASIC DIVIDER	PLUS TRIM DIVIDER
9600		614.4 KH	÷30	–
4800	19.2K	307.2 KH	÷30	÷2
2400	9600	153.6 KH	÷30	÷4
1200	4800	76.8 KH	÷30	÷8
600	2400	38.4 KH	÷30	÷16
300	1200	19.2 KH	÷30	÷32
	600	9.6 KH	÷30	÷64
	300	4.8 KH	÷30	÷128
*109.1		6.982 KH	÷30	÷88

*For 109.1 (64x) Baud rate divide 1200 Baud Frequency (76.8 KH) by 11.

Figure 2. Baud Rate Chart

ELECTRICAL CHARACTERISTICS

Recommended Drive Level 5mW
Type of Resonance . . . . . Series
Equivalent Resistance . . . . . 20 ohms
Maximum Shunt Capacity 7pF
Maximum Frequency Deviation
0° – 70°C . . . . . ±.005%
-55°– 125°C . . . . . ±.002%

8228/8238
SYSTEM CONTROLLER AND BUS DRIVER FOR 8080A CPU

- **Single Chip System Control for MCS-80™ Systems**
- **Built-In Bidirectional Bus Driver for Data Bus Isolation**
- **Allows the Use of Multiple Byte Instructions (e.g. CALL) for Interrupt Acknowledge**
- **User Selected Single Level Interrupt Vector (RST 7)**
- **28-Pin Dual In-Line Package**
- **Reduces System Package Count**
- ***8238 Has Advanced IOW/MEMW for Large System Timing Control**

The Intel® 8228 is a single chip system controller and bus driver for MCS-80. It generates all signals required to directly interface MCS-80 family RAM, ROM, and I/O components.

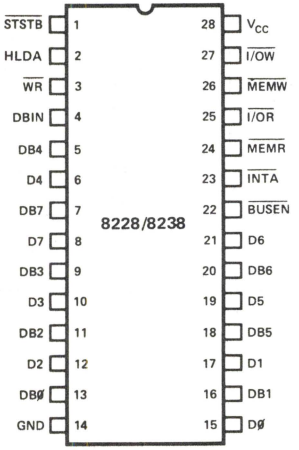
A bidirectional bus driver is included to provide high system TTL fan-out. It also provides isolation of the 8080 data bus from memory and I/O. This allows for the optimization of control signals, enabling the systems designer to use slower memory and I/O. The isolation of the bus driver also provides for enhanced system noise immunity.

A user selected single level interrupt vector (RST 7) is provided to simplify real time, interrupt driven, small system requirements. The 8228 also generates the correct control signals to allow the use of multiple byte instructions (e.g., CALL) in response to an interrupt acknowledge by the 8080A. This feature permits large, interrupt driven systems to have an unlimited number of interrupt levels.

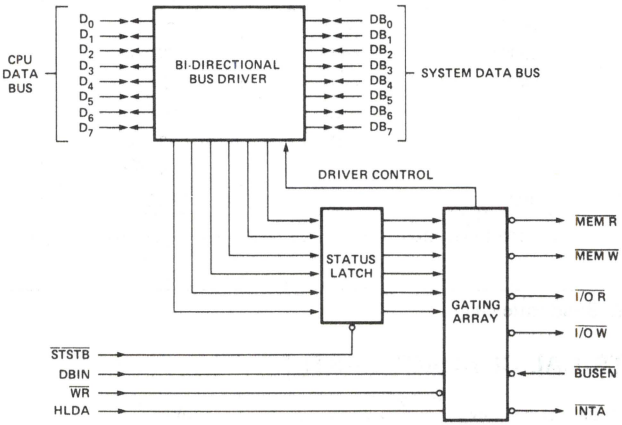
The 8228 is designed to support a wide variety of system bus structures and also reduce system package count for cost effective, reliable design of the MCS-80 systems.

MCS-80/85

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

D7-D0	DATA BUS (8080 SIDE)	INTA	INTERRUPT ACKNOWLEDGE
DB7-DB0	DATA BUS (SYSTEM SIDE)	HLDA	HLDA (FROM 8080)
I/OR	I/O READ	WR	WR (FROM 8080)
I/OW	I/O WRITE	BUSEN	BUS ENABLE INPUT
MEMR	MEMORY READ	STSTB	STATUS STROBE (FROM 8224)
MEMW	MEMORY WRITE	V_{CC}	+5V
DBIN	DBIN (FROM 8080)	GND	0 VOLTS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . −0°C to 70°C
Storage Temperature . . . . . −65°C to 150°C
Supply Voltage, V_{CC} . . . . . −0.5V to +7V
Input Voltage . . . . . −1.5V to +7V
Output Current 100mA

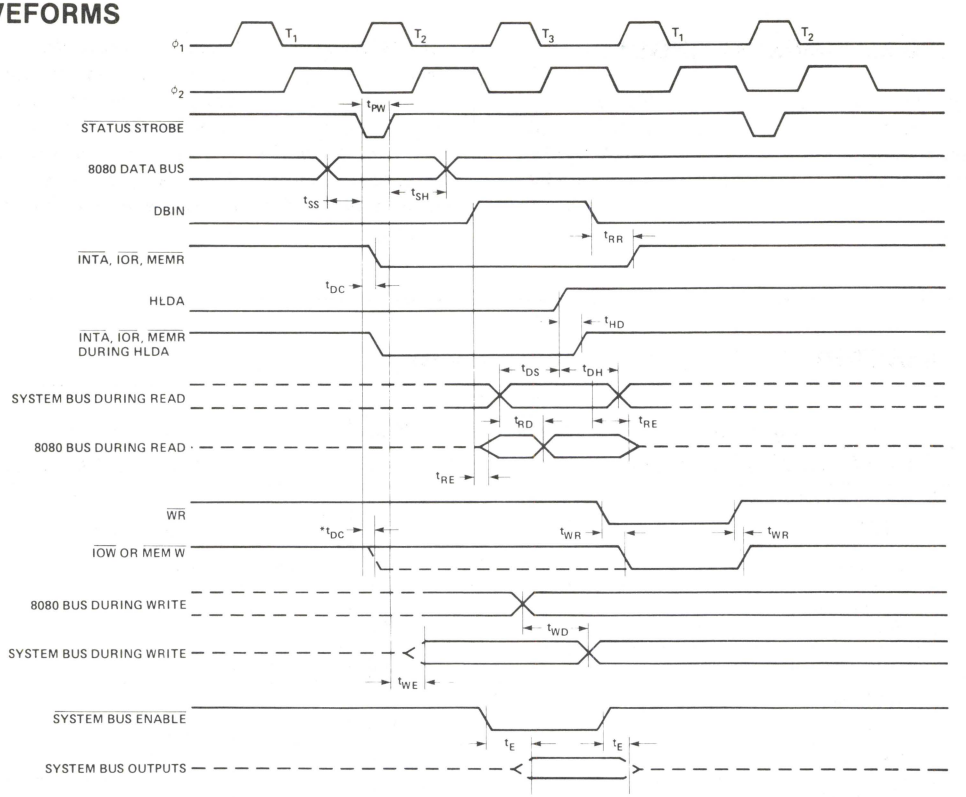
**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS T_A = 0°C to 70°C; V_{CC} = 5V ±5%.

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
V_C	Input Clamp Voltage, All Inputs		.75	-1.0	V	V_{CC}=4.75V; I_C=-5mA
I_F	Input Load Current, $\overline{STSTB}$			500	μA	V_{CC} = 5.25V
	D_2 & D_6			750	μA	V_F = 0.45V
	D_0, D_1, D_4, D_5, & D_7			250	μA	
	All Other Inputs			250	μA	
I_R	Input Leakage Current $\overline{STSTB}$			100	μA	V_{CC} = 5.25V
	DB_0-DB_7			20	μA	V_R = 5.25V
	All Other Inputs			100	μA	
V_{TH}	Input Threshold Voltage, All Inputs	0.8		2.0	V	V_{CC} = 5V
I_{CC}	Power Supply Current		140	190	mA	V_{CC}=5.25V
V_{OL}	Output Low Voltage, D_0-D_7			.45	V	V_{CC}=4.75V; I_{OL}=2mA
	All Other Outputs			.45	V	I_{OL} = 10mA
V_{OH}	Output High Voltage, D_0-D_7	3.6	3.8		V	V_{CC}=4.75V; I_{OH}=-10μA
	All Other Outputs	2.4			V	I_{OH} = -1mA
I_{OS}	Short Circuit Current, All Outputs	15		90	mA	V_{CC}=5V
$I_{O(off)}$	Off State Output Current, All Control Outputs			100	μA	V_{CC}=5.25V; V_O=5.25
				-100	μA	V_O=.45V
I_{INT}	INTA Current			5	mA	(See Figure below)

Note 1: Typical values are for T_A = 25°C and nominal supply voltages.

WAVEFORMS



VOLTAGE MEASUREMENT POINTS: D_0-D_7 (when outputs) Logic "0" = 0.8V, Logic "1" = 3.0V. All other signals measured at 1.5V.

*ADVANCED $\overline{IOW}$/$\overline{MEMW}$ FOR 8238 ONLY.

A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$; $V_{CC} = 5V \pm 5\%$.

Symbol	Parameter	Limits		Units	Condition
		Min.	Max.		
t_{PW}	Width of Status Strobe	22		ns	
t_{SS}	Setup Time, Status Inputs D_0-D_7	8		ns	
t_{SH}	Hold Time, Status Inputs D_0-D_7	5		ns	
t_{DC}	Delay from $\overline{STSTB}$ to any Control Signal	20	60	ns	C_L = 100pF
t_{RR}	Delay from DBIN to Control Outputs		30	ns	C_L = 100pF
t_{RE}	Delay from DBIN to Enable/Disable 8080 Bus		45	ns	C_L = 25pF
t_{RD}	Delay from System Bus to 8080 Bus during Read		30	ns	C_L = 25pF
t_{WR}	Delay from $\overline{WR}$ to Control Outputs	5	45	ns	C_L = 100pF
t_{WE}	Delay to Enable System Bus DB_0-DB_7 after $\overline{STSTB}$		30	ns	C_L = 100pF
t_{WD}	Delay from 8080 Bus D_0-D_7 to System Bus DB_0-DB_7 during Write	5	40	ns	C_L = 100pF
t_E	Delay from $\overline{System\ Bus\ Enable}$ to System Bus DB_0-DB_7		30	ns	C_L = 100pF
t_{HD}	HLDA to Read Status Outputs		25	ns	
t_{DS}	Setup Time, System Bus Inputs to HLDA	10		ns	
t_{DH}	Hold Time, System Bus Inputs to HLDA	20		ns	C_L = 100pF

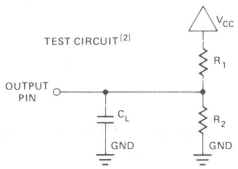
CAPACITANCE

This parameter is periodically sampled and not 100% tested.

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit
C_{IN}	Input Capacitance		8	12	pF
C_{OUT}	Output Capacitance Control Signals		7	15	pF
I/O	I/O Capacitance (D or DB)		8	15	pF

Test Conditions: NS: $V_{BIAS} = 2.5V$, $V_{CC} = 5.0V$, $T_A = 25°C$, f = 1MHz.

Note 2: For D_0-D_7: $R_1 = 4K\Omega$, $R_2 = \infty\Omega$, $C_L = 25pF$. For all other outputs: $R_1 = 500\Omega$, $R_2 = 1K\Omega$, $C_L = 100pF$.



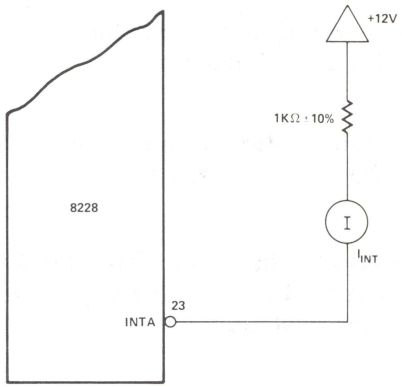


Figure 1. INTA Test Circuit (for RST 7)

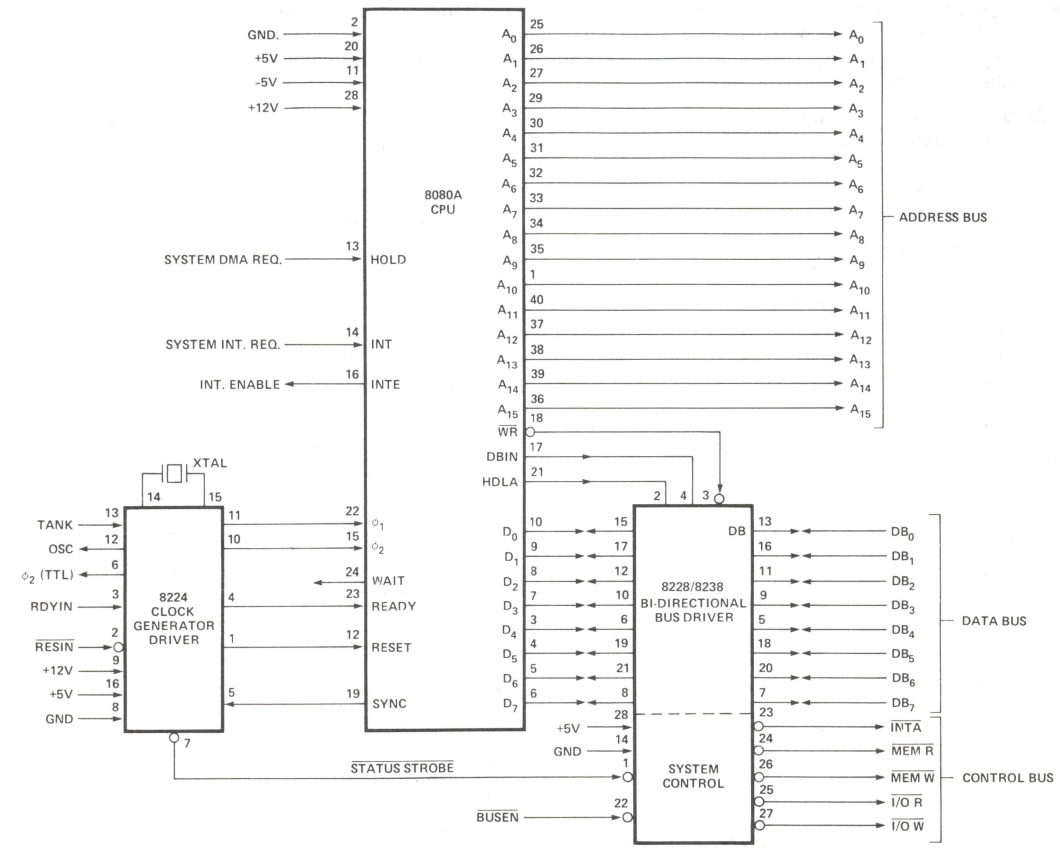


Figure 2. CPU Standard Interface

MILITARY TEMP.

M8228
SYSTEM CONTROLLER AND BUS DRIVER FOR M8080A CPU

- **Single Chip System Control for MCS-80™ Systems**
- **Built-In Bidirectional Bus Driver for Data Bus Isolation**
- **Allows the Use of Multiple Byte Instructions (e.g. CALL) for Interrupt Acknowledge**
- **User Selected Single Level Interrupt Vector (RST 7)**
- **28-Pin Dual In-Line Package**
- **Reduces System Package Count**
- **Full Military Temperature Range −55°C to +125°C**
- **±10% Power Supply Tolerance**

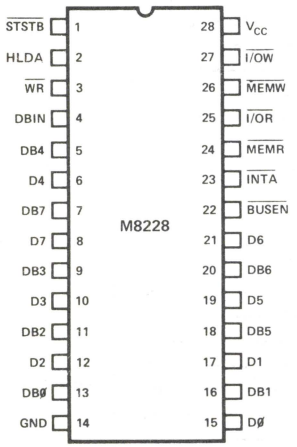
The Intel® M8228 is a single chip system controller and bus driver for MCS-80. It generates all signals required to directly interface MCS-80 family RAM, ROM, and I/O components.

A bidirectional bus driver is included to provide high system TTL fan-out. It also provides isolation of the 8080 data bus from memory and I/O. This allows for the optimization of control signals, enabling the systems designer to use slower memory and I/O. The isolation of the bus driver also provides for enhanced system noise immunity.

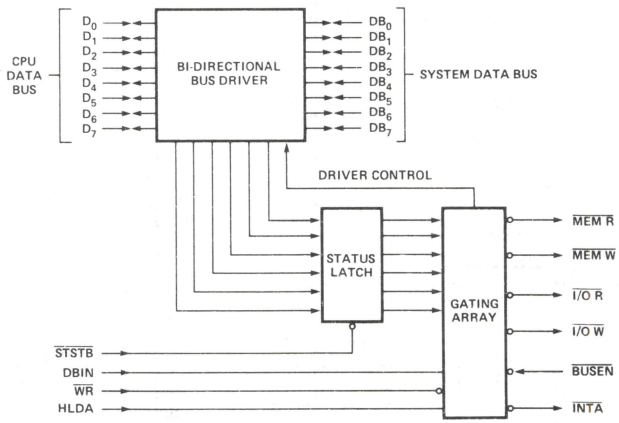
A user selected single level interrupt vector (RST 7) is provided to simplify real time, interrupt driven, small system requirements. The M8228 also generates the correct control signals to allow the use of multiple byte instructions (e.g., CALL) in response to an interrupt acknowledge by the M8080A. This feature permits large, interrupt driven systems to have an unlimited number of interrupt levels.

The M8228 is designed to support a wide variety of system bus structures and also reduce system package count for cost effective, reliable, design of the MCS-80 systems.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

D7-D0	DATA BUS (8080 SIDE)	$\overline{INTA}$	INTERRUPT ACKNOWLEDGE
DB7-DB0	DATA BUS (SYSTEM SIDE)	HLDA	HLDA (FROM 8080)
$\overline{I/OR}$	I/O READ	$\overline{WR}$	WR (FROM 8080)
$\overline{I/OW}$	I/O WRITE	$\overline{BUSEN}$	BUS ENABLE INPUT
$\overline{MEMR}$	MEMORY READ	$\overline{STSTB}$	STATUS STROBE (FROM 8224)
$\overline{MEMW}$	MEMORY WRITE	V_{CC}	+5V
DBIN	DBIN (FROM 8080)	GND	0 VOLTS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . -55°C to 125°C
Storage Temperature . . . . . -65°C to 150°C
Supply Voltage, V_{CC} . . . . . -0.5V to +7V
Input Voltage . . . . . -1.0V to +7V
Output Current 100mA

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS T_A = -55°C to 125°C; V_{CC} = 5V ±10%.

Symbol	Parameter	Limits Min.	Limits Max.	Unit	Test Conditions
V_C	Input Clamp Voltage, All Inputs		-1.2	V	I_C = -5mA
I_F	Input Load Current, $\overline{STSTB}$		500	μA	V_F = 0.4V
	D_2, D_6		750	μA	
	D_0, D_1, D_4, D_5, D_7		250	μA	
	All Other Inputs		250	μA	
I_R	Input Leakage Current DB_0 - D_7		20	μA	V_R = 5.5V
	All Other Inputs		100	μA	
V_{TH}	Input Threshold Voltage, All Inputs	0.8	2.0	V	V_{CC} = 5V
I_{CC}	Power Supply Current		210	mA	
V_{OL}	Output Low Voltage, D_0 - D_7		.5	V	I_{OL} = 2mA
	All Other Outputs		.5	V	I_{OL} = 10mA
V_{OH}	Output High Voltage, D_0 - D_7	3.3		V	I_{OH} = -10μA
	All Other Outputs	2.4		V	I_{OH} = -1mA
I_{OS}	Short Circuit Current, All Outputs	15	90	mA	V_{CC} = 5V
$I_{O\ (Off)}$	Off State Output Current, All Controls Outputs		100	μA	V_O = 5.5V
			-100	μA	V_O = .45V
I_{INT}	$\overline{INTA}$ Current		5	mA	(See Figure 1)

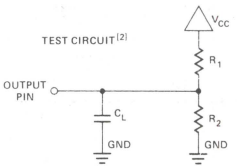
Note 1: Typical values are for T_A = 25°C and nominal supply voltages.

CAPACITANCE This parameter is periodically sampled and not 100% tested.

Symbol	Parameter	Limits			Unit
		Min.	Typ.[1]	Max.	
C_{IN}	Input Capacitance		8	12	pF
C_{OUT}	Output Capacitance Control Signals		7	15	pF
I/O	I/O Capacitance (D or DB)		8	15	pF

TEST CONDITIONS: $V_{BIAS} = 2.5V$, $V_{CC} = 5.0V$, $T_A = 25°C$, $f = 1MHz$.

Note 2: For D_0-D_7: $R_1 = 4K\Omega$, $R_2 = \infty\Omega$, $C_L = 25pF$. For all other outputs: $R_1 = 500\Omega$, $R_2 = 1K\Omega$, $C_L = 100pF$.



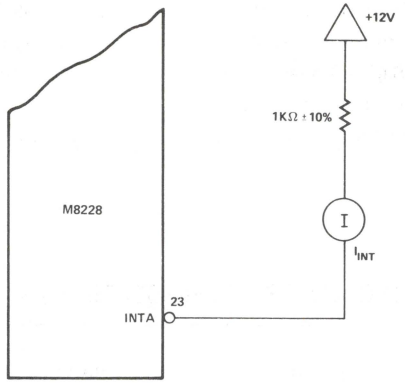


Figure 1. INTA Test Circuit (for RST 7)

A.C. CHARACTERISTICS $T_A = -55°C$ to $125°C$; $V_{CC} = 5V \pm 10\%$.

Symbol	Parameter	Limits		Units	Condition
		Min.	Max.		
t_{PW}	Width of Status Strobe	25		ns	
t_{SS}	Setup Time, Status Inputs D_0-D_7	8		ns	
t_{SH}	Hold Time, Status Inputs D_0-D_7	5		ns	
t_{DC}	Delay from $\overline{STSTB}$ to any Control Signal	20	75	ns	$C_L = 100pF$
t_{RR}	Delay from DBIN to Control Outputs		30	ns	$C_L = 100pF$
t_{RE}	Delay from DBIN to Enable/Disable 8080 Bus		45	ns	$C_L = 25pF$
t_{RD}	Delay from System Bus to 8080 Bus during Read		45	ns	$C_L = 25pF$
t_{WR}	Delay from $\overline{WR}$ to Control Outputs	5	60	ns	$C_L = 100pF$
t_{WE}	Delay to Enable System Bus DB_0-DB_7 after $\overline{STSTB}$		30	ns	$C_L = 100pF$
t_{WD}	Delay from 8080 Bus D_0-D_7 to System Bus DB_0-DB_7 during Write	5	40	ns	$C_L = 100pF$
t_E	Delay from $\overline{System\ Bus\ Enable}$ to System Bus DB_0-DB_7		30	ns	$C_L = 100pF$
t_{HD}	HLDA to Read Status Outputs		25	ns	$C_L = 100pF$
t_{DS}	Setup Time, System Bus Inputs to HLDA	10		ns	
t_{DH}	Hold Time, System Bus Inputs to HLDA	20		ns	

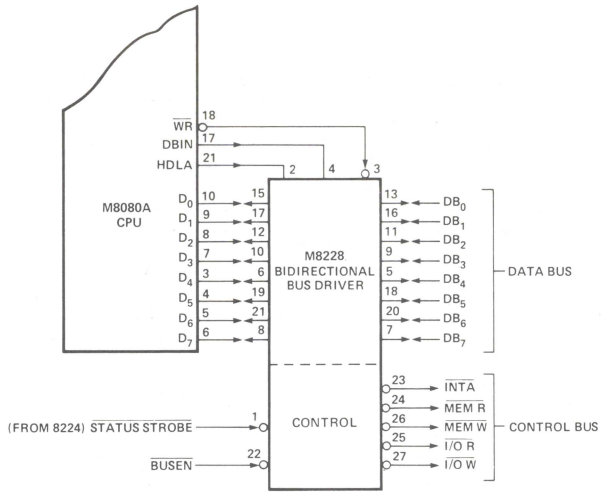


Figure 2. M8080A CPU Interface

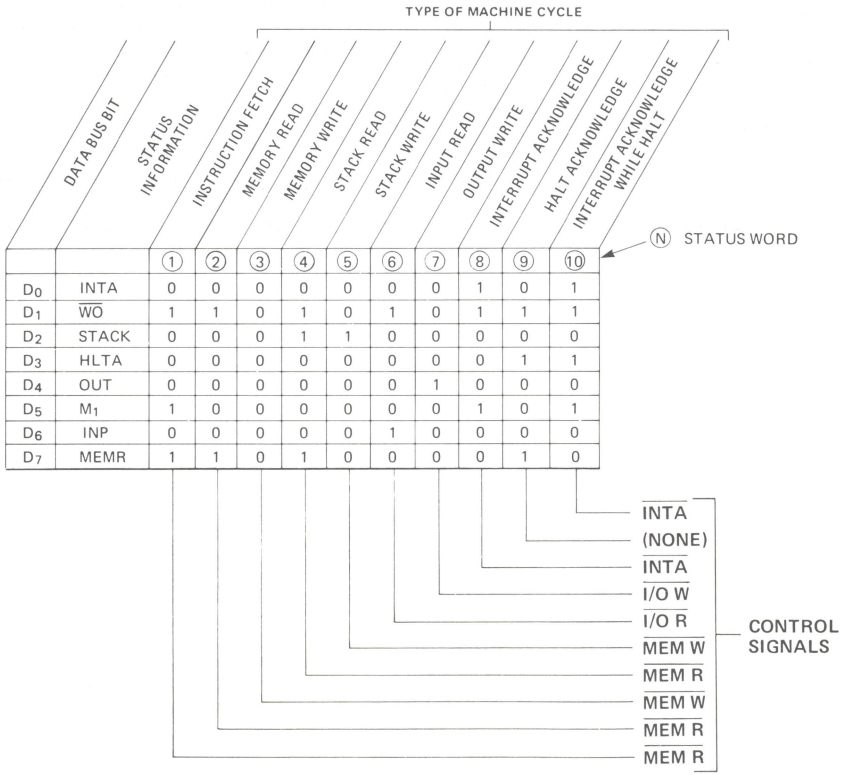
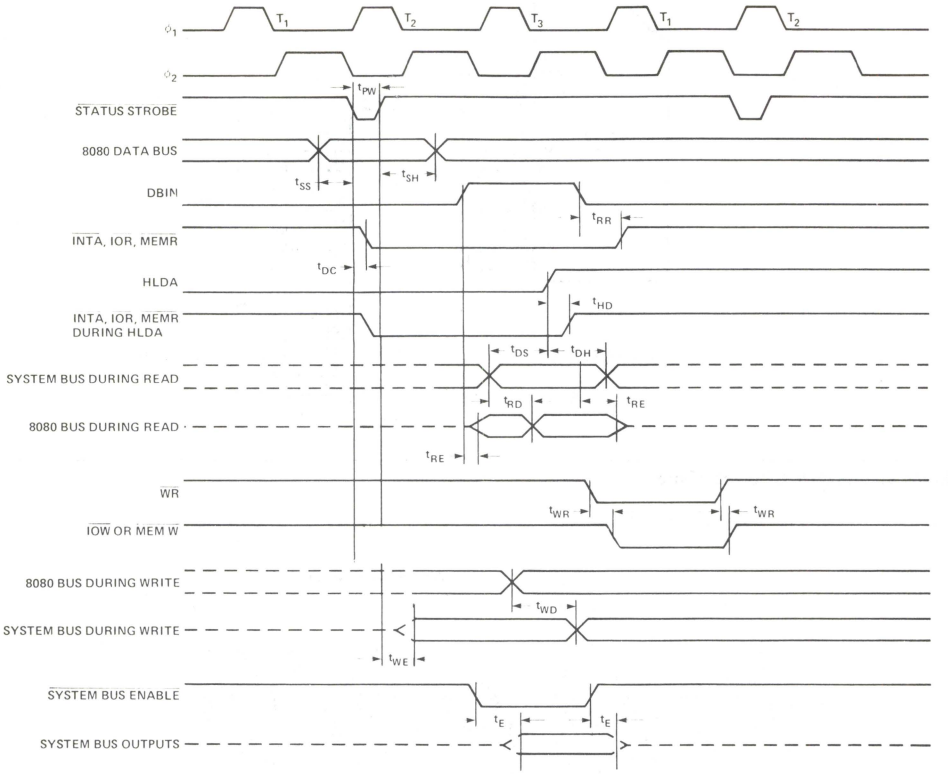


Figure 3. Status Word Chart

WAVEFORMS



VOLTAGE MEASUREMENT POINTS: D_0-D_7 (when outputs) Logic "0" = 0.8V, Logic "1" = 3.0V. All other signals measured at 1.5V.

8085A

SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSOR

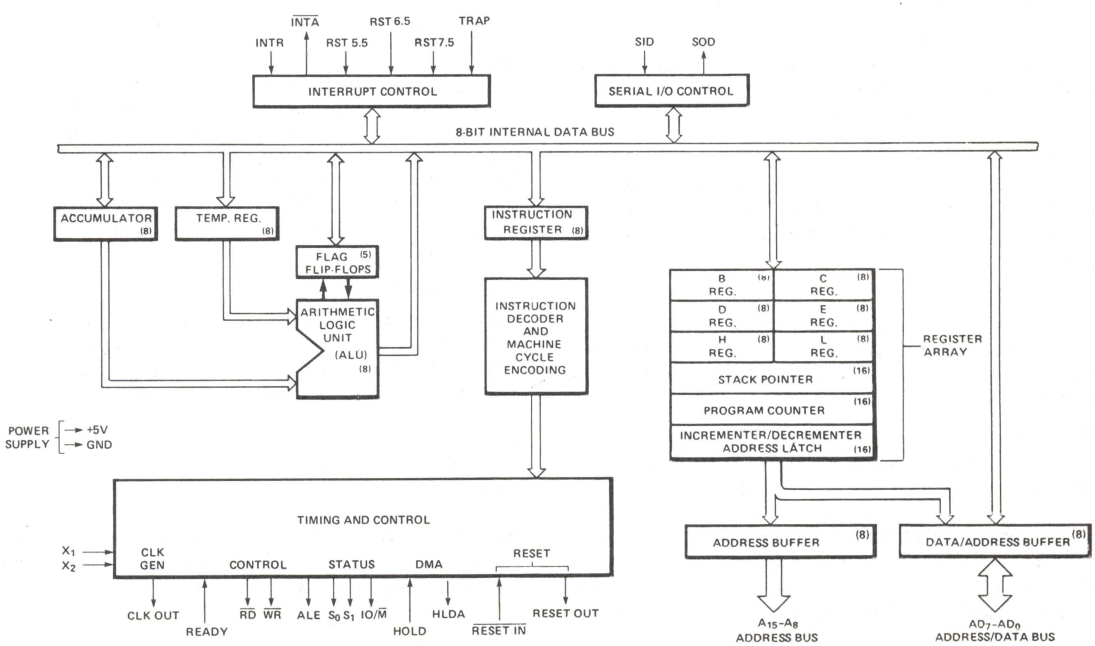
- **Single +5V Supply**
- **100% Software Compatible with 8080A**
- **1.3 μs Instruction Cycle**
- **On-Chip Clock Generator (with External Crystal or RC Network)**
- **On-Chip System Controller; Advanced Cycle Status Information Available for Large System Control**
- **4 Vectored Interrupts (One is Non-Maskable)**
- **Serial In/Serial Out Port**
- **Decimal, Binary, and Double Precision Arithmetic**
- **Direct Addressing Capability to 64K Bytes of Memory**

The Intel® 8085A is a new generation, complete 8 bit parallel central processing unit (CPU). Its instruction set is 100% software compatible with the 8080A microprocessor, and it is designed to improve the present 8080's performance by higher system speed. Its high level of system integration allows a minimum system of 3 IC's: 8085A (CPU), 8156 (RAM), and 8355/8755A (ROM/PROM).

The 8085A incorporates all of the features that the 8224 (clock generator) and 8228 (system controller) provided for the 8080, thereby offering a high level of system integration.

The 8085A uses a multiplexed data bus. The address is split between the 8-bit address bus and the 8-bit data bus. The on-chip address latches of 8155/8156/8355/8755A memory products allows a direct interface with the 8085A.

BLOCK DIAGRAM



MCS-80/85

PIN DESCRIPTION

The following describes the function of each pin:

A_8-A_{15} (Output 3-State)

Address Bus; The most significant 8-bits of the memory address or the 8-bits of the I/O address, 3-stated during Hold and Halt modes.

AD_{0-7} (Input/Output 3-state)

Multiplexed Address/Data Bus; Lower 8-bits of the memory address (or I/O address) appear on the bus during the first clock cycle of a machine state. It then becomes the data bus during the second and third clock cycles.

3-stated during Hold and Halt modes.

ALE (Output)

Address Latch Enable: It occurs during the first clock cycle of a machine state and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. ALE can also be used to strobe the status information. ALE is never 3-stated.

S0, S1 (Output)

Data Bus Status. Encoded status of the bus cycle:

S_1	S_0	
0	0	HALT
0	1	WRITE
1	0	READ
1	1	FETCH

S_1 can be used as an advanced R/$\overline{W}$ status.

$\overline{RD}$ (Output 3-state)

READ; indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer. 3-stated during Hold and Halt.

$\overline{WR}$ (Output 3-state)

WRITE; indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of $\overline{WR}$. 3-stated during Hold and Halt modes.

READY (Input)

If Ready is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If Ready is low, the CPU will wait for Ready to go high before completing the read or write cycle.

HOLD (Input)

HOLD; indicates that another Master is requesting the use of the Address and Data Buses. The CPU, upon receiving the Hold request, will relinquish the use of buses as soon as the completion of the current machine cycle. Internal processing can continue. The processor can regain the buses only after the Hold is removed. When the Hold is acknowledged, the Address, Data, $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$ lines are 3-stated.

HLDA (Output)

HOLD ACKNOWLEDGE; indicates that the CPU has received the Hold request and that it will relinquish the buses in the next clock cycle. HLDA goes low after the Hold request is removed. The CPU takes the buses one half clock cycle after HLDA goes low.

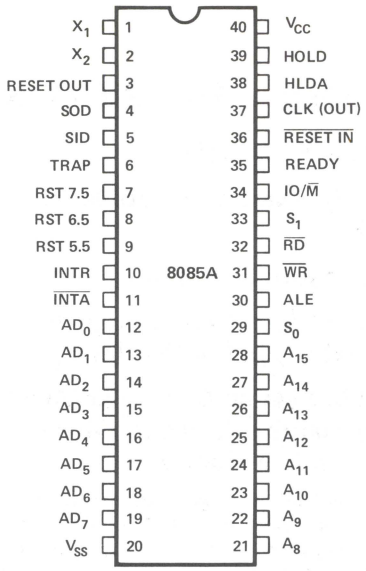


Figure 1. Pin Configuration

INTR (Input)

INTERRUPT REQUEST; is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of the instruction. If it is active, the Program Counter (PC) will be inhibited from incrementing and an $\overline{INTA}$ will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.

$\overline{INTA}$ (Output)

INTERRUPT ACKNOWLEDGE; is used instead of (and has the same timing as) $\overline{RD}$ during the Instruction cycle after an INTR is accepted. It can be used to activate the 8259 Interrupt chip or some other interrupt port.

RST 5.5
RST 6.5
RST 7.5
(Inputs)

RESTART INTERRUPTS; These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted.

RST 7.5 → Highest Priority
RST 6.5
RST 5.5 → Lowest Priority

The priority of these interrupts is ordered as shown above. These interrupts have a higher priority than the INTR.

TRAP (Input)

Trap interrupt is a nonmaskable restart interrupt. It is recognized at the same time as INTR. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt.

$\overline{\text{RESET IN}}$ (Input)

Reset sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. None of the other flags or registers (except the instruction register) are affected. The CPU is held in the reset condition as long as Reset is applied.

RESET OUT (Output)

Indicates CPU is being reset. Can be used as a system RESET. The signal is synchronized to the processor clock.

X_1, X_2 (Input)

Crystal or R/C network connections to set the internal clock generator. X1 can also be an external clock input instead of a crystal. The input frequency is divided by 2 to give the internal operating frequency.

CLK (Output)

Clock Output for use as a system clock when a crystal or R/C network is used as an input to the CPU. The period of CLK is twice the X_1, X_2 input period.

IO/$\overline{\text{M}}$ (Output)

IO/$\overline{\text{M}}$ indicates whether the Read/Write is to memory or I/O. Tri-stated during Hold and Halt modes.

SID (Input)

Serial input data line. The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.

SOD (output)

Serial output data line. The output SOD is set or reset as specified by the SIM instruction.

V_{CC}

+5 volt supply.

V_{SS}

Ground Reference.

FUNCTIONAL DESCRIPTION

The 8085A is a complete 8-bit parallel central processor. It is designed with N-channel depletion loads and requires a single +5 volt supply. Its basic clock speed is 3 MHz thus improving on the present 8080's performance with higher system speed. Also it is designed to fit into a minimum system of three IC's: The CPU, a RAM/IO, and a ROM or PROM/IO chip.

The 8085A uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first cycle the address is sent out. The lower 8-bits are latched into the peripherals by the Address Latch Enable (ALE). During the rest of the machine cycle the Data Bus is used for memory or I/O data.

The 8085A provides $\overline{\text{RD}}$, $\overline{\text{WR}}$, and IO/$\overline{\text{Memory}}$ signals for bus control. An Interrupt Acknowledge signal ($\overline{\text{INTA}}$) is also provided. Hold, Ready, and all Interrupts are synchronized. The 8085A also provides serial input data (SID) and serial output data (SOD) lines for simple serial interface.

In addition to these features, the 8085A has three maskable, restart interrupts and one nonmaskable trap interrupt.

8085A vs. 8080A

The 8085A includes the following features on-chip in addition to all of the 8080A functions.

a. Internal clock generator
b. Clock output
c. Fully synchronized Ready
d. Schmitt action on $\overline{\text{RESET IN}}$
e. RESET OUT pin
f. $\overline{\text{RD}}$, $\overline{\text{WR}}$, and IO/$\overline{\text{M}}$ Bus Control Signals
g. Encoded Status information
h. Multiplexed Address and Data
i. Direct Restarts and nonmaskable Interrupt
j. Serial Input/Output lines.

The internal clock generator requires an external crystal or R-C network. It will oscillate at twice the basic CPU operating frequency. A 50% duty cycle, two phase, nonoverlapping clock is generated from this oscillator internally and one phase of the clock ($\phi 2$) is available as an external clock. The 8085A directly provides the external RDY synchronization previously provided by the 8224. The $\overline{\text{RESET IN}}$ input is provided with a Schmitt action input so that power-on reset only requires a resistor and capacitor. RESET OUT is provided for System RESET.

The 8085A provides $\overline{\text{RD}}$, $\overline{\text{WR}}$ and IO/$\overline{\text{M}}$ signals for Bus control. An $\overline{\text{INTA}}$ which was previously provided by the 8228 in 8080 system is also included in 8085A.

Status Information

Status information is directly available from the 8085A. ALE serves as a status stobe. The status is partially encoded, and provides the user with advanced timing of the type of bus transfer being done. IO/$\overline{\text{M}}$ cycle status signal is provided directly also. Decoded S_0, S_1carries the following status information:

	S_1	S_0
HALT	0	0
WRITE	0	1
READ	1	0
FETCH	1	1

S1 can be interpreted as R/$\overline{\text{W}}$ in all bus transfers.

In the 8085A the 8 LSB of address are multiplexed with the data instead of status. The ALE line is used as a strobe to enter the lower half of the address into the memory or peripheral address latch. This also frees extra pins for expanded interrupt capability.

Interrupt and Serial I/O

The 8085A has 5 interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP. INTR is identical in function to the 8080 INT. Each of three RESTART inputs, 5.5, 6.5, 7.5, has a programmable mask. TRAP is also a RESTART interrupt except it is non-maskable.

The three RESTART interrupts cause the internal execution of RST (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The nonmaskable TRAP causes the internal execution of a RST independent of the state of the interrupt enable or masks.

Name	RESTART Address (Hex)
TRAP	24_{16}
RST 5.5	$2C_{16}$
RST 6.5	34_{16}
RST 7.5	$3C_{16}$

There are two different types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are high level-sensitive like INTR (and INT on the 8080) and are recognized with the same timing as INTR. RST 7.5 is rising edge-sensitive.

For RST 7.5, only a pulse is required to set an internal flip flop which generates the internal interrupt request. The RST 7.5 request flip flop remains set until the request is serviced. Then it is reset automatically. This flip flop may also be reset by using the SIM instruction or by issuing a RESET IN to the 8085A. The RST 7.5 internal flip flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out.

The status of the three RST interrupt masks can only be affected by the SIM instruction and RESET IN.

The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending as follows: TRAP - highest priority, RST 7.5, RST 6.5, RST 5.5, INTR - lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt a RST 7.5 routine if the interrupts were re-enabled before the end of the RST 7.5 routine.

The TRAP interrupt is useful for catastrophic errors such as power failure or bus error. The TRAP input is recognized just as any other interrupt but has the highest priority. It is not affected by any flag or mask. The TRAP input is both edge and level sensitive. The TRAP input must go high and

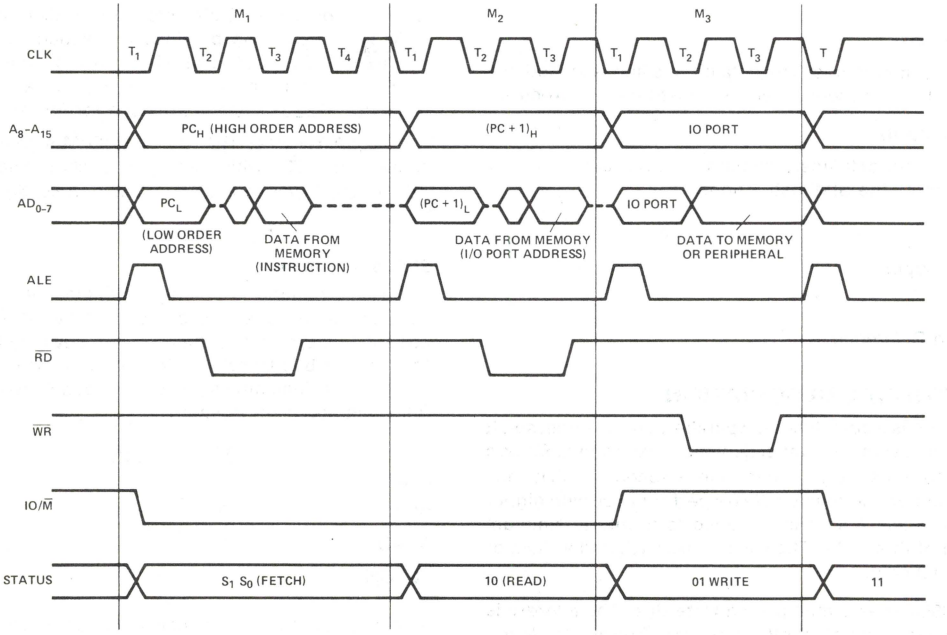


Figure 2. 8085A Basic System Timing

remain high to be acknowledged, but will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches.

The following diagram illustrates the TRAP interrupt request circuitry within the 8085A.

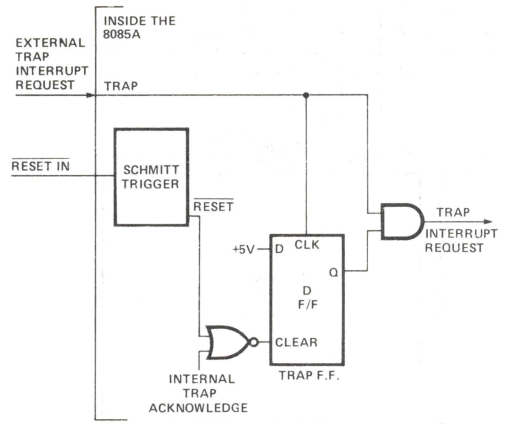


Figure 3. 8085A Trap Interrupt Request Circuitry

Note that the servicing of any interrupt (TRAP, RST 7.5, RST 6.5, RST 5.5, INTR) disables all future interrupts (except TRAPs) until an EI instruction is executed.

The TRAP interrupt is special in that it preserves the previous interrupt enable status. Performing the first RIM instruction following a TRAP interrupt allows you to determine whether interrupts were enabled or disabled prior to the TRAP. All subsequent RIM instructions provide current interrupt enable status.

The serial I/O system is also controlled by the RIM and SIM instructions. SID is read by RIM, and SIM sets the SOD data.

Basic System Timing

The 8085A has a multiplexed Data Bus. ALE is used as a strobe to sample the lower 8-bits of address on the Data Bus. Figure 2 shows an instruction fetch, memory read and I/O write cycle (OUT). Note that during the I/O write and read cycle that the I/O port address is copied on both the upper and lower half of the address.

As in the 8080, the READY line is used to extend the read and write pulse lengths so that the 8085A can be used with slow memory. Hold causes the CPU to relinguish the bus when it is through with it by floating the Address and Data Buses.

System Interface

8085A family includes memory components, which are directly compatible to the 8085A CPU. For example, a system consisting of the three chips, 8085A, 8156, and 8355 will have the following features:

- 2K Bytes ROM
- 256 Bytes RAM
- 1 Timer/Counter
- 4 8-bit I/O Ports
- 1 6-bit I/O Port
- 4 Interrupt Levels
- Serial In/Serial Out Ports

This minimum system, using the standard I/O technique is as shown in Figure 3.

In addition to standard I/O, the memory mapped I/O offers an efficient I/O addressing technique. With this technique, an area of memory address space is assigned for I/O address, thereby, using the memory address for I/O manipulation. Figure 4 shows the system configuration of Memory Mapped I/O using 8085A.

The 8085A CPU can also interface with the standard memory that does *not* have the multiplexed address/data bus. It will require a simple 8212 (8-bit latch) as shown in Figure 5.

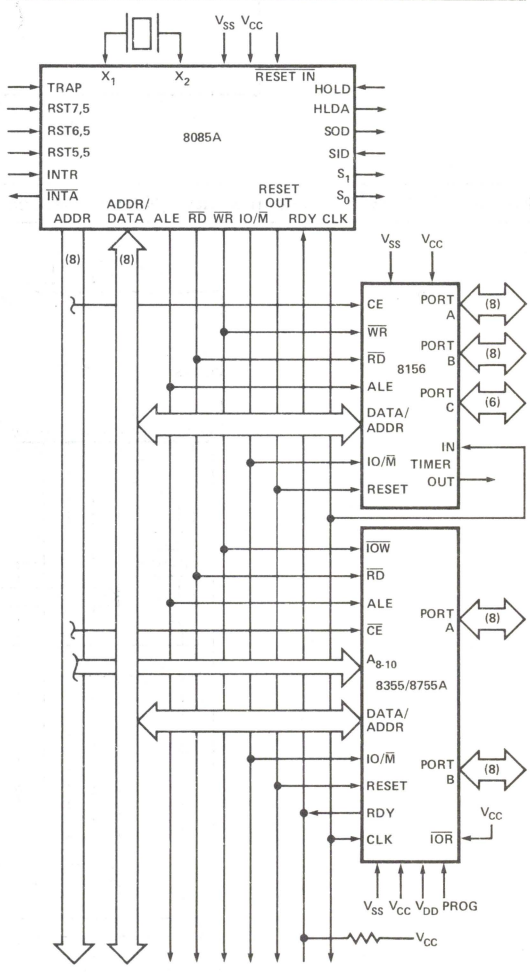


Figure 4. 8085A Minimum System (Standard I/O Technique)

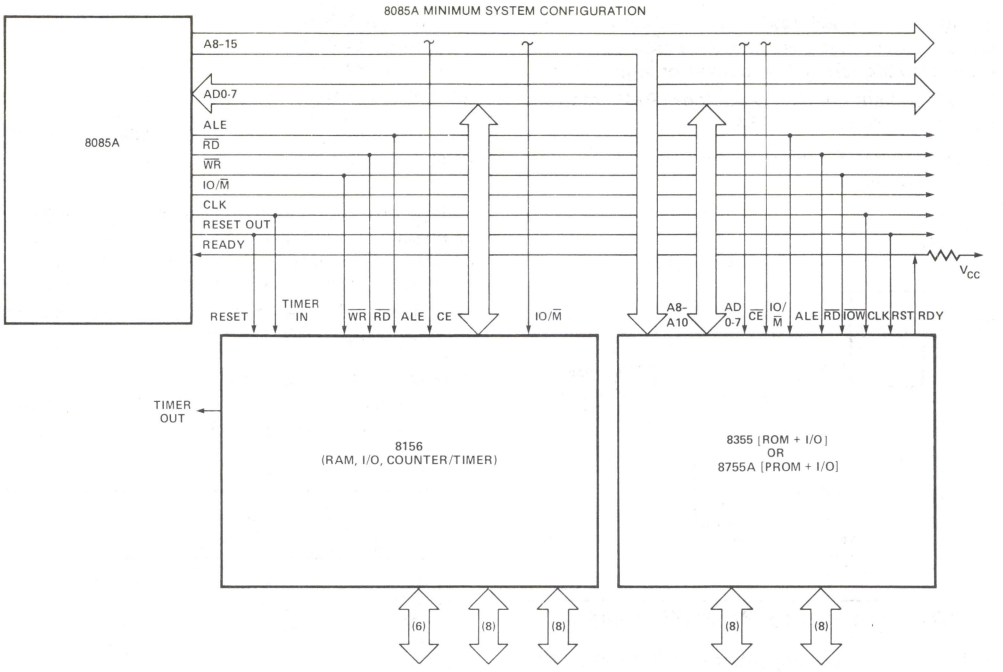


Figure 5. MCS-85™ Minimum System (Memory Mapped I/O)

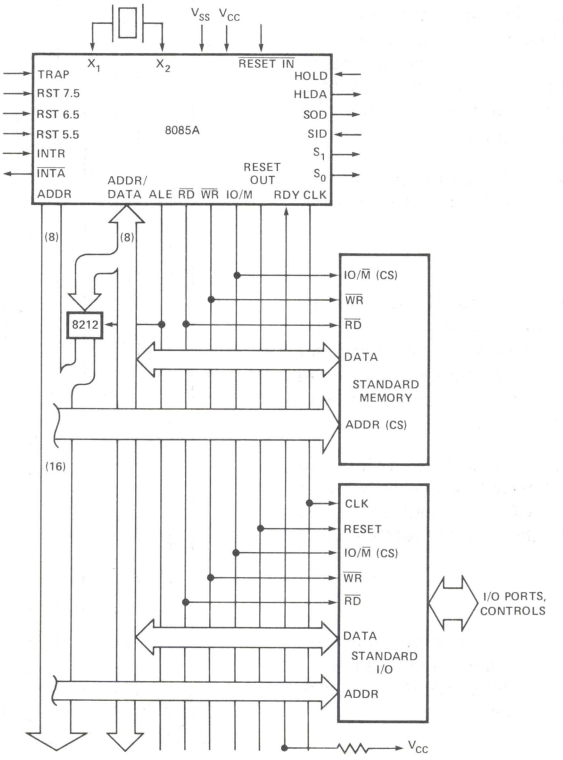
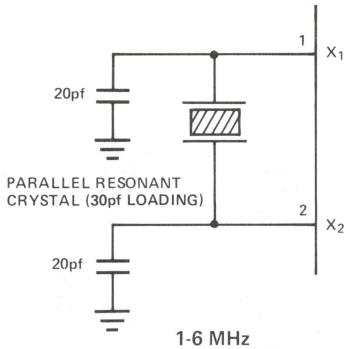


Figure 6. MCS-85™ System (Using Standard Memories)

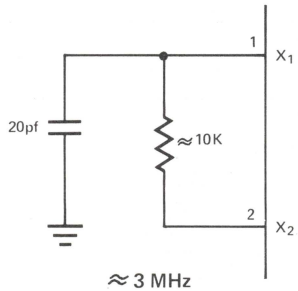
Driving the X_1 and X_2 Inputs

The user may drive the X_1 and X_2 inputs of the 8085A with a crystal, an external clock source or an RC network as shown below. The driving frequency must be twice the desired internal operating frequency (the 8085A would require a 6MHz crystal for 3MHz internal operation).



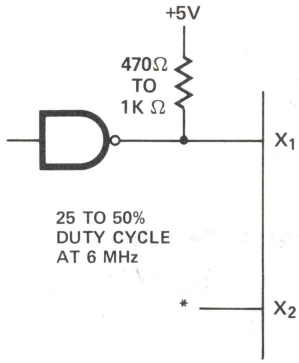
1-6 MHz
INPUT FREQUENCY

The 20pF capacitors are required to guarantee oscillation at the proper frequency during system startup.



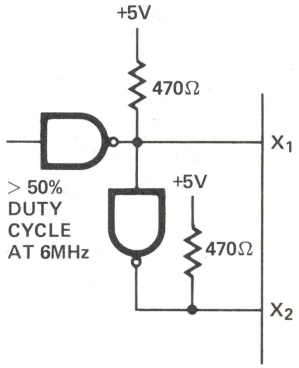
≈ 3 MHz
INPUT FREQUENCY

RC Mode causes a large drift in clock frequency because of the variation in on-chip timing generation parameters. Use of RC Mode should be limited to an application, which can tolerate a wide frequency variation.



1-6 MHz
INPUT FREQUENCY

*X_2 LEFT FLOATING.



~6 MHz
INPUT FREQUENCY

NOTE:
Duty cycle refers to the percentage of the clock input cycle when X_1 is high.

Figure 7. Driving the Clock Inputs (X_1 and X_2) of 8085A

Generating the 8085A Wait State

The following circuit may be used to insert one WAIT state in each 8085A machine cycle.

The D flip flops should be chosen such that
- CLK is rising edge triggered
- CLEAR is low-level active.

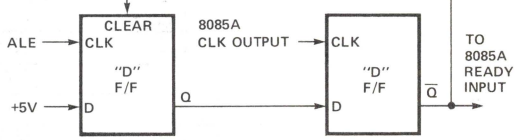


Figure 8. Generation of a Wait State for 8085A CPU

PRELIMINARY
Notice: This is a preliminary data sheet. Specifications and information herein are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . 0°C to 70°C
Storage Temperature . . . . . –65°C to +150°C
Voltage on Any Pin
With Respect to Ground . . . . . – 0.5 to + 7V
Power Dissipation . . . . . 1.5 Watt

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

(T_A = 0°C to 70°C; V_{CC} = 5V ±5%; V_{SS} = 0V; unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} +0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400μA
I_{CC}	Power Supply Current		170	mA	
I_{IL}	Input Leakage		±10	μA	$V_{in} = V_{CC}$
I_{LO}	Output Leakage		±10	μA	$0.45V \leqslant V_{out} \leqslant V_{CC}$
V_{ILR}	Input Low Level, RESET	-0.5	+0.8	V	
V_{IHR}	Input High Level, RESET	2.4	V_{CC} +0.5	V	
V_{HY}	Hysteresis, RESET	0.25		V	

TIMING CHARACTERISTICS

Bus Timing Specification as a T_{CYC} Dependent

t_{AL}	–	(1/2) T - 50	MIN
t_{LA}	–	(1/2) T - 60	MIN
t_{LL}	–	(1/2) T - 20	MIN
t_{LCK}	–	(1/2) T - 60	MIN
t_{LC}	–	(1/2) T - 30	MIN
t_{AD}	–	(5/2 + N) T - 225	MAX
t_{RD}	–	(3/2 + N) T - 180	MAX
t_{RAE}	–	(1/2) T - 10	MIN
t_{CA}	–	(1/2) T - 40	MIN
t_{DW}	–	(3/2 + N) T - 60	MIN
t_{WD}	–	(1/2) T - 60	MIN
t_{CC}	–	(3/2 + N) T - 80	MIN
t_{CL}	–	(1/2) T - 110	MIN
t_{ARY}	–	(3/2) T - 260	MAX
t_{HACK}	–	(1/2) T - 50	MIN
t_{HABF}	–	(1/2) T + 50	MAX
t_{HABE}	–	(1/2) T + 50	MAX
t_{AC}	–	(2/2) T - 50	MIN
t_1	–	(1/2) T - 80	MIN
t_2	–	(1/2) T - 40	MIN
t_{RV}	–	(3/2) T - 80	MIN

NOTE: N is equal to the total WAIT states.
T = t_{CYC}.

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

A.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ±5%; V_{SS} = 0V)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
T_{CYC}	CLK Cycle Period	320	2000	ns	See notes 1, 2, 3, 4, 5
t_1	CLK Low Time	80		ns	
t_2	CLK High Time	120		ns	
t_r, t_f	CLK Rise and Fall Time		30	ns	
t_{AL}	Address Valid Before Trailing Edge of ALE	110		ns	
t_{LA}	Address Hold Time After ALE	100		ns	
t_{LL}	ALE Width	140		ns	
t_{LCK}	ALE Low During CLK High	100		ns	
t_{LC}	Trailing Edge of ALE to Leading Edge of Control	130		ns	
t_{AFR}	Address Float After Leading Edge of $\overline{READ}$ ($\overline{INTA}$)		0	ns	
t_{AD}	Valid Address to Valid Data In		575	ns	
t_{RD}	$\overline{READ}$ (or $\overline{INTA}$) to Valid Data		300	ns	
t_{RDH}	Data Hold Time After $\overline{READ}$ ($\overline{INTA}$)	0		ns	
t_{RAE}	Trailing Edge of $\overline{READ}$ to Re-Enabling of Address	150		ns	T_{CYC} = 320ns; C_L = 150 pF
t_{CA}	Address (A8–A15) Valid After Control	120		ns	
t_{DW}	Data Valid to Trailing Edge of $\overline{WRITE}$	420		ns	
t_{WD}	Data Valid After Trailing Edge of $\overline{WRITE}$	100		ns	
t_{CC}	Width of Control Low ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$)	400		ns	
t_{CL}	Trailing Edge of Control to Leading Edge of ALE	50		ns	
t_{ARY}	READY Valid From Address Valid		220	ns	
t_{RYS}	READY Setup Time to Leading Edge of CLK	110		ns	
t_{RYH}	READY Hold Time	0		ns	
t_{HACK}	HLDA Valid to Trailing Edge of CLK	110		ns	
t_{HABF}	Bus Float After HLDA		210	ns	
t_{HABE}	HLDA to Bus Enable		210	ns	
t_{LDR}	ALE to Valid Data In		460	ns	
t_{RV}	Control Trailing Edge to Leading Edge of Next Control	400		ns	
t_{AC}	Address Valid to Leading Edge of Control	270		ns	
t_{HDS}	HOLD Setup Time to Trailing Edge of CLK	170		ns	
t_{HDH}	HOLD Hold Time	0		ns	
t_{INS}	INTR Setup Time to Falling Edge of CLK (M1, T1 only). Also RST and TRAP	160		ns	
t_{INH}	INTR Hold Time	0		ns	

NOTES:
1. A8-15 Address Specs apply to IO/$\overline{M}$, S0 and S1.
2. For all output timing where $C_L \neq$ 150pf use the following correction factors:
   25pf $\leq C_L <$ 150pf : -.10 ns/pf
   150pf $< C_L \leq$ 300pf : +.30 ns/pf
3. Output timings are measured with purely capacitive load.
4. All timings are measured at output voltage V_L = .8V, V_H = 2.0V, and 1.5V with 20ns rise and fall time on inputs.
5. To calculate timing specifications at other values of T_{CYC} use the table in Table 2.
6. L.E. = Leading Edge T.E. = Trailing Edge

WAVEFORMS

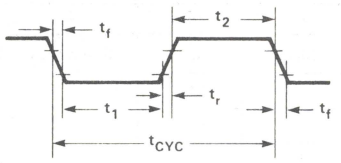
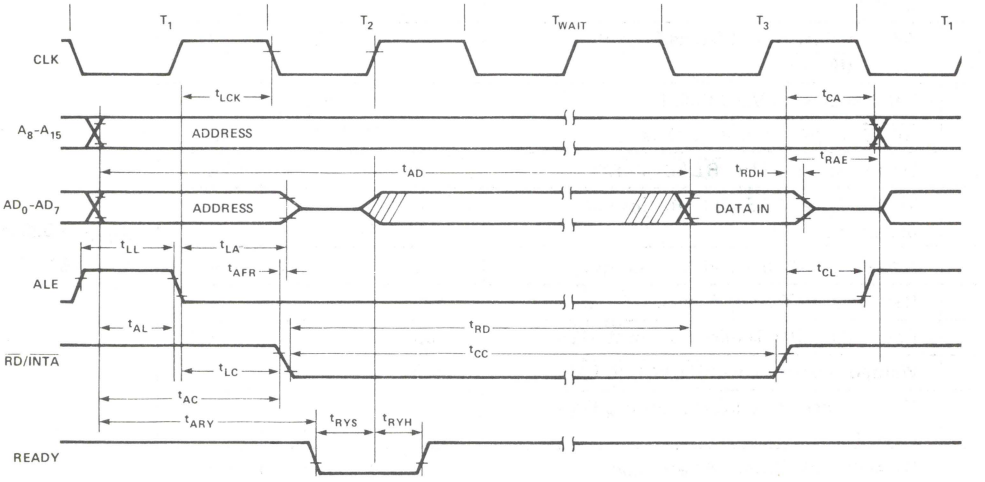


Figure 10. Clock Timing Waveform

Read Operation



Write Operation

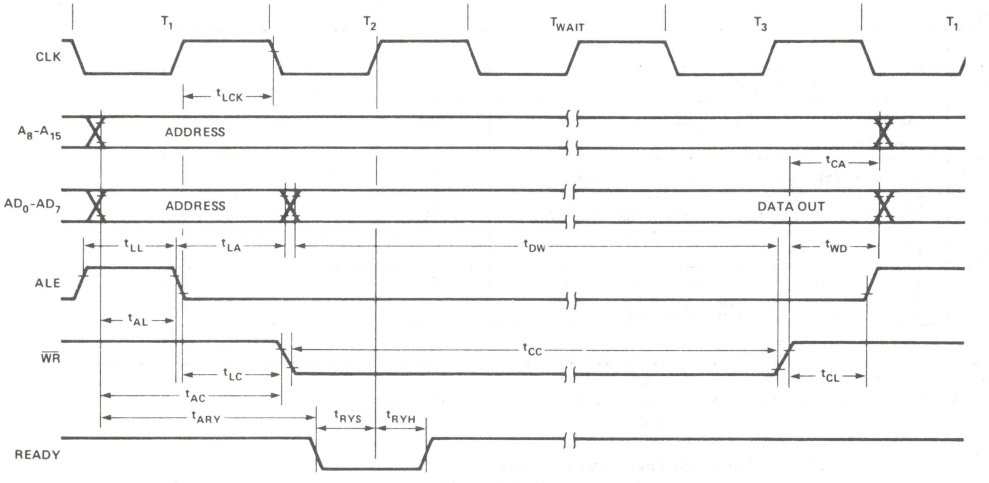


Figure 11. 8085A Bus Timing

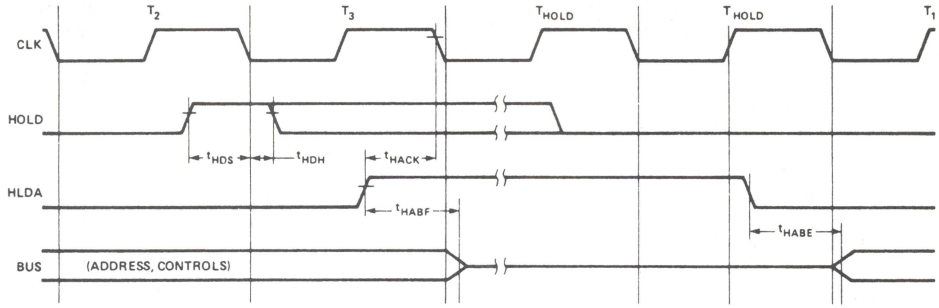


Figure 13. 8085A Hold Timing

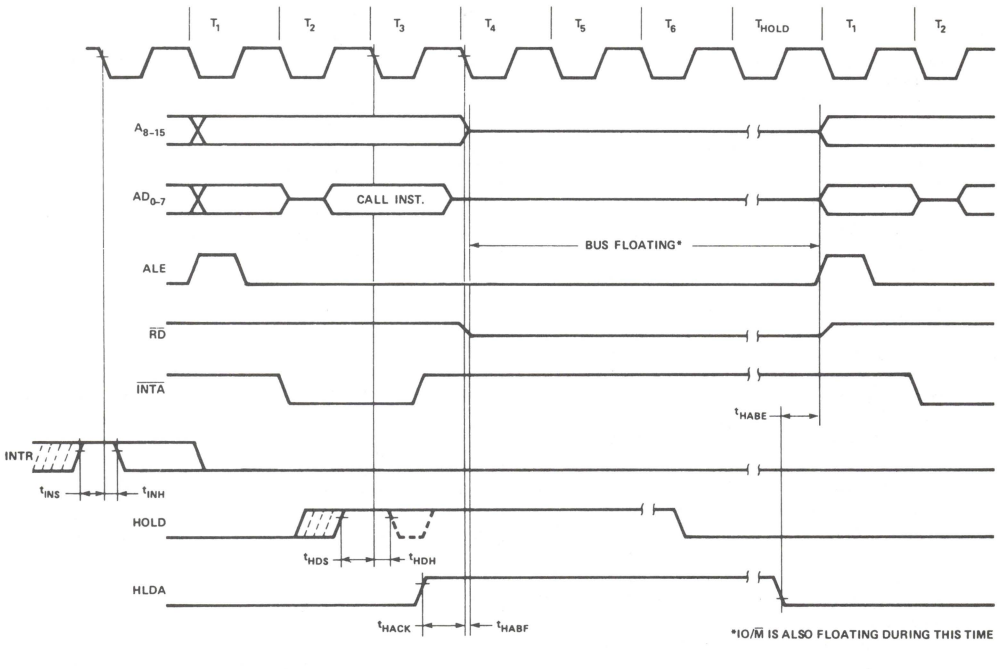


Figure 14. 8085A Interrupt and Hold Timing

INSTRUCTION SET

Mnemonic	Description	Instruction Code[1] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock[2] Cycles
MOVE, LOAD, AND STORE										
MOVr1,r2	Move register to register	0	1	D	D	D	S	S	S	4
MOV M,r	Move register to memory	0	1	1	1	0	S	S	S	7
MOV r,M	Move memory to register	0	1	D	D	D	1	1	0	7
MVI r	Move immediate register	0	0	D	D	D	1	1	0	7
MVI M	Move immediate memory	0	0	1	1	0	1	1	0	10
LXI B	Load immediate register Pair B & C	0	0	0	0	0	0	0	1	10
LXI D	Load immediate register Pair D & E	0	0	0	1	0	0	0	1	10
LXI H	Load immediate register Pair H & L	0	0	1	0	0	0	0	1	10
LXI SP	Load immediate stack pointer	0	0	1	1	0	0	0	1	10
STAX B	Store A indirect	0	0	0	0	0	0	1	0	7
STAX D	Store A indirect	0	0	0	1	0	0	1	0	7
LDAX B	Load A indirect	0	0	0	0	1	0	1	0	7
LDAX D	Load A indirect	0	0	0	1	1	0	1	0	7
STA	Store A direct	0	0	1	1	0	0	1	0	13
LDA	Load A direct	0	0	1	1	1	0	1	0	13
SHLD	Store H & L direct	0	0	1	0	0	0	1	0	16
LHLD	Load H & L direct	0	0	1	0	1	0	1	0	16
XCHG	Exchange D & E, H & L Registers	1	1	1	0	1	0	1	1	4
STACK OPS										
PUSH B	Push register Pair B & C on stack	1	1	0	0	0	1	0	1	12
PUSH D	Push register Pair D & E on stack	1	1	0	1	0	1	0	1	12
PUSH H	Push register Pair H & L on stack	1	1	1	0	0	1	0	1	12
PUSH PSW	Push A and Flags on stack	1	1	1	1	0	1	0	1	12
POP B	Pop register Pair B & C off stack	1	1	0	0	0	0	0	1	10
POP D	Pop register Pair D & E off stack	1	1	0	1	0	0	0	1	10
POP H	Pop register Pair H & L off stack	1	1	1	0	0	0	0	1	10
POP PSW	Pop A and Flags off stack	1	1	1	1	0	0	0	1	10
XTHL	Exchange top of stack, H & L	1	1	1	0	0	0	1	1	16
SPHL	H & L to stack pointer	1	1	1	1	1	0	0	1	6
JUMP										
JMP	Jump unconditional	1	1	0	0	0	0	1	1	10
JC	Jump on carry	1	1	0	1	1	0	1	0	7/10
JNC	Jump on no carry	1	1	0	1	0	0	1	0	7/10
JZ	Jump on zero	1	1	0	0	1	0	1	0	7/10
JNZ	Jump on no zero	1	1	0	0	0	0	1	0	7/10
JP	Jump on positive	1	1	1	1	0	0	1	0	7/10
JM	Jump on minus	1	1	1	1	1	0	1	0	7/10
JPE	Jump on parity even	1	1	1	0	1	0	1	0	7/10
JPO	Jump on parity odd	1	1	1	0	0	0	1	0	7/10
PCHL	H & L to program counter	1	1	1	0	1	0	0	1	6
CALL										
CALL	Call unconditional	1	1	0	0	1	1	0	1	18
CC	Call on carry	1	1	0	1	1	1	0	0	9/18
CNC	Call on no carry	1	1	0	1	0	1	0	0	9/18
CZ	Call on zero	1	1	0	0	1	1	0	0	9/18
CNZ	Call on no zero	1	1	0	0	0	1	0	0	9/18
CP	Call on positive	1	1	1	1	0	1	0	0	9/18
CM	Call on minus	1	1	1	1	1	1	0	0	9/18
CPE	Call on parity even	1	1	1	0	1	1	0	0	9/18
CPO	Call on parity odd	1	1	1	0	0	1	0	0	9/18
RETURN										
RET	Return	1	1	0	0	1	0	0	1	10
RC	Return on carry	1	1	0	1	1	0	0	0	6/12
RNC	Return on no carry	1	1	0	1	0	0	0	0	6/12
RZ	Return on zero	1	1	0	0	1	0	0	0	6/12
RNZ	Return on no zero	1	1	0	0	0	0	0	0	6/12
RP	Return on positive	1	1	1	1	0	0	0	0	6/12
RM	Return on minus	1	1	1	1	1	0	0	0	6/12
RPE	Return on parity even	1	1	1	0	1	0	0	0	6/12
RPO	Return on parity odd	1	1	1	0	0	0	0	0	6/12
RESTART										
RST	Restart	1	1	A	A	A	1	1	1	12
INPUT/OUTPUT										
IN	Input	1	1	0	1	1	0	1	1	10
OUT	Output	1	1	0	1	0	0	1	1	10
INCREMENT AND DECREMENT										
INR r	Increment register	0	0	D	D	D	1	0	0	4
DCR r	Decrement register	0	0	D	D	D	1	0	1	4
INR M	Increment memory	0	0	1	1	0	1	0	0	10
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10
INX B	Increment B & C registers	0	0	0	0	0	0	1	1	6
INX D	Increment D & E registers	0	0	0	1	0	0	1	1	6
INX H	Increment H & L registers	0	0	1	0	0	0	1	1	6
INX SP	Increment stack pointer	0	0	1	1	0	0	1	1	6
DCX B	Decrement B & C	0	0	0	0	1	0	1	1	6
DCX D	Decrement D & E	0	0	0	1	1	0	1	1	6
DCX H	Decrement H & L	0	0	1	0	1	0	1	1	6
DCX SP	Decrement stack pointer	0	0	1	1	1	0	1	1	6
ADD										
ADD r	Add register to A	1	0	0	0	0	S	S	S	4
ADC r	Add register to A with carry	1	0	0	0	1	S	S	S	4
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7
ADI	Add immediate to A	1	1	0	0	0	1	1	0	7
ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0	7
DAD B	Add B & C to H & L	0	0	0	0	1	0	0	1	10
DAD D	Add D & E to H & L	0	0	0	1	1	0	0	1	10
DAD H	Add H & L to H & L	0	0	1	0	1	0	0	1	10
DAD SP	Add stack pointer to H & L	0	0	1	1	1	0	0	1	10
SUBTRACT										
SUB r	Subtract register from A	1	0	0	1	0	S	S	S	4
SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S	4
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7
SUI	Subtract immediate from A	1	1	0	1	0	1	1	0	7
SBI	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7
LOGICAL										
ANA r	And register with A	1	0	1	0	0	S	S	S	4

Mnemonic	Description	Instruction Code[1] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock[2] Cycles
XRA r	Exclusive Or register with A	1	0	1	0	1	S	S	S	4
ORA r	Or register with A	1	0	1	1	0	S	S	S	4
CMP r	Compare register with A	1	0	1	1	1	S	S	S	4
ANA M	And memory with A	1	0	1	0	0	1	1	0	7
XRA M	Exclusive Or memory with A	1	0	1	0	1	1	1	0	7
ORA M	Or memory with A	1	0	1	1	0	1	1	0	7
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7
ANI	And immediate with A	1	1	1	0	0	1	1	0	7
XRI	Exclusive Or immediate with A	1	1	1	0	1	1	1	0	7
ORI	Or immediate with A	1	1	1	1	0	1	1	0	7
CPI	Compare immediate with A	1	1	1	1	1	1	1	0	7
ROTATE										
RLC	Rotate A left	0	0	0	0	0	1	1	1	4
RRC	Rotate A right	0	0	0	0	1	1	1	1	4
RAL	Rotate A left through carry	0	0	0	1	0	1	1	1	4
RAR	Rotate A right through carry	0	0	0	1	1	1	1	1	4
SPECIALS										
CMA	Complement A	0	0	1	0	1	1	1	1	4
STC	Set carry	0	0	1	1	0	1	1	1	4
CMC	Complement carry	0	0	1	1	1	1	1	1	4
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4
CONTROL										
EI	Enable Interrupts	1	1	1	1	1	0	1	1	4
DI	Disable Interrupt	1	1	1	1	0	0	1	1	4
NOP	No-operation	0	0	0	0	0	0	0	0	4
HLT	Halt	0	1	1	1	0	1	1	0	5
NEW 8085A INSTRUCTIONS										
RIM	Read Interrupt Mask	0	0	1	0	0	0	0	0	4
SIM	Set Interrupt Mask	0	0	1	1	0	0	0	0	4

NOTES: 1. DDD or SSS: B 000, C 001, D 010, E 011, H 100, L 101, Memory 110, A 111.
2. Two possible cycle times, (6/12) indicate instruction cycles dependent on condition flags.

*All mnemonics copyright ©Intel Corporation 1977

MACHINE CYCLE			STATUS			CONTROL		
			IO/$\overline{M}$	S1	S0	$\overline{RD}$	$\overline{WR}$	$\overline{INTA}$
OPCODE FETCH	(OF)		0	1	1	0	1	1
MEMORY READ	(MR)		0	1	0	0	1	1
MEMORY WRITE	(MW)		0	0	1	1	0	1
I/O READ	(IOR)		1	1	0	0	1	1
I/O WRITE	(IOW)		1	0	1	1	0	1
ACKNOWLEDGE OF INTR	(INA)		1	1	1	1	1	0
BUS IDLE	(BI):	DAD	0	1	0	1	1	1
		ACK. OF RST,TRAP	1	1	1	1	1	1
		HALT	TS	0	0	TS	TS	1

Figure 15. 8085A Machine Cycle Chart

Machine State	Status & Buses				Control		
	S1,S0	IO/$\overline{M}$	A_8-A_{15}	AD_0-AD_7	$\overline{RD}$,$\overline{WR}$	$\overline{INTA}$	ALE
T_1	X	X	X	X	1	1	1*
T_2	X	X	X	X	X	X	0
T_{WAIT}	X	X	X	X	X	X	0
T_3	X	X	X	X	X	X	0
T_4	1	0†	X	TS	1	1	0
T_5	1	0†	X	TS	1	1	0
T_6	1	0†	X	TS	1	1	0
T_{RESET}	X	TS	TS	TS	TS	1	0
T_{HALT}	0	TS	TS	TS	TS	1	0
T_{HOLD}	X	TS	TS	TS	TS	1	0

0 = Logic "0" TS = High Impedance
1 = Logic "1" X = Unspecified

* ALE not generated during 2nd and 3rd machine cycles of DAD instruction.
† IO/M = 1 during T_4-T_6 of INA machine cycle.

Figure 16. 8085A Machine State Chart

ADVANCE INFORMATION
Characteristics are subject to change without notice.

8085A-2
SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSOR

- 0.8 μs Instruction Cycle; 5 MHz Internal Clock
- Single +5V Power Supply
- 100% Software Compatible with 8080A
- On-Chip Clock Generator (with External Crystal or RC Network)
- On-Chip System Controller; Advanced Cycle Status Information Available for Large System Control
- 4-Vectored Interrupts (One is Non-Maskable)
- Serial In/Serial Out Port
- Decimal, Binary, and Double Precision Arithmetic
- Direct Addressing Capability to 64K Bytes of Memory

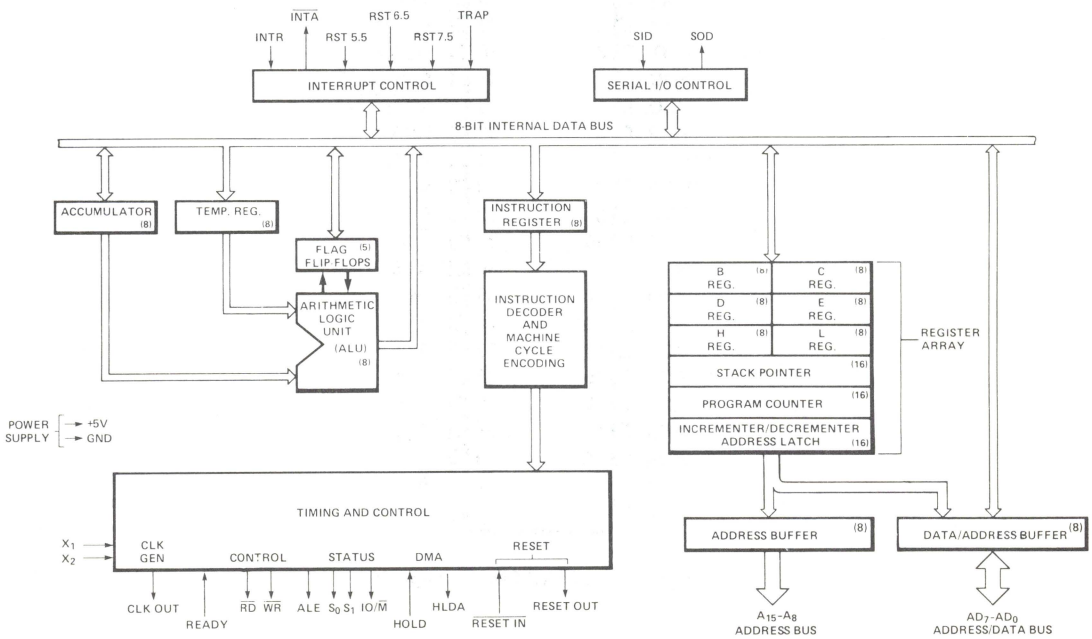
The Intel® 8085A is a new generation, complete 8-bit parallel central processing unit (CPU). Its instruction set is 100% software compatible with the 8080A microprocessor, and it is designed to improve the present 8080's performance by higher system speeds. Its high level of system integration allows a minimum system of three ICs: 8085A (CPU), 8156 (RAM), and 8355/8755A (ROM/PROM).

The 8085A incorporates all of the features that the 8224 (clock generator) and 8228 (system controller) provided for the 8080, thereby offering a high level of system integration.

The 8085A uses a multiplexed data bus. The address is split between the 8-bit address bus and the 8-bit data bus. The on-chip address latches of 8155/8355/8755 memory products allows a direct interface with 8085A.

The 8085A-2 is a higher performance version of the 8085A.

BLOCK DIAGRAM



ADVANCE INFORMATION
Characteristics subject to change without notice

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . 0°C to 70°C
Storage Temperature . . . . . –65°C to +150°C
Voltage on Any Pin
With Respect to Ground . . . . . – 0.5 to 7V
Power Dissipation . . . . . 1.5 Watt

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

(T_A = 0°C to 70°C; V_{CC} = 5V ±5%; V_{SS} = 0V; unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} +0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400μA
I_{CC}	Power Supply Current		170	mA	
I_{IL}	Input Leakage		±10	μA	$V_{in} = V_{CC}$
I_{LO}	Output Leakage		±10	μA	$0.45V \leqslant V_{out} \leqslant V_{CC}$
V_{ILR}	Input Low Level, RESET	-0.5	+0.8	V	
V_{IHR}	Input High Level, RESET	2.4	V_{CC} +0.5	V	
V_{HY}	Hysteresis, RESET	0.25		V	

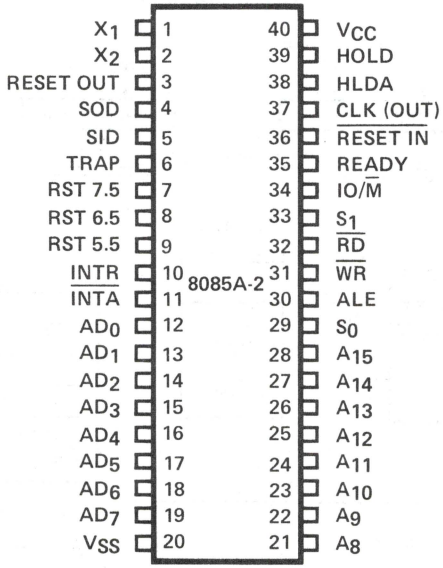


Figure 1. 8085A-2 Pinout Diagram

ADVANCE INFORMATION
Characteristics are subject to change without notice.

A.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ±5%; V_{SS} = 0V)

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{CYC}	CLK Cycle Period	200	2000	ns	See notes 1, 2, 3, 4, 5
t_1	CLK Low Time	30		ns	
t_2	CLK High Time	50		ns	
t_r, t_f	CLK Rise and Fall Time		30	ns	
t_{AL}	Address Valid Before Trailing Edge of ALE	50		ns	
t_{LA}	Address Hold Time After ALE	50		ns	
t_{LL}	ALE Width	80		ns	
t_{LCK}	ALE Low During CLK High	50		ns	
t_{LC}	Trailing Edge of ALE to Leading Edge of Control	60		ns	
t_{AFR}	Address Float After Leading Edge of $\overline{READ}$ ($\overline{INTA}$)		0	ns	
t_{AD}	Valid Address to Valid Data In		350	ns	
t_{RD}	$\overline{READ}$ (or $\overline{INTA}$) to Valid Data		150	ns	
t_{RDH}	Data Hold Time After $\overline{READ}$ ($\overline{INTA}$)	0		ns	
t_{RAE}	Trailing Edge of $\overline{READ}$ to Re-Enabling of Address	80		ns	t_{CYC} = 200ns
t_{CA}	Address (A8-A15) Valid After Control	60		ns	C_L = 150pF
t_{DW}	Data Valid to Trailing Edge of $\overline{WRITE}$	230		ns	
t_{WD}	Data Valid After Trailing Edge of $\overline{WRITE}$	40		ns	
t_{CC}	Width of Control Low ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$)	230		ns	
t_{CL}	Trailing Edge of Control to Leading Edge of ALE	25		ns	
t_{ARY}	READY Valid from Address Valid		100	ns	
t_{RYS}	READY Setup Time to Leading Edge of CLK	100		ns	
t_{RYH}	READY Hold Time	0		ns	
t_{HACK}	HLDA Valid to Trailing Edge of CLK	40		ns	
t_{HABF}	Bus Float After HLDA		150	ns	
t_{HABE}	HLDA to Bus Enable		150	ns	
t_{RV}	Control Trailing Edge to Leading Edge of Next Control	220		ns	
t_{AC}	Address Valid to Leading Edge of Control	115		ns	
t_{HDS}	HOLD Setup Time to Trailing Edge of CLK	120		ns	
t_{HDH}	HOLD Hold Time	0		ns	
t_{INS}	INTR Setup Time to Falling Edge of CLK (M1, T1 only); also RST and TRAP	150		ns	
t_{INH}	INTR Hold Time	0		ns	

NOTES:
1. A8-A15 Address Specs apply to IO/M, S0, and S1.
2. For all output timing where $C_L \neq 150pF$ use the following correction factors:
   $25pF \leq C_L < 150pF$: −0.10ns/pF
   $150pF < C_L \leq 300pF$: +0.30ns/pF
3. Output timings are measured with purely capacitive load.
4. All timings are measured at output voltage V_L = 0.8V, V_H = 2.0V, and 1.5V with 20ns rise and fall time on inputs.
5. To calculate timing specifications at other values of t_{CYC} use Table 2.

ADVANCE INFORMATION
Characteristics are subject to change without notice.

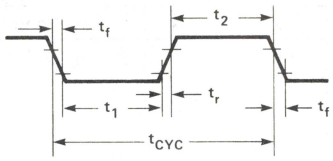
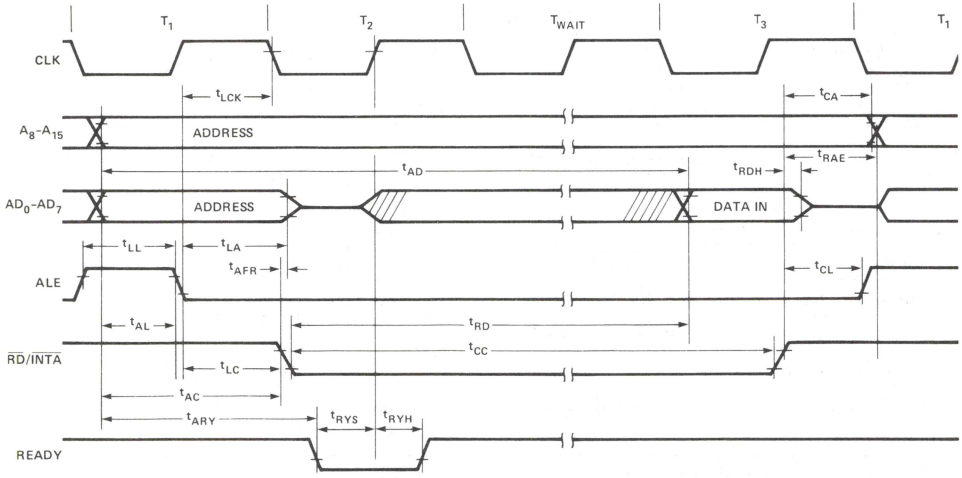


Figure 2. Clock Timing Waveform

Read Operation



Write Operation

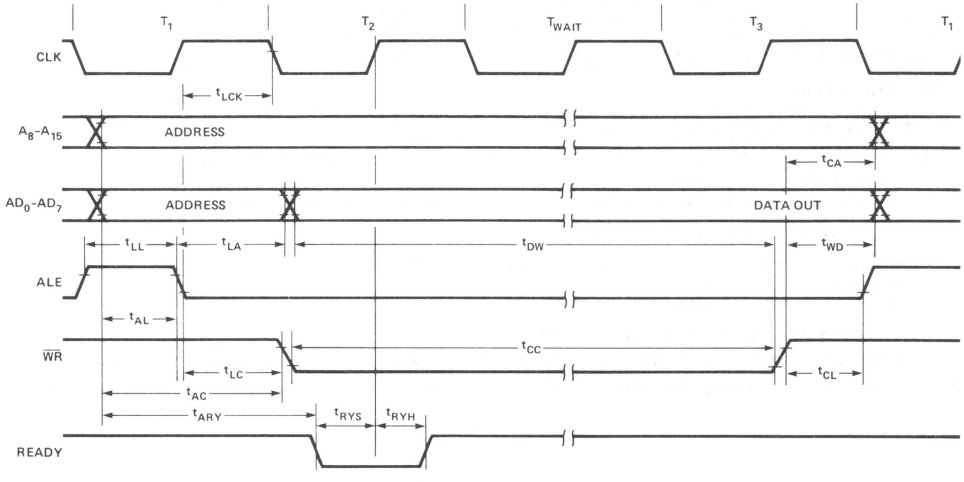


Figure 3. 8085A-2 Bus Timing

ADVANCE INFORMATION
Characteristics are subject to change without notice

Hold Operation

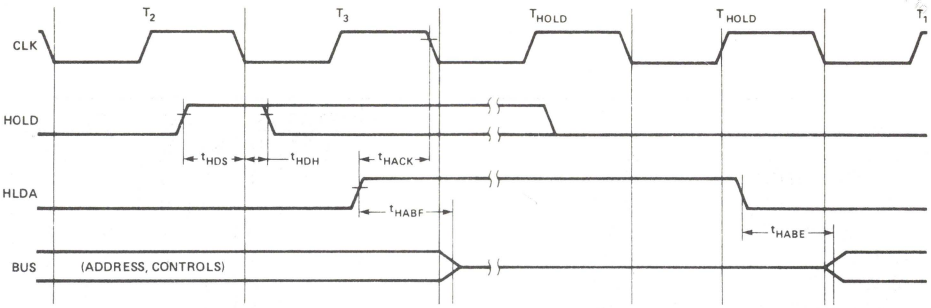


Figure 4. 8085A-2 Hold Timing

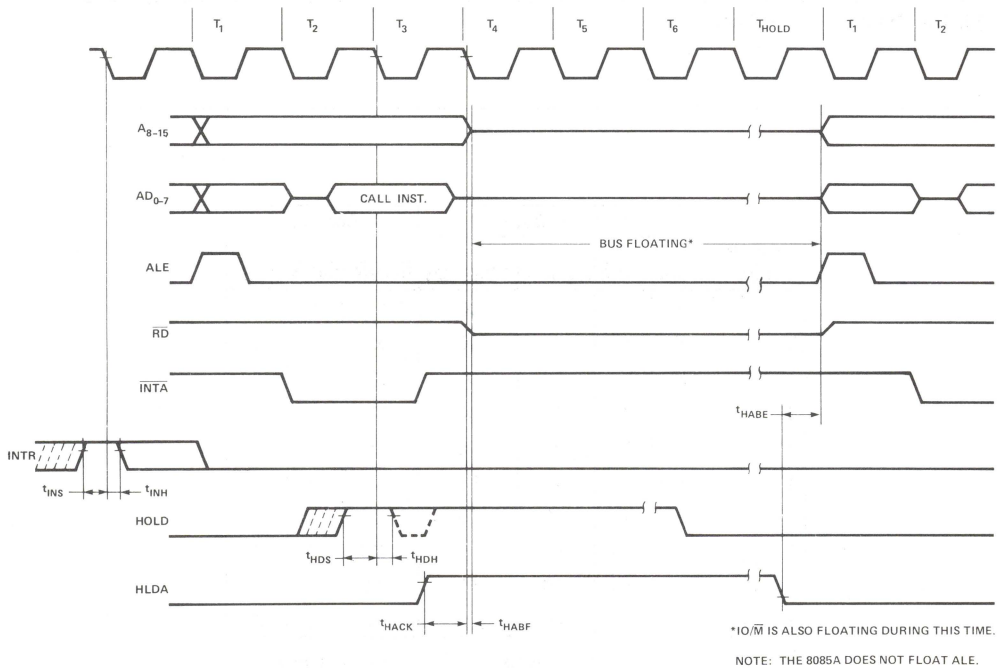


Figure 5. 8085A-2 Interrupt and Hold Timing

ADVANCE INFORMATION
Characteristics are subject to change without notice

MACHINE CYCLE			STATUS			CONTROL		
			IO/$\overline{M}$	S1	S0	$\overline{RD}$	$\overline{WR}$	$\overline{INTA}$
OPCODE FETCH	(OF)		0	1	1	0	1	1
MEMORY READ	(MR)		0	1	0	0	1	1
MEMORY WRITE	(MW)		0	0	1	1	0	1
I/O READ	(IOR)		1	1	0	0	1	1
I/O WRITE	(IOW)		1	0	1	1	0	1
ACKNOWLEDGE OF INTR	(INA)		1	1	1	1	1	0
BUS IDLE	(BI):	DAD	0	1	0	1	1	1
		ACK. OF RST,TRAP	1	1	1	1	1	1
		HALT	TS	0	0	TS	TS	1

Figure 6. 8085A-2 Machine Cycle Chart

Machine State	Status & Buses				Control		
	S1,S0	IO/$\overline{M}$	A_8-A_{15}	AD_0-AD_7	$\overline{RD}$,$\overline{WR}$	$\overline{INTA}$	ALE
T_1	X	X	X	X	1	1	1*
T_2	X	X	X	X	X	X	0
T_{WAIT}	X	X	X	X	X	X	0
T_3	X	X	X	X	X	X	0
T_4	1	0†	X	TS	1	1	0
T_5	1	0†	X	TS	1	1	0
T_6	1	0†	X	TS	1	1	0
T_{RESET}	X	TS	TS	TS	TS	1	0
T_{HALT}	0	TS	TS	TS	TS	1	0
T_{HOLD}	X	TS	TS	TS	TS	1	0

0 = Logic "0" TS = High Impedance
1 = Logic "1" X = Unspecified

* ALE not generated during 2nd and 3rd machine cycles of DAD instruction.
† IO/M = 1 during T_4-T_6 of INA machine cycle.

Figure 7. 8085A-2 Machine State Chart

8155/8156
2048-BIT STATIC MOS RAM WITH I/O PORTS AND TIMER

*Directly Compatible with 8080A and 8048 CPU

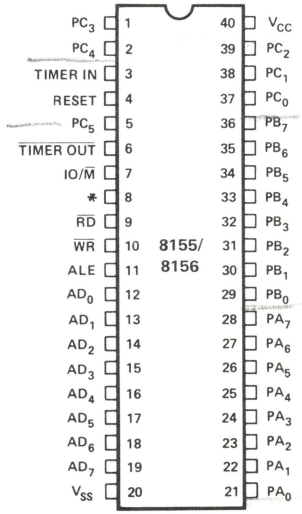
- 256 Words x 8 Bits
- Single +5V Power Supply
- Completely Static Operation
- Internal Address Latch
- 2 Programmable 8-Bit I/O Ports
- 1 Programmable 6-Bit I/O Port
- Programmable 14-Bit Binary Counter/ Timer
- Multiplexed Address and Data Bus
- 40-Pin DIP
- Chip Enable Active High (8156) or Low (8155)

The Intel® 8155 and 8156 are RAM and I/O chips to be used in the MCS-85™ and MCS-48™ microcomputer systems. Th RAM portion is designed with 2K-bit static cells organized as 256 x 8. They have maximum access times of 400 ns to permit use with no wait system in an 8085A system.

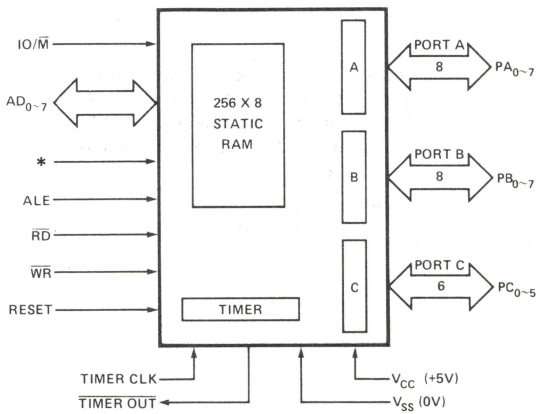
The I/O portion consists of 3 general purpose I/O ports. One of the 3 ports can be programmed to be status pins, thus allowing the other 2 ports to operate in handshake mode.

A 14-bit programmable counter/timer is also included on chip to provide either a square wave or terminal count pulse for the CPU system. It operates in binary countdown mode, and its timer modes are programmable.

PIN CONFIGURATION



BLOCK DIAGRAM



* : 8155 = $\overline{CE}$, 8156 = CE

PIN DESCRIPTION

The following describes the functions of all of the 8155/8156 pins.

Symbol	Function
RESET	The Reset signal is a pulse provided by the 8085 to initialize the system. Input high on this line resets the chip and initializes the three I/O ports to input mode. The width of RESET pulse should typically be 600 nsec. (Two 8085A clock cycle times).
AD_{0-7}	These are 3-state Address/Data lines that interface with the CPU lower 8-bit Address/Data Bus. The 8-bit address is latched into the address latch on the falling edge of the ALE. The address can be either for the memory section or the I/O section depending on the polarity of the IO/$\overline{M}$ input signal. The 8-bit data is either written into the chip or Read from the chip depending on the status of $\overline{WRITE}$ or $\overline{READ}$ input signal.
CE or $\overline{CE}$	Chip Enable: On the 8155, this pin is $\overline{CE}$ and is ACTIVE LOW. On the 8156, this pin is CE and is ACTIVE HIGH.
$\overline{RD}$	Input low on this line with the Chip Enable active enables the AD_{0-7} buffers. If IO/$\overline{M}$ pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port will be read to the AD bus.
$\overline{WR}$	Input low on this line with the Chip Enable active causes the data on the AD lines to be written to the RAM or I/O ports depending on the polarity of IO/$\overline{M}$.
ALE	Address Latch Enable: This control signal latches both the address on the AD_{0-7} lines and the state of the Chip Enable and IO/$\overline{M}$ into the chip at the falling edge of ALE.
IO/$\overline{M}$	IO/$\overline{Memory}$ Select: This line selects the memory if low and selects the IO if high.

Symbol	Function
$PA_{0-7}(8)$	These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the Command/Status Register.
$PB_{0-7}(8)$	These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the Command/Status Register.
$PC_{0-5}(6)$	These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the C/S Register. When PC_{0-5} are used as control signals, they will provide the following: PC0 — A INTR (Port A Interrupt) PC1 — A BF (Port A Buffer full) PC2 — $\overline{A\ STB}$ (Port A Strobe) PC3 — B INTR (Port B Interrupt) PC4 — $\overline{B\ BF}$ (Port B Buffer Full) PC5 — $\overline{B\ STB}$ (Port B Strobe)
TIMER IN	This is the input to the counter timer.
$\overline{TIMER\ OUT}$	This pin is the timer output. This output can be either a square wave or a pulse depending on the timer mode.
V_{CC}	+5 volt supply.
V_{SS}	Ground Reference.

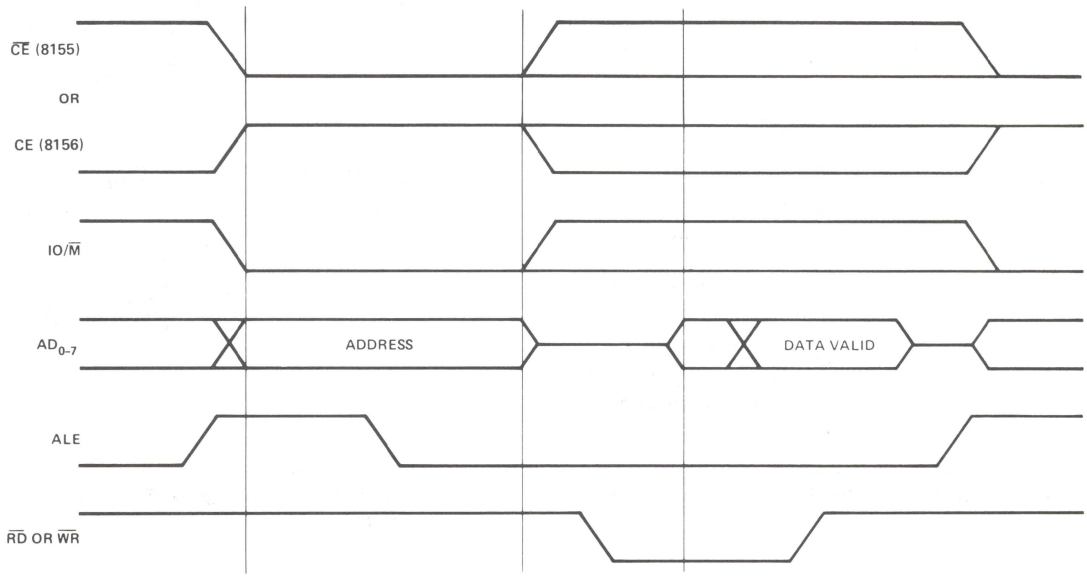
OPERATIONAL DESCRIPTION

The 8155/8156 includes the following operational features:

- 2K Bit Static RAM organized as 256 x 8
- Two 8-bit I/O ports (PA & PB) and one 6-bit I/O port (PC)
- 14-bit down counter

The I/O portion contains four registers (Command/Status, PA_{0-7}, PB_{0-7}, PC_{0-5}). The IO/M (IO/Memory Select) pin selects the I/O or the memory (RAM) portion. Detailed descriptions of memory, I/O ports and timer functions will follow.

The 8-bit address on the AD lines, the Chip Enable input, and IO/$\overline{M}$ are all latched on chip at the falling edge of ALE. A low on the IO/$\overline{M}$ must be provided to select the memory section.



NOTE: FOR DETAILED TIMING DIAGRAM INFORMATION, SEE FIGURE 7 AND A.C. CHARACTERISTICS.

Figure 1. Memory Read/Write Cycle

PROGRAMMING OF THE COMMAND/ STATUS REGISTER

The command register consists of eight latches one for each bit. Four bits (0-3) define the mode of the ports, two bits (4-5) enable or disable the interrupt from port C when it acts as control port, and the last two bits (6-7) are for the timer.

The C/S register contents can be altered at any time by using the I/O address XXXXX000 during a WRITE operation. The meaning of each bit of the command byte is defined as follows:

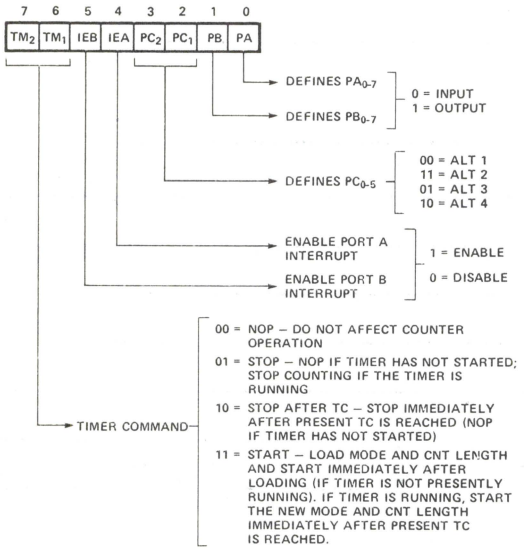


Figure 2. Command/Status Register Bit Assignments

READING THE COMMAND/STATUS REGISTER

The status register consists of seven latches one for each bit; six (0-5) for the status of the ports and one (6) for the status of the timer.

The status of the timer and the I/O section can be polled by reading the C/S Register (Address XXXXX000). Status word format is shown below:

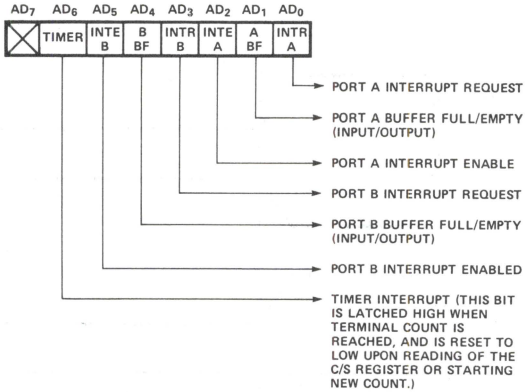


Figure 3. Command/Status Register Status Word Format

INPUT/OUTPUT SECTION

The I/O section of the 8155/8156 consists of four registers as described below.

- **Command/Status Register (C/S)** — This register is assigned the address XXXXX000. The C/S address serves the dual purpose.

  When the C/S register is selected during WRITE operation, a command is written into the command register. The contents of this register are *not* accessible through the pins.

  When the C/S (XXXXX000) is selected during a READ operation, the status information of the I/O ports and the timer become available on the AD_{0-7} lines.

- **PA Register** — This register can be programmed to be either input or output ports depending on the status of the contents of the C/S Register. Also depending on the command, this port can operate in either the basic mode or the strobed mode (See timing diagram). The I/O pins assigned in relation to this register are PA_{0-7}. The address of this register is XXXXX001.

- **PB Register** — This register functions the same as PA Register. The I/O pins assigned are PB_{0-7}. The address of this register is XXXXX010.

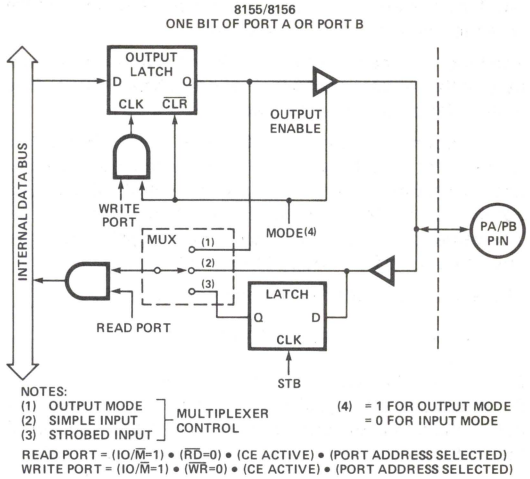
- **PC Register** — This register has the address XXXXX011 and contains only 6-bits. The 6-bits can be programmed to be either input ports, output ports or as control signals for PA and PB by properly programming the AD_2 and AD_3 bits of the C/S register.

  When PC_{0-5} is used as a control port, 3-bits are assigned for Port A and 3 for Port B. The first bit is an interrupt that the 8155 sends out. The second is an output signal indicating whether the buffer is full or empty, and the third is an input pin to accept a strobe for the strobed input mode. See Table 1.

When the 'C' port is programmed to either ALT3 or ALT4, the control signals for PA and PB are initialized as follows:

CONTROL	INPUT MODE	OUTPUT MODE
BF	Low	Low
INTR	Low	High
$\overline{STB}$	Input Control	Input Control

The following diagram shows how I/O ports A and B are structured within the 8155 and 8156:



Note in the diagram that when the I/O ports are programmed to be output ports, the contents of the output ports can still be read by a READ operation when appropriately addressed.

Note also that the output latch is cleared when the port enters the input mode. The output latch cannot be loaded by writing to the port if the port is in the input mode. The result is that each time a port mode is changed from input to output, the output pins will go low. When the 8155/56 is RESET, the output latches are all cleared and all 3 ports enter the input mode.

When in the ALT 1 or ALT 2 modes, the bits of PORT C are structured like the diagram above in the simple input or output mode, respectively.

Reading from an input port with nothing connected to the pins will provide unpredictable results.

Table 1. Table of Port Control Assignment

Pin	ALT 1	ALT 2	ALT 3	ALT 4
PC0	Input Port	Output Port	A INTR (Port A Interrupt)	A INTR (Port A Interrupt)
PC1	Input Port	Output Port	A BF (Port A Buffer Full)	A BF (Port A Buffer Full)
PC2	Input Port	Output Port	A $\overline{STB}$ (Port A Strobe)	A $\overline{STB}$ (Port A Strobe)
PC3	Input Port	Output Port	Output Port	B INTR (Port B Interrupt)
PC4	Input Port	Output Port	Output Port	B BF (Port B Buffer Full)
PC5	Input Port	Output Port	Output Port	B $\overline{STB}$ (Port B Strobe)

The set and reset of INTR and BF with respect to $\overline{STB}$, $\overline{WR}$ and $\overline{RD}$ timing is shown in Figure 8.

To summarize, the registers' assignments are:

Address	Pinouts	Functions	No. of Bits
XXXXX000	Internal	Command/Status Register	8
XXXXX001	PA0-7	General Purpose I/O Port	8
XXXXX010	PB0-7	General Purpose I/O Port	8
XXXXX011	PC0-5	General Purpose I/O Port or Control Lines	6

TIMER SECTION

The timer is a 14-bit down counter that counts the 'timer input' pulses and provides either a square wave or pulse when terminal count (TC) is reached.

The timer has the I/O address XXXXX100 for the low order byte of the register and the I/O address XXXXX101 for the high order byte of the register.

To program the timer, the COUNT LENGTH REG is loaded first, one byte at a time, by selecting the timer addresses. Bits 0-13 will specify the length of the next count and bits 14-15 will specify the timer output mode. The value loaded into the count length register can have any value from 2_H through $3FFF_H$ in Bits 0-13.

There are four modes to choose from:

0. Puts out low during second half of count.
1. Square wave
2. Single pulse upon TC being reached
3. Repetitive single pulse everytime TC is readied and automatic reload of counter upon TC being reached, until instructed to stop by a new command loaded into C/S.

Bits 6-7 of Command/Status Register Contents are used to start and stop the counter. There are four commands to choose from:

Note: See the further description on Command/Status Register.

C/S7	C/S6	
0	0	NOP — Do not affect counter operation.
0	1	STOP — NOP if timer has not started; stop counting if the timer is running.
1	0	STOP AFTER TC — Stop immediately after present TC is reached (NOP if timer has not started)
1	1	START — Load mode and CNT length and start immediately after loading (if timer is not presently running). If timer is running, start the new mode and CNT length immediately after present TC is reached.

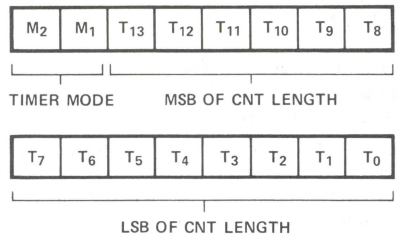
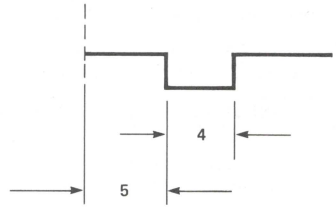


Figure 4. Timer Format

M2 M1 defines the timer mode as follows:

M2	M1	
0	0	Puts out low during second half of count.
0	1	Square wave, i.e., the period of the square wave equals the count length programmed with automatic reload at terminal count.
1	0	Single pulse upon TC being reached.
1	1	Automatic reload, i.e., single pulse everytime TC is reached.

Note: In case of an asymmetric count, i.e. 9, larger half of the count will be high, the larger count will stay active as shown in Figure 5.



Note: 5 and 4 refer to the number of clock cycles in that time period.

Figure 5. Asymmetric Count

The counter in the 8155 is not initialized to any particular mode or count when hardware RESET occurs, but RESET does stop the counting. Therefore, counting cannot begin following RESET until a START command is issued via the C/S register.

8085A MINIMUM SYSTEM CONFIGURATION

Figure 6 shows that a minimum system is possible using only three chips:

- 256 Bytes RAM
- 2K Bytes ROM
- 38 I/O Pins
- 1 Interval Timer
- 4 Interrupt Levels

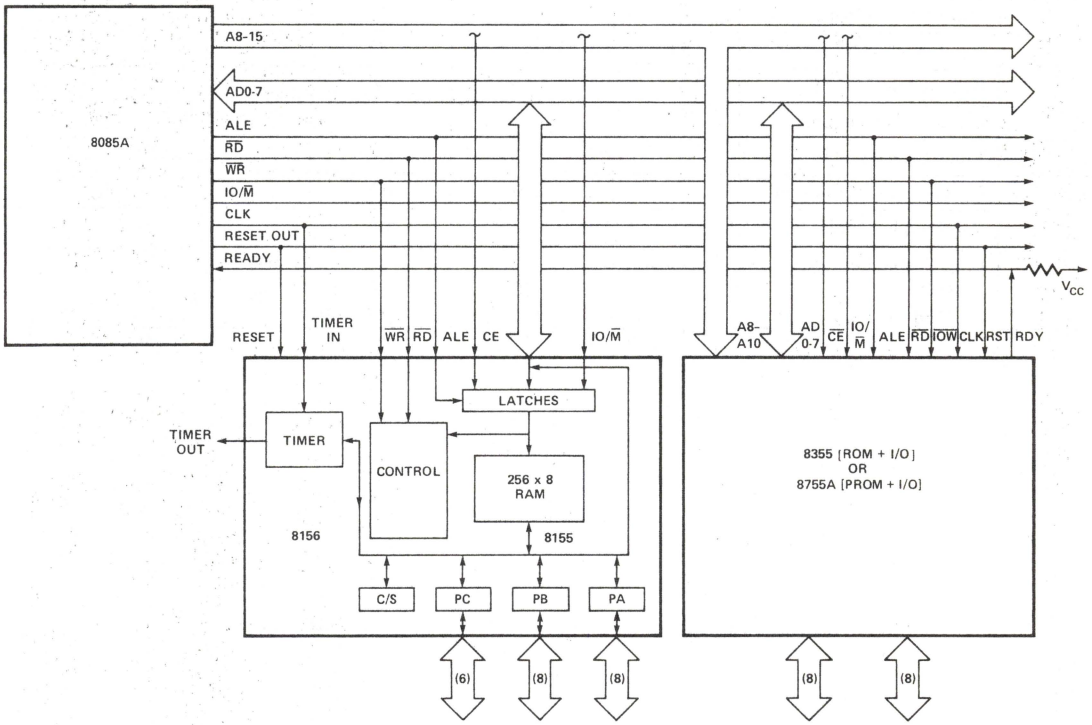


Figure 6. 8085 Minimum System Configuration

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... 0°C to +70°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin
With Respect to Ground ..... -0.3V to +7V
Power Dissipation 1.5W

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400μA
I_{IL}	Input Leakage		±10	μA	V_{IN} = V_{CC} to 0V
I_{LO}	Output Leakage Current		±10	μA	0.45V ≤V_{OUT} ≤V_{CC}
I_{CC}	V_{CC} Supply Current		180	mA	
I_{IL}(CE)	Chip Enable Leakage 8155 8156		 +100 −100	 μA μA	V_{IN} = V_{CC} to 0V

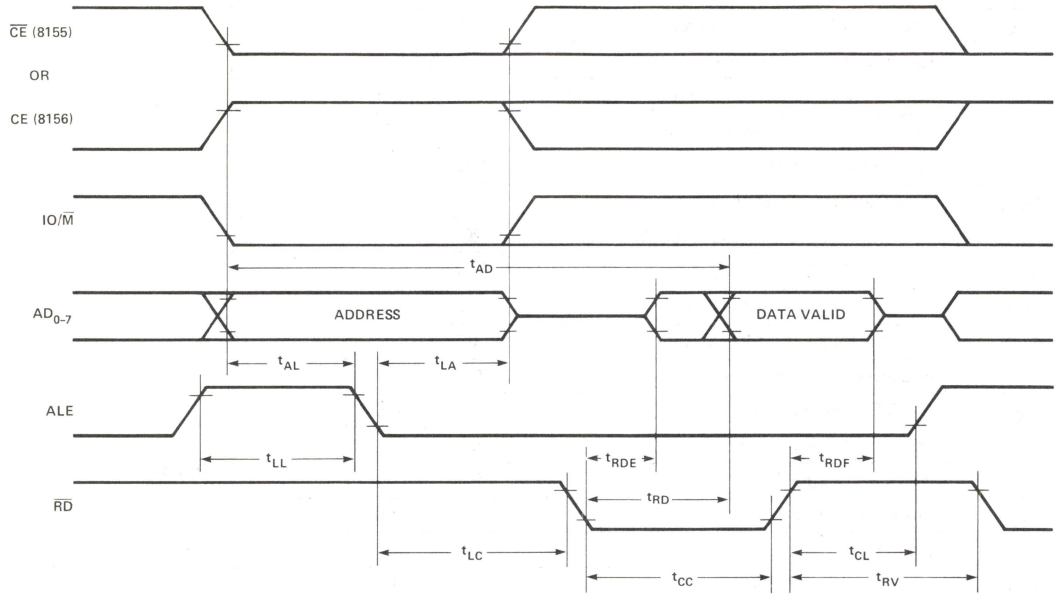
A.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
t_{AL}	Address to Latch Set Up Time	50		ns	
t_{LA}	Address Hold Time after Latch	80		ns	
t_{LC}	Latch to READ/WRITE Control	100		ns	
t_{RD}	Valid Data Out Delay from READ Control		170	ns	
t_{AD}	Address Stable to Data Out Valid		400	ns	
t_{LL}	Latch Enable Width	100		ns	
t_{RDF}	Data Bus Float After READ	0	100	ns	
t_{CL}	READ/WRITE Control to Latch Enable	20		ns	
t_{CC}	READ/WRITE Control Width	250		ns	
t_{DW}	Data In to WRITE Set Up Time	150		ns	
t_{WD}	Data In Hold Time After WRITE	0		ns	
t_{RV}	Recovery Time Between Controls	300		ns	
t_{WP}	WRITE to Port Output		400	ns	
t_{PR}	Port Input Setup Time	70		ns	
t_{RP}	Port Input Hold Time	50		ns	150 pF Load
t_{SBF}	Strobe to Buffer Full		400	ns	
t_{SS}	Strobe Width	200		ns	
t_{RBE}	READ to Buffer Empty		400	ns	
t_{SI}	Strobe to INTR On		400	ns	
t_{RDI}	READ to INTR Off		400	ns	
t_{PSS}	Port Setup Time to Strobe Strobe	50		ns	
t_{PHS}	Port Hold Time After Strobe	120		ns	
t_{SBE}	Strobe to Buffer Empty		400	ns	
t_{WBF}	WRITE to Buffer Full		400	ns	
t_{WI}	WRITE to INTR Off		400	ns	
t_{TL}	TIMER-IN to $\overline{\text{TIMER-OUT}}$ Low		400	ns	
t_{TH}	TIMER-IN to $\overline{\text{TIMER-OUT}}$ High		400	ns	
t_{RDE}	Data Bus Enable from READ Control	10		ns	

Note: For Timer Input Specification, see Figure 10.

WAVEFORMS

Read Cycle



Write Cycle

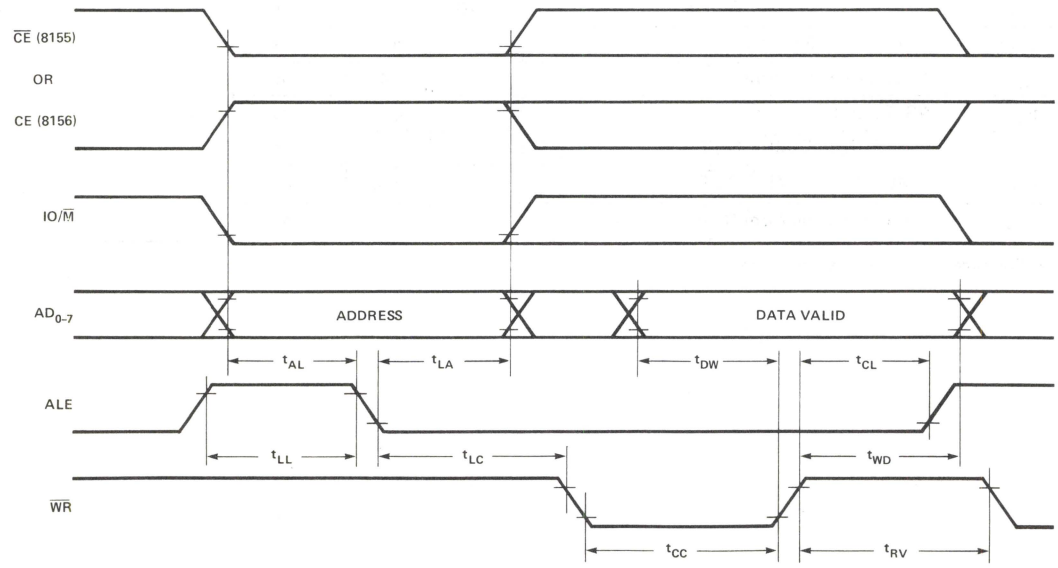
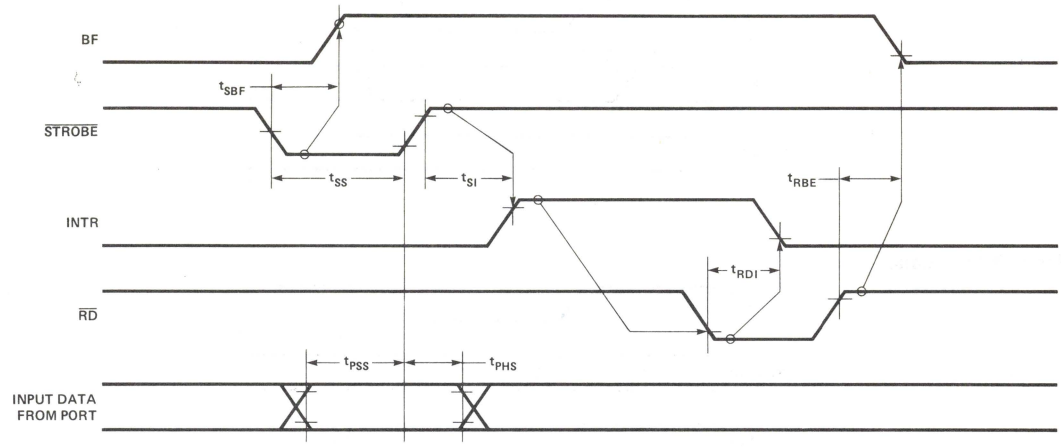


Figure 7. 8155/8156 Read/Write Timing Diagrams

Strobed Input Mode



Strobed Output Mode

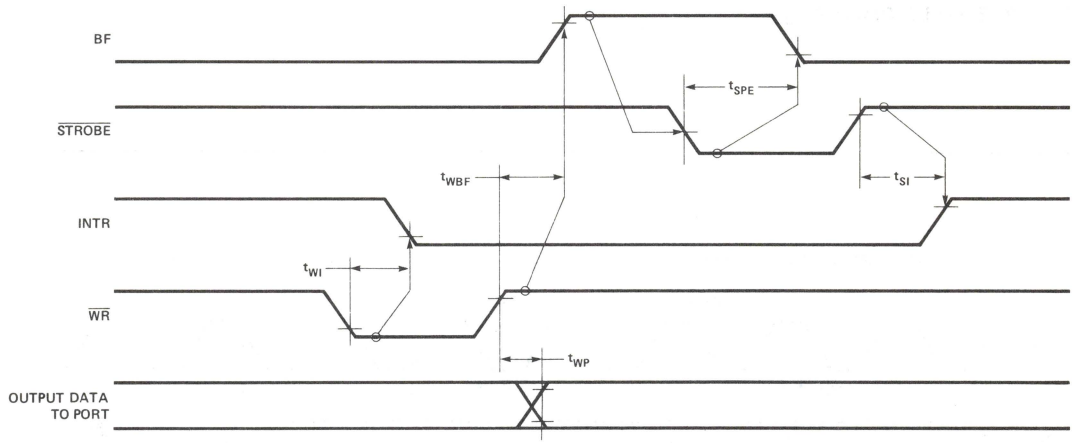
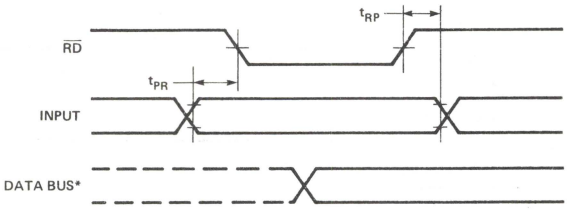
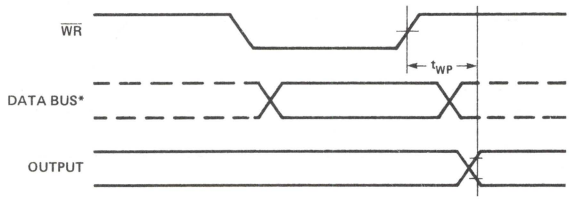


Figure 8. Strobed I/O Timing

Basic Input Mode

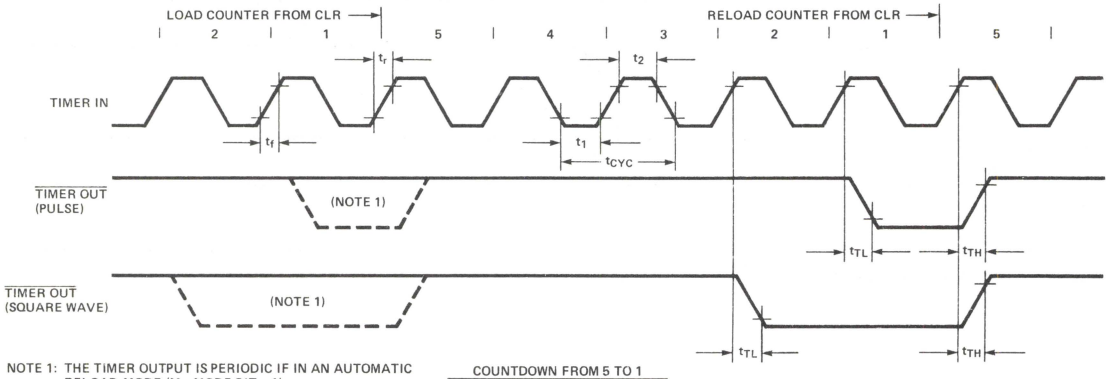


Basic Output Mode



*DATA BUS TIMING IS SHOWN IN FIGURE 7.

Figure 9. Basic I/O Timing Diagram



NOTE 1: THE TIMER OUTPUT IS PERIODIC IF IN AN AUTOMATIC RELOAD MODE (M_1 MODE BIT = 1)

COUNTDOWN FROM 5 TO 1		
t_{CYC}	320 nsec	MIN.
t_r AND t_f	30 nsec	MAX.
t_1	80 nsec	MIN.
t_2	120 nsec	MIN.
t_{TL} AND t_{TH}	400 nsec	MAX.

Figure 10. Timer Output Waveform

APPLICATION EXAMPLES

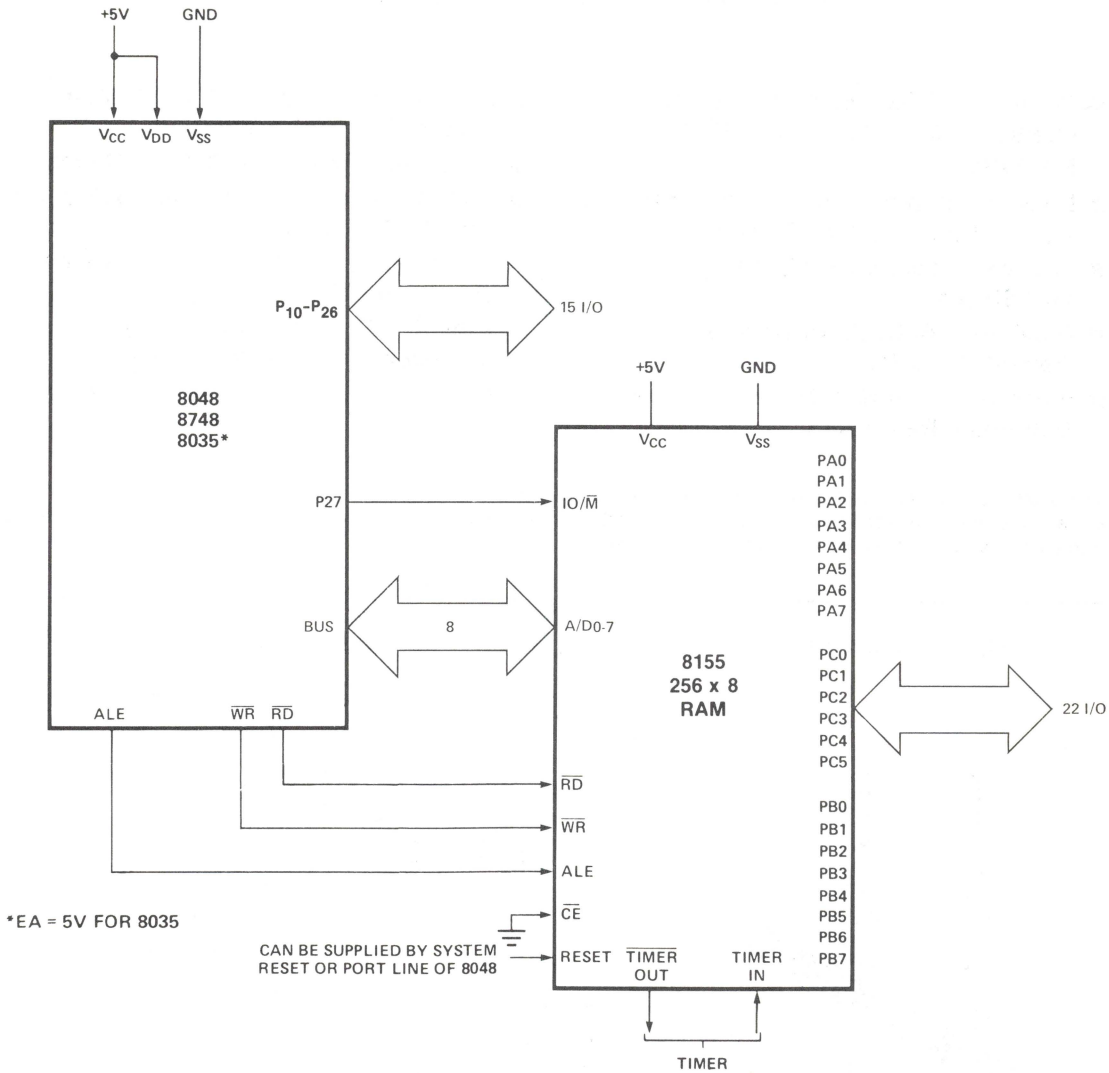


Figure 11. 8048 Interface to 8155

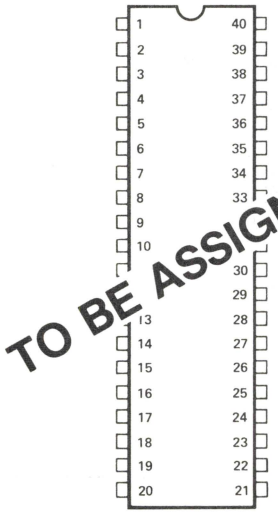
ADVANCE INFORMATION
Characteristics are subject to change without notice

8202
DYNAMIC RAM CONTROLLER

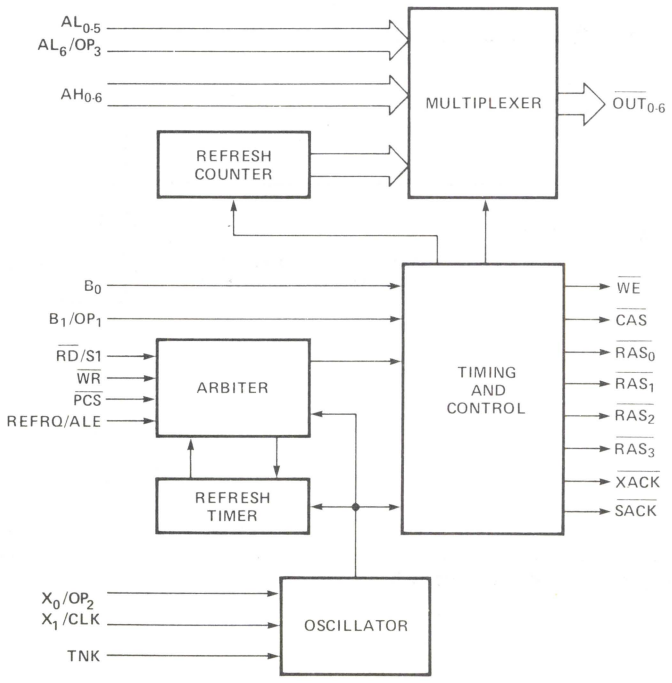
- **Provides All Signals Necessary to Control 2104A, 2116, or 2117 Dynamic Memories**
- **Directly Addresses and Drives Up to 64K Bytes Without External Drivers**
- **Provides Address Multiplexing and Strobes**
- **Provides a Refresh Timer and a Refresh Counter**
- **Refresh Cycles May be Internally or Externally Requested**
- **Provides High Speed Refresh/Memory Access Request Arbitration**
- **Provides Transparent Refresh Capability**
- **Fully Compatible with Intel® 8080A and 8085A Microprocessors**
- **Decodes 8085A Status for Advanced Read Capability**
- **Provides System Acknowledge and Transfer Acknowledge Signals**
- **Internal or External Clock Capability**

The 8202 is a Dynamic RAM System Controller designed to provide all signals necessary to use 2104A, 2116, or 2117 Dynamic RAMs in microcomputer systems. The 8202 provides multiplexed addresses and address strobes, as well as refresh/access arbitration. Refresh cycles can be started internally or externally.

PIN CONFIGURATION



8202 BLOCK DIAGRAM



8355
16,384-BIT ROM WITH I/O PORTS

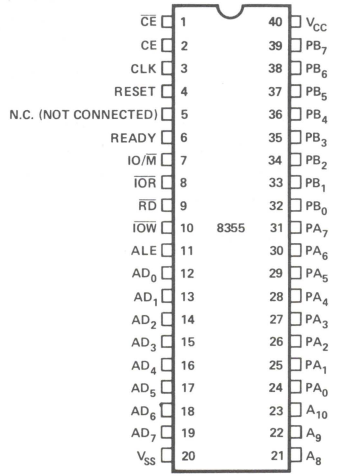
- **Directly Compatible with 8085A and 8048 CPU**

- **2048 Words × 8 Bits**
- **Single +5V Power Supply**
- **Internal Address Latch**
- **2 General Purpose 8-Bit I/O Ports**
- **Each I/O Port Line Individually Programmable as Input or Output**
- **Multiplexed Address and Data Bus**
- **40-Pin DIP**

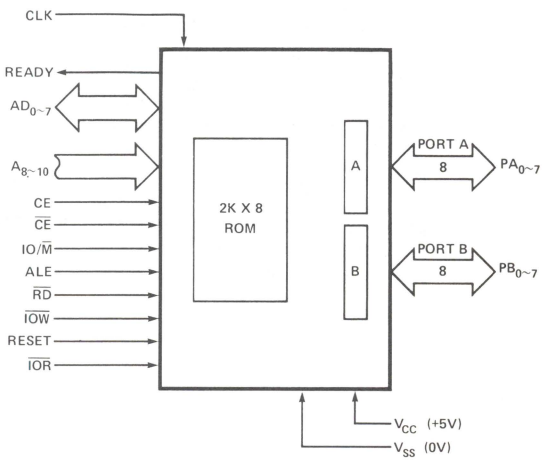
The Intel® 8355 is a ROM and I/O chip to be used in the MCS-85™ and MCS-48™ microcomputer systems. The ROM portion is organized as 2048 words by 8 bits. It has a maximum access time of 400 ns to permit use with no wait states in the 8085A CPU.

The I/O portion consists of 2 general purpose I/O ports. Each I/O port has 8 port lines, and each I/O port line is indivdually programmable as input or output.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN DESCRIPTION

Symbol	Function
ALE	When ALE (Address Latch Enable) is high, AD_{0-7}, IO/$\overline{M}$, A_{8-10}, CE, and $\overline{CE}$ enter address latched. The signals (AD, IO/$\overline{M}$, A_{8-10}, CE, $\overline{CE}$) are latched in at the trailing edge of ALE.
AD_{0-7}	Bi-directional Address/Data bus. The lower 8-bits of the ROM or I/O address are applied to the bus lines when ALE is high. During an I/O cycle, Port A or B are selected based on the latched value of AD_0. If $\overline{RD}$ or $\overline{IOR}$ is low when latched Chip Enables are active, the output buffers present data on the bus.
A_{8-10}	These are the high order bits of the ROM address. They do not affect I/O operations.
$\overline{CE}$ CE	Chip Enable Inputs: $\overline{CE}$ is active low and CE is active high. The 8355 can be accessed only when BOTH Chip Enables are active at the time the ALE signal latches them up. If either Chip Enable input is not active, the AD_{0-7} and READY outputs will be in a high impedance state.
IO/$\overline{M}$	If the latched IO/$\overline{M}$ is high when $\overline{RD}$ is low, the output data comes from an I/O port. If it is low the output data comes from the ROM.
$\overline{RD}$	If the latched Chip Enables are active when $\overline{RD}$ goes low, the AD_{0-7} output buffers are enabled and output either the selected ROM location or I/O port. When both $\overline{RD}$ and $\overline{IOR}$ are high, the AD_{0-7} output buffers are tri-stated.
$\overline{IOW}$	If the latched Chip Enables are active, a low on $\overline{IOW}$ causes the output port pointed to by the latched value of AD_0 to be written with the data on AD_{0-7}. The state of IO/$\overline{M}$ is ignored.

Symbol	Function
CLK	The CLK is used to force the READY into its high impedance state after it has been forced low by $\overline{CE}$ low, CE high and ALE high.
READY	Ready is a tri-state output controlled by $\overline{CE}$, CE, ALE and CLK. READY is forced low when the Chip Enables are active during the time ALE is high, and remains low until the rising edge of the next CLK (see Figure 4).
PA_{0-7}	These are general purpose I/O pins. Their input/output direction is determined by the contents of Data Direction Register (DDR). Port A is selected for write operations when the Chip Enables are active and $\overline{IOW}$ is low and a 0 was previously latched from AD_0. Read operation is selected by $\overline{IOR}$ low when the Chip is enabled and AD_0 low. Alternately, IO/$\overline{M}$ high and $\overline{RD}$ low may be used in place of $\overline{IOR}$ when the chip is enabled and AD_0 is low to allow reading from a port.
PB_{0-7}	This general purpose I/O port is identical to Port A except that it is selected by a 1 latched from AD_0.
RESET	An input high on RESET causes all pins in Ports A and B to assume input mode.
$\overline{IOR}$	When the Chip Enables are active, a low on $\overline{IOR}$ will output the selected I/O port onto the AD bus. $\overline{IOR}$ low performs the same function as the combination IO/$\overline{M}$ high and $\overline{RD}$ low.
V_{CC}	+5 volt supply.
V_{SS}	0 volt supply.

FUNCTIONAL DESCRIPTION

ROM Section

The ROM section of the chip is addressed by an 11-bit address and the Chip Enables. The address and levels on the Chip Enable pins are latched into the address latches on the falling edge of ALE. If the latched Chip Enables are active and IO/$\overline{M}$ is low when $\overline{RD}$ goes low, the contents of the ROM location addressed by the latched address are put out through AD_{0-7} output buffers.

I/O Section

The I/O section of the chip is addressed by the latched value of AD_{0-1}. Two 8-bit Data Direction Registers in 8355 determine the input/output status of each pin in the corresponding ports. A 0 specifies an input mode, and a 1 specifies an output mode. The table summarizes port and DDR designation. *DDR's cannot be read.*

AD_1	AD_0	Selection
0	0	Port A
0	1	Port B
1	0	Port A Data Direction Register (DDR A)
1	1	Port B Data Direction Register (DDR B)

When $\overline{IOW}$ goes low and the Chip Enables are active, the data on the AD_{0-7} is written into I/O port selected by the latched value of AD_{0-1}.

During this operation all I/O bits of the selected port are affected, regardless of their I/O mode and the state of IO/$\overline{M}$. The actual output level does not change until $\overline{IOW}$ returns high (glitch free output).

A port can be read out when the latched Chip Enables are active and either $\overline{RD}$ goes low with IO/$\overline{M}$ high, or $\overline{IOR}$ goes low. Both input and output mode bits of a selected port will appear on lines AD_{0-7}.

To clarify the function of the I/O ports and Data Direction Registers, Figure 1 shows the configuration of one bit of PORT A and DDR A. The same logic applies to PORT B and DDR B.

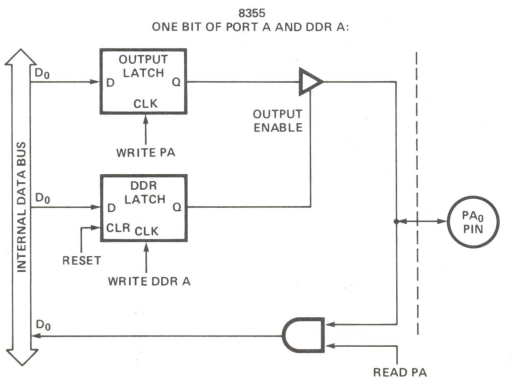


Figure 1. 8355 Block Diagram Showing One Bit of Port A and DDR A

Note that hardware RESET or writing a zero to the DDR latch will cause the output latch's output buffer to be disabled, preventing the data in the output latch from being passed through to the pin. This is equivalent to putting the port in the input mode. Note also that the data can be written to the Output Latch even though the Output Buffer has been disabled. This enables a port to be initialized with a value prior to enabling the output.

The diagram also shows that the contents of PORT A and PORT B can be read even when the ports are configured as outputs.

System Interface with 8085A

A system using the 8355 can use either one of the two I/O Interface techniques:

- Memory Mapped I/O
- Standard I/O

If a memory mapped I/O approach is used the 8355 will be selected by the combination of both the Chip Enables and IO/$\overline{M}$ using the AD_{8-15} address lines. See Figure 2.

If a standard I/O technique is used, the system can use the feature of both CE and $\overline{CE}$. By using a combination of unused address lines A_{11-15} and the Chip Enable inputs, the 8085A system can use up to 5 each 8335's without requiring a CE decoder. See Figure 3.

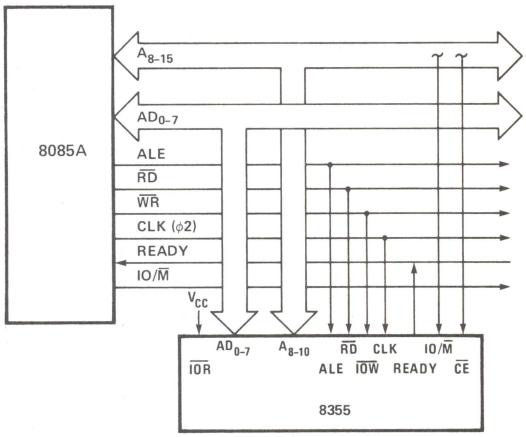
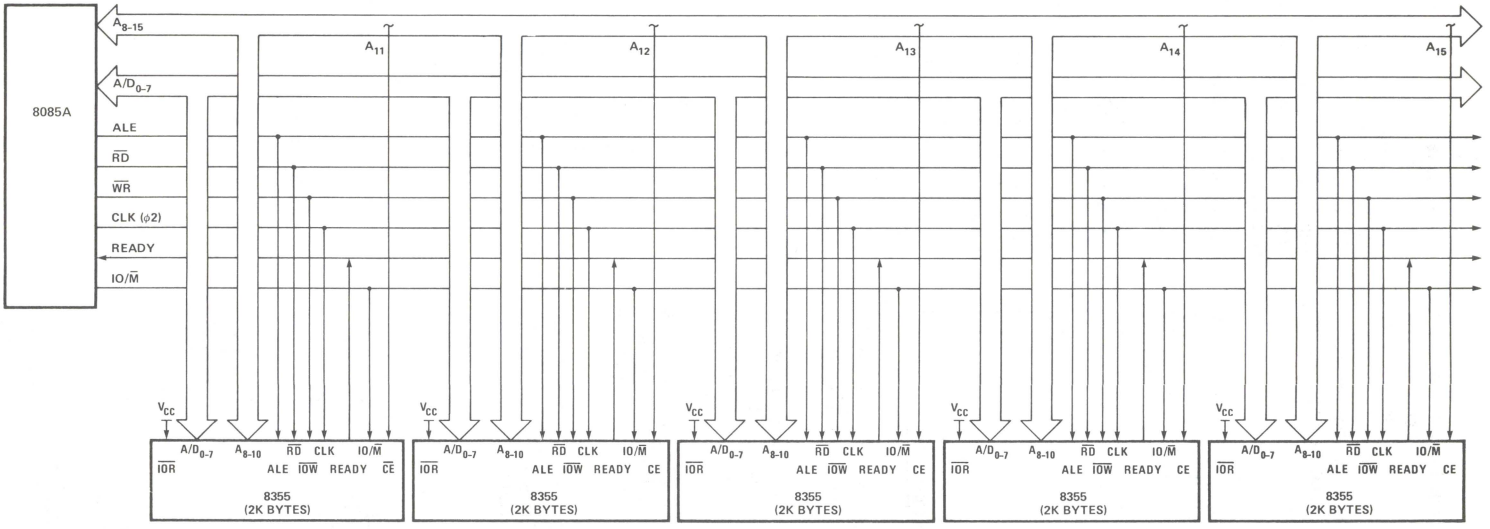


Figure 2. 8355 in 8085A System (Memory Mapped I/O)



Note: Use $\overline{CE}$ for the first 8355 in the system, and CE for the other 8355's. Permits up to 5 ea. 8355's in a system without CE decoder.

Figure 3. 8355 in 8085A System (Standard IO)

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... 0°C to +70°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin
With Respect to Ground ..... -0.3V to +7V
Power Dissipation 1.5W

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	V	V_{CC} = 5.0V
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	V_{CC} = 5.0V
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400μA
I_{IL}	Input Leakage		10	μA	V_{IN} = V_{CC} to 0V
I_{LO}	Output Leakage Current		±10	μA	0.45V ≤V_{OUT} ≤V_{CC}
I_{CC}	V_{CC} Supply Current		180	mA	

A.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
t_{CYC}	Clock Cycle Time	320		ns	
T_1	CLK Pulse Width	80		ns	C_{LOAD} = 150 pF
T_2	CLK Pulse Width	120		ns	
t_f,t_r	CLK Rise and Fall Time		30	ns	
t_{AL}	Address to Latch Set Up Time	50		ns	
t_{LA}	Address Hold Time after Latch	80		ns	
t_{LC}	Latch to READ/WRITE Control	100		ns	
t_{RD}	Valid Data Out Delay from READ Control		170	ns	
t_{AD}	Address Stable to Data Out Valid		400	ns	150 pF Load
t_{LL}	Latch Enable Width	100		ns	
t_{RDF}	Data Bus Float after READ	0	100	ns	
t_{CL}	READ/WRITE Control to Latch Enable	20		ns	
t_{CC}	READ/WRITE Control Width	250		ns	
t_{DW}	Data In to WRITE Set Up Time	150		ns	
t_{WD}	Data In Hold Time After WRITE	10		ns	
t_{WP}	WRITE to Port Output		400	ns	
t_{PR}	Port Input Set Up Time	50		ns	
t_{RP}	Port Input Hold Time	50		ns	
t_{RYH}	READY HOLD TIME	0	160	ns	
t_{ARY}	ADDRESS (CE) to READY		160	ns	
t_{RV}	Recovery Time between Controls	300		ns	
t_{RDE}	Data Out Delay from READ Control	10		ns	

WAVEFORMS

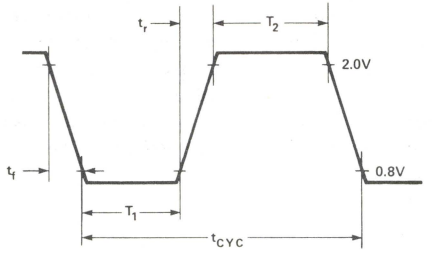


Figure 4. Clock Specification for 8355

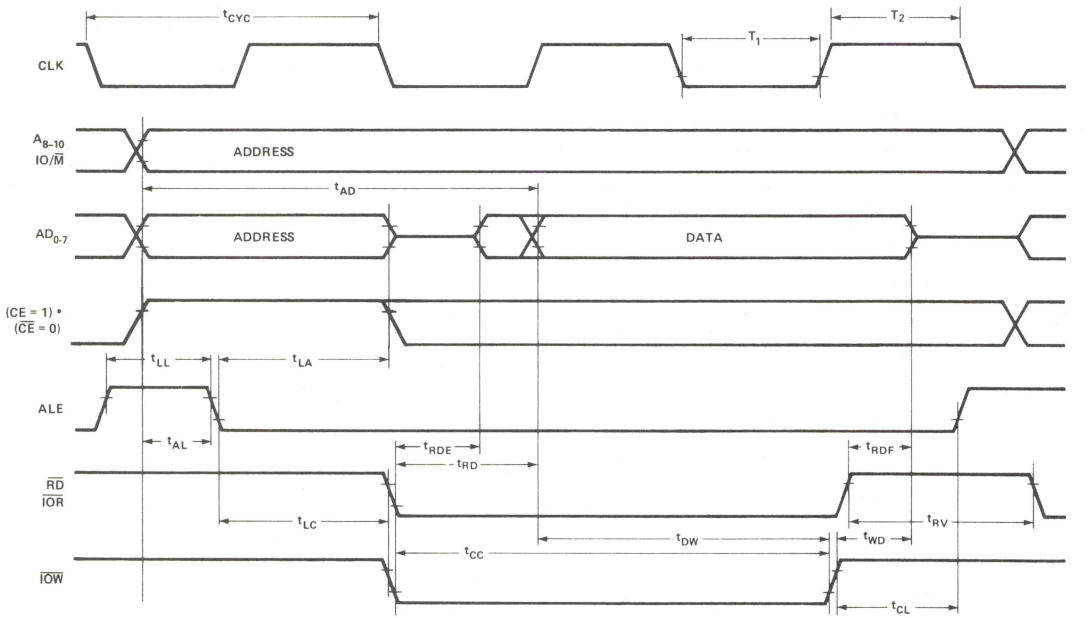


Figure 5. ROM Read and I/O Read and Write

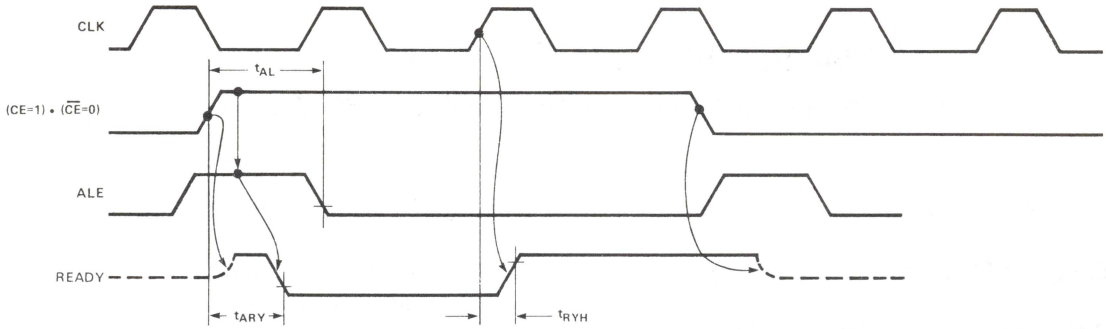


Figure 6. Wait State Timing (READY 5 0)

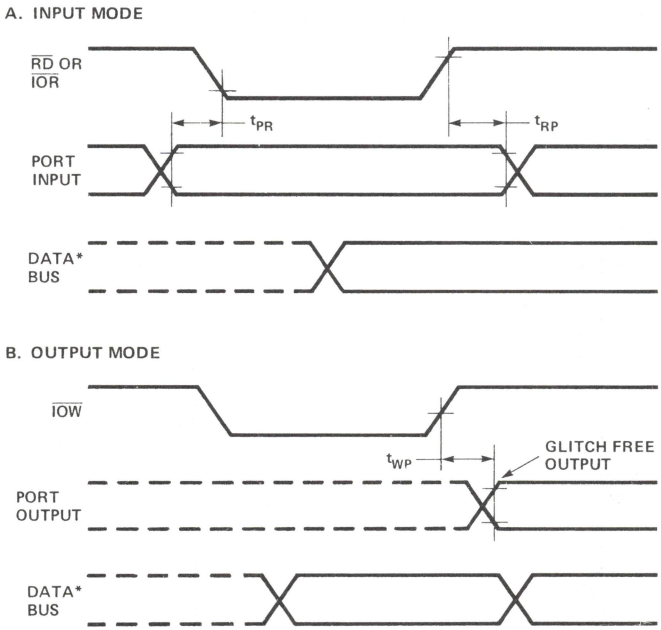


Figure 7. I/O Port Timing

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

8755A
16,384-BIT EPROM WITH I/O PORTS

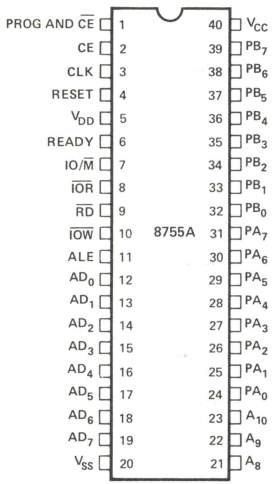
- **Directly Compatible with 8085A and 8048 CPU**

- **2048 Words × 8 Bits**
- **Single +5V Power Supply (V_{CC})**
- **U.V. Erasable and Electrically Reprogrammable**
- **Internal Address Latch**
- **2 General Purpose 8-Bit I/O Ports**
- **Each I/O Port Line Individually Programmable as Input or Output**
- **Multiplexed Address and Data Bus**
- **40-Pin DIP**

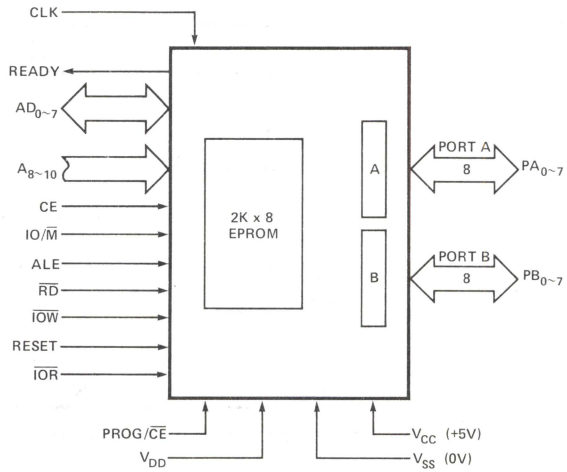
The Intel® 8755A is an erasable and electrically reprogrammable ROM (EPROM) and I/O chip to be used in the MCS-85™ and MCS-48™ microcomputer systems. The PROM portion is organized as 2048 words by 8 bits. It has a maximum access time of 400 ns to permit use with no wait states in an 8085A CPU.

The I/O portion consists of 2 general purpose I/O ports. Each I/O port has 8 port lines, and each I/O port line is individually programmable as input or output.

PIN CONFIGURATION



BLOCK DIAGRAM



MCS-80/85

PIN DESCRIPTION

Symbol	Function
ALE	When Address Latch Enable is high, AD_{0-7}, IO/$\overline{M}$, A_{8-10}, CE, and $\overline{CE}$ enter the address latches. The signals (AD, IO/M, A_{8-10}, CE) are latched in at the trailing edge of ALE.
AD_{0-7}	Bi-directional Address/Data bus. The lower 8-bits of the PROM or I/O address are applied to the bus lines when ALE is high. During an I/O cycle, Port A or B are selected based on the latched value of AD_0. If $\overline{RD}$ or $\overline{IOR}$ is low when the latched Chip Enables are active, the output buffers present data on the bus.
A_{8-10}	These are the high order bits of the PROM address. They do not affect I/O operations.
$\overline{CE}$/PROG CE	CHIP ENABLE INPUTS: $\overline{CE}$ is active low and CE is active high. Both chip enables must be active to permit accessing the PROM. $\overline{CE}$ is also used as a programming pin (see section on programming).
IO/$\overline{M}$	If the latched IO/$\overline{M}$ is high when $\overline{RD}$ is low, the output data comes from an I/O port. If it is low the output data comes from the PROM.
$\overline{RD}$	If the latched Chip Enables are active when $\overline{RD}$ goes low, the AD_{0-7} output buffers are enabled and output either the selected PROM location or I/O port. When both $\overline{RD}$ and $\overline{IOR}$ are high, the AD_{0-7} output buffers are tri-stated.
$\overline{IOW}$	If the latched Chip Enables are active, a low on $\overline{IOW}$ causes the output port pointed to by the latched value of AD_0 to be written with the data on AD_{0-7}. The state of IO/$\overline{M}$ is ignored.
CLK	The CLK is used to force the READY into its high impedance state after it has been forced low by $\overline{CE}$ low, CE high, and ALE high.
READY	READY is a 3-state output controlled by CE, $\overline{CE}$, ALE and CLK. READY is forced low when the Chip Enables are active during the time ALE is high, and remains low until the rising edge of the next CLK (see Figure 2.).
PA_{0-7}	These are general purpose I/O pins. Their input/output direction is determined by the contents of Data Direction Register (DDR). Port A is selected for write operations when the Chip Enables are active and $\overline{IOW}$ is low and a 0 was previously latched from AD_0. Read operation is selected by either $\overline{IOR}$ low and active Chip Enables and AD_0 low, or IO/$\overline{M}$ high, $\overline{RD}$ low, active Chip Enables, and AD_0 low.
PB_{0-7}	This general purpose I/O port is identical to Port A except that it is selected by a 1 latched from AD_0.
RESET	In normal operation, an input high on RESET causes all pins in Ports A and B to assume input mode (clear DDR register).
$\overline{IOR}$	When the Chip Enables are active, a low on $\overline{IOR}$ will output the selected I/O port onto the AD bus. $\overline{IOR}$ low performs the same function as the combination of IO/$\overline{M}$ high and $\overline{RD}$ low. When $\overline{IOR}$ is not used in a system, $\overline{IOR}$ should be tied to V_{CC} ("1").
V_{CC}	+5 volt supply.
V_{SS}	Ground Reference.
V_{DD}	V_{DD} is a programming voltage, and it is normally tied to +5V. For programming, a high voltage is supplied with V_{DD}, = 25V, typical.

FUNCTIONAL DESCRIPTION

PROM Section

The 8755A contains an 8-bit address latch which allows it to interface directly to MCS-48 and MCS-85 Microcomputers without additional hardware.

The PROM section of the chip is addressed by the 11-bit address and CE. The address, $\overline{CE}$ and CE are latched into the address latches on the falling edge of ALE. If the latched Chip Enables are active and IO/$\overline{M}$ is low when $\overline{RD}$ goes low, the contents of the PROM location addressed by the latched address are put out on the AD_{0-7} lines.

I/O Section

The I/O section of the chip is addressed by the latched value of AD_{0-1}. Two 8-bit Data Direction Registers determine the input/output status of each pin in the corresponding port. A 0 specifies an input mode, and a 1 specifies an output mode. The table summarizes port and DDR designation. Contents of the DDR's cannot be read.

AD_1	AD_0	Selection
0	0	Port A
0	1	Port B
1	0	Port A Data Direction Register (DDR A)
1	1	Port B Data Direction Register (DDR B)

When $\overline{IOW}$ goes low and the Chip Enables are active, the data on the AD is written into I/O port selected by the latched value of AD_{0-1}. During this operation all I/O bits of the selected port are affected, regardless of their I/O mode and the state of IO/$\overline{M}$. The actual output level does not change until $\overline{IOW}$ returns high. (glitch free output).

A port can be read out when the latched Chip Enables are active and either $\overline{RD}$ goes low with IO/$\overline{M}$ high, or $\overline{IOR}$ goes low. Both input and output mode bits of a selected port will appear on lines AD_{0-7}.

To clarify the function of the I/O Ports and Data Direction Registers, the following diagram shows the configuration of one bit of PORT A and DDR A. The same logic applies to PORT B and DDR B.

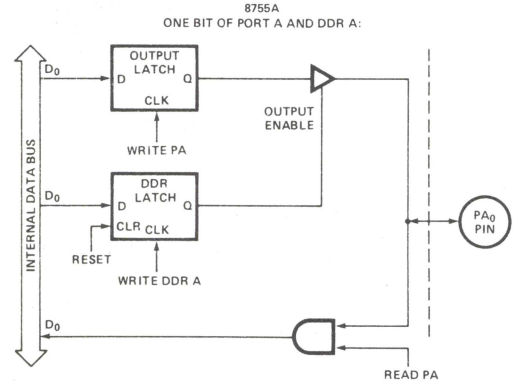


Figure 1. 8755A: One Bit of Port A and DDR A

Note that hardware RESET or writing a zero to the DDR latch will cause the output latch's output buffer to be disabled, preventing the data in the Output Latch from being passed through to the pin. This is equivalent to putting the port in the input mode. Note also that the data can be written to the Output Latch even though the Output Buffer has been disabled. This enables a port to be initialized with a value prior to enabling the output.

The diagram also shows that the contents of PORT A and PORT B can be read even when the ports are configured as outputs.

Table 1. 8755/8755A Programming Module Cross Reference

MODULE NAME	USE WITH	WILL PROGRAM
UPP 855	UPP[1]	8755
UPP 955	UPP	8755A
UPP UP1[4]	UPP 955	8755
UPP UP2[4]	UPP 855	8755A
PROMPT™ 875	PROMPT 80/85[2]	8755
PROMPT 975	PROMPT 80/85	8755A
PROMPT 475	PROMPT 48[3]	8755A

NOTES:
1. Intel's Universal PROM Programmer module, described on p. 13-71 of the Intel 1977 Data Catalog.
2. Described on p. 13-39 of 1978 Data Catalog.
3. Described on p. 13-34 of 1978 Data Catalog.
4. Special adaptor socket.

Erasure Characteristics

The erasure characteristics of the 8755A are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data show that constant exposure to room level flourescent lighting could erase the typical 8755A in approximately 3 years while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the 8755A is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 8755 window to prevent unintentional erasure.

The recommended erasure procedure (see page 3-55) for the 8755A is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000μW/cm^2 power rating. The 8755A should be placed within one inch from the lamp tubes during erasure. Some lamps have a filter on their tubes and this filter should be removed before erasure.

Programming

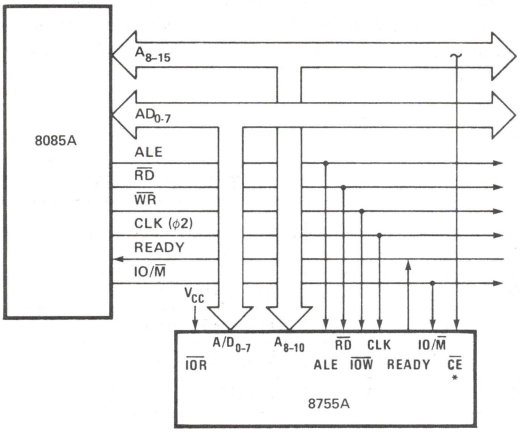
Initially, and after each erasure, all bits of the EPROM portions of the 8755A are in the "1" state. Information is introduced by selectively programming "0" into the desired bit locations. A programmed "0" can only be changed to a "1" by UV erasure.

The 8755A can be programmed on the Intel® Universal PROM Programmer (UPP), and the PROMPT™ 80/85 and PROMPT-48™ design aids. The appropriate programming modules and adapters for use in programming both 8755A's and 8755's are shown in the table below.

The program mode itself consists of programming a single address at a time, giving a single 50 msec pulse for every address. Generally, it is desirable to have a verify cycle after a program cycle for the same address as shown in the attached timing diagram. In the verify cycle (i.e., normal memory read cycle) 'V_{DD}' should be at 0 volts for the 8755, but for 8755A it should be V_{CC} (+5V). Except for the V_{DD} level during the read cycle, the 8755 and 8755A are functionally identical.

Preliminary timing diagrams and parameter values pertaining to the 8755/8755A programming operation are contained on pp. 11-91 and 11-92.

SYSTEM APPLICATIONS



*USE $\overline{CE}$ FOR FIRST 8755A IN SYSTEM, AND CE FOR OTHERS. BY CONNECTING CE OF EACH 8755A CHIP TO EACH OF A_{11} THROUGH A_{15}, THE MINIMUM SYSTEM CAN USE 5-8755A's (10K BYTES) WITHOUT REQUIRING CE DECODER.

Figure 2. 8755A in 8085A System (Standard I/O)

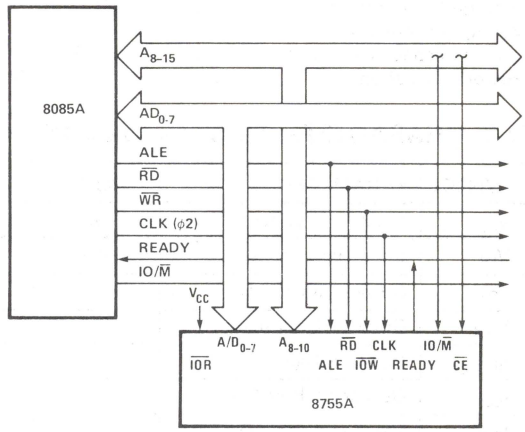


Figure 3. 8755A in 8085A System (Memory Mapped I/O)

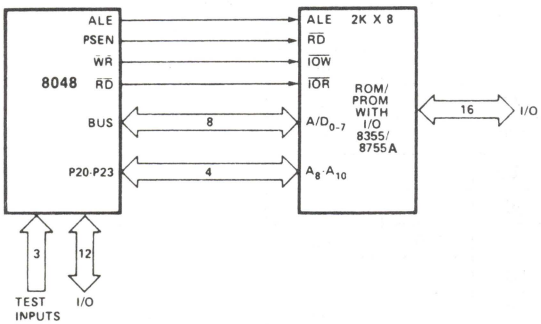


Figure 4. Interface to MCS-48™ Microcomputers

System Interface with 8048

The 8755A contains an 8-bit address latch which allows it to interface directly to MCS-48™ microcomputers without additional hardware (Figure 4). Program memory is accessed by applying 11 bits of address to the A_0–A_{10} inputs and a low level on the IO/$\overline{M}$ and $\overline{CE}$ inputs, then latching these inputs with ALE. The $\overline{CE}$ input serves to select one of several possible 8755A's in a system and the IO/$\overline{M}$ signal indicates that a subsequent read operation will be from program memory. While ALE is high the A_0–A_{10}, IO/$\overline{M}$, and $\overline{CE}$ inputs are allowed into the 8755A and when ALE is brought low, these inputs are latched. If the latched conditions indicate that a program memory fetch is to occur, a low level on $\overline{RD}$ will cause the data to be outputted on the data bus.

PRELIMINARY
Notice: This is a final specification. Some parameters may change.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-10°C to +70°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin With Respect to Ground	-0.5V to +7V
Power Dissipation	1.5W

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400μA
I_{IL}	Input Leakage		10	μA	V_{IN} = V_{CC} to 0V
I_{LO}	Output Leakage Current		±10	μA	0.45V ≤V_{OUT} ≤V_{CC}
I_{CC}	V_{CC} Supply Current		180	mA	

A.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
t_{CYC}	Clock Cycle Time	320		ns	
T_1	CLK Pulse Width	80		ns	C_{LOAD} = 150 pF
T_2	CLK Pulse Width	120		ns	(See Figure 3)
t_f,t_r	CLK Rise and Fall Time		30	ns	
t_{AL}	Address to Latch Set Up Time	50		ns	
t_{LA}	Address Hold Time after Latch	80		ns	
t_{LC}	Latch to READ/WRITE Control	100		ns	
t_{RD}	Valid Data Out Delay from READ Control		170	ns	
t_{AD}	Address Stable to Data Out Valid		450	ns	150 pF Load
t_{LL}	Latch Enable Width	100		ns	
t_{RDF}	Data Bus Float after READ	0	100	ns	
t_{CL}	READ/WRITE Control to Latch Enable	20		ns	
t_{CC}	READ/WRITE Control Width	250		ns	
t_{DW}	Data In to WRITE Set Up Time	150		ns	
t_{WD}	Data In Hold Time After WRITE	30		ns	
t_{WP}	WRITE to Port Output		400	ns	
t_{PR}	Port Input Set Up Time	50		ns	
t_{RP}	Port Input Hold Time	50		ns	
t_{RYH}	READY HOLD TIME	0	160	ns	
t_{ARY}	ADDRESS (CE) to READY		160	ns	
t_{RV}	Recovery Time between Controls	300		ns	
t_{RDE}	Data Out Delay from READ Control	10		ns	

WAVEFORMS

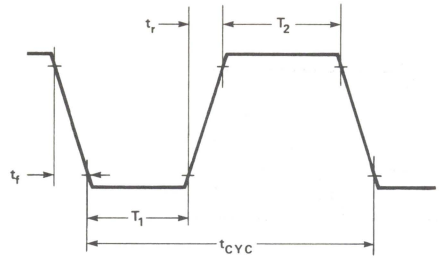


Figure 5. Clock Specification for 8755A

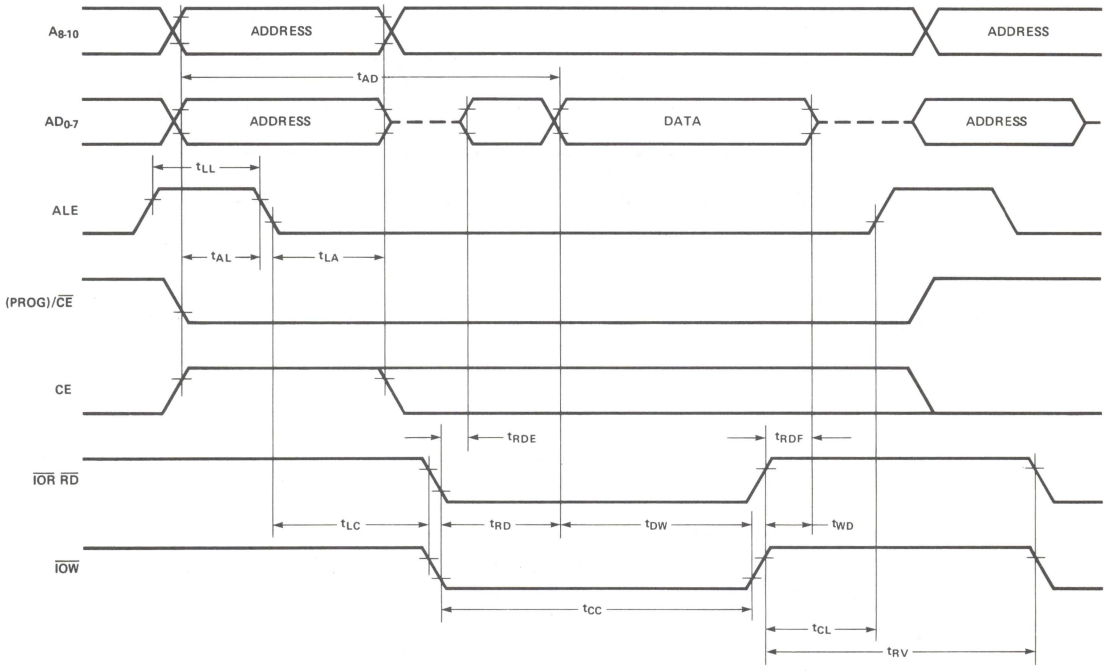
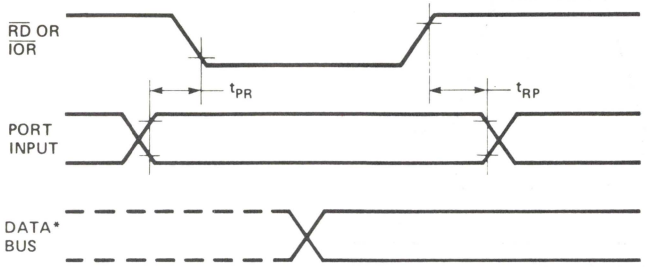


Figure 6. PROM Read, I/O Read and Write Timing

Please note that $\overline{CE1}$ must remain low for the entire cycle. This is due to the fact that the programming enable function common to this pin will disrupt internal data bus levels if $\overline{CE1}$ is taken high during the read.

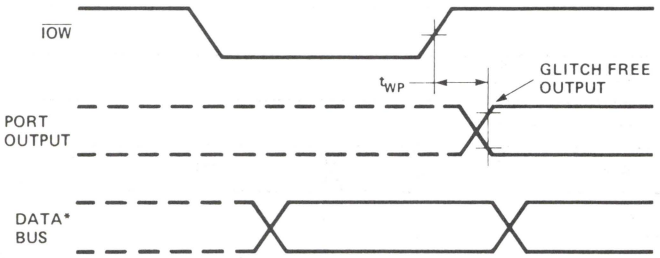
Input Mode

A. INPUT MODE



Output Mode

B. OUTPUT MODE



*DATA BUS TIMING IS SHOWN IN FIGURE 6.

Figure 7. I/O Port Timing

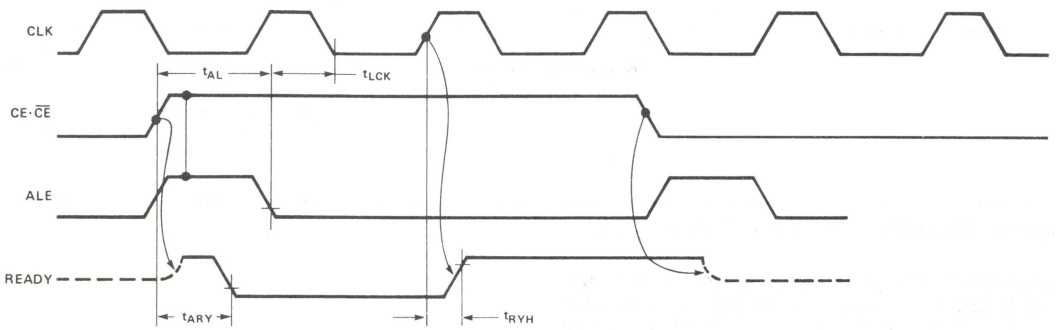


Figure 8. Wait State Timing (READY = 0)

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

D.C. SPECIFICATION FOR PROGRAMMING

(T_A = 0°C to 70°C; V_{CC} = 5V ±5%; V_{SS} = 0V)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Programming Voltage (during write to EPROM)	24	25	26	V
I_{DD}	Prog Supply Current		15	30	mA

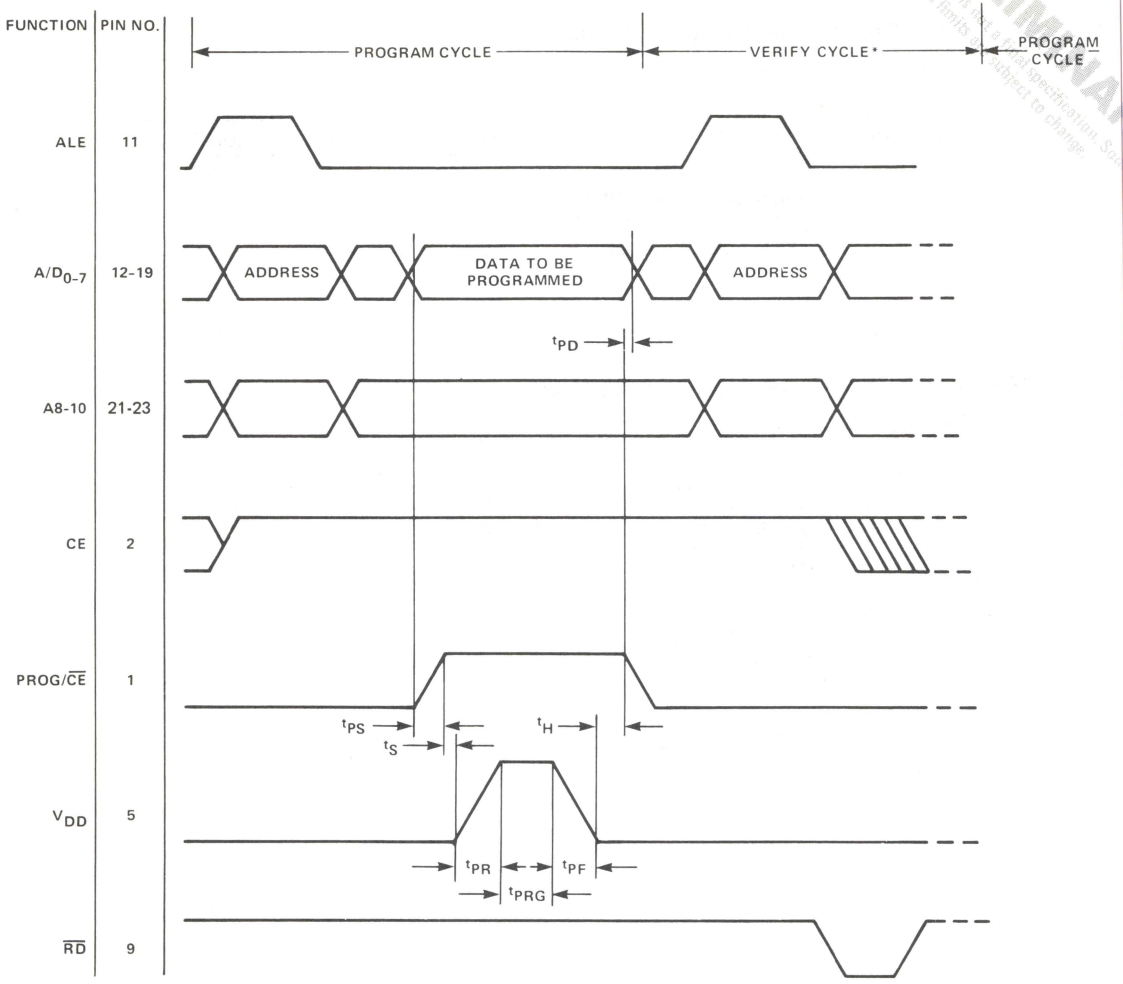
A.C. SPECIFICATION FOR PROGRAMMING

(T_A = 0°C to 70°C; V_{CC} = 5V ±5%; V_{SS} = 0V)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{PS}	Data Setup Time	10			ns
t_{PD}	Data Hold Time	0			ns
t_S	Prog Pulse Setup Time	2			μs
t_H	Prog Pulse Hold Time	2			μs
t_{PR}	Prog Pulse Rise Time	0.01	2		μs
t_{PF}	Prog Pulse Fall Time	0.01	2		μs
t_{PRG}	Prog Pulse Width	45	50		msec

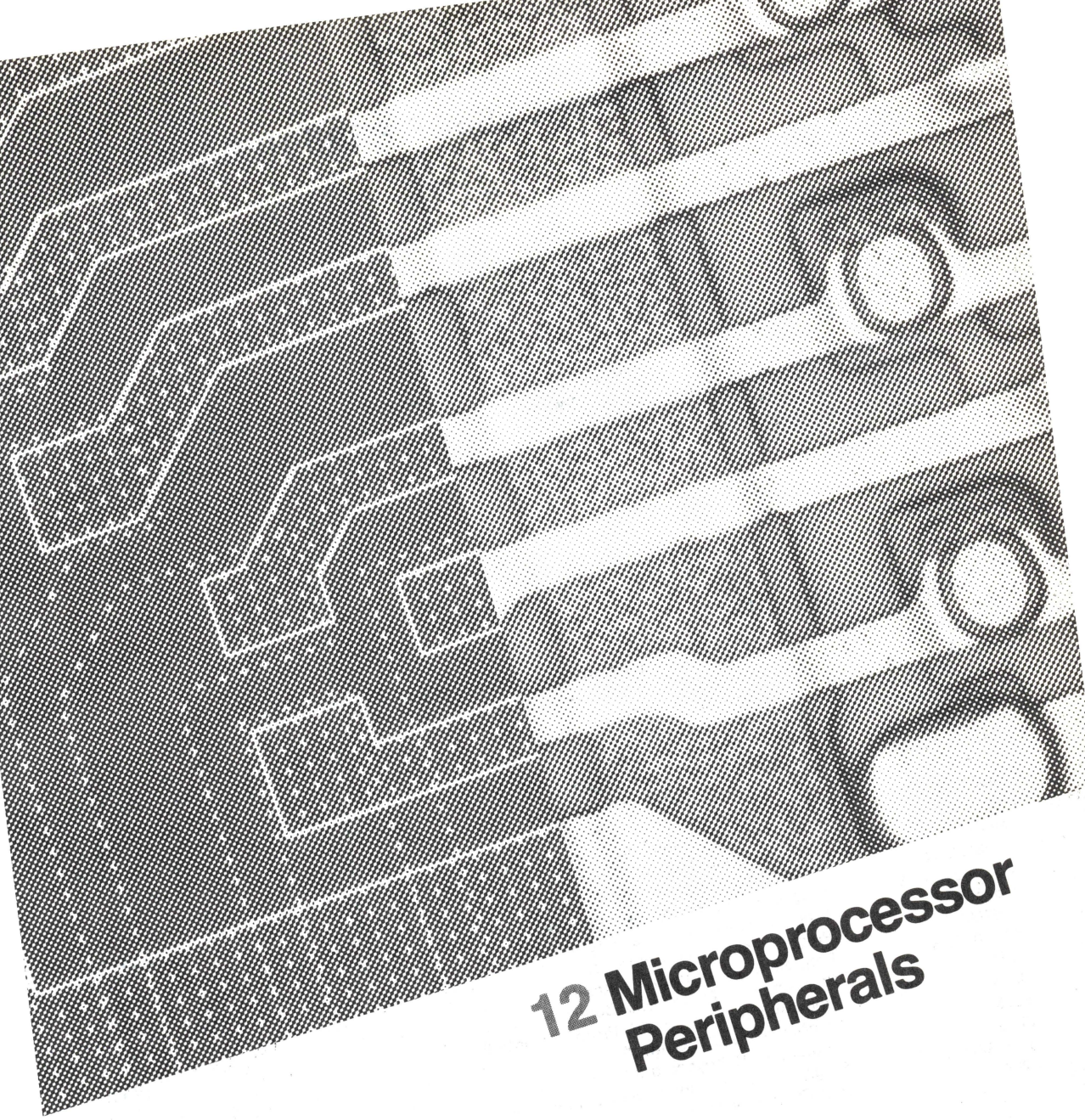
PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

WAVEFORMS



* VERIFY CYCLE IS A REGULAR MEMORY READ CYCLE (WITH V_{DD} = +5V FOR 8755A, V_{DD} = 0V FOR 8755.)

Figure 10. 8755/8755A Program Mode Timing Diagram



12 Microprocessor Peripherals

MICROPROCESSOR PERIPHERALS

INTRODUCTION

Intel peripherals greatly enhance the 8080, the 8085, and many other microcomputers. These peripherals can significantly reduce development time, operating software, package count, board space, and parts costs while improving performance and increasing throughput in microcomputer systems. This section contains the most up-to-date data about Intel peripherals now available.

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PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

8041/8741
UNIVERSAL PERIPHERAL INTERFACE
8-BIT MICROCOMPUTER

- **Fully Compatible with MCS-80™ and MCS-48™ Microprocessor Families**
- **Single Level Interrupt**
- **8-Bit CPU plus ROM, RAM, I/O, Timer and Clock in a Single Package**
- **Single 5V Supply**
- **Alternative to Custom LSI**
- **Pin Compatible ROM and EPROM Versions**
- **1K x 8 ROM/EPROM, 64 x 8 RAM, 18 Programmable I/O Pins**
- **Asynchronous Data Register for Interface to Master Processor**
- **Expandable I/O**

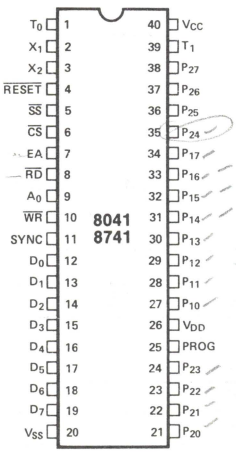
The Intel® 8041/8741 is a general purpose, programmable interface device designed for use with a variety of 8-bit microprocessor systems. It contains a low cost microcomputer with program memory, data memory, 8-bit CPU, I/O ports, timer/counter, and clock in a single 40-pin package. Interface registers are included to enable the UPI device to function as a peripheral controller in MCS-80™, MCS-85™, MCS-48™, and other 8-bit systems.

The UPI-41™ has 1K words of program memory and 64 words of data memory on-chip. To allow full user flexibility the program memory is available as ROM in the 8041 version or as UV-erasable EPROM in the 8741 version. The 8741 and the 8041 are fully pin compatible for easy transition from prototype to production level designs.

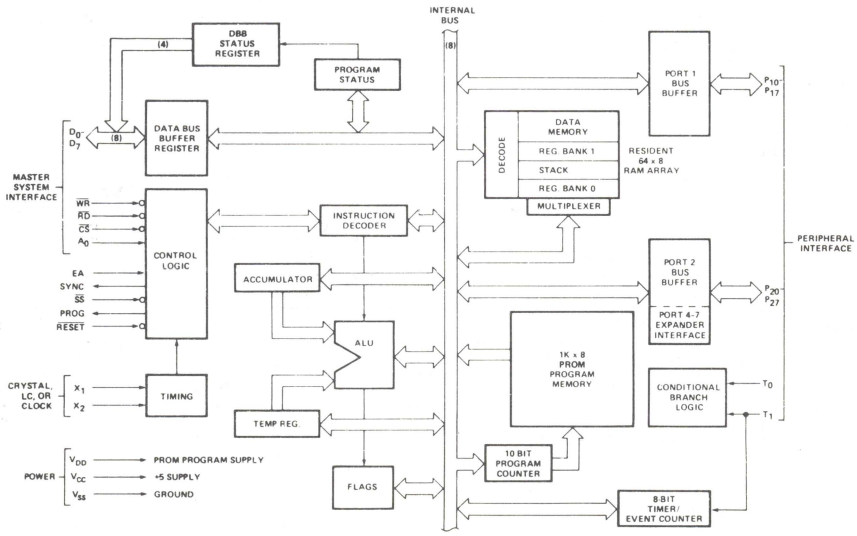
The device has two 8-bit, TTL compatible I/O ports and two test inputs. Individual port lines can function as either inputs or outputs under software control. I/O can be expanded with the 8243 device which is directly compatible and has 16 I/O lines. An 8-bit programmable timer/counter is included in the UPI device for generating timing sequences or counting external inputs. Additional UPI features include: single 5V supply, low power standby mode (in the 8041), single-step mode for debug (in the 8741), single level interrupt, and dual working register banks.

Because it's a complete microcomputer, the UPI provides more flexibility for the designer than conventional LSI interface devices. It is designed to be an efficient controller as well as an arithmetic processor. Applications include keyboard scanning, printer control, display multiplexing and similar functions which involve interfacing peripheral devices to microprocessor systems.

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin With
Respect to Ground ..... 0.5V to +7V
Power Dissipation ..... 1.5 Watt

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = V_{DD} = +5V ±5%, V_{SS} = 0V

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
V_{IL}	Input Low Voltage (All Except X_1, X_2)	-0.5		0.8	V	
V_{IH}	Input High Voltage (All Except X_1, X_2 $\overline{RESET}$)	2.0		V_{CC}	V	
V_{IH2}	Input High Voltage (X_1, $\overline{RESET}$)	3.0		V_{CC}	V	
V_{OL}	Output Low Voltage (D_0-D_7, Sync)			0.45	V	I_{OL} = 2.0 mA
V_{OL2}	Output Low Voltage (All Other Outputs Except Prog)			0.45	V	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage (D_0-D_7)	2.4			V	I_{OH} = -400 μA
V_{OH1}	Output High Voltage (All Other Outputs)	2.4			V	I_{OH} = -50 μA
I_{IL}	Input Leakage Current (T_0, T_1, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, A_0, EA)			±10	μA	$V_{SS} \le V_{IN} \le V_{CC}$
I_{OL}	Output Leakage Current (D_0-D_7, High Z State)			±10	μA	V_{SS} + 0.45 $\le V_{IN} \le V_{CC}$
I_{DD}	V_{DD} Supply Current		10	25	mA	
$I_{CC} + I_{DD}$	Total Supply Current		65	135	mA	
V_{OL3}	Output Low Voltage (Prog)			0.45	V	I_{OL} = 1.0 mA
I_{LI1}	Low Input Source Current P_{10}-P_{17} P_{20}-P_{27}			0.4	mA	V_{IL} = 0.8V
I_{LI2}	Low Input Source Current $\overline{RESET}$, SS			0.2	mA	V_{IL} = 0.8V

A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = V_{DD} = +5V ±5%, V_{SS} = 0V

DBB Read:

Symbol	Parameter	8741		8041		Units	Test Conditions
		Min.	Max.	Min.	Max.		
t_{AR}	$\overline{CS}$, A_0 Setup to $\overline{RD}$ ↓	60		0		ns	
t_{RA}	$\overline{CS}$, A_0 Hold After $\overline{RD}$ ↑	30		0		ns	
t_{RR}	$\overline{RD}$ Pulse Width	300	2 × t_{CY}	250		ns	t_{CY} = 2.5 μs
t_{AD}	$\overline{CS}$, A_0 to Data Out Delay		370		150	ns	
t_{RD}	$\overline{RD}$ ↓ to Data Out Delay		200		150	ns	
t_{DF}	$\overline{RD}$ ↑ to Data Float Delay	10		10		ns	
			140		100	ns	
t_{RV}	Recovery Time Between Reads And/Or Write	1		1		μs	
t_{CY}	Cycle Time	2.5		2.5		μs	6 MHz Crystal

DBB Write:

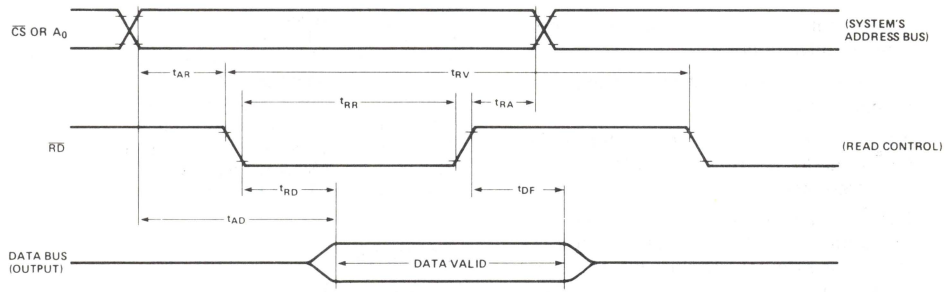
Symbol	Parameter	8741		8041		Units	Test Conditions
		Min.	Max.	Min.	Max.		
t_{AW}	$\overline{CS}$, A_0 Setup to $\overline{WR}$ ↓	60		0		ns	
t_{WA}	CS, A_0 Hold After WR ↑	30		0		ns	
t_{WW}	WR Pulse Width	300	$2 \times t_{CY}$	250		ns	$t_{CY} = 2.5\ \mu s$
t_{DW}	Data Setup to WR ↑	250		150		ns	
t_{WD}	Data Hold After WR ↑	30		0		ns	

A.C. TEST CONDITIONS

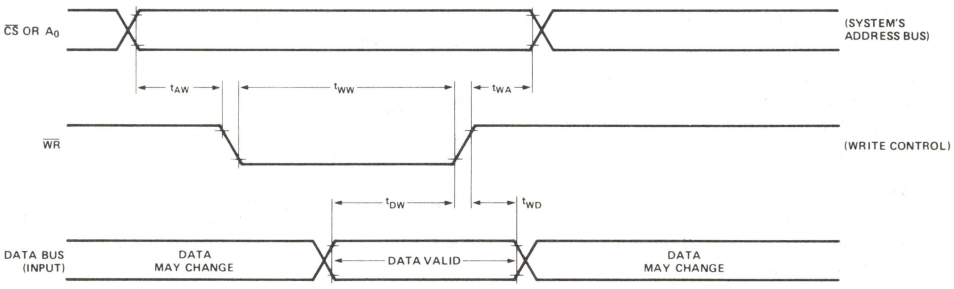
D_7-D_0 Outputs R_L = 2.2k to V_{SS}
4.3k to V_{CC}
C_L = 100 pF

WAVEFORMS

Read Operation — Data Bus Buffer Register



Write Operation — Data Bus Buffer Register



PIN DESCRIPTION

Signal	Description
D_0-D_7	Three-state, bi-directional, DATA BUS BUFFER lines used to interface the UPI-41 to an 8-bit master system data bus.
P_{10}-P_{17}	8-bit, PORT 1, quasi-bi-directional I/O lines.
P_{20}-P_{27}	8-bit, PORT 2, quasi-bi-directional I/O lines The lower 4-bits (P_{20}-P_{23}) interface directly to the 8243 I/O expander device and contain address and data information during PORT 4-7 access.
$\overline{WR}$	I/O write input which enables the master CPU to write data and command words to the UPI-41 DATA BUS BUFFER.
$\overline{RD}$	I/O read input which enables the master CPU to read data and status words from the DATA BUS BUFFER or status register.
$\overline{CS}$	Chip select input used to select one UPI-41 out of several connected to a common data bus.
A_0	Address input used by the master processor to indicate whether byte transfer is data or command.
T_0, T_1	Input pins which can be directly tested using conditional branch instructions. T_1 also functions as the event timer input (under software control). T_0 is used during PROM programming and verification in the 8741.
X_1, X_2	Inputs for a crystal, LC or an external timing signal to determine the internal oscillator frequency.
SYNC	Output signal which occurs once per UPI-41 instruction cycle. SYNC can be used as a strobe for external circuitry; it is also used to synchronize single step operation.
EA	External access input which allows emulation, testing and PROM/ROM verification.
PROG	Multifunction pin used as the program pulse input during PROM programming. During I/O expander access the PROG pin acts as an address/data strobe to the 8243.
$\overline{RESET}$	Input used to reset status flip-flops and to set the program counter to zero. $\overline{RESET}$ is also used during PROM programming and verification.
$\overline{SS}$	Single step input used in the 8741 in conjunction with the SYNC output to step the program through each instruction.
V_{CC}	+5V power supply pin.
V_{DD}	+5V during normal operation.Programming supply pin during PROM programming. Low power standby pin in ROM version.
V_{SS}	Circuit ground potential.

UPI INSTRUCTION SET

Mnemonic	Description	Bytes	Cycles
ACCUMULATOR			
ADD A,Rr	Add register to A	1	1
ADD A,@Rr	Add data memory to A	1	1
ADD A,#data	Add immediate to A	2	2
ADDC A,Rr	Add immed. to A with carry	1	1
ADDC A,@Rr	Add immed. to A with carry	1	1
ADDC A,#data	Add immed. to A with carry	2	2
ANL A,Rr	AND register to A	1	1
ANL A,@Rr	AND data memory to A	1	1
ANL A,#data	AND immediate to A	2	2
ORL A,Rr	OR register to A	1	1
ORL A,@Rr	OR data memory to A	1	1
ORL A,#data	OR immediate to A	2	2
XRL A,Rr	Exclusive OR register to A	1	1
XRL A,@Rr	Exclusive OR data memory to A	1	1
XRL A,#data	Exclusive OR immediate to A	2	2
INC A	Increment A	1	1
DEC A	Decrement A	1	1
CLR A	Clear A	1	1
CPL A	Complement A	1	1
DA A	Decimal Adjust A	1	1
SWAP A	Swap digits of A	1	1
RL A	Rotate A left	1	1
RLC A	Rotate A left through carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through carry	1	1
INPUT/OUTPUT			
IN A,Pp	Input port to A	1	2
OUTL Pp,A	Output A to port	1	2
ANL Pp,#data	AND immediate to port	2	2
ORL Pp,#data	OR immediate to port	2	2
IN A,DBB	Input DBB to A, clear IBF	1	1
OUT DBB,A	Output A to DBB, set OBF	1	1
MOVD A,Pp	Input Expander port to A	1	2
MOVD Pp,A	Output A to Expander port	1	2
ANLD Pp,A	AND A to Expander port	1	2
ORLD Pp,A	OR A to Expander port	1	2
DATA MOVES			
MOV A,Rr	Move register to A	1	1
MOV A,@Rr	Move data memory to A	1	1
MOV A,#data	Move immediate to A	2	2
MOV Rr,A	Move A to register	1	1
MOV @Rr,A	Move A to data memory	1	1
MOV Rr,#data	Move immediate to register	2	2
MOV @Rr,#data	Move immediate to data memory	2	2
MOV A,PSW	Move PSW to A	1	1
MOV PSW,A	Move A to PSW	1	1
XCH A,Rr	Exchange A and register	1	1
XCH A,@Rr	Exchange A and data memory	1	1
XCHD A,@Rr	Exchange digit of A and register	1	1
MOVP A,@A	Move to A from current page	1	2
MOVP3, A,@A	Move to A from page 3	1	2
TIMER/COUNTER			
MOV A,T	Read Timer/Counter	1	1
MOV T,A	Load Timer/Counter	1	1
STRT T	Start Timer	1	1
STRT CNT	Start Counter	1	1
STOP TCNT	Stop Timer/Counter	1	1
EN TCNTI	Enable Timer/Counter Interrupt	1	1
DIS TCNTI	Disable Timer/Counter Interrupt	1	1

Mnemonic	Description	Bytes	Cycles
CONTROL			
EN I	Enable IBF Interrupt	1	1
DIS I	Disable IBF Interrupt	1	1
SEL RB0	Select register bank 0	1	1
SEL RB1	Select register bank 1	1	1
NOP	No Operation	1	1
REGISTERS			
INC Rr	Increment register	1	1
INC @Rr	Increment data memory	1	1
DEC Rr	Decrement register	1	1
SUBROUTINE			
CALL addr	Jump to subroutine	2	2
RET	Return	1	2
RETR	Return and restore status	1	2
FLAGS			
CLR C	Clear Carry	1	1
CPL C	Complement Carry	1	1
CLR F0	Clear Flag 0	1	1
CPL F0	Complement Flag 0	1	1
CLR F1	Clear F1 Flag	1	1
CPL F1	Complement F1 Flag	1	1
BRANCH			
JMP addr	Jump unconditional	2	2
JMPP @A	Jump indirect	1	2
DJNZ R,addr	Decrement register and skip	2	2
JC addr	Jump on Carry = 1	2	2
JNC addr	Jump on Carry = 0	2	2
JZ addr	Jump on A Zero	2	2
JNZ addr	Jump on A not Zero	2	2
JT0 addr	Jump on T0 = 1	2	2
JNT0 addr	Jump on T0 = 0	2	2
JT1 addr	Jump on T1 = 1	2	2
JNT1 addr	Jump on T1 = 0	2	2
JF0 addr	Jump on F0 Flag = 1	2	2
JF1 addr	Jump on F1 Flag = 1	2	2
JTF addr	Jump on Timer Flag = 1, Clear Flag	2	2
JNIBF addr	Jump on IBF Flag = 0	2	2
JOBF addr	Jump on OBF Flag = 1	2	2
JBb addr	Jump on Accumulator Bit	2	2

APPLICATIONS

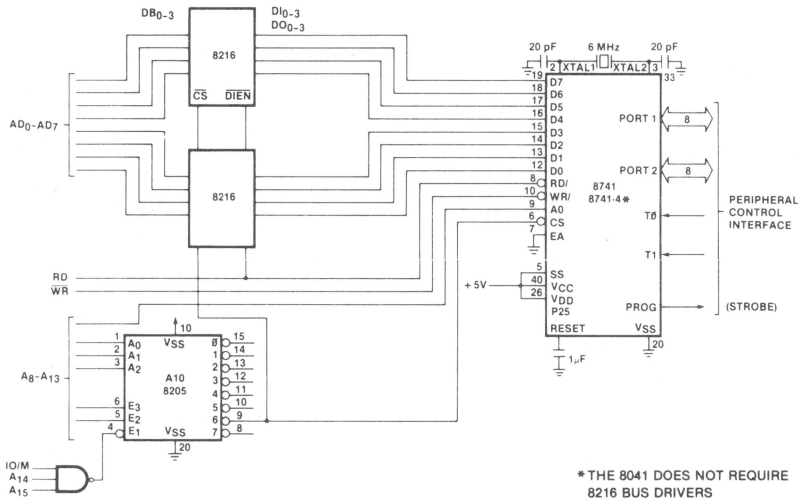


Figure 1. Recommended 8741 Interface to an 8085 System

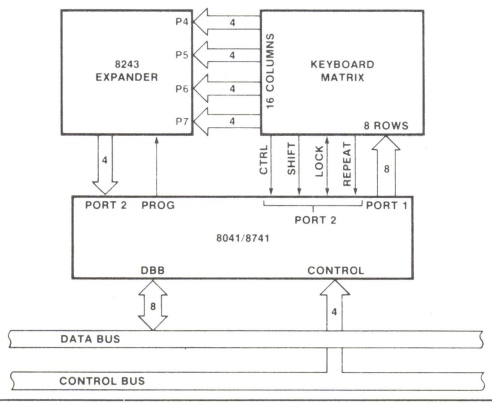


Figure 2. 8041-8243 Keyboard Scanner

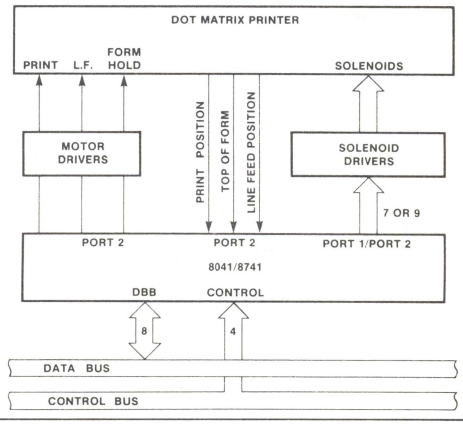


Figure 3. 8041 Matrix Printer Interface

PROGRAMMING, VERIFYING, AND ERASING THE 8748 EPROM

Programming/Verification

In brief, the programming process consists of: activating the program mode, applying an address, latching the address, applying data, and applying a programming pulse. Each word is programmed completely before moving on to the next and is followed by a verification step. The following is a list of the pins used for programming and a description of their functions:

Pin	Function
XTAL 1	Clock input (1 to 6 MHz)
RESET	Initialization and address latching
TEST 0	Selection of program or verify mode
EA	Activation of program/verify modes
BUS	Address and data input data output during verify
P20-1	Address input
V_{DD}	Programming power supply
PROG	Program pulse input

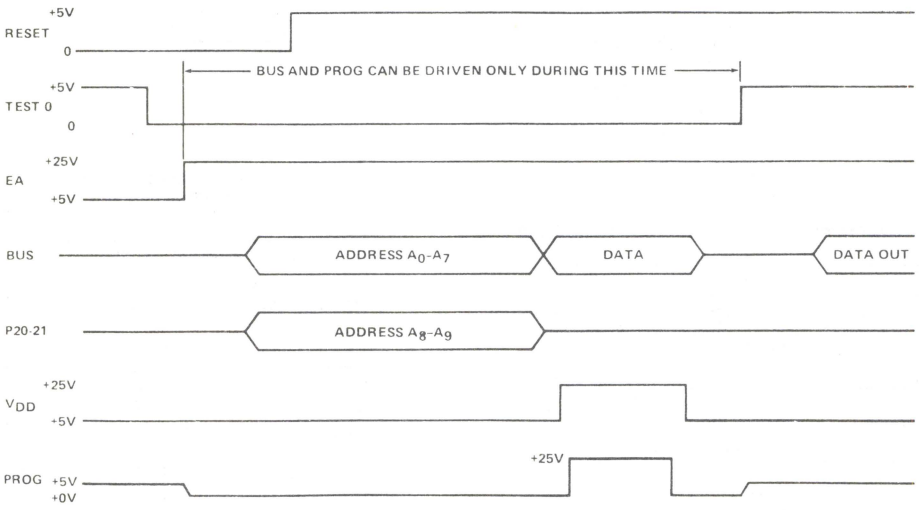
The program/verify sequence is:

1. V_{DD} = 5V, clock applied or internal oscillator operating, RESET = 0V, TEST 0 = 5V, EA = 5V, BUS and PROG floating.
2. Insert 8748 in programming socket.
3. TEST 0 = 0V (select program mode).
4. EA = 25V (activate program mode).
5. Address applied to BUS and P20-1.
6. RESET = 5V (latch address).
7. Data applied to BUS.
8. V_D = 25V (programming power).
9. PROG = 0V followed by one 50 ms pulse to 25V.
10. V_{DD} = 5V.
11. TEST 0 = 5V (verify mode).
12. Read and verify data on BUS.
13. TEST 0 = 0V.
14. RESET = 0V and repeat from step 5.
15. Programmer should be at conditions of step 1 when 8748 is removed from socket.

Programming Options

The 8748 EPROM can be programmed by either of two Intel products:

1. PROMPT-48 Microcomputer Design Aid.
2. Universal PROM Programmer (UPP-101 or UPP-102) Peripheral of the Intellec® Development System with a UPP-848 Personality Card.



WARNING: An attempt to program a missocketed 8748 will result in severe damage to the part. An indication of a properly socketed part is the appearance of the ALE clock output. The lack of this clock may be used to disable the programmer.

Figure 5. Programming/Verification Sequence

8748 Erasure Characteristics

The erasure characteristics of the 8748 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (A). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical 8748 in approximately 3 years while it would take approximately one week to cause erasure when exposed to direct sunlight. If the 8748 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 8748 window to prevent unintentional erasure.

The recommended erasure procedure for the 8748 is exposure to shortwave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000 μW/cm^2 power rating. The 8748 should be placed within one inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

A.C. TIMING SPECIFICATION FOR PROGRAMMING

T_A = 25°C ±5°C, V_{CC} = 5V ±5%, V_{DD} = 25V ±1V

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{AW}	Address Setup Time to $\overline{\text{RESET}}$ ↑	4tcy			
t_{WA}	Address Hold Time After $\overline{\text{RESET}}$ ↑	4tcy			
t_{DW}	Data in Setup Time to PROG ↑	4tcy			
t_{WD}	Data in Hold Time After PROG ↓	4tcy			
t_{PH}	$\overline{\text{RESET}}$ Hold Time to Verify	4tcy			
t_{VDDW}	V_{DD}	4tcy			
t_{VDDH}	V_{DD} Hold Time After PROG ↓	0			
t_{PW}	Program Pulse Width	50	60	MS	
t_{TW}	Test 0 Setup Time for Program Mode	4tcy			
t_{WT}	Test 0 Hold Time After Program Mode	4tcy			
t_{DO}	Test 0 to Data Out Delay		4tcy		
t_{WW}	$\overline{\text{RESET}}$ Pulse Width to Latch Address	4tcy			
t_r, t_f	V_{DD} and PROG Rise and Fall Times	0.5	2.0	μs	
t_{CY}	CPU Operation Cycle Time	5.0		μs	
t_{RE}	$\overline{\text{RESET}}$ Setup Time Before EA ↑	4tcy			

Note: If TEST 0 is high, t_{DO} can be triggered by $\overline{\text{RESET}}$ 1.

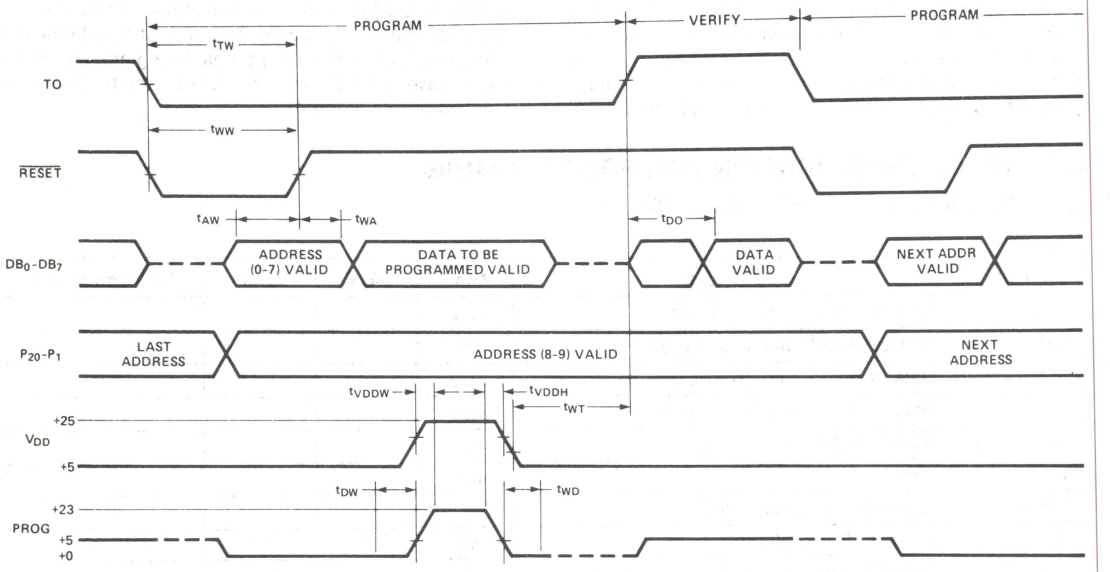
D.C. SPECIFICATION FOR PROGRAMMING

T_A = 25°C ±5°C, V_{CC} = 5V ±5%, V_{DD} = 25V ±1V

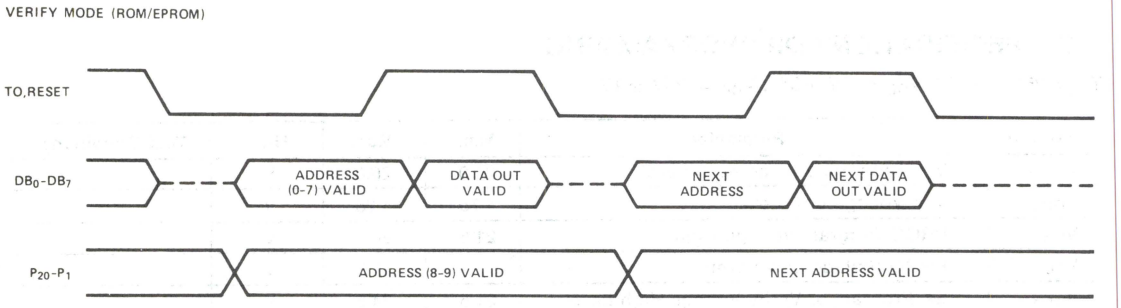
Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{DOH}	V_{DD} Program Voltage High Level	24.0	26.0	V	
V_{DDL}	V_{DD} Voltage Low Level	4.75	5.25	V	
V_{PH}	PROG Program Voltage High Level	21.5	24.5	V	
V_{PL}	PROG Voltage Low Level		0.2	V	
V_{EAH}	EA Program or Verify Voltage High Level	21.5	24.5	V	
V_{EAL}	EA Voltage Low Level		5.25	V	
I_{DD}	V_{DD} High Voltage Supply Current		30.0	mA	
I_{PROG}	PROG High Voltage Supply Current		16.0	mA	
I_{EA}	EA High Voltage Supply Current		1.0	mA	

WAVEFORMS

Combination Program/Verify Mode (EPROMs Only)



Verify Mode (ROM/EPROM)



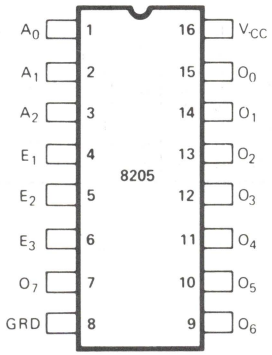
8205
HIGH SPEED 1 OUT OF 8 BINARY DECODER

- **I/O Port or Memory Selector**
- **Simple Expansion — Enable Inputs**
- **High Speed Schottky Bipolar Technology — 18 ns Max Delay**
- **Directly Compatible with TTL Logic Circuits**
- **Low Input Load Current — 0.25 mA Max, 1/6 Standard TTL Input Load**
- **Minimum Line Reflection — Low Voltage Diode Input Clamp**
- **Outputs Sink 10 mA Min**
- **16-Pin Dual In-Line Ceramic or Plastic Package**

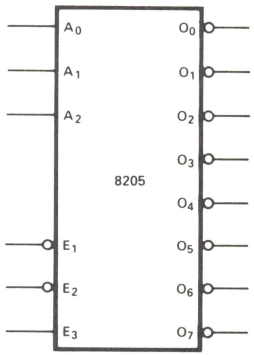
The Intel® 8205 decoder can be used for expansion of systems which utilize input ports, output ports, and memory components with active low chip select input. When the 8205 is enabled, one of its 8 outputs goes "low", thus a single row of a memory system is selected. The 3-chip enable inputs on the 8205 allow easy system expansion. For very large systems, 8205 decoders can be cascaded such that each decoder can drive 8 other decoders for arbitrary memory expansions.

The 8205 is packaged in a standard 16-pin dual in-line package, and its performance is specified over the temperature range of 0°C to +75°C, ambient. The use of Schottky barrier diode clamped transistors to obtain fast switching speeds results in higher performance than equivalent devices made with a gold diffussion process.

PIN CONFIGURATION



LOGIC SYMBOL



PIN NAMES

A_0- A_2	ADDRESS INPUTS
$\overline{E_1}$- $\overline{E_3}$	ENABLE INPUTS
$\overline{O_0}$- $\overline{O_7}$	DECODED OUTPUTS

ADDRESS			ENABLE			OUTPUTS							
A_0	A_1	A_2	E_1	E_2	E_3	0	1	2	3	4	5	6	7
L	L	L	L	L	H	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	H	L	H	H	H	H	H
H	H	L	L	L	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	H	H	H	L	H	H
L	H	H	L	L	H	H	H	H	H	H	H	L	H
H	H	H	L	L	H	H	H	H	H	H	H	H	L
X	X	X	L	L	L	H	H	H	H	H	H	H	H
X	X	X	H	L	L	H	H	H	H	H	H	H	H
X	X	X	L	H	L	H	H	H	H	H	H	H	H
X	X	X	H	H	L	H	H	H	H	H	H	H	H
X	X	X	H	L	H	H	H	H	H	H	H	H	H
X	X	X	L	H	H	H	H	H	H	H	H	H	H
X	X	X	H	H	H	H	H	H	H	H	H	H	H

MPU PERIPHERALS

FUNCTIONAL DESCRIPTION

Decoder

The 8205 contains a one out of eight binary decoder. It accepts a three bit binary code and by gating this input, creates an exclusive output that represents the value of the input code.

For example, if a binary code of 101 was present on the A0, A1 and A2 address input lines, and the device was enabled, an active low signal would appear on the $\overline{05}$ output line. Note that all of the other output pins are sitting at a logic high, thus the decoded output is said to be exclusive. The decoders outputs will follow the truth table shown below in the same manner for all other input variations.

Enable Gate

When using a decoder it is often necessary to gate the outputs with timing or enabling signals so that the exclusive output of the decoded value is synchronous with the overall system.

The 8205 has a built-in function for such gating. The three enable inputs ($\overline{E1}$, $\overline{E2}$, E3) are ANDed together and create a single enable signal for the decoder. The combination of both active "high" and active "low" device enable inputs provides the designer with a powerfully flexible gating function to help reduce package count in his system.

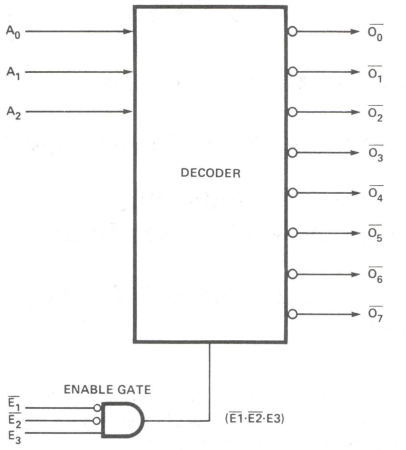


Figure 1. Enable Gate

ADDRESS			ENABLE			OUTPUTS							
A_0	A_1	A_2	E_1	E_2	E_3	0	1	2	3	4	5	6	7
L	L	L	L	L	H	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	H	L	H	H	H	H	H
H	H	L	L	L	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	H	H	H	L	H	H
L	H	H	L	L	H	H	H	H	H	H	H	L	H
H	H	H	L	L	H	H	H	H	H	H	H	H	L
X	X	X	L	L	L	H	H	H	H	H	H	H	H
X	X	X	H	L	L	H	H	H	H	H	H	H	H
X	X	X	L	H	L	H	H	H	H	H	H	H	H
X	X	X	H	H	L	H	H	H	H	H	H	H	H
X	X	X	H	L	H	H	H	H	H	H	H	H	H
X	X	X	L	H	H	H	H	H	H	H	H	H	H
X	X	X	H	H	H	H	H	H	H	H	H	H	H

APPLICATIONS OF THE 8205

The 8205 can be used in a wide variety of applications in microcomputer systems. I/O ports can be decoded from the address bus, chip select signals can be generated to select memory devices and the type of machine state such as in 8008 systems can be derived from a simple decoding of the state lines (S0, S1, S2) of the 8008 CPU.

I/O Port Decoder

Shown in the figure below is a typical application of the 8205. Address input lines are decoded by a group of 8205s (3). Each input has a binary weight. For example, A0 is assigned a value of 1 and is the LSB; A4 is assigned a value of 16 and is the MSB. By connecting them to the decoders as shown, an active low signal that is exclusive in nature and represents the value of the input address lines, is available at the outputs of the 8205s.

This circuit can be used to generate enable signals for I/O ports or any other decoder related application.

Note that no external gating is required to decode up to 24 exclusive devices and that a simple addition of an inverter or two will allow expansion to even larger decoder networks.

Chip Select Decoder

Using a very similar circuit to the I/O port decoder, an array of 8205s can be used to create a simple interface to a 24K memory system.

The memory devices used can be either ROM or RAM and are 1K in storage capacity. 8308s and 8102s are the devices typically used for this application. This type of memory device has ten (10) address inputs and an active "low" chip select ($\overline{CS}$). The lower order address bits A0-A9 which come from the microprocessor are "bussed" to all memory elements and the chip select to enable a specific device or group of devices comes from the array of 8205s. The output of the 8205 is active low so it is directly compatible with the memory components.

Basic operation is that the CPU issues an address to identify a specific memory location in which it wishes to "write" or "read" data. The most significant address bits A10-A14 are decoded by the array of 8205s and an exclusive, active low, chip select is generated that enables a specific memory device. The least significant address bits A0-A9 identify a specific location within the selected device. Thus, all addresses throughout the entire memory array are exclusive in nature and are non-redundant.

This technique can be expanded almost indefinitely to support even larger systems with the addition of a few inverters and an extra decoder (8205).

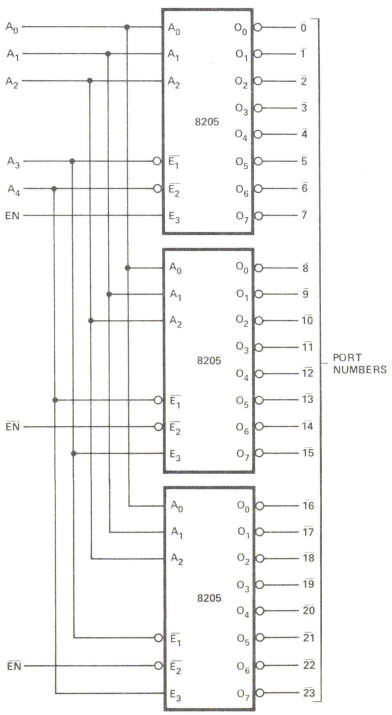


Figure 2. I/O Port Decoder

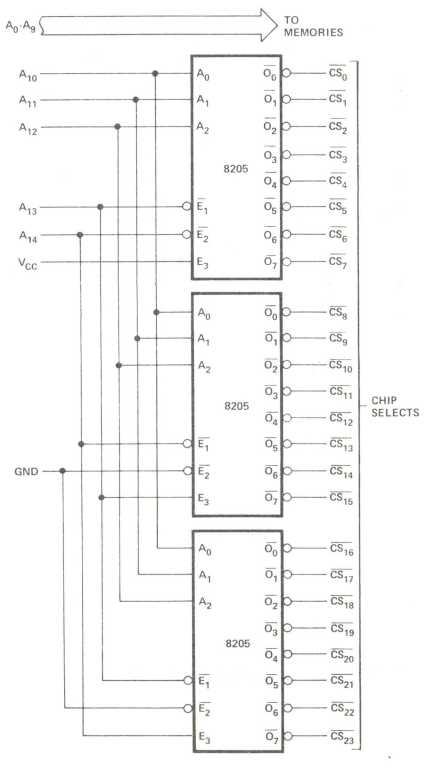


Figure 3. 32K Memory Interface

Logic Element Example

Probably the most overlooked application of the 8205 is that of a general purpose logic element. Using the "on-chip" enabling gate, the 8205 can be configured to gate its decoded outputs with system timing signals and generate strobes that can be directly connected to latches, flip-flops and one-shots that are used throughout the system.

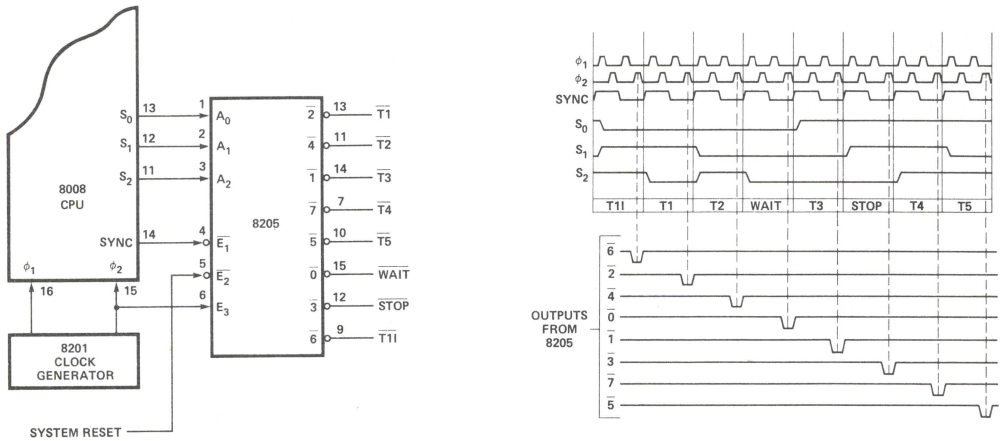
An excellent example of such an application is the "state decoder" in an 8008 CPU based system. The 8008 CPU issues three bits of information (S0, S1, S2) that indicate the nature of the data on the Data Bus during each machine state. Decoding of these signals is vital to generate strobes that can load the address latches, control bus discipline and general machine functions.

In the figure below a circuit is shown using the 8205 as the "state decoder" for an 8008 CPU that not only decodes the S0, S1, S2 outputs but gates these signals with the clock (phase 2) and the SYNC output of the 8008 CPU. The $\overline{T1}$ and $\overline{T2}$ decoded strobes can connect directly to devices like 8212s for latching the address information. The other decoded strobes can be used to generate signals to control the system data bus, memory timing functions and interrupt structure. RESET is connected to the enable gate so that strobes are not generated during system reset, eliminating accidental loading.

The power of such a circuit becomes evident when a single decoded strobe is logically broken down. Consider $\overline{T1}$ output, the boolean equation for it would be:

$$\overline{T1} = (\overline{S0} \cdot S1 \cdot \overline{S2}) \cdot (\overline{SYNC} \cdot \text{Phase } 2 \cdot \overline{\text{Reset}})$$

A six input NAND gate plus a few inverters would be needed to implement this function. The seven remaining outputs would need a similar circuit to duplicate their function, obviously a substantial savings in components can be achieved when using such a technique.



State Control Coding

S_0	S_1	S_2	STATE
0	1	0	T1
0	1	1	T1I
0	0	1	T2
0	0	0	WAIT
1	0	0	T3
1	1	0	STOP
1	1	1	T4
1	0	1	T5

Figure 4. 8205 State Decoder Circuit

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias:	Ceramic	−65°C to +125°C
	Plastic	−65°C to +75°C
Storage Temperature		−65°C to +160°C
All Output or Supply Voltages		−0.5 to +7 Volts
All Input Voltages		−1.0 to +5.5 Volts
Output Currents		125 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

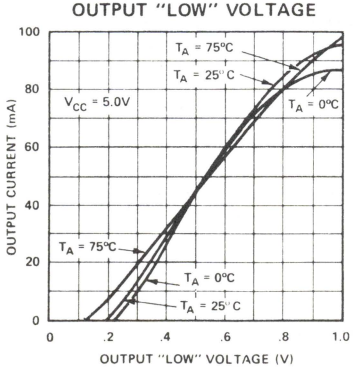
T_A = 0°C to +75°C, V_{CC} = 5V ±5%

8205

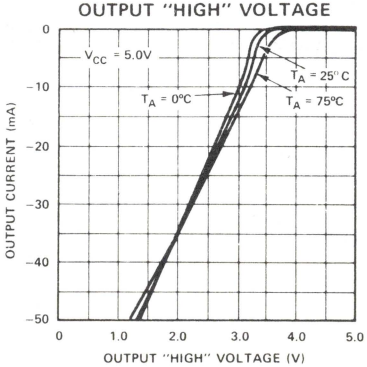
SYMBOL	PARAMETER	LIMIT MIN.	LIMIT MAX.	UNIT	TEST CONDITIONS
I_F	INPUT LOAD CURRENT		−0.25	mA	V_{CC} = 5.25V, V_F = 0.45V
I_R	INPUT LEAKAGE CURRENT		10	μA	V_{CC} = 5.25V, V_R = 5.25V
V_C	INPUT FORWARD CLAMP VOLTAGE		−1.0	V	V_{CC} = 4.75V, I_C = −5.0 mA
V_{OL}	OUTPUT "LOW" VOLTAGE		0.45	V	V_{CC} = 4.75V, I_{OL} = 10.0 mA
V_{OH}	OUTPUT HIGH VOLTAGE	2.4		V	V_{CC} = 4.75V, I_{OH} = −1.5 mA
V_{IL}	INPUT "LOW" VOLTAGE		0.85	V	V_{CC} = 5.0V
V_{IH}	INPUT "HIGH" VOLTAGE	2.0		V	V_{CC} = 5.0V
I_{SC}	OUTPUT HIGH SHORT CIRCUIT CURRENT	−40	−120	mA	V_{CC} = 5.0V, V_{OUT} = 0V
V_{OX}	OUTPUT "LOW" VOLTAGE @ HIGH CURRENT		0.8	V	V_{CC} = 5.0V, I_{OX} = 40 mA
I_{CC}	POWER SUPPLY CURRENT		70	mA	V_{CC} = 5.25V

TYPICAL CHARACTERISTICS

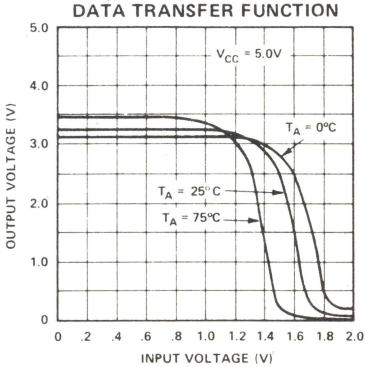
OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE



OUTPUT CURRENT VS. OUTPUT "HIGH" VOLTAGE



DATA TRANSFER FUNCTION



SWITCHING CHARACTERISTICS

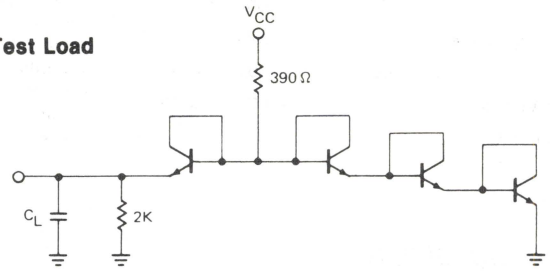
Conditions of Test:

Input pulse amplitudes: 2.5V

Input rise and fall times: 5 nsec between 1V and 2V

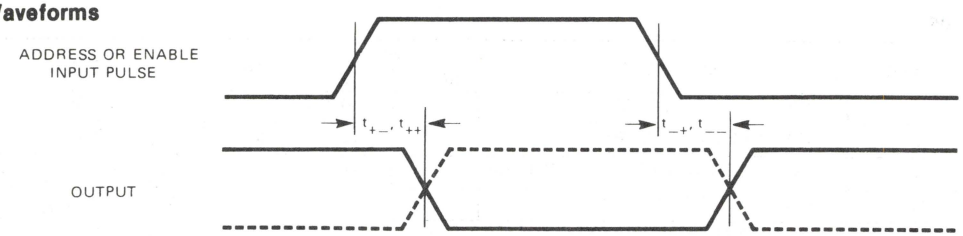
Measurements are made at 1.5V

Test Load



All Transistors 2N2369 or Equivalent. C_L = 30 pF

Test Waveforms



A.C. CHARACTRISTICS

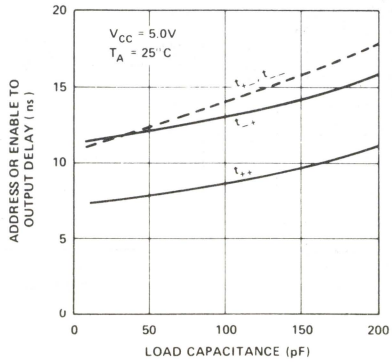
T_A = 0°C to +75°C, V_{CC} = 5V ±5% unless otherwise specified.

SYMBOL	PARAMETER		MAX. LIMIT	UNIT	TEST CONDITIONS
t_{++}	ADDRESS OR ENABLE TO OUTPUT DELAY		18	ns	
t_{-+}			18	ns	
t_{+-}			18	ns	
t_{--}			18	ns	
C_{IN} [1]	INPUT CAPACITANCE	P8205	4(typ.)	pF	f = 1 MHz, V_{CC} = 0V
		C8205	5(typ.)	pF	V_{BIAS} = 2.0V, T_A = 25°C

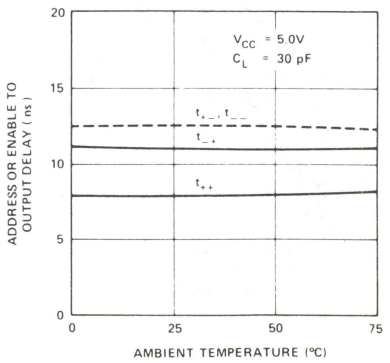
1. This parameter is periodically sampled and is not 100% tested.

TYPICAL CHARACTERISTICS

ADDRESS OR ENABLE TO OUTPUT DELAY VS. LOAD CAPACITANCE



ADDRESS OR ENABLE TO OUTPUT DELAY VS. AMBIENT TEMPERATURE



MPU PERIPHERALS

8212/3212*
8-BIT INPUT/OUTPUT PORT

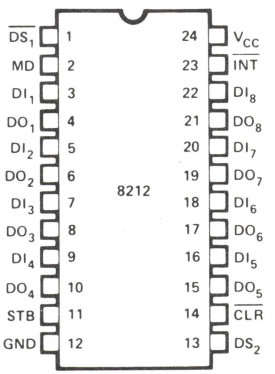
- **Fully Parallel 8-Bit Data Register and Buffer**
- **Service Request Flip-Flop for Interrupt Generation**
- **Low Input Load Current — 0.25 mA Max**
- **3-State Outputs**
- **Outputs Sink 15 mA**
- **3.65V Output High Voltage for Direct Interface to 8080 CPU or 8008 CPU**
- **Asynchronous Register Clear**
- **Replaces Buffers, Latches, and Multiplexers in Microcomputer Systems**
- **Reduces System Package Count**

The Intel® 8212 input/output port consists of an 8-bit latch with 3-state output buffers along with control and device selection logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

The device is multimode in nature. It can be used to implement latches, gated buffers or multiplexers. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with this device.

*Note: The specifications for the 3212 are identical with those for the 8212.

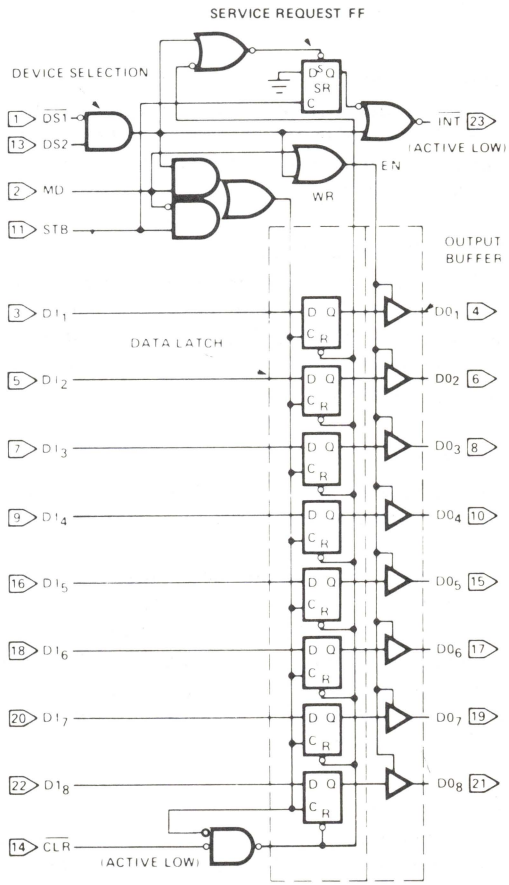
PIN CONFIGURATION



PIN NAMES

DI_1-DI_8	DATA IN
DO_1-DO_8	DATA OUT
$\overline{DS_1}$-DS_2	DEVICE SELECT
MD	MODE
STB	STROBE
$\overline{INT}$	INTERRUPT (ACTIVE LOW)
$\overline{CLR}$	CLEAR (ACTIVE LOW)

LOGIC DIAGRAM



MPU PERIPHERALS

FUNCTIONAL DESCRIPTION

Data Latch

The 8 flip-flops that make up the data latch are of a "D" type design. The output (Q) of the flip-flop will follow the data input (D) while the clock input (C) is high. Latching will occur when the clock (C) returns low.

The data latch is cleared by an asynchronous reset input ($\overline{CLR}$). (Note: Clock (C) Overides Reset ($\overline{CLR}$).)

Output Buffer

The outputs of the data latch (Q) are connected to 3-state, non-inverting output buffers. These buffers have a common control line (EN); this control line either enables the buffer to transmit the data from the outputs of the data latch (Q) or disables the buffer, forcing the output into a high impedance state. (3-state)

This high-impedance state allows the designer to connect the 8212 directly onto the microprocessor bi-directional data bus.

Control Logic

The 8212 has control inputs $\overline{DS1}$, DS2, MD and STB. These inputs are used to control device selection, data latching, output buffer state and service request flip-flop.

DS1, DS2 (Device Select)

These 2 inputs are used for device selection. When $\overline{DS1}$ is low and DS2 is high ($\overline{DS1} \cdot DS2$) the device is selected. In the selected state the output buffer is enabled and the service request flip-flop (SR) is asynchronously set.

MD (Mode)

This input is used to control the state of the output buffer and to determine the source of the clock input (C) to the data latch.

When MD is high (output mode) the output buffers are enabled and the source of clock (C) to the data latch is from the device selection logic ($\overline{DS1} \cdot DS2$).

When MD is low (input mode) the output buffer state is determined by the device selection logic ($\overline{DS1} \cdot DS2$) and the source of clock (C) to the data latch is the STB (Strobe) input.

STB (Strobe)

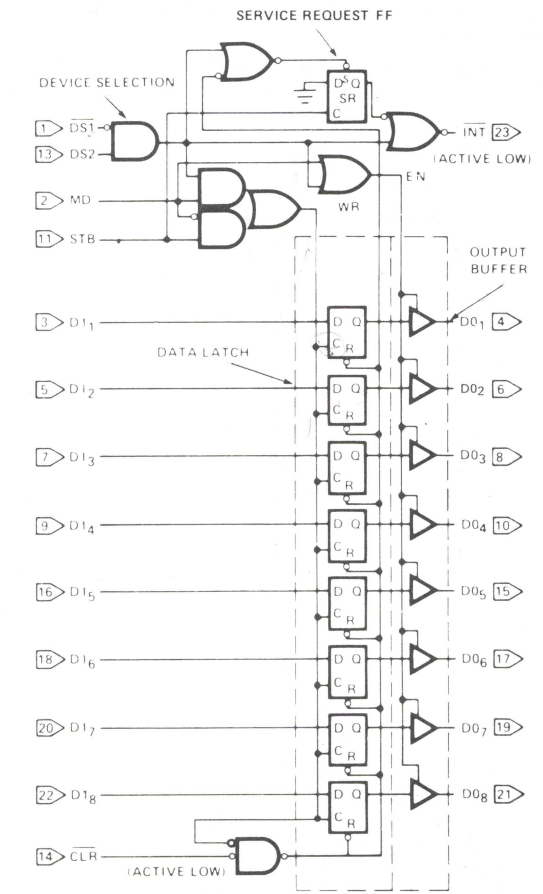
This input is used as the clock (C) to the data latch for the input mode MD = 0) and to synchronously reset the service request flip-flop (SR).

Note that the SR flip-flop is negative edge triggered.

Service Reqeust Flip-Flop

The (SR) flip-flop is used to generate and control interrupts in microcomputer systems. It is asynchronously set by the $\overline{CLR}$ input (active low). When the (SR) flip-flop is set it is in the non-interrupting state.

The output of the (SR) flip-flop (Q) is connected to an inverting input of a "NOR" gate. The other input to the "NOR" gate is non-inverting and is connected to the device selection logic ($\overline{DS1} \cdot DS2$). The output of the "NOR" gate ($\overline{INT}$) is active low (interrupting state) for connection to active low input priority generating circuits.



STB	MD	($DS_1 \cdot DS_2$)	DATA OUT EQUALS
0	0	0	3-STATE
1	0	0	3-STATE
0	1	0	DATA LATCH
1	1	0	DATA LATCH
0	0	1	DATA LATCH
1	0	1	DATA IN
0	1	1	DATA IN
1	1	1	DATA IN

CLR	($\overline{DS_1} \cdot DS_2$)	STB	*SR	INT
0	0	0	1	1
0	1	0	1	0
1	1	↓	0	0
1	1	0	1	0
1	0	0	1	1
1	1	↓	1	0

*INTERNAL SR FLIP-FLOP

$\overline{CLR}$ – RESETS DATA LATCH
SETS SR FLIP-FLOP
(NO EFFECT ON OUTPUT BUFFER)

Figure 1. Service Flip-Flop Function

APPLICATIONS OF THE 8212 — FOR MICROCOMPUTER SYSTEMS

- Basic schematic symbols
- Gated buffer
- Bidirectional bus driver
- Interrupting input port
- Interrupt instruction port
- Output port
- 8080A status latch
- 8085A address latch

Basic Schematic Symbols

Two examples of ways to draw the 8212 on system schematics—(1) the top being the detailed view showing pin numbers, and (2) the bottom being the symbolic view showing the system input or output as a system bus (bus containing 8 parallel lines). The output to the data bus is symbolic in referencing 8 parallel lines.

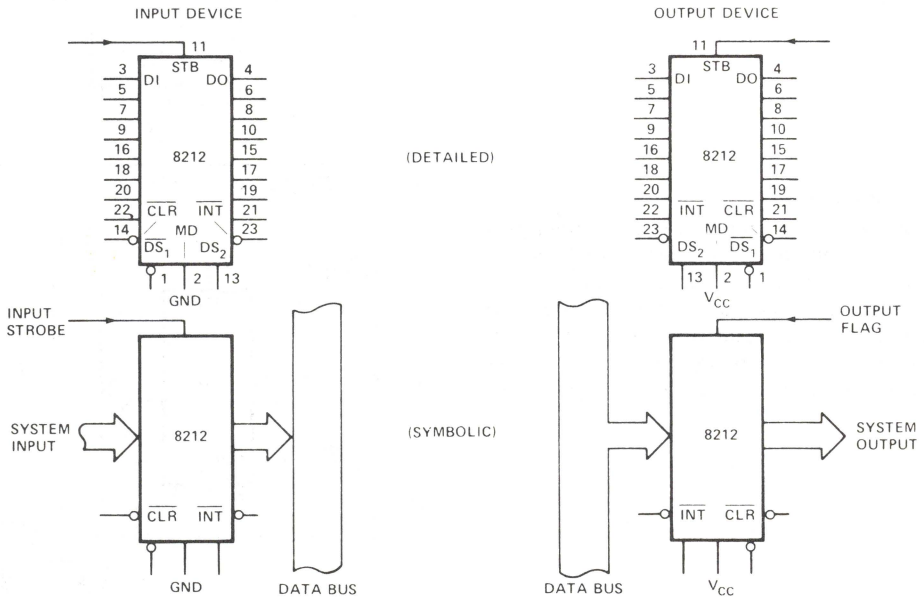


Figure 2. Basic Schematic Symbols

Gated Buffer (3-State)

The simplest use of the 8212 is that of a gated buffer. By tying the mode signal low and the strobe input high, the data latch is acting as a straight through gate. The output buffers are then enabled from the device selection logic $\overline{DS1}$ and DS2.

When the device selection logic is false, the outputs are 3-state.

When the device selection logic is true, the input data from the system is directly transferred to the output. The input data load is 250 micro amps. The output data can sink 15 milli amps. The minimum high output is 3.65 volts.

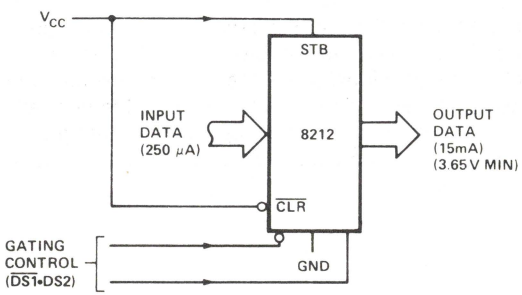


Figure 3. Gated Buffer (3-State)

Bidirectional Bus Driver

A pair of 8212's wired (back-to-back) can be used as a symmetrical drive, bi-directional bus driver. The devices are controlled by the data bus input control which is connected to $\overline{DS1}$ on the first 8212 and to DS2 on the second. One device is active, and acting as a straight through buffer the other is in 3-state mode. This is a very useful circuit in small system design.

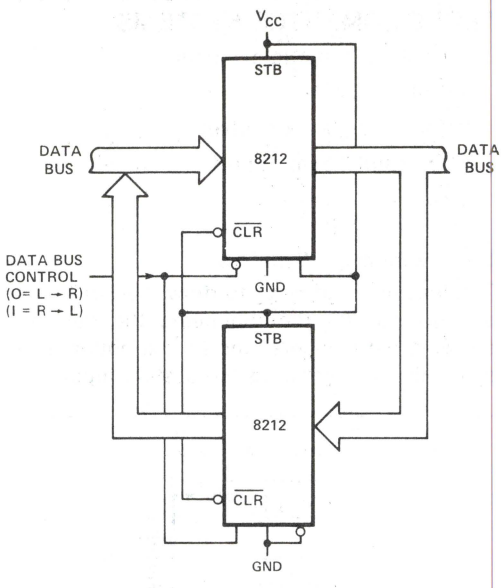


Figure 4. Bidirectional Bus Driver

Interrupting Input Port

This use of an 8212 is that of a system input port that accepts a strobe from the system input source, which in turn clears the service request flip-flop and interrupts the processor. The processor then goes through a service routine, identifies the port, and causes the device selection logic to go true — enabling the system input data onto the data bus.

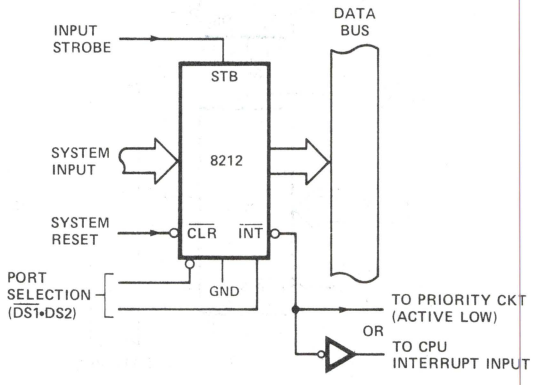


Figure 5. Interrupting Input Port

Interrupt Instruction Port

The 8212 can be used to gate the interrupt instruction, normally RESTART instructions, onto the data bus. The device is enabled from the interrupt acknowledge signal from the microprocessor and from a port selection signal. This signal is normally tied to ground. ($\overline{DS1}$ could be used to multiplex a variety of interrupt instruction ports onto a common bus).

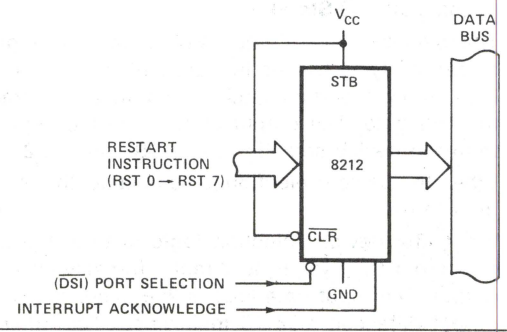


Figure 6. Interrupt Instruction Port

Output Port (With Handshaking)

The 8212 can be used to transmit data from the data bus to a system output. The output strobe could be a hand-shaking signal such as "reception of data" from the device that the system is outputting to. It in turn, can interrupt the system signifying the reception of data. The selection of the port comes from the device selection logic. ($\overline{DS1} \cdot DS2$)

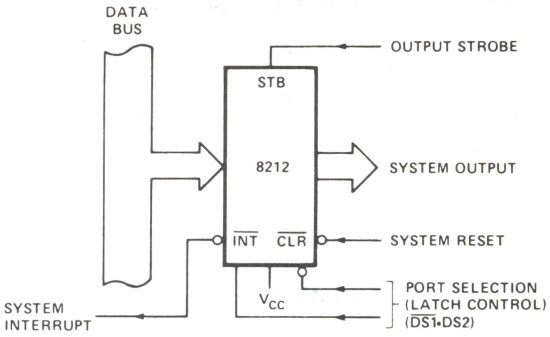


Figure 8. 8080 Status Latch

8080 Status Latch

Here the 8212 is used as the status latch for an 8080 microcomputer system. The input to the 8212 latch is directly from the 8080 data bus. Timing shows that when the SYNC signal is true, which is connected to the DS2 input and the phase 1 signal is true, which is a TTL level coming from the clock generator; then, the status data will be latched into the 8212.

Note: The mode signal is tied high so that the output on the latch is active and enabled all the time.

It is shown that the two areas of concern are the bidirectional data bus of the microprocessor and the control bus.

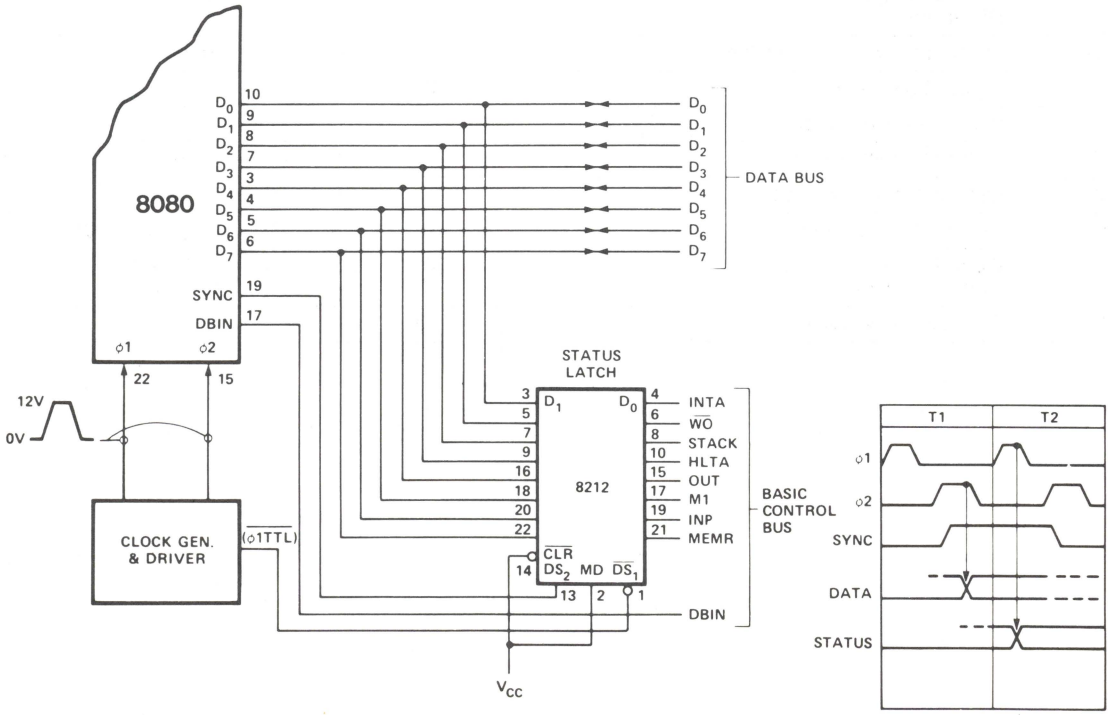


Figure 7. Output Port (With Handshaking)

ABSOLUTE MAXIMUM RATINGS*

Temperature under bias plastic . . . . . 0°C to 75°C
Storage temperature . . . . . 0°C to 75°C
All output or supply voltages . . . . . – 0.5V to + 7V
All input voltages . . . . . – 1.0V to + 5.5V
Output currents . . . . . 100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

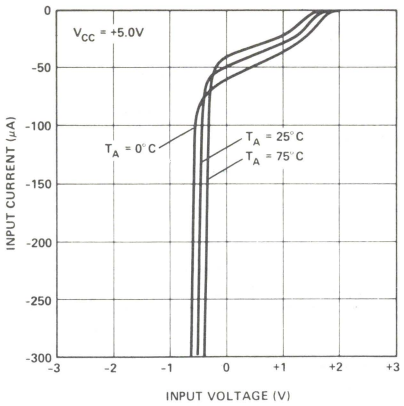
D.C. CHARACTERISTICS

T_A = 0°C to +75°C V_{CC} = +5V ±5%

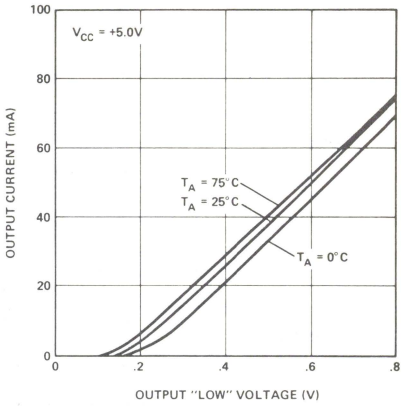
Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
I_F	Input Load Current ACK, DS_2, CR, DI_1-DI_8 Inputs			–.25	mA	V_F = .45V
I_F	Input Load Current MD Input			–.75	mA	V_F = .45V
I_F	Input Load Current DS_1 Input			–1.0	mA	V_F = .45V
I_R	Input Leakage Current ACK, DS, CR, DI_1-DI_8 Inputs			10	μA	$V_R \leq V_{CC}$
I_R	Input Leakage Current MO Input			30	μA	$V_R \leq V_{CC}$
I_R	Input Leakage Current DS_1 Input			40	μA	$V_R \leq V_{CC}$
V_C	Input Forward Voltage Clamp			–1	V	I_C = –5 mA
V_{IL}	Input "Low" Voltage			.85	V	
V_{IH}	Input "High" Voltage	2.0			V	
V_{OL}	Output "Low" Voltage			.45	V	I_{OL} = 15 mA
V_{OH}	Output "High" Voltage	3.65	4.0		V	I_{OH} = –1 mA
I_{SC}	Short Circuit Output Current	-15		-75	mA	V_O = 0V, V_{CC} = 5.0V
I_O	Output Leakage Current High Impedance State			20	μA	V_O = .45V/5.25V
I_{CC}	Power Supply Current		90	130	mA	

TYPICAL CHARACTERISTICS

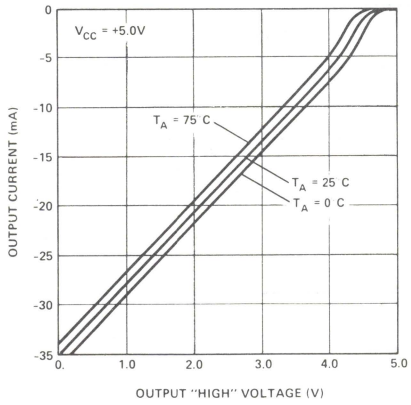
INPUT CURRENT VS. INPUT VOLTAGE



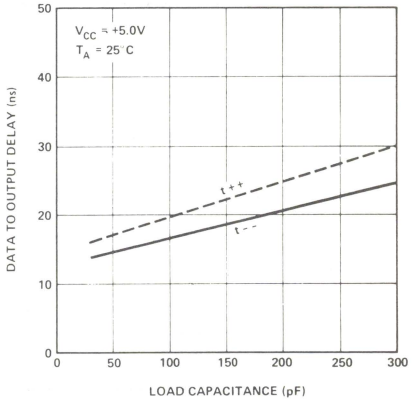
OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE



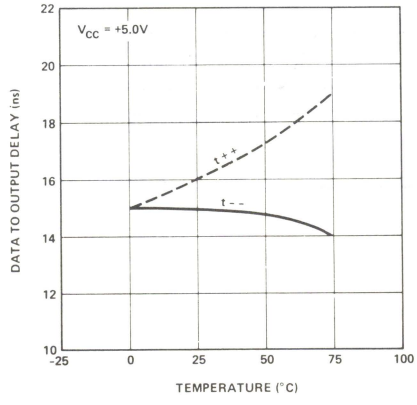
OUTPUT CURRENT VS. OUTPUT "HIGH" VOLTAGE



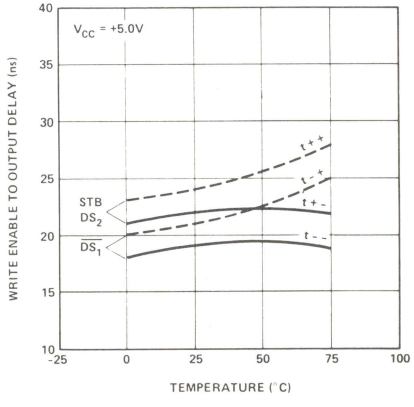
DATA TO OUTPUT DELAY VS. LOAD CAPACITANCE



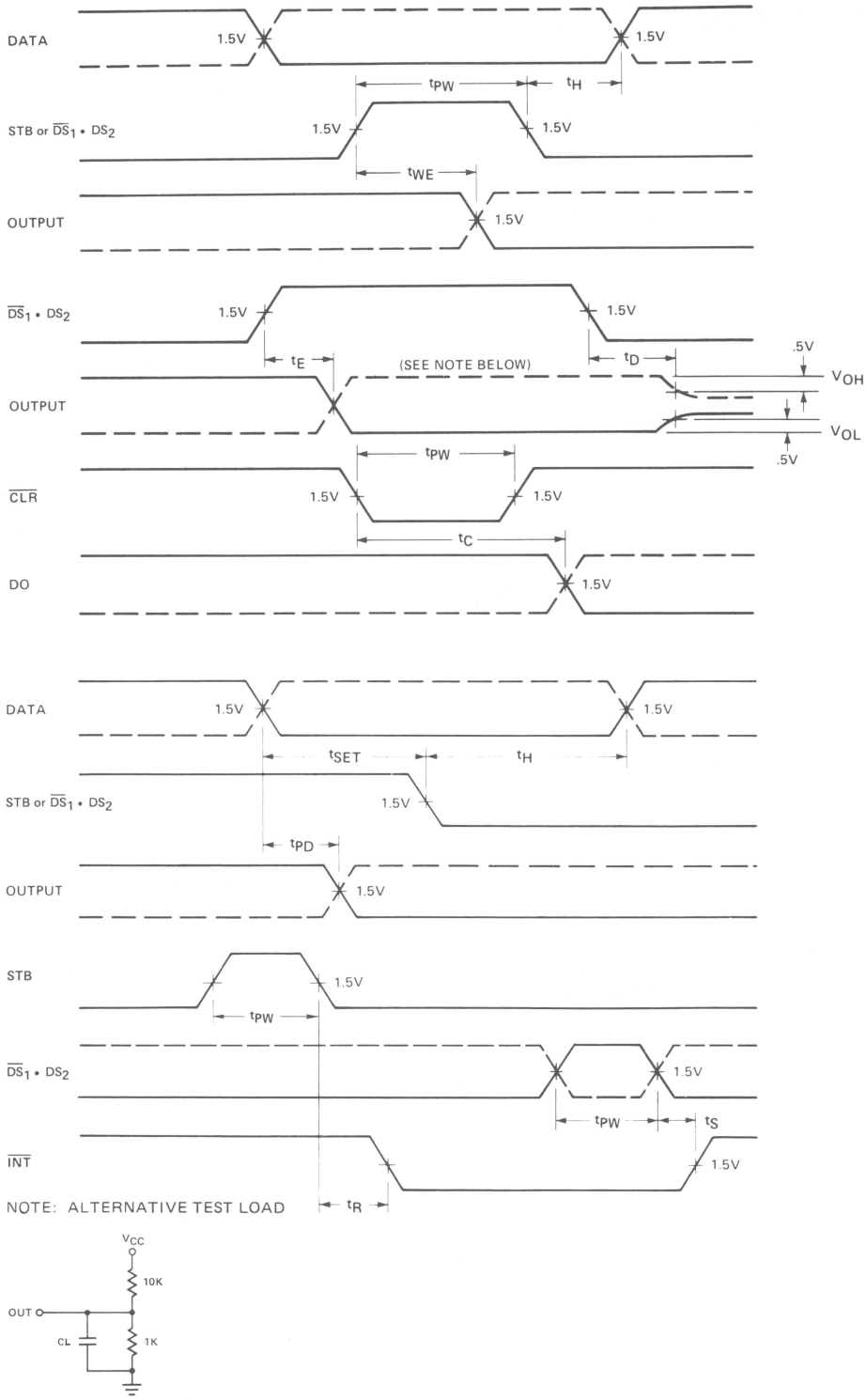
DATA TO OUTPUT DELAY VS. TEMPERATURE



WRITE ENABLE TO OUTPUT DELAY VS. TEMPERATURE



TIMING DIAGRAM



A.C. CHARACTERISTICS

T_A = 0°C to +75°C, V_{CC} = +5V ±5%

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
t_{pw}	Pulse Width	25			ns	
t_{pd}	Data To Output Delay			30	ns	
t_{we}	Write Enable To Output Delay			40	ns	
t_{set}	Data Setup Time	15			ns	
t_h	Data Hold Time	20			ns	
t_r	Reset To Output Delay			40	ns	
t_s	Set To Output Delay			30	ns	
t_e	Output Enable/Disable Time			45	ns	
t_c	Clear To Output Delay			55	ns	

CAPACITANCE*

F = 1 MHz, V_{BIAS} = 2.5V, V_{CC} = +5V, T_A = 25°C

Symbol	Test	LIMITS	
		Typ.	Max.
C_{IN}	DS_1 MD Input Capacitance	9 pF	12 pF
C_{IN}	DS_2, CK, ACK, DI_1-DI_8 Input Capacitance	5 pF	9 pF
C_{OUT}	DO_1-DO_8 Output Capacitance	8 pF	12 pF

*This parameter is sampled and not 100% tested.

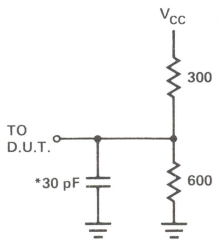
SWITCHING CHARACTERISTICS

Conditions of Test

Input Pulse Amplitude = 2.5 V
Input Rise and Fall Times 5 ns
Between 1V and 2V Measurements made at 1.5V
with 15 mA & 30 pF Test Load

Test Load

15mA & 30pF



* INCLUDING JIG & PROBE CAPACITANCE

M8212/M3212*
8-BIT INPUT/OUTPUT PORT

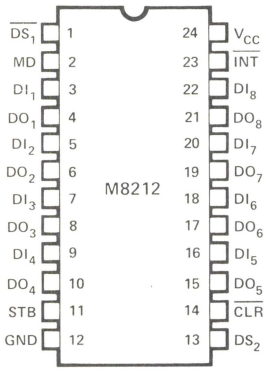
- Fully Parallel 8-Bit Data Register and Buffer
- Service Request Flip-Flop for Interrupt Generation
- Low Input Load Current 0.25 mA Max
- 3-State Outputs
- Full Military Temperature Range −55°C to +125°C
- 3.4V Output High Voltage for Direct Interface to M8080A CPU
- Asynchronous Register Clear
- Replaces Buffers, Latches, and Multiplexers in Microcomputer Systems
- Reduces System Package Count
- ±10% Power Supply Tolerance
- 24-Pin Dual In-Line Package

The Intel® M8212/M3212 input/output port consists of an 8-bit latch with 3-state output buffers along with control and device selection logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

The device is multimode in nature. It can be used to implement latches, gated buffers or multiplexers. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with this device.

*Note: The specifications for the M3212 are identical with those for the M8212.

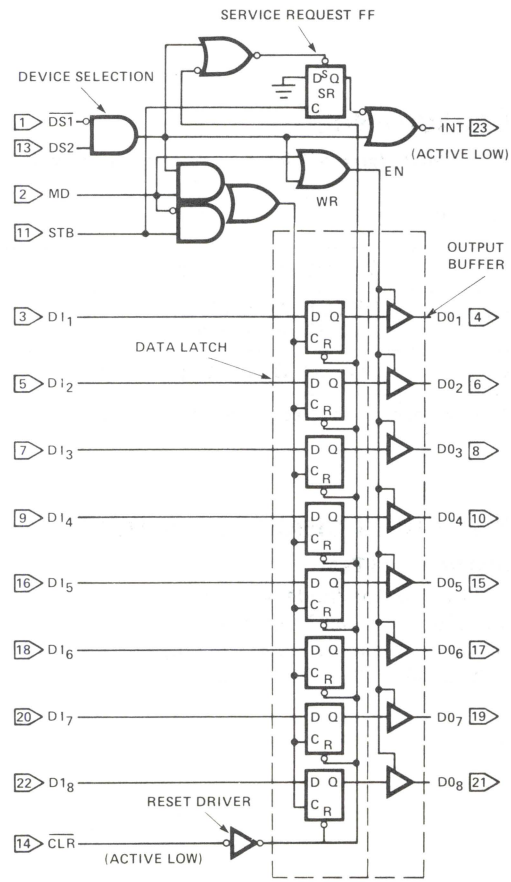
PIN CONFIGURATION



PIN NAMES

DI_1-DI_8	DATA IN
DO_1-DO_8	DATA OUT
$\overline{DS_1}$-DS_2	DEVICE SELECT
MD	MODE
STB	STROBE
$\overline{INT}$	INTERRUPT (ACTIVE LOW)
$\overline{CLR}$	CLEAR (ACTIVE LOW)

LOGIC DIAGRAM



MPU PERIPHERALS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −55°C to +125°C
Storage Temperature ..... −65°C to +160°C
All Output or Supply Voltages .... −0.5 to +7 Volts
All Input Voltages ..... −1.0 to 5.5 Volts
Output Currents ..... 100 mA

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = -55°C to +125°C V_{CC} = +5V ±10%

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
I_F	Input Load Current ACK, DS_2, CR, DI_1-DI_8 Inputs			−.25	mA	V_F = .45V
I_F	Input Load Current MD Input			−.75	mA	V_F = .45V
I_F	Input Load Current DS_1 Input			−1.0	mA	V_F = .45V
I_R	Input Leakage Current ACK, DS, CR, DI_1-DI_8 Inputs			10	μA	V_R = V_{CC}
I_R	Input Leakage Current MD Input			30	μA	V_R = V_{CC}
I_R	Input Leakage Current DS_1 Input			40	μA	V_R = V_{CC}
V_C	Input Forward Voltage Clamp			−1.2	V	I_C = −5 mA
V_{IL}	Input "Low" Voltage			.80	V	
V_{IH}	Input "High" Voltage	2.0			V	
V_{OL}	Output "Low" Voltage			.45	V	I_{OL} = 10mA
V_{OH}	Output "High" Voltage	3.4	4.0		V	I_{OH} = -.5mA
I_{OS}	Short Circuit Output Current	-15		-75	mA	V_{CC} = 5.0V
$\|I_O\|$	Output Leakage Current High Impedance State			20	μA	V_O = .45V to V_{CC}
I_{CC}	Power Supply Current		90	145	mA	

A.C. CHARACTERISTICS

T_A = -55°C to +125°C V_{CC} = +5V ±10%

Symbol	Parameter	Limits		Unit	Test Conditions
		Min.	Max.		
t_{PW}	Pulse Width	40		ns	
t_{PD}	Data To Output Delay		30	ns	NOTE 1
t_{WE}	Write Enable To Output Delay		50	ns	NOTE 1
t_{SET}	Data Setup Time	20		ns	
t_H	Data Hold Time	30		ns	
t_R	Reset To Output Delay		55	ns	NOTE 1
t_S	Set To Output Delay		35	ns	NOTE 1
t_E	Output Enable/Disable Time		50	ns	NOTE 1 C_L = 30 pF
t_C	Clear To Output Delay		55	ns	NOTE 1

CAPACITANCE F = 1 MHz, V_{BIAS} = 2.5V, V_{CC} = +5V, T_A = 25°C

Symbol	Test	LIMITS	
		Typ.	Max.
C_{IN}	$\overline{DS}_1$ MD Input Capacitance	9 pF	12 pF
C_{IN}	DS_2, $\overline{CLR}$, STB, DI_1-DI_8 Input Capacitance	5 pF	9 pF
C_{OUT}	DO_1-DO_8 Output Capacitance	8 pF	12 pF

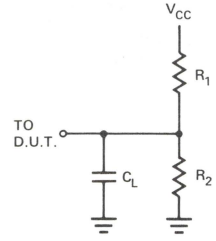
SWITCHING CHARACTERISTICS

Conditions of Test

Input Pulse Amplitude = 2.5V

Input Rise and Fall Times: 5 ns between 1V and 2V

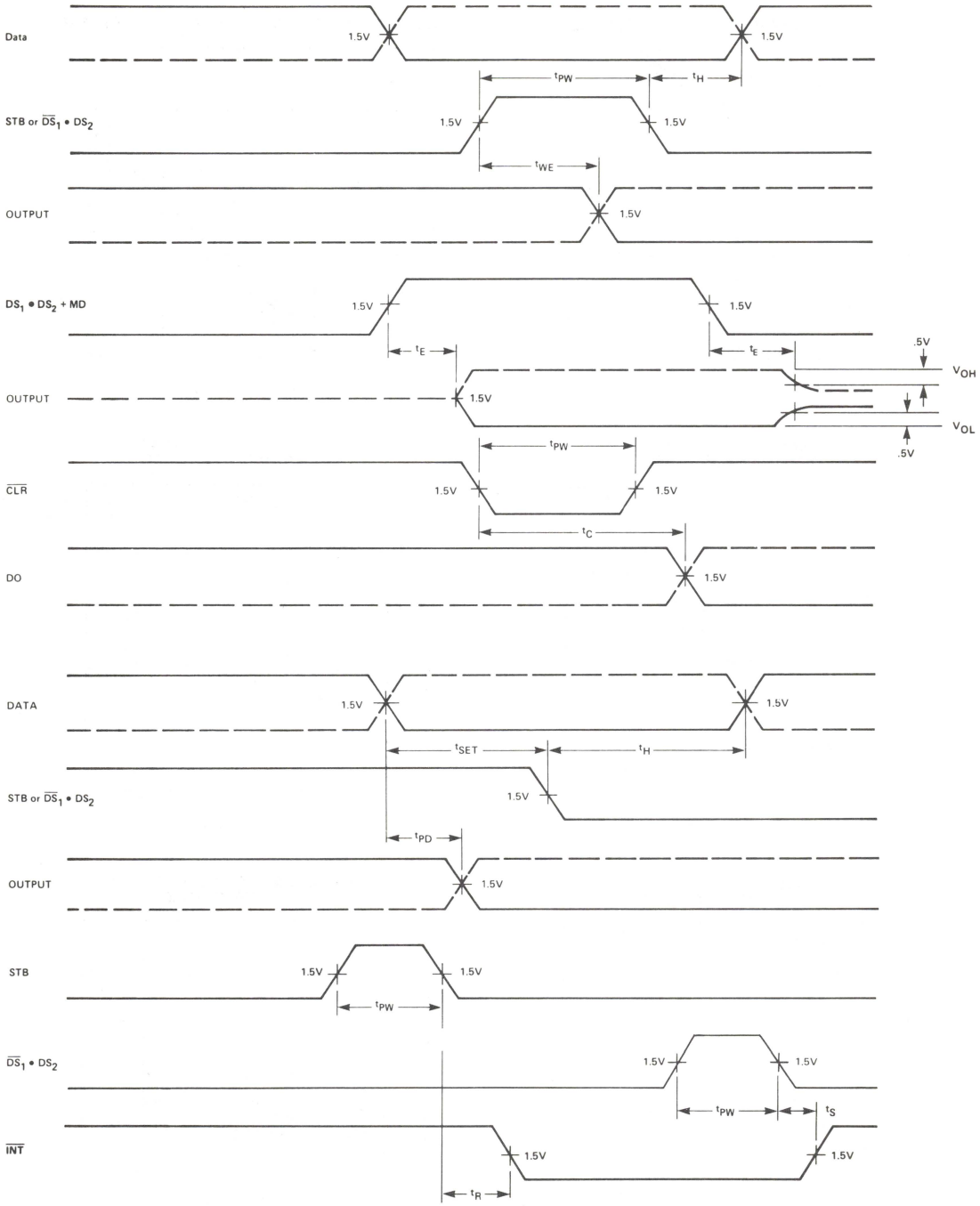
Test Load



NOTE 1:

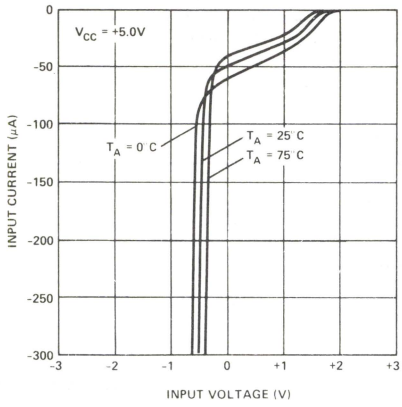
TEST	C_L	R_1	R_2
t_{PD}, t_{WE}, t_R, t_S, t_C	30pF	300Ω	600Ω
t_E, ENABLE↑	30pF	10KΩ	1KΩ
t_E, ENABLE↓	30pF	300Ω	600Ω
t_E, DISABLE↑	5pF	300Ω	600Ω
t_E, DISABLE↓	5pF	10KΩ	1KΩ

TIMING DIAGRAM

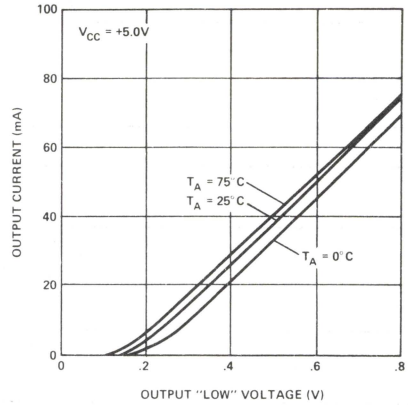


TYPICAL CHARACTERISTICS

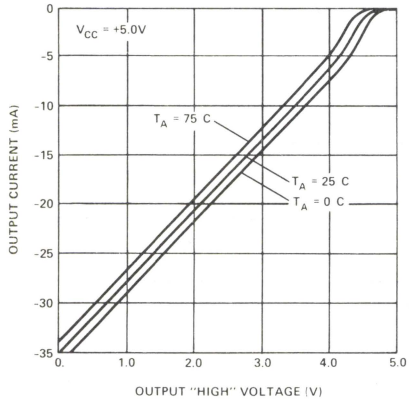
INPUT CURRENT VS. INPUT VOLTAGE



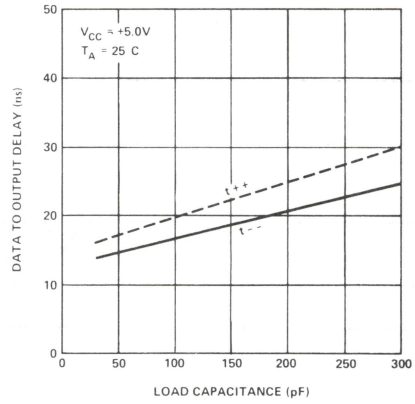
OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE



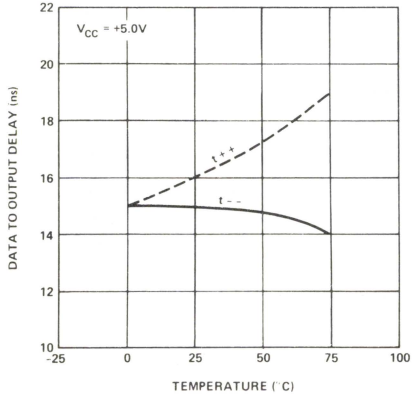
OUTPUT CURRENT VS. OUTPUT "HIGH" VOLTAGE



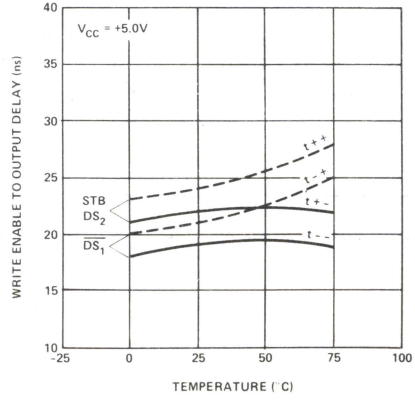
DATA TO OUTPUT DELAY VS. LOAD CAPACITANCE



DATA TO OUTPUT DELAY VS. TEMPERATURE



WRITE ENABLE TO OUTPUT DELAY VS. TEMPERATURE



MPU PERIPHERALS

8214/3214*
PRIORITY INTERRUPT CONTROL UNIT

- **8 Priority Levels**
- **Current Status Register**
- **Priority Comparator**
- **Fully Expandable**
- **High Performance (50 ns)**
- **24-Pin Dual In-Line Package**

The Intel® 8214 is an 8-level priority interrupt control unit (PICU) designed to simplify interrupt-driven microcomputer systems.

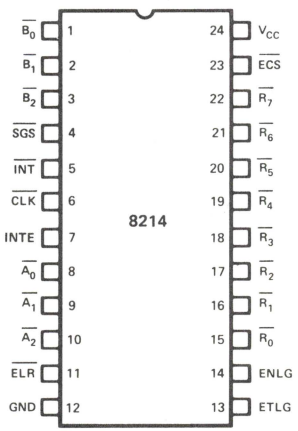
The PICU can accept 8 requesting levels; determine the highest priority, compare this priority to a software controlled current status register and issue an interrupt to the system along with vector information to identify the service routine.

The 8214 is fully expandable by the use of open collector interrupt output vector information. Control signals are also provided to simplify this function.

The PICU is designed to support a wide variety of vectored interrupt structures and reduce package count in interrupt-driven microcomputer systems.

*Note: The specifications for the 3214 are identical with those for the 8214.

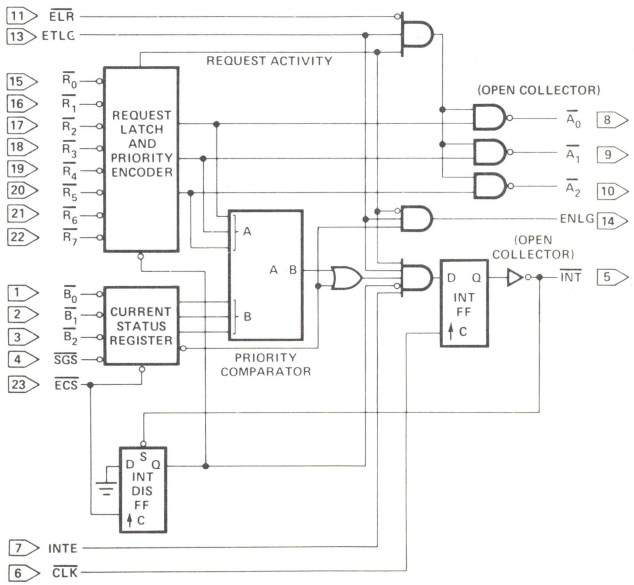
PIN CONFIGURATION



PIN NAMES

INPUTS		
$\overline{R_0}$-$\overline{R_7}$	REQUEST LEVELS (R_7 HIGHEST PRIORITY)	
$\overline{B_0}$-$\overline{B_2}$	CURRENT STATUS	
$\overline{SGS}$	STATUS GROUP SELECT	
$\overline{ECS}$	ENABLE CURRENT STATUS	
INTE	INTERRUPT ENABLE	
$\overline{CLK}$	CLOCK (INT F-F)	
$\overline{ELR}$	ENABLE LEVEL READ	
ETLG	ENABLE THIS LEVEL GROUP	
OUTPUTS:		
$\overline{A_0}$-$\overline{A_2}$	REQUEST LEVELS	OPEN COLLECTOR
$\overline{INT}$	INTERRUPT (ACT. LOW)	OPEN COLLECTOR
ENLG	ENABLE NEXT LEVEL GROUP	

LOGIC DIAGRAM



MPU PERIPHERALS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . 0°C to 75°C
Storage Temperature . . . . . −65°C to +160°C
All Output and Supply Voltages . . . . . −0.5V to +7V
All Input Voltages . . . . . −1.0V to +5.5V
Output Currents . . . . . 100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specifications is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5V ±5%.

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[1]	Max.		
V_C	Input Clamp Voltage (all inputs)			-1.0	V	I_C=-5mA
I_F	Input Forward Current: ETLG input all other inputs		-.15 -.08	-0.5 -0.25	mA mA	V_F=0.45V
I_R	Input Reverse Current: ETLG input all other inputs			80 40	µA µA	V_R=5.25V
V_{IL}	Input LOW Voltage: all inputs			0.8	V	V_{CC}=5.0V
V_{IH}	Input HIGH Voltage: all inputs	2.0			V	V_{CC}=5.0V
I_{CC}	Power Supply Current		90	130	mA	See Note 2.
V_{OL}	Output LOW Voltage: all outputs		.3	.45	V	I_{OL}=15mA
V_{OH}	Output HIGH Voltage: ENLG output	2.4	3.0		V	I_{OH}=-1mA
I_{OS}	Short Circuit Output Current: ENLG output	-20	-35	-55	mA	V_{OS}=0V, V_{CC}=5.0V
I_{CEX}	Output Leakage Current: $\overline{INT}$ and $\overline{A_0}$-$\overline{A_2}$			100	µA	V_{CEX}=5.25V

NOTES:
1. Typical values are for T_A = 25° C, V_{CC} = 5.0V.
2. B_0-B_2, $\overline{SGS}$, CLK, $\overline{R_0}$-$\overline{R_4}$ grounded, all other inputs and all outputs open.

A.C. CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

Symbol	Parameter	Limits			Unit
		Min.	Typ.[1]	Max.	
t_{CY}	$\overline{CLK}$ Cycle Time	80	50		ns
t_{PW}	$\overline{CLK}$, $\overline{ECS}$, $\overline{INT}$ Pulse Width	25	15		ns
t_{ISS}	INTE Setup Time to $\overline{CLK}$	16	12		ns
t_{ISH}	INTE Hold Time after $\overline{CLK}$	20	10		ns
t_{ETCS}[2]	ETLG Setup Time to $\overline{CLK}$	25	12		ns
t_{ETCH}[2]	ETLG Hold Time After $\overline{CLK}$	20	10		ns
t_{ECCS}[2]	$\overline{ECS}$ Setup Time to $\overline{CLK}$	80	25		ns
t_{ECCH}[3]	$\overline{ECS}$ Hold Time After $\overline{CLK}$	0			ns
t_{ECRS}[3]	$\overline{ECS}$ Setup Time to $\overline{CLK}$	110	70		ns
t_{ECRH}[3]	$\overline{ECS}$ Hold Time After $\overline{CLK}$	0			
t_{ECSS}[2]	$\overline{ECS}$ Setup Time to $\overline{CLK}$	75	70		ns
t_{ECSH}[2]	$\overline{ECS}$ Hold Time After $\overline{CLK}$	0			ns
t_{DCS}[2]	$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Setup Time to $\overline{CLK}$	70	50		ns
t_{DCH}[2]	$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Hold Time After $\overline{CLK}$	0			ns
t_{RCS}[3]	$\overline{R_0}$-$\overline{R_7}$ Setup Time to $\overline{CLK}$	90	55		ns
t_{RCH}[3]	$\overline{R_0}$-$\overline{R_7}$ Hold Time After $\overline{CLK}$	0			ns
t_{ICS}	$\overline{INT}$ Setup Time to $\overline{CLK}$	55	35		ns
t_{CI}	$\overline{CLK}$ to $\overline{INT}$ Propagation Delay		15	25	ns
t_{RIS}[4]	$\overline{R_0}$-$\overline{R_7}$ Setup Time to $\overline{INT}$	10	0		ns
t_{RIH}[4]	$\overline{R_0}$-$\overline{R_7}$ Hold Time After $\overline{INT}$	35	20		ns
t_{RA}	$\overline{R_0}$-$\overline{R_7}$ to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay		80	100	ns
t_{ELA}	$\overline{ELR}$ to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay		40	55	ns
t_{ECA}	$\overline{ECS}$ to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay		100	120	ns
t_{ETA}	ETLG to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay		35	70	ns
t_{DECS}[4]	$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Setup Time to $\overline{ECS}$	15	10		ns
t_{DECH}[4]	$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Hold Time After $\overline{ECS}$	15	10		ns
t_{REN}	$\overline{R_0}$-$\overline{R_7}$ to ENLG Propagation Delay		45	70	ns
t_{ETEN}	ETLG to ENLG Propagation Delay		20	25	ns
t_{ECRN}	$\overline{ECS}$ to ENLG Propagation Delay		85	90	ns
t_{ECSN}	$\overline{ECS}$ to ENLG Propagation Delay		35	55	ns

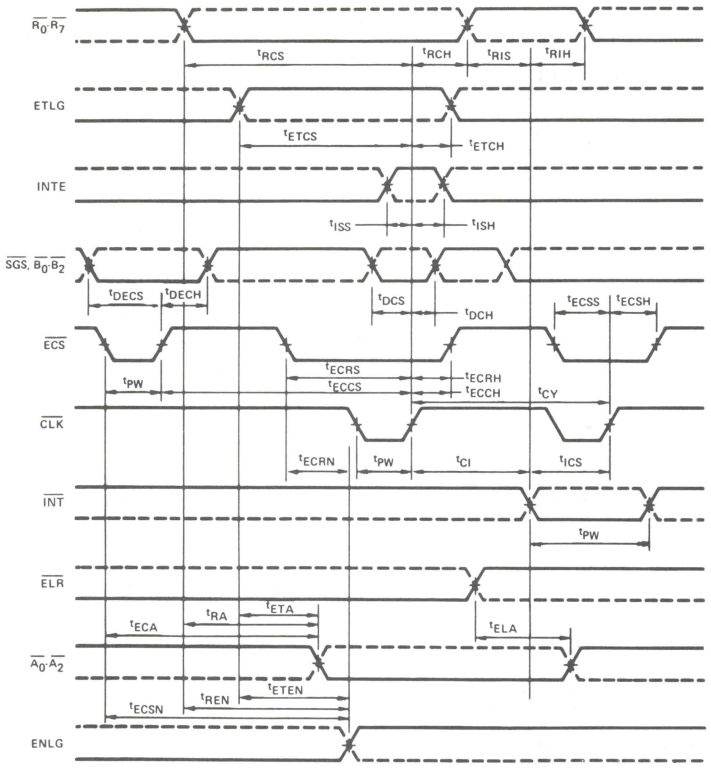
CAPACITANCE[5]

Symbol	Parameter	Limits			Unit
		Min.	Typ.[1]	Max	
C_{IN}	Input Capacitance		5	10	pF
C_{OUT}	Output Capacitance		7	12	pF

Test Conditions: $V_{BIAS} = 2.5V$, $V_{CC} = 5V$, $T_A = 25°C$, f = 1 MHz

NOTE 5. This parameter is periodically sampled and not 100% tested.

WAVEFORMS



NOTES:

(1) Typical values are for $T_A = 25°C$, $V_{CC} = 5.0V$.

(2) Required for proper operation if ISE is enabled during next clock pulse.

(3) These times are not required for proper operation but for desired change in interrupt flip-flop.

(4) Required for new request or status to be properly loaded.

Test Conditions

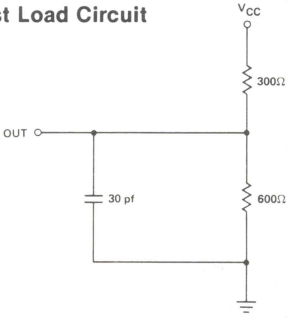
Input pulse amplitude: 2.5 volts.

Input rise and fall times: 5 ns between 1 and 2 volts.

Output loading of 15 mA and 30 pf.

Speed measurements taken at the 1.5V levels.

Test Load Circuit



MPU PERIPHERALS

M8214/M3214*
PRIORITY INTERRUPT CONTROL UNIT

- 8 Priority Levels
- Fully Expandable
- Current Status Register
- Priority Comparator
- 24-Pin Dual In-Line Package
- Full Military Temperature Range −55°C to +125°C
- +10% Power Supply Tolerance

The Intel® M8214 is an 8-level priority interrupt control unit (PICU) designed to simplify interrupt-driven microcomputer systems.

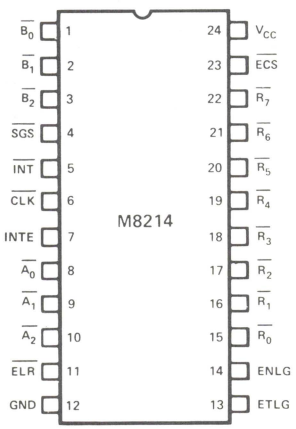
The PICU can accept 8 requesting levels; determine the highest priority, compare this priority to a software controlled current status register and issue and interrupt to the system along with vector information to identify the service routine.

The M8214 is fully expandable by the use of open collector interrupt output vector information. Control signals are also provided to simplify this function.

The PICU is designed to support a wide variety of vectored interrupt structures and reduce package count in interrupt-driven microcomputer systems.

*Note: The specifications for the M3214 are identical with those for the M8214.

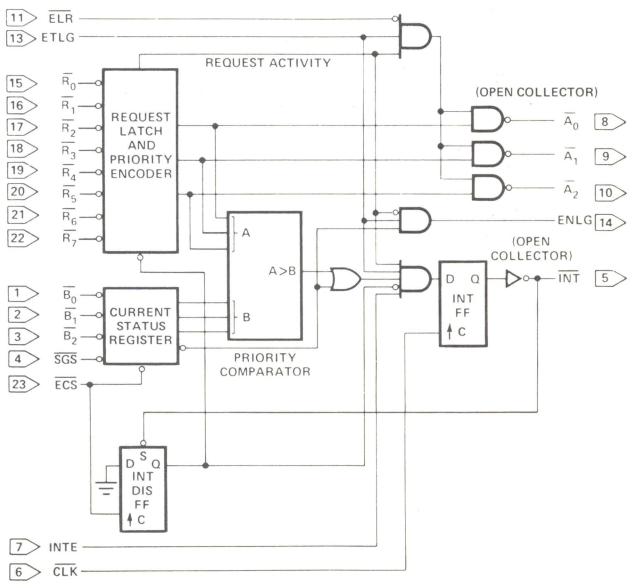
PIN CONFIGURATION



PIN NAMES

INPUTS		
$\overline{R_0}$-$\overline{R_7}$	REQUEST LEVELS (R_7 HIGHEST PRIORITY)	
$\overline{B_0}$-$\overline{B_2}$	CURRENT STATUS	
$\overline{SGS}$	STATUS GROUP SELECT	
$\overline{ECS}$	ENABLE CURRENT STATUS	
INTE	INTERRUPT ENABLE	
$\overline{CLK}$	CLOCK (INT F-F)	
$\overline{ELR}$	ENABLE LEVEL READ	
ETLG	ENABLE THIS LEVEL GROUP	
OUTPUTS:		
$\overline{A_0}$-$\overline{A_2}$	REQUEST LEVELS	OPEN COLLECTOR
$\overline{INT}$	INTERRUPT (ACT. LOW)	OPEN COLLECTOR
ENLG	ENABLE NEXT LEVEL GROUP	

LOGIC DIAGRAM



MPU PERIPHERALS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +160°C
All Output and Supply Voltages . . . . . −0.5V to +7V
All Input Voltages . . . . . −1.0V to +5.5V
Output Currents . . . . . 100 mA

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. AND OPERATING CHARACTERISTICS

T_A = 55°C to 125°C V_{CC} = 5V ±10%

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[1]	Max.		
V_C	Input Clamp Voltage (all inputs)			-1.2	V	I_C=-5mA
I_F	Input Forward Current: ETLG input all other inputs		-.15 -.08	-0.5 -0.25	mA mA	V_F=0.45V
I_R	Input Reverse Current: ETLG input all other inputs			80 40	μA μA	V_R=5.5V
V_{IL}	Input LOW Voltage: all inputs			0.8	V	V_{CC}=5.0V
V_{IH}	Input HIGH Voltage: all inputs	2.0			V	V_{CC}=5.0V
I_{CC}	Power Supply Current		90	130	mA	See Note 2.
V_{OL}	Output LOW Voltage: all outputs		.3	.45	V	I_{OL}=10mA
V_{OH}	Output HIGH Voltage: ENLG output	2.4	3.0		V	I_{OH}=-1mA
I_{OS}	Short Circuit Output Current: ENLG output	-15	-35	-55	mA	V_{CC}=5.0V
I_{CEX}	Output Leakage Current: $\overline{INT}$, $\overline{A_0}$, $\overline{A_1}$, $\overline{A_2}$			100	μA	V_{CEX}=5.5V

NOTES:
1. Typical values are for T_A = 25° C, V_{CC} = 5.0V.
2. B_0-B_2, $\overline{SGS}$, CLK, $\overline{R_0}$-$\overline{R_4}$ grounded, all other inputs and all outputs open.

A.C. CHARACTERISTICS T_A = -55°C to +125°C, V_{CC} = +5V ±10%

Symbol	Parameter	Limits			Unit
		Min.	Typ.[1]	Max.	
t_{CY}	$\overline{CLK}$ Cycle Time	85			ns
t_{PW}	$\overline{CLK}$, $\overline{ECS}$, $\overline{INT}$ Pulse Width	25	15		ns
t_{ISS}	INTE Setup Time to $\overline{CLK}$	16	12		ns
t_{ISH}	INTE Hold Time after $\overline{CLK}$	20	10		ns
t_{ETCS}[2]	ETLG Setup Time to $\overline{CLK}$	25	12		ns
t_{ETCH}[2]	ETLG Hold Time After $\overline{CLK}$	20	10		ns
t_{ECCS}[2]	$\overline{ECS}$ Setup Time to $\overline{CLK}$	85	25		ns
t_{ECCH}[3]	$\overline{ECS}$ Hold Time After $\overline{CLK}$	0			ns
t_{ECRS}[3]	$\overline{ECS}$ Setup Time to $\overline{CLK}$	110	70		ns
t_{ECRH}[3]	$\overline{ECS}$ Hold Time After $\overline{CLK}$	0			
t_{ECSS}[2]	$\overline{ECS}$ Setup Time to $\overline{CLK}$	85	70		ns
t_{ECSH}[2]	$\overline{ECS}$ Hold Time After $\overline{CLK}$	0			ns
t_{DCS}[2]	$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Setup Time to $\overline{CLK}$	90	50		ns
t_{DCH}[2]	$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Hold Time After $\overline{CLK}$	0			ns
t_{RCS}[3]	$\overline{R_0}$-$\overline{R_7}$ Setup Time to $\overline{CLK}$	100	55		ns
t_{RCH}[3]	$\overline{R_0}$-$\overline{R_7}$ Hold Time After $\overline{CLK}$	0			ns
t_{ICS}	$\overline{INT}$ Setup Time to $\overline{CLK}$	55	35		ns
t_{CI}	$\overline{CLK}$ to $\overline{INT}$ Propagation Delay		15	30	ns
t_{RIS}[4]	$\overline{R_0}$-$\overline{R_7}$ Setup Time to $\overline{INT}$	10	0		ns
t_{RIH}[4]	$\overline{R_0}$-$\overline{R_7}$ Hold Time After $\overline{INT}$	35	20		ns
t_{RA}	$\overline{R_0}$-$\overline{R_7}$ to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay		80	100	ns
t_{ELA}	$\overline{ELR}$ to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay		40	55	ns
t_{ECA}	$\overline{ECS}$ to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay		100	130	ns
t_{ETA}	ETLG to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay		35	70	ns
t_{DECS}[4]	$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Setup Time to $\overline{ECS}$	20	10		ns
t_{DECH}[4]	$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Hold Time After $\overline{ECS}$	20	10		ns
t_{REN}	$\overline{R_0}$-$\overline{R_7}$ to ENLG Propagation Delay		45	70	ns
t_{ETEN}	ETLG to ENLG Propagation Delay		20	30	ns
t_{ECRN}	$\overline{ECS}$ to ENLG Propagation Delay		85	110	ns
t_{ECSN}	$\overline{ECS}$ to ENLG Propagation Delay		35	55	ns

CAPACITANCE

Symbol	Parameter	Limits			Unit
		Min.	Typ.[1]	Max	
C_{IN}	Input Capacitance		5	10	pF
C_{OUT}	Output Capacitance		7	12	pF

Test Conditions: V_{BIAS} = 2.5V, V_{CC} = 5V, T_A = 25°C, f = 1 MHz

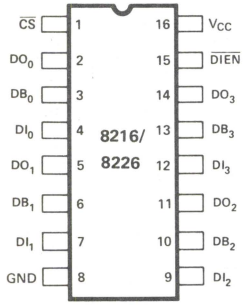
8216/8226, 3216/3226*
4-BIT PARALLEL BIDIRECTIONAL BUS DRIVER

- **Data Bus Buffer Driver for 8080 CPU**
- **Low Input Load Current — 0.25 mA Maximum**
- **High Output Drive Capability for Driving System Bus**
- **3.65V Output High Voltage for Direct Interface to 8080 CPU**
- **3-State Outputs**
- **Reduces System Package Count**

The 8215/8226 is a 4-bit bidirectional bus driver/receiver. All inputs are low power TTL compatible. For driving MOS, the DO outputs provide a high 3.65V V_{OH}, and for high capacitance terminated bus structures, the DB outputs provide a high 50 mA I_{OL} capability. A non-inverting (8216) and an inverting (8226) are available to meet a wide variety of applications for buffering in microcomputer systems.

*Note: The specifications for the 3216/3226 are identical with those for the 8216/8226.

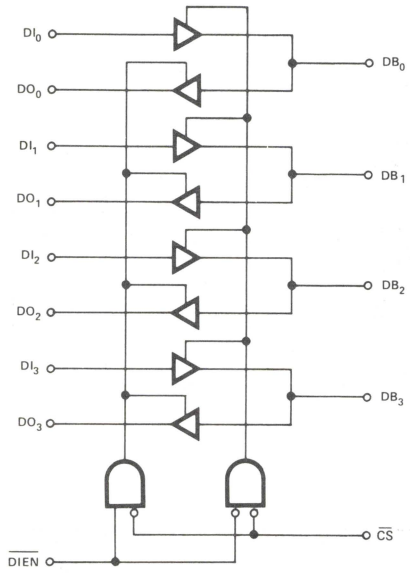
PIN CONFIGURATION



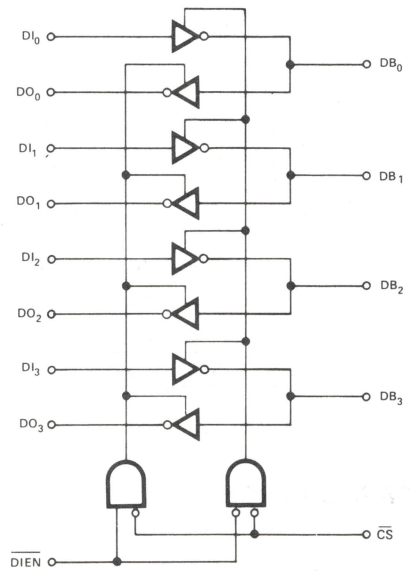
PIN NAMES

DB_0-DB_3	DATA BUS BI-DIRECTIONAL
DI_0-DI_3	DATA INPUT
DO_0-DO_3	DATA OUTPUT
$\overline{DIEN}$	DATA IN ENABLE DIRECTION CONTROL
$\overline{CS}$	CHIP SELECT

LOGIC DIAGRAM
8216



LOGIC DIAGRAM
8226



MPU PERIPHERALS

FUNCTIONAL DESCRIPTION

Microprocessors like the 8080 are MOS devices and are generally capable of driving a single TTL load. The same is true for MOS memory devices. While this type of drive is sufficient in small systems with few components, quite often it is necessary to buffer the microprocessor and memories when adding components or expanding to a multi-board system.

The 8216/8226 is a four bit bi-directional bus driver specifically designed to buffer microcomputer system components.

Bidirectional Driver

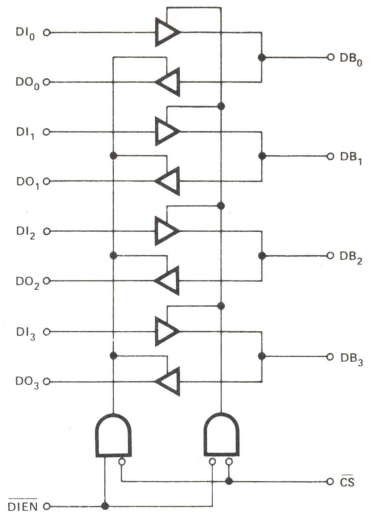
Each buffered line of the four bit driver consists of two separate buffers that are tri-state in nature to achieve direct bus interface and bi-directional capability. On one side of the driver the output of one buffer and the input of another are tied together (DB), this side is used to interface to the system side components such as memories, I/O, etc., because its interface is direct TTL compatible and it has high drive (50mA). On the other side of the driver the inputs and outputs are separated to provide maximum flexibility. Of course, they can be tied together so that the driver can be used to buffer a true bi-directional bus such as the 8080 Data Bus. The DO outputs on this side of the driver have a special high voltage output drive capability (3.65V) so that direct interface to the 8080 and 8008 CPUs is achieved with an adequate amount of noise immunity (350mV worst case).

Control Gating $\overline{\text{DIEN}}$, $\overline{\text{CS}}$

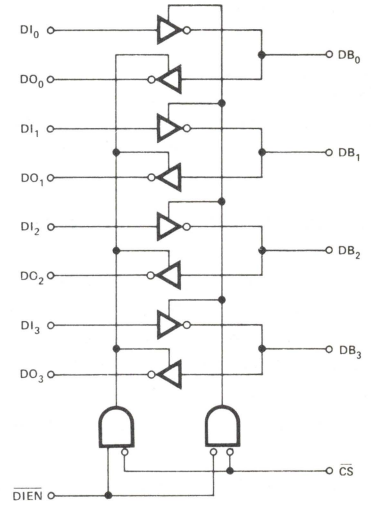
The $\overline{\text{CS}}$ input is actually a device select. When it is "high" the output drivers are all forced to their high-impedance state. When it is at "zero" the device is selected (enabled) and the direction of the data flow is determined by the $\overline{\text{DIEN}}$ input.

The $\overline{\text{DIEN}}$ input controls the direction of data flow (see Figure 1) for complete truth table. This direction control is accomplished by forcing one of the pair of buffers into its high impedance state and allowing the other to transmit its data. A simple two gate circuit is used for this function.

The 8216/8226 is a device that will reduce component count in microcomputer systems and at the same time enhance noise immunity to assure reliable, high performance operation.



(a) 8216



(b) 8226

$\overline{\text{DIEN}}$	$\overline{\text{CS}}$	
0	0	DI → DB
1	0	DB → DO
0	1	HIGH IMPEDANCE
1	1	

Figure 1. 8216/8226 Logic Diagrams

APPLICATIONS OF THE 8216/8226

8080 Data Bus Buffer

The 8080 CPU Data Bus is capable of driving a single TTL load and is more than adequate for small, single board systems. When expanding such a system to more than one board to increase I/O or Memory size, it is necessary to provide a buffer. The 8216/8226 is a device that is exactly fitted to this application.

Shown in Figure 2 are a pair of 8216/8226 connected directly to the 8080 Data Bus and associated control signals. The buffer is bi-directional in nature and serves to isolate the CPU data bus.

On the system side, the DB lines interface with standard semiconductor I/O and Memory components and are completely TTL compatible. The DB lines also provide a high drive capability (50mA) so that an extremely large system can be dirven along with possible bus termination networks.

On the 8080 side the DI and DO lines are tied together and are directly connected to the 8080 Data Bus for bi-directional operation. The DO outputs of the 8216/8226 have a high voltage output capability of 3.65 volts which allows direct connection to the 8080 whose minimum input voltage is 3.3 volts. It also gives a very adequate noise margin of 350mV (worst case).

The $\overline{\text{DIEN}}$ inputs to 8216/8226 is connected directly to the 8080. $\overline{\text{DIEN}}$ is tied to DBIN so that proper bus flow is maintained, and $\overline{\text{CS}}$ is tied to $\overline{\text{BUSEN}}$ so that the system side Data Bus will be 3-stated when a Hold request has been acknowledged during a DMA activity.

Memory and I/O Interface to a Bidirectional Bus

In large microcomputer systems it is often necessary to provide Memory and I/O with their own buffers and at the same time maintain a direct, common interface to a bi-directional Data Bus. The 8216/8226 has separated data in and data out lines on one side and a common bi-directional set on the other to accomodate such a function.

Shown in Figure 3 is an example of how the 8216/8226 is used in this type of application.

The interface to Memory is simple and direct. The memories used are typically Intel® 8102, 8102A, 8101 or 8107B-4 and have separate data inputs and outputs. The DI and DO lines of the 8216/8226 tie to them directly and under control of the $\overline{\text{MEMR}}$ signal, which is connected to the $\overline{\text{DIEN}}$ input, an interface to the bi-directional Data Bus is maintained.

The interface to I/O is similar to Memory. The I/O devices used are typically Intel® 8255s, and can be used for both input and output ports. The $\overline{\text{I/O R}}$ signal is connected directly to the $\overline{\text{DIEN}}$ input so that proper data flow from the I/O device to the Data Bus is maintained.

The 8216/8226 can be used in a wide variety of other buffering functions in microcomputer systems such as Address Bus Drivers, Drivers to peripheral devices such as printers, and as Drivers for long length cables to other peripherals or systems.

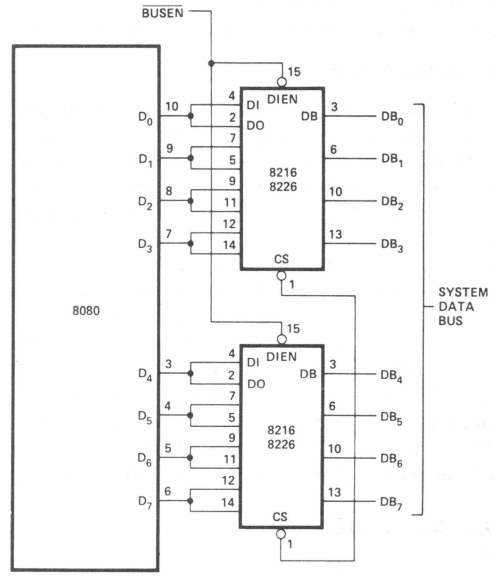


Figure 2. 8080 Data Bus Buffer

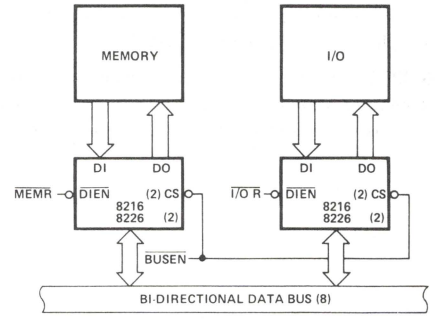


Figure 3. Memory and I/O Interface to a Bidirectional Bus

MPU PERIPHERALS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . -65°C to +150°C
All Output and Supply Voltages . . . . . -0.5V to +7V
All Input Voltages . . . . . -1.0V to +5.5V
Output Currents . . . . . 125 mA

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

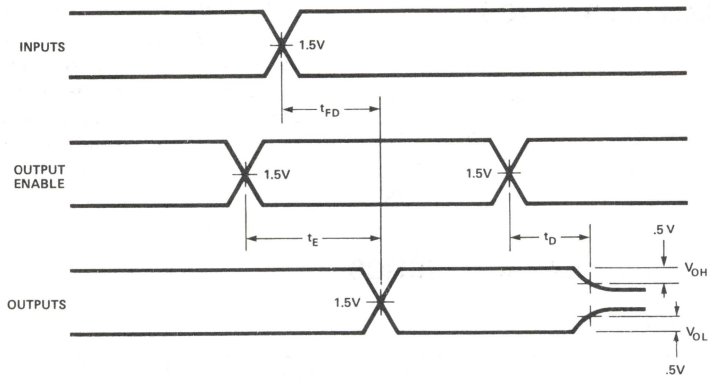
D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC}=+5V ±5%

Symbol	Parameter		Limits Min.	Typ.	Max.	Unit	Conditions
I_{F1}	Input Load Current $\overline{DIEN}$, $\overline{CS}$			-0.15	-.5	mA	V_F = 0.45
I_{F2}	Input Load Current All Other Inputs			-0.08	-.25	mA	V_F = 0.45
I_{R1}	Input Leakage Current $\overline{DIEN}$, $\overline{CS}$				80	μA	V_R = 5.25V
I_{R2}	Input Leakage Current DI Inputs				40	μA	V_R = 5.25V
V_C	Input Forward Voltage Clamp				-1	V	I_C = -5mA
V_{IL}	Input "Low" Voltage				.95	V	
V_{IH}	Input "High" Voltage		2.0			V	
$\|I_O\|$	Output Leakage Current (3-State)	DO DB			20 100	μA	V_O = 0.45V/5.25V
I_{CC}	Power Supply Current	8216		95	130	mA	
		8226		85	120	mA	
V_{OL1}	Output "Low" Voltage			0.3	.45	V	DO Outputs I_{OL}=15mA DB Outputs I_{OL}=25mA
V_{OL2}	Output "Low" Voltage	8216		0.5	.6	V	DB Outputs I_{OL}=55mA
		8226		0.5	.6	V	DB Outputs I_{OL}=50mA
V_{OH1}	Output "High" Voltage		3.65	4.0		V	DO Outputs I_{OH} = -1mA
V_{OH2}	Output "High" Voltage		2.4	3.0		V	DB Outputs I_{OH} = -10mA
I_{OS}	Output Short Circuit Current		-15 -30	-35 -75	-65 -120	mA mA	DO Outputs $V_O \cong 0V$, DB Outputs V_{CC}=5.0V

NOTE: Typical values are for T_A = 25°C, V_{CC} = 5.0V.

WAVEFORMS



A.C. CHARACTERISTICS

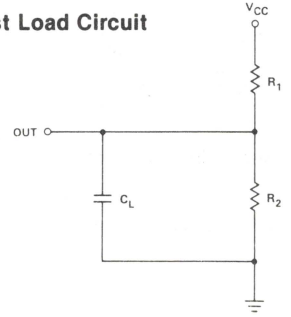
T_A = 0°C to +70°C, V_{CC} = +5V ±5%

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Conditions
T_{PD1}	Input to Output Delay DO Outputs		15	25	ns	C_L=30pF, R_1=300Ω R_2=600Ω
T_{PD2}	Input to Output Delay DB Outputs 8216		19	30	ns	C_L=300pF, R_1=90Ω
	8226		16	25	ns	R_2 = 180Ω
T_E	Output Enable Time 8216		42	65	ns	(Note 2)
	8226		36	54	ns	(Note 3)
T_D	Output Disable Time		16	35	ns	(Note 4)

Test Conditions:

Input pulse amplitude of 2.5V.
Input rise and fall times of 5 ns between 1 and 2 volts.
Output loading is 5 mA and 10 pF.
Speed measurements are made at 1.5 volt levels.

Test Load Circuit



CAPACITANCE[5]

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit
C_{IN}	Input Capacitance		4	8	pF
C_{OUT1}	Output Capacitance		6	10	pF
C_{OUT2}	Output Capacitance		13	18	pF

Test Conditions V_{BIAS} = 2.5V, V_{CC} = 5.0V, T_A = 25°C, f = 1 MHz.

NOTES:
1. Typical values are for T_A = 25°C, V_{CC} = 5.0V.
2. DO Outputs, C_L = 30pF, R_1 = 300/10 KΩ, R_2 = 180/1KΩ; DB Outputs, C_L = 300pF, R_1 = 90/10 KΩ, R_2 = 180/1 KΩ.
3. DO Outputs, C_L = 30pF, R_1 = 300/10 KΩ, R_2 = 600/1K; DB Outputs, C_L = 300pF, R_1 = 90/10 KΩ, R_2 = 180/1 KΩ.
4. DO Outputs, C_L = 5pF, R_1 = 300/10 KΩ, R_2 = 600/1 KΩ; DB Outputs, C_L = 5pF, R_1 = 90/10 KΩ, R_2 = 180/1 KΩ.
5. This parameter is periodically sampled and not 100% tested.

MILITARY TEMP.

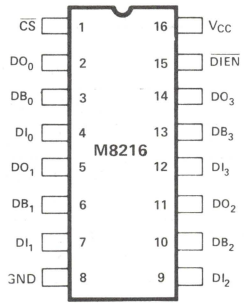
M8216/M3216*
4-BIT PARALLEL BIDIRECTIONAL BUS DRIVER

- **Data Bus Buffer Driver for 8080 CPU**
- **Low Input Load Current: 0.25 mA Maximum**
- **High Output Drive Capability for Driving System Data Bus**
- **16-Pin Dual In-Line Package**
- **3.40V Output High Voltage for Direct Interface to 8080 CPU**
- **3-State Outputs**
- **Full Military Temperature Range −55°C to +125°C**
- **± 10% Power Supply Tolerance**

The M8216 is a 4-bit bidirectional bus driver/receiver. All inputs are low power TTL compatible. For driving MOS, the DO outputs provide a high 3.40V V_{OH}, and for high capacitance terminated bus structures, the DB outputs provide a high 50 mA I_{OL} capability. The M8216 is used to meet a wide variety of applications for buffering in microcomputer systems.

*Note: The specifications for the M3216 are identical with those for the M8216.

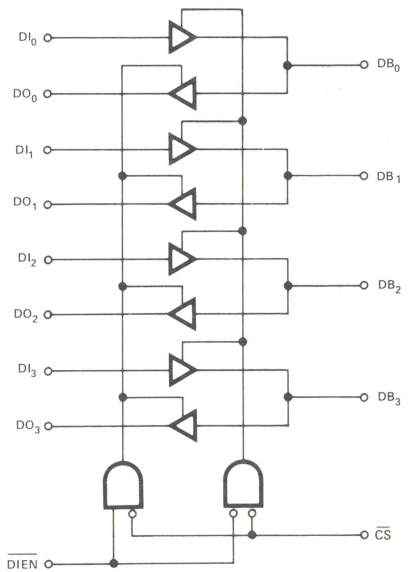
PIN CONFIGURATION



PIN NAMES

DB_0-DB_3	DATA BUS BI-DIRECTIONAL
DI_0-DI_3	DATA INPUT
DO_0-DO_3	DATA OUTPUT
$\overline{DIEN}$	DATA IN ENABLE DIRECTION CONTROL
$\overline{CS}$	CHIP SELECT

LOGIC DIAGRAM
8216



MPU PERIPHERALS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +160°C
All Output and Supply Voltages . . . . . −0.5V to +7V
All Input Voltages . . . . . −1.0V to +5.5V
Output Currents . . . . . 125 mA

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

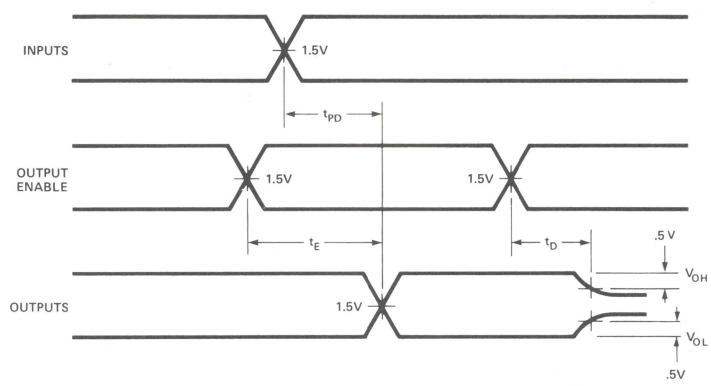
D.C. AND OPERATING CHARACTERISTICS

T_A = -55°C to +125°C, V_{CC} = +5V ±10%

Symbol	Parameter	Limits Min.	Typ.	Max.	Unit	Conditions
I_{F1}	Input Load Current $\overline{DIEN}$, $\overline{CS}$		-0.15	-.5	mA	V_F = 0.45
I_{F2}	Input Load Current All Other Inputs		-0.08	-.25	mA	V_F = 0.45
I_{R1}	Input Leakage Current $\overline{DIEN}$, $\overline{CS}$			80	µA	V_R = 5.5V
I_{R2}	Input Leakage Current DI Inputs			40	µA	V_R = 5.5V
V_C	Input Forward Voltage Clamp			-1.2	V	I_C = -5mA
V_{IL}	Input "Low" Voltage			.95	V	V_{CC} = 5V
V_{IH}	Input "High" Voltage	2.0			V	V_{CC} = 5V
$\|I_O\|$	Output Leakage Current (3-State) DO DB			20 100	µA	V_O = .45V to V_{CC}
I_{CC}	Power Supply Current		95	130	mA	
V_{OL1}	Output "Low" Voltage		0.3	.45	V	DO Outputs I_{OL}=15mA DB Outputs I_{OL}=25mA
V_{OL2}	Output "Low" Voltage		0.5	.6	V	DB Outputs I_{OL}= 45 mA
V_{OH1}	Output "High" Voltage	3.4	3.8		V	DO Outputs I_{OH} = -.5mA
V_{OH2}	Output "High" Voltage	2.4	3.0		V	DO Outputs I_{OH} = -2mA DB Outputs I_{OH} = -5.0mA
I_{OS}	Output Short Circuit Current	-15 -30	-35 -75	-65 -120	mA mA	DO Outputs V_{CC} = 5.0V DB Outputs V_{CC} = 5.0V

NOTE: Typical values are for T_A = 25°C, V_{CC} = 5.0V.

WAVEFORMS



A.C. CHARACTERISTICS

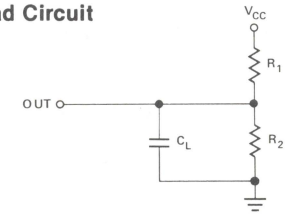
T_A = -55°C to +125°C, V_{CC} = +5V ±10%

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Conditions
T_{PD1}	Input to Output Delay DO Outputs		15	25	ns	(NOTE 2)
T_{PD2}	Input to Output Delay DB Outputs		19	33	ns	(NOTE 2)
T_E	Output Enable Time		42	75	ns	(NOTE 2)
T_D	Output Disable Time		16	40	ns	(NOTE 2)

Test Conditions

Input pulse amplitude of 2.5V.
Input rise and fall times of 5 ns between 1 and 2 volts.

Test Load Circuit



CAPACITANCE

Symbol	Parameter		Limits Min.	Typ.[1]	Max.	Unit
C_{IN}	Input Capacitance			4	6	pF
C_{OUT1}	Output Capacitance	DO Outputs		6	10	pF
C_{OUT2}	Output Capacitance	DB Outputs		13	18	pF

Test Conditions: V_{BIAS} = 2.5V, V_{CC} = 5.0V, T_A = 25°C, f = 1 MHz.

NOTES: 1. Typical values are for T_A = 25°C, V_{CC} = 5.0V.

2.

TEST	C_L	R_1	R_2
T_{PD1}	30pF	300Ω	600Ω
T_{PD2}	300pF	90Ω	180Ω
T_E, (DO, ENABLE↑)	30pF	10KΩ	1KΩ
T_E, (DO, ENABLE↓)	30pF	300Ω	600Ω
T_E, (DB, ENABLE↑)	300pF	10KΩ	1KΩ
T_E, (DB, ENABLE↓)	300pF	90Ω	180Ω
T_D, (DO, DISABLE↑)	5pF	300Ω	600Ω
T_D, (DO, DISABLE↓)	5pF	10KΩ	1KΩ
T_D, (DB, DISABLE↑)	5pF	90Ω	180Ω
T_D, (DB, DISABLE↓)	5pF	10KΩ	1KΩ

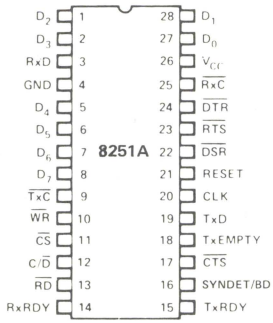
8251A
PROGRAMMABLE COMMUNICATION INTERFACE

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

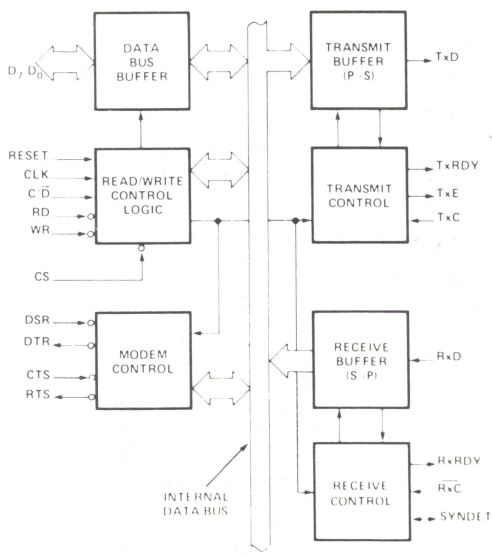
- **Synchronous and Asynchronous Operation**
- **Synchronous — 5-8 Bit Characters; Internal or External Character Synchronization; Automatic Sync Insertion**
- **Asynchronous — 5-8 Bit Characters; Clock Rate — 1, 16, or 64 Times Baud Rate; Break Character Generation; 1, 1½, or 2-Stop Bits; False Start Bit Detection; Automatic Break Detect and Handling**
- **Baud Rate — DC to 64K Baud**
- **Full Duplex, Double Buffered, Transmitter and Receiver**
- **Error Detection — Parity, Overrun and Framing**
- **Fully Compatible with 8080/8085 CPU**
- **28-Pin DIP Package**
- **All Inputs and Outputs are TTL Compatible**
- **Single +5V Supply**
- **Single TTL Clock**

The Intel® 8251A is the enhanced version of the industry standard, Intel® 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART), designed for data communications with Intel's new high performance family of microprocessors such as the 8085. The 8251A is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM "bi-sync"). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously, it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time. These include data transmission errors and control signals such as SYNDET, TxEMPTY. The chip is constructed using N-channel silicon gate technology.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

D_7-D_0	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
RD	Read Data Command
WR	Write Data or Control Command
CS	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
TxC	Transmitter Clock
TxD	Transmitter Data
RxC	Receiver Clock
RxD	Receiver Data
RxRDY	Receiver Ready (has character for 8080)
TxRDY	Transmitter Ready (ready for char. from 8080)

DSR	Data Set Ready
DTR	Data Terminal Ready
SYNDET/BD	Sync Detect/ Break Detect
RTS	Request to Send Data
CTS	Clear to Send Data
TxE	Transmitter Empty
V_{CC}	+5 Volt Supply
GND	Ground

MPU PERIPHERALS

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FEATURES AND ENHANCEMENTS

8251A is an advanced design of the industry standard USART, the Intel® 8251. The 8251A operates with an extended range of Intel microprocessors that includes the new 8085 CPU and maintains compatibility with the 8251. Familiarization time is minimal because of compatibility and involves only knowing the additional features and enhancements, and reviewing the AC and DC specifications of the 8251A.

The 8251A incorporates all the key features of the 8251 and has the following additional features and enhancements:

- 8251A has double-buffered data paths with separate I/O registers for control, status, Data In, and Data Out, which considerably simplifies control programming and minimizes CPU overhead.
- In asynchronous operations, the Receiver detects and handles "break" automatically, relieving the CPU of this task.
- A refined Rx initialization prevents the Receiver from starting when in "break" state, preventing unwanted interrupts from a disconnected USART.
- At the conclusion of a transmission, TxD line will always return to the marking state unless SBRK is programmed.
- Tx Enable logic enhancement prevents a Tx Disable command from halting transmission until all data previously written has been transmitted. The logic also prevents the transmitter from turning off in the middle of a word.
- When External Sync Detect is programmed, Internal Sync Detect is disabled, and an External Sync Detect status is provided via a flip-flop which clears itself upon a status read.
- Possibility of false sync detect is minimized by ensuring that if double character sync is programmed, the characters be contiguously detected and also by clearing the Rx register to all ones whenever Enter Hunt command is issued in Sync mode.
- As long as the 8251A is not selected, the $\overline{RD}$ and $\overline{WR}$ do not affect the internal operation of the device.
- The 8251A Status can be read at any time but the status update will be inhibited during status read.
- The 8251A is free from extraneous glitches and has enhanced AC and DC characteristics, providing higher speed and better operating margins.
- Baud rate from DC to 64K.
- Fully compatible with Intel's new industry standard, the MCS-85.

8251A BASIC FUNCTIONAL DESCRIPTION

General

The 8251A is a Universal Synchronous/Asynchronous Receiver/Transmitter designed specifically for the 80/85 Microcomputer Systems. Like other I/O devices in a Microcomputer System, its functional configuration is programmed by the system's software for maximum flexibility. The 8251A can support virtually any serial data technique currently in use (including IBM "bi-sync").

In a communication environment an interface device must convert parallel format system data into serial format for transmission and convert incoming serial format data into parallel system data for reception. The interface device must also delete or insert bits or characters that are functionally unique to the communication technique. In essence, the interface should appear "transparent" to the CPU, a simple input or output of byte-oriented system data.

Data Bus Buffer

This 3-state, bidirectional, 8-bit buffer is used to interface the 8251A to the system Data Bus. Data is transmitted or received by the buffer upon execution of INput or OUTput instructions of the CPU. Control words, Command words and Status information are also transferred through the Data Bus Buffer. The command status and data in, and data out are separate 8-bit registers to provide double buffering.

This functional block accepts inputs from the system Control bus and generates control signals for overall device operation. It contains the Control Word Register and Command Word Register that store the various control formats for the device functional definition.

RESET (Reset)

A "high" on this input forces the 8251A into an "Idle" mode. The device will remain at "Idle" until a new set of control words is written into the 8251A to program its functional definition. Minimum RESET pulse width is 6 t_{CY} (clock must be running).

CLK (Clock)

The CLK input is used to generate internal device timing and is normally connected to the Phase 2 (TTL) output of the 8224 Clock Generator. No external inputs or outputs are referenced to CLK but the frequency of CLK must be greater than 30 times the Receiver or Transmitter data bit rates.

$\overline{WR}$ (Write)

A "low" on this input informs the 8251A that the CPU is writing data or control words to the 8251A.

$\overline{RD}$ (Read)

A "low" on this input informs the 8251A that the CPU is reading data or status information from the 8251A.

C/$\overline{D}$ (Control/Data)

This input, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs, informs the 8251A that the word on the Data Bus is either a data character, control word or status information.
1 = CONTROL/STATUS 0 = DATA

$\overline{CS}$ (Chip Select)

A "low" on this input selects the 8251A. No reading or writing will occur unless the device is selected. When $\overline{CS}$ is high, the Data Bus in the float state and $\overline{RD}$ and $\overline{WR}$ will have no effect on the chip.

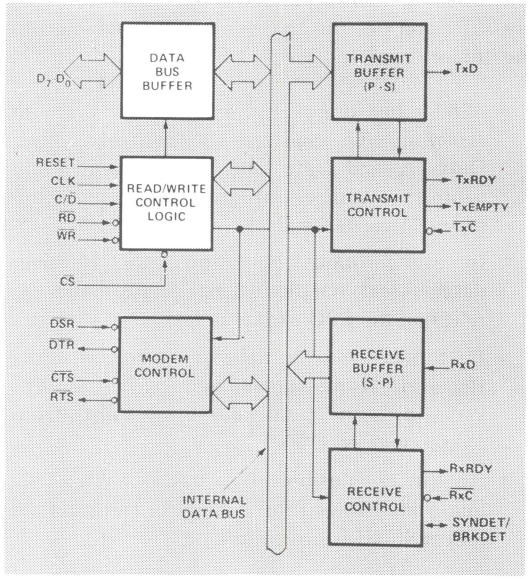


Figure 1. 8251A Block Diagram Showing Data Bus Buffer and Read/Write Logic Functions

C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	8251A DATA ⇒ DATA BUS
0	1	0	0	DATA BUS ⇒ 8251A DATA
1	0	1	0	STATUS ⇒ DATA BUS
1	1	0	0	DATA BUS ⇒ CONTROL
X	1	1	0	DATA BUS ⇒ 3-STATE
X	X	X	1	DATA BUS ⇒ 3-STATE

Modem Control

The 8251A has a set of control inputs and outputs that can be used to simplify the interface to almost any Modem. The Modem control signals are general purpose in nature and can be used for functions other than Modem control, if necessary.

$\overline{\text{DSR}}$ (Data Set Ready)

The $\overline{\text{DSR}}$ input signal is a general purpose, 1-bit inverting input port. Its condition can be tested by the CPU using a Status Read operation. The $\overline{\text{DSR}}$ input is normally used to test Modem conditions such as Data Set Ready.

$\overline{\text{DTR}}$ (Data Terminal Ready)

The $\overline{\text{DTR}}$ output signal is a general purpose, 1-bit inverting output port. It can be set "low" by programming the appropriate bit in the Command Instruction word. The $\overline{\text{DTR}}$ output signal is normally used for Modem control such as Data Terminal Ready or Rate Select.

$\overline{\text{RTS}}$ (Request to Send)

The $\overline{\text{RTS}}$ output signal is a general purpose, 1-bit inverting output port. It can be set "low" by programming the appropriate bit in the Command Instruction word. The $\overline{\text{RTS}}$ output signal is normally used for Modem control such as Request to Send.

$\overline{\text{CTS}}$ (Clear to Send)

A "low" on this input enables the 8251A to transmit serial data if the Tx Enable bit in the Command byte is set to a "one." If either a Tx Enable off or CTS off condition occurs while the Tx is in operation, the Tx will transmit all the data in the USART, written prior to Tx Disable command before shutting down.

Transmitter Buffer

The Transmitter Buffer accepts parallel data from the Data Bus Buffer, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin on the falling edge of $\overline{\text{TxC}}$. The transmitter will begin transmission upon being enabled if $\overline{\text{CTS}}$ = 0. The TxD line will be held in the marking state immediately upon a master Reset or when Tx Enable/$\overline{\text{CTS}}$ off or TxEMPTY.

Transmitter Control

The transmitter Control manages all activities associated with the transmission of serial data. It accepts and issues signals both externally and internally to accomplish this function.

TxRDY (Transmitter Ready)

This output signals the CPU that the transmitter is ready to accept a data character. The TxRDY output pin can be used as an interrupt to the system, since it is masked by Tx Disabled, or, for Polled operation, the CPU can check TxRDY using a Status Read operation. TxRDY is automatically reset by the leading edge of $\overline{\text{WR}}$ when a data character is loaded from the CPU.

Note that when using the Polled operation, the TxRDY status bit is *not* masked by Tx Enabled, but will only indicate the Empty/Full Status of the Tx Data Input Register.

TxE (Transmitter Empty)

When the 8251A has no characters to transmit, the TxEMPTY output will go "high". It resets automatically upon receiving a character from the CPU. TxEMPTY can be used to indicate the end of a transmission mode, so that the CPU "knows" when to "turn the line around" in the half-duplexed operational mode. TxEMPTY is independent of the Tx Enable bit in the Command instruction.

In SYNChronous mode, a "high" on this output indicates that a character has not been loaded and the SYNC character or characters are about to be or are being transmitted automatically as "fillers". TxEMPTY does not go low when the SYNC characters are being shifted out.

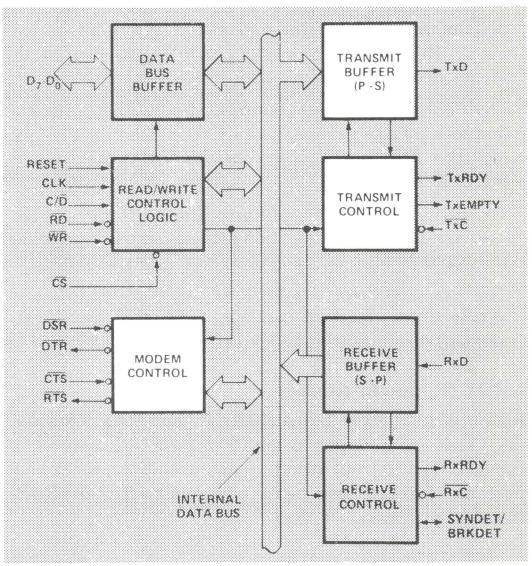


Figure 2. 8251A Block Diagram Showing Modem and Transmitter Buffer and Control Functions

$\overline{\text{TxC}}$ (Transmitter Clock)

The Transmitter Clock controls the rate at which the character is to be transmitted. In the Synchronous transmission mode, the Baud Rate (1x) is equal to the $\overline{\text{TxC}}$ frequency. In Asynchronous transmission mode the baud rate is a fraction of the actual $\overline{\text{TxC}}$ frequency. A portion of the mode instruction selects this factor; it can be 1, 1/16 or 1/64 the $\overline{\text{TxC}}$.

For Example:

If Baud Rate equals 110 Baud,
$\overline{\text{TxC}}$ equals 110 Hz (1x)
$\overline{\text{TxC}}$ equals 1.76 kHz (16x)
$\overline{\text{TxC}}$ equals 7.04 kHz (64x).

The falling edge of $\overline{\text{TxC}}$ shifts the serial data out of the 8251A.

Receiver Buffer

The Receiver accepts serial data, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and sends an "assembled" character to the CPU. Serial data is input to RxD pin, and is clocked in on the rising edge of $\overline{RxC}$.

Receiver Control

This functional block manages all receiver-related activities which consist of the following features:

The RxD initialization circuit prevents the 8251A from mistaking an unused input line for an active low data line in the "break condition". Before starting to receive serial characters on the RxD line, a valid "1" must first be detected after a chip master Reset. Once this has been determined, a search for a valid low (Start bit) is enabled. This feature is only active in the asynchronous mode, and is only done once for each master Reset.

The False Start bit detection circuit prevents false starts due to a transient noise spike by first detecting the falling edge and then strobing the nominal center of the Start bit (RxD = low).

The Parity Toggle F/F and Parity Error F/F circuits are used for parity error detection and set the corresponding status bit.

The Framing Error Flag F/F is set if the Stop bit is absent at the end of the data byte (asynchronous mode), and also sets the corresponding status bit.

RxRDY (Receiver Ready)

This output indicates that the 8251A contains a character that is ready to be input to the CPU. Rx RDY can be connected to the interrupt structure of the CPU or, for Polled operation, the CPU can check the condition of RxRDY using a Status Read operation.

Rx Enable off both masks and holds RxRDY in the Reset Condition. For Asynchronous mode, to set RxRDY, the Receiver must be Enabled to sense a Start Bit and a complete character must be assembled and transferred to the Data Output Register. For Synchronous mode, to set RxRDY, the Receiver must be enabled and a character must finish assembly and be transferred to the Data Output Register.

Failure to read the received character from the Rx Data Output Register prior to the assembly of the next Rx Data character will set overrun condition error and the previous character will be written over and lost. If the Rx Data is being read by the CPU when the internal transfer is occurring, overrun error will be set and the old character will be lost.

$\overline{RxC}$ (Receiver Clock)

The Receiver Clock controls the rate at which the character is to be received. In Synchronous Mode, the Baud Rate (1x) is equal to the actual frequency of $\overline{RxC}$. In Asynchronous Mode, the Baud Rate is a fraction of the actual $\overline{RxC}$ frequency. A portion of the mode instruction selects this factor; 1, 1/16 or 1/64 the $\overline{RxC}$.

For Example:

Baud Rate equals 300 Baud, if
$\overline{RxC}$ equals 300 Hz (1x)
$\overline{RxC}$ equals 4800 Hz (16x)
$\overline{RxC}$ equals 19.2 kHz (64x).

Baud Rate equals 2400 Baud, if
$\overline{RxC}$ equals 2400 Hz (1x)
$\overline{RxC}$ equals 38.4 kHz (16x)
$\overline{RxC}$ equals 153.6 kHz (64x).

Data is sampled into the 8251A on the rising edge of $\overline{RxC}$.

NOTE: In most communications systems, the 8251A will be handling both the transmission and reception operations of a single link. Consequently, the Receive and Transmit Baud Rates will be the same. Both $\overline{TxC}$ and $\overline{RxC}$ will require identical frequencies for this operation and can be tied together and connected to a single frequency source (Baud Rate Generator) to simplify the interface.

SYNDET (SYNC Detect)/BRKDET (Break Detect))

This pin is used in SYNChronous Mode for SYNDET and may be used as either input or output, programmable through the Control Word. It is reset to output mode low upon RESET. When used as an output (internal Sync mode), the SYNDET pin will go "high" to indicate that the 8251A has located the SYNC character in the Receive mode. If the 8251A is programmed to use double Sync characters (bisync), then SYNDET will go "high" in the middle of the last bit of the second Sync character. SYNDET is automatically reset upon a Status Read operation.

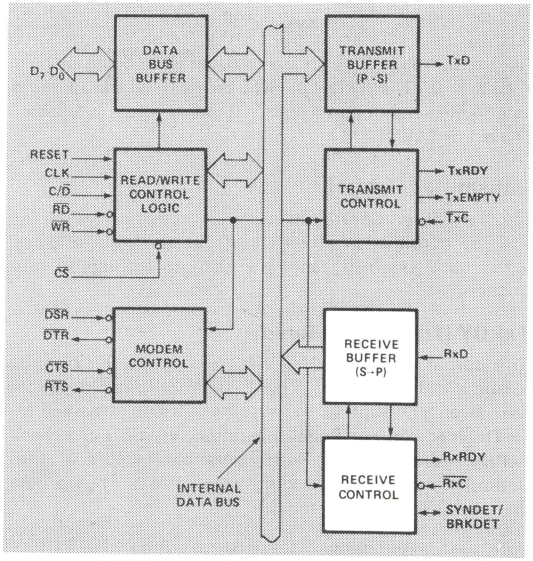


Figure 3. 8251A Block Diagram Showing Receiver Buffer and Control Functions

When used as an input (external SYNC detect mode), a positive going signal will cause the 8251A to start assembling data characters on the rising edge of the next $\overline{RxC}$. Once in SYNC, the "high" input signal can be removed. the period of $\overline{RxC}$. When External SYNC Detect is programmed, the Internal SYNC Detect is disabled.

BREAK DETECT (Async Mode Only)

This output will go high whenever an all zero word of the programmed length (including start bit, data bit, parity bit, and *one* stop bit) is received. Break Detect may also be read as a Status bit. It is reset only upon a master chip Reset or Rx Data returning to a "one" state.

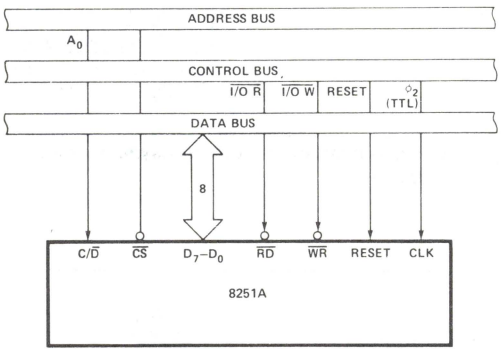


Figure 4. 8251A Interface to 8080 Standard System Bus

DETAILED OPERATION DESCRIPTION

General

The complete functional definition of the 8251A is programmed by the system's software. A set of control words must be sent out by the CPU to initialize the 8251A to support the desired communications format. These control words will program the: BAUD RATE, CHARACTER LENGTH, NUMBER OF STOP BITS, SYNCHRONOUS or ASYNCHRONOUS OPERATION, EVEN/ODD/OFF PARITY, etc. In the Synchronous Mode, options are also provided to select either internal or external character synchronization.

Once programmed, the 8251A is ready to perform its communication functions. The TxRDY output is raised "high" to signal the CPU that the 8251A is ready to receive a data character from the CPU. This output (TxRDY) is reset automatically when the CPU writes a character into the 8251A. On the other hand, the 8251A receives serial data from the MODEM or I/O device. Upon receiving an entire character, the RxRDY output is raised "high" to signal the CPU that the 8251A has a complete character ready for the CPU to fetch. RxRDY is reset automatically upon the CPU data read operation.

The 8251A cannot begin transmission until the Tx Enable (Transmitter Enable) bit is set in the Command Instruction and it has received a Clear To Send ($\overline{CTS}$) input. The TxD output will be held in the marking state upon Reset.

Programming the 8251A

Prior to starting data transmission or reception, the 8251A must be loaded with a set of control words generated by the CPU. These control signals define the complete functional definition of the 8251A and must immediately follow a Reset operation (internal or external).

The control words are split into two formats:

1. Mode Instruction
2. Command Instruction

Mode Instruction

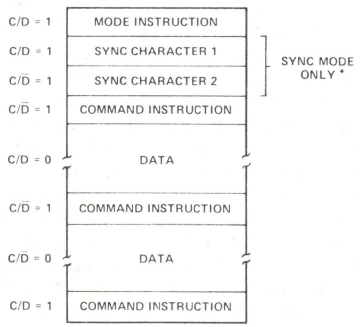
This format defines the general operational characteristics of the 8251A. It must follow a Reset operation (internal or external). Once the Mode Instruction has been written into the 8251A by the CPU, SYNC characters or Command Instructions may be inserted.

Command Instruction

This format defines a status word that is used to control the actual operation of the 8251A.

Both the Mode and Command Instructions must conform to a specified sequence for proper device operation. The Mode Instruction must be inserted immediately following a Reset operation, prior to using the 8251A for data communication.

All control words written into the 8251A after the Mode Instruction will load the Command Instruction. Command Instructions can be written into the 8251A at any time in the data block during the operation of the 8251A. To return to the Mode Instruction format, the master Reset bit in the Command Instruction word can be set to initiate an internal Reset operation which automatically places the 8251A back into the Mode Instruction format. Command Instructions must follow the Mode Instructions or Sync characters.



* The second SYNC character is skipped if MODE instruction has programmed the 8251A to single character Internal SYNC Mode. Both SYNC characters are skipped if MODE instruction has programmed the 8251A to ASYNC mode.

Figure 5. Typical Data Block

Mode Instruction Definition

The 8251A can be used for either Asynchronous or Synchronous data communication. To understand how the Mode Instruction defines the functional operation of the 8251A, the designer can best view the device as two separate components sharing the same package, one Asynchronous the other Synchronous. The format definition can be changed only after a master chip Reset. For explanation purposes the two formats will be isolated.

NOTE: When parity is enabled it is not considered as one of the data bits for the purpose of programming the word length. The actual parity bit received on the Rx Data line cannot be read on the Data Bus. In the case of a programmed character length of less than 8 bits, the least significant Data Bus bits will hold the data; unused bits are "don't care" when writing data to the 8251A, and will be "zeros" when reading the data from the 8251A.

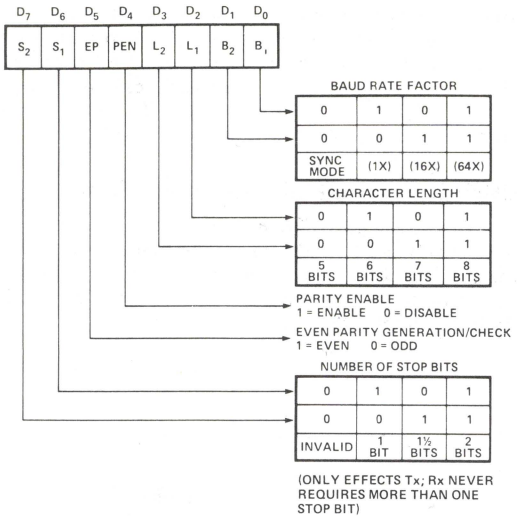


Figure 6. Mode Instruction Format, Asynchronous Mode

Asynchronous Mode (Transmission)

Whenever a data character is sent by the CPU the 8251A automatically adds a Start bit (low level) followed by the data bits (least significant bit first), and the programmed number of Stop bits to each character. Also, an even or odd Parity bit is inserted prior to the Stop bit(s), as defined by the Mode Instruction. The character is then transmitted as a serial data stream on the TxD output. The serial data is shifted out on the falling edge of $\overline{TxC}$ at a rate equal to 1, 1/16, or 1/64 that of the $\overline{TxC}$, as defined by the Mode Instruction. BREAK characters can be continuously sent to the TxD if commanded to do so.

When no data characters have been loaded into the 8251A the TxD output remains "high" (marking) unless a Break (continuously low) has been programmed.

Asynchronous Mode (Receive)

The RxD line is normally high. A falling edge on this line triggers the beginning of a START bit. The validity of this START bit is checked by again strobing this bit at its nominal center (16X or 64X mode only). If a low is detected again, it is a valid START bit, and the bit counter will start counting. The bit counter thus locates the center of the data bits, the parity bit (if it exists) and the stop bits. If parity error occurs, the parity error flag is set. Data and parity bits are sampled on the RxD pin with the rising edge of $\overline{RxC}$. If a low level is detected as the STOP bit, the Framing Error flag will be set. The STOP bit signals the end of a character. Note that the *receiver* requires only *one* stop bit, regardless of the number of stop bits programmed. This character is then loaded into the parallel I/O buffer of the 8251A. The RxRDY pin is raised to signal the CPU that a character is ready to be fetched. If a previous character has not been fetched by the CPU, the present character replaces it in the I/O buffer, and the OVERRUN Error flag is raised (thus the previous character is lost). All of the error flags can be reset by an Error Reset Instruction. The occurrence of any of these errors will not affect the operation of the 8251A.

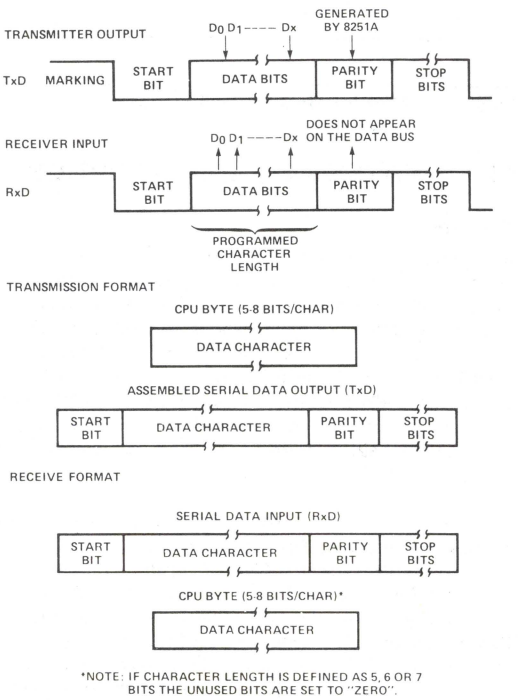
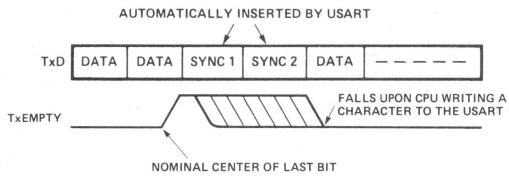


Figure 7. Asynchronous Mode

Synchronous Mode (Transmission)

The TxD output is continuously high until the CPU sends its first character to the 8251A which usually is a SYNC character. When the $\overline{CTS}$ line goes low, the first character is serially transmitted out. All characters are shifted out on the falling edge of $\overline{TxC}$. Data is shifted out at the same rate as the $\overline{TxC}$.

Once transmission has started, the data stream at the TxD output must continue at the $\overline{TxC}$ rate. If the CPU does not provide the 8251A with a data character before the 8251A Transmitter Buffers become empty, the SYNC characters (or character if in single SYNC character mode) will be automatically inserted in the TxD data stream. In this case, the TxEMPTY pin is raised high to signal that the 8251A is empty and SYNC characters are being sent out. TxEMPTY does not go low when the SYNC is being shifted out (see figure below). The TxEMPTY pin is internally reset by a data character being written into the 8251A.



Synchronous Mode (Receive)

In this mode, character synchronization can be internally or externally achieved. If the SYNC mode has been programmed, ENTER HUNT command should be included in the first command instruction word written. Data on the RxD pin is then sampled in on the rising edge of $\overline{RxC}$. The content of the Rx buffer is compared at every bit boundary with the first SYNC character until a match occurs. If the 8251A has been programmed for two SYNC characters, the subsequent received character is also compared; when both SYNC characters have been detected, the USART ends the HUNT mode and is in character synchronization. The SYNDET pin is then set high, and is reset automatically by a STATUS READ. If parity is programmed, SYNDET will not be set until the middle of the parity bit instead of the middle of the last data bit.

In the external SYNC mode, synchronization is achieved by applying a high level on the SYNDET pin, thus forcing the 8251A out of the HUNT mode. The high level can be removed after one $\overline{RxC}$ cycle. An ENTER HUNT command has no effect in the asynchronous mode of operation.

Parity error and overrun error are both checked in the same way as in the Asynchronous Rx mode. Parity is checked when not in Hunt, regardless of whether the Receiver is enabled or not.

The CPU can command the receiver to enter the HUNT mode if synchronization is lost. This will also set all the used character bits in the buffer to a "one", thus preventing a possible false SYNDET caused by data that happens to be in the Rx Buffer at ENTER HUNT time. Note that the SYNDET F/F is reset at each Status Read, regardless of whether internal or external SYNC has been programmed. This does not cause the 8251A to return to the HUNT mode. When in SYNC mode, but not in HUNT, Sync Detection is still functional, but only occurs at the "known" word boundaries. Thus, if one Status Read indicates SYNDET and a second Status Read also indicates SYNDET, then the programmed SYNDET characters have been received since the previous Status Read. (If double character sync has been programmed, then both sync characters have been contiguously received to gate a SYNDET indication.) When external SYNDET mode is selected, internal Sync Detect is disabled, and the SYNDET F/F may be set at any bit boundary.

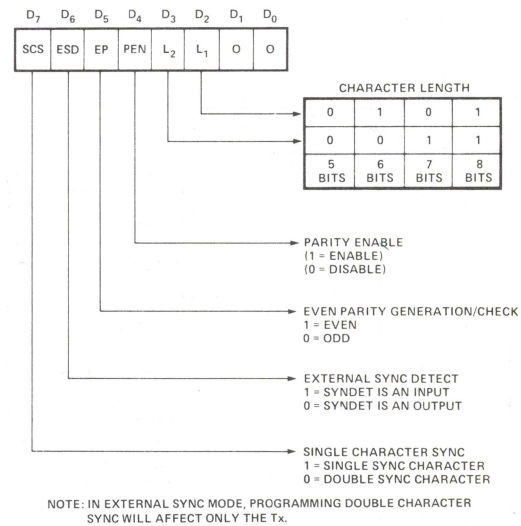


Figure 8. Mode Instruction Format

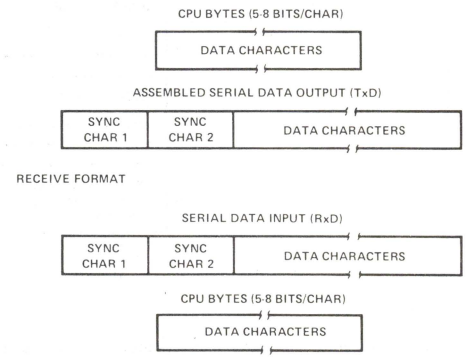
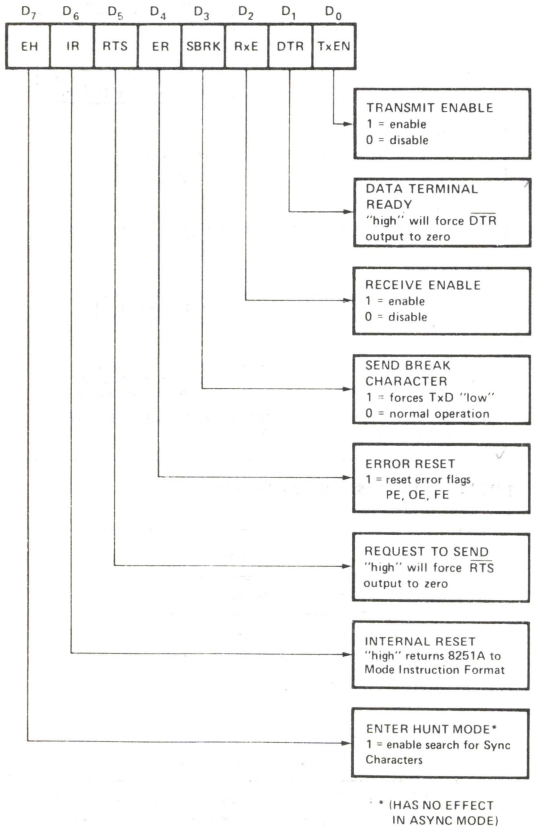


Figure 9. Data Format, Synchronous Mode

COMMAND INSTRUCTION DEFINITION

Once the functional definition of the 8251A has been programmed by the Mode Instruction and the Sync Characters are loaded (if in Sync Mode) then the device is ready to be used for data communication. The Command Instruction controls the actual operation of the selected format. Functions such as: Enable Transmit/Receive, Error Reset and Modem Controls are provided by the Command Instruction.

Once the Mode Instruction has been written into the 8251A and Sync characters inserted, if necessary, then all further "control writes" ($C/\overline{D}$ = 1) will load a Command Instruction. A Reset Operation (internal or external) will return the 8251A to the Mode Instruction format.



Note: Error Reset must be performed whenever RxEnable and Enter Hunt are programmed.

Figure 10. Command Instruction Format

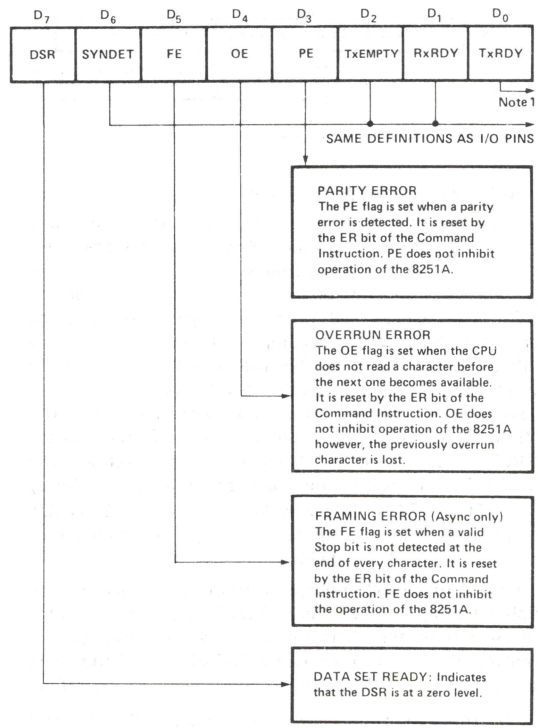
STATUS READ DEFINITION

In data communication systems it is often necessary to examine the "status" of the active device to ascertain if errors have occurred or other conditions that require the processor's attention. The 8251A has facilities that allow the programmer to "read" the status of the device at any time during the functional operation. (The status update is inhibited during status read).

A normal "read" command is issued by the CPU with $C/\overline{D}$ = 1 to accomplish this function.

Some of the bits in the Status Read Format have identical meanings to external output pins so that the 8251A can be used in a completely Polled environment or in an interrupt driven environment. TxRDY is an exception.

Note that status update can have a maximum delay of 28 clock periods from the actual event affecting the status.



Note 1: TxRDY status bit has different meanings from the TxRDY output pin. The former is not conditioned by $\overline{CTS}$ and TxEN; the latter is conditioned by both $\overline{CTS}$ and TxEN.

i.e. TxRDY status bit = DB Buffer Empty

TxRDY pin out = DB Buffer Empty · (CTS=0) · (TxEN=1)

Figure 11. Status Read Format

APPLICATIONS OF THE 8251A

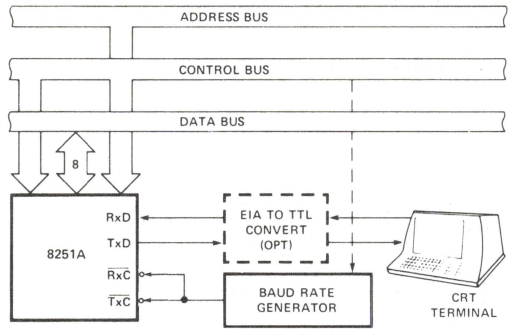


Figure 12. Asynchronous Serial Interface to CRT Terminal, DC—9600 Baud

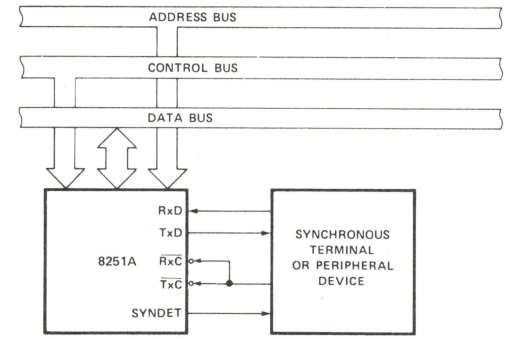


Figure 13. Synchronous Interface to Terminal or Peripheral Device

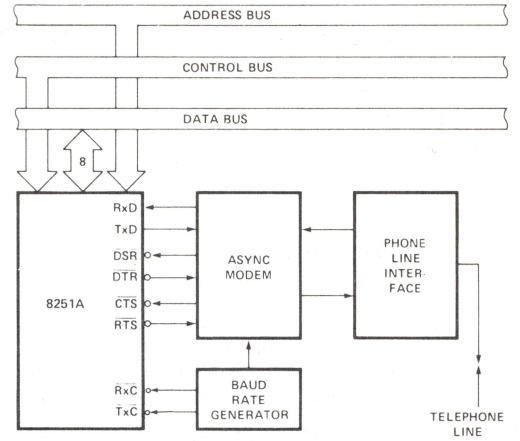


Figure 14. Asynchronous Interface to Telephone Lines

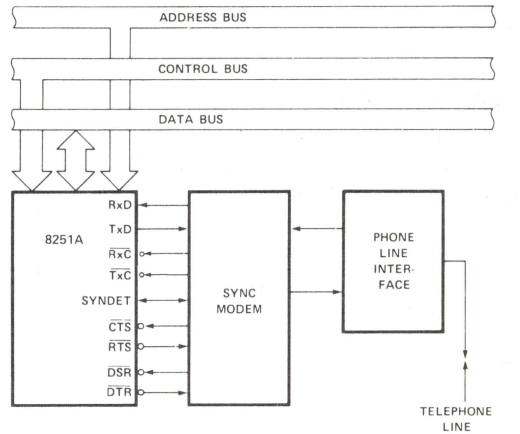


Figure 15. Synchronous Interface to Telephone Lines

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . 0°C to 70°C
Storage Temperature . . . . . –65°C to +150°C
Voltage On Any Pin
With Respect to Ground . . . . . –0.5V to +7V
Power Dissipation . . . . . 1 Watt

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = 0°C to 70°C; V_{CC} = 5.0V ±5%; GND = 0V

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	–0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = –400 μA
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = V_{CC} TO 0.45V
I_{IL}	Input Leakage		±10	μA	V_{IN} = V_{CC} TO 0.45V
I_{CC}	Power Supply Current		100	mA	All Outputs = High

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance		10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance		20	pF	Unmeasured pins returned to GND

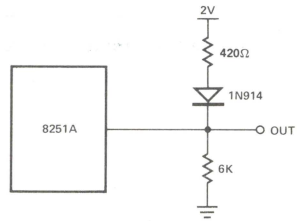


Figure 16. Test Load Circuit

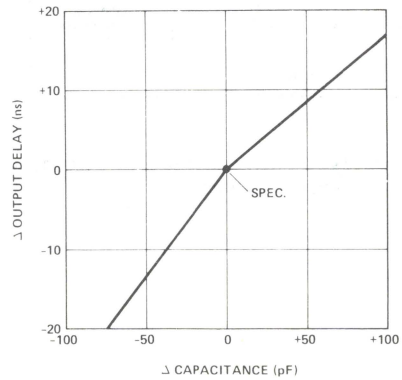


Figure 17. Typical Δ Output Delay vs. Δ Capacitance (pF)

A.C. CHARACTERISTICS

T_A = 0°C to 70°C; V_{CC} = 5.0V ±5%; GND = 0V

Bus Parameters (Note 1)

Read Cycle:

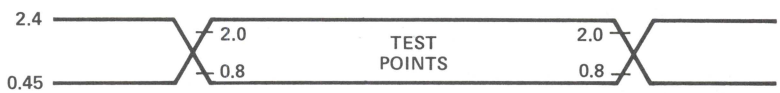
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
t_{AR}	Address Stable Before $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)	0		ns	Note 2
t_{RA}	Address Hold Time for $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)	0		ns	Note 2
t_{RR}	$\overline{READ}$ Pulse Width	250		ns	
t_{RD}	Data Delay from $\overline{READ}$		200	ns	3, C_L = 150 pF
t_{DF}	$\overline{READ}$ to Data Floating	10	100	ns	

Write Cycle:

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
t_{AW}	Address Stable Before $\overline{WRITE}$	0		ns	
t_{WA}	Address Hold Time for $\overline{WRITE}$	0		ns	
t_{WW}	$\overline{WRITE}$ Pulse Width	250		ns	
t_{DW}	Data Set Up Time for $\overline{WRITE}$	150		ns	
t_{WD}	Data Hold Time for $\overline{WRITE}$	0		ns	
t_{RV}	Recovery Time Between WRITES	6		t_{CY}	Note 4

NOTES:
1. AC timings measured V_{OH} = 2.0, V_{OL} = 0.8, and with load circuit of Figure 1.
2. Chip Select ($\overline{CS}$) and Command/Data (C/$\overline{D}$) are considered as Addresses.
3. Assumes that Address is valid before $\overline{R_D}\downarrow$.
4. This recovery time is for Mode Initialization only. Write Data is allowed only when TxRDY = 1. Recovery Time between Writes for Asynchronous Mode is 8 t_{CY} and for Synchronous Mode is 16 t_{CY}.

Input Waveforms for AC Tests



Other Timings:

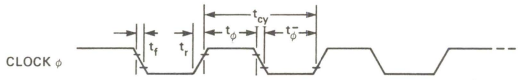
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
t_{CY}	Clock Period	320	1.35	μs	Notes 5, 6
t_{ϕ}	Clock High Pulse Width	120	t_{CY-90}	ns	
$t_{\overline{\phi}}$	Clock Low Pulse Width	90		ns	
t_R, t_F	Clock Rise and Fall Time	5	20	ns	
t_{DTx}	TxD Delay from Falling Edge of $\overline{TxC}$		1	μs	
t_{SRx}	Rx Data Set-Up Time to Sampling Pulse	2		μs	
t_{HRx}	Rx Data Hold Time to Sampling Pulse	2		μs	
f_{Tx}	Transmitter Input Clock Frequency				
	1x Baud Rate	DC	64	kHz	
	16x Baud Rate	DC	310	kHz	
	64x Baud Rate	DC	615	kHz	
t_{TPW}	Transmitter Input Clock Pulse Width				
	1x Baud Rate	12		t_{CY}	
	16x and 64x Baud Rate	1		t_{CY}	
t_{TPD}	Transmitter Input Clock Pulse Delay				
	1x Baud Rate	15		t_{CY}	
	16x and 64x Baud Rate	3		t_{CY}	
f_{Rx}	Receiver Input Clock Frequency				
	1x Baud Rate	DC	64	kHz	
	16x Baud Rate	DC	310	kHz	
	64x Baud Rate	DC	615	kHz	
t_{RPW}	Receiver Input Clock Pulse Width				
	1x Baud Rate	12		t_{CY}	
	16x and 64x Baud Rate	1		t_{CY}	
t_{RPD}	Receiver Input Clock Pulse Delay				
	1x Baud Rate	15		t_{CY}	
	16x and 64x Baud Rate	3		t_{CY}	
t_{TxRDY}	TxRDY Pin Delay from Center of last Bit		8	t_{CY}	Note 7
$t_{TxRDY\ CLEAR}$	TxRDY ↓ from Leading Edge of $\overline{WR}$		150	ns	Note 7
t_{RxRDY}	RxRDY Pin Delay from Center of last Bit		24	t_{CY}	Note 7
$t_{RxRDY\ CLEAR}$	RxRDY ↓ from Leading Edge of $\overline{RD}$		150	ns	Note 7
t_{IS}	Internal SYNDET Delay from Rising Edge of $\overline{RxC}$		24	t_{CY}	Note 7
t_{ES}	External SYNDET Set-Up Time Before Falling Edge of $\overline{RxC}$		16	t_{CY}	Note 7
$t_{TxEMPTY}$	TxEMPTY Delay from Center of Data Bit		20	t_{CY}	Note 7
t_{WC}	Control Delay from Rising Edge of WRITE (TxEn, $\overline{DTR}$, $\overline{RTS}$)		8	t_{CY}	Note 7
t_{CR}	Control to READ Set-Up Time ($\overline{DSR}$, $\overline{CTS}$)		20	t_{CY}	Note 7

MPU PERIPHERALS

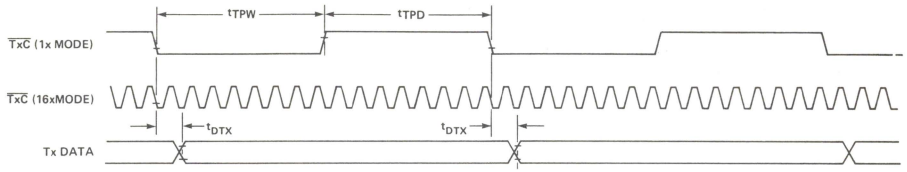
5. The TxC and RxC frequencies have the following limitations with respect to CLK.
   For 1x Baud Rate, f_{Tx} or $f_{Rx} \leq 1/(30\ t_{CY})$
   For 16x and 64x Baud Rate, f_{Tx} or $f_{Rx} \leq 1/(4.5\ t_{CY})$
6. Reset Pulse Width = 6 t_{CY} minimum; System Clock must be running during Reset.
7. Status update can have a maximum delay of 28 clock periods from the event affecting the status.

WAVEFORMS

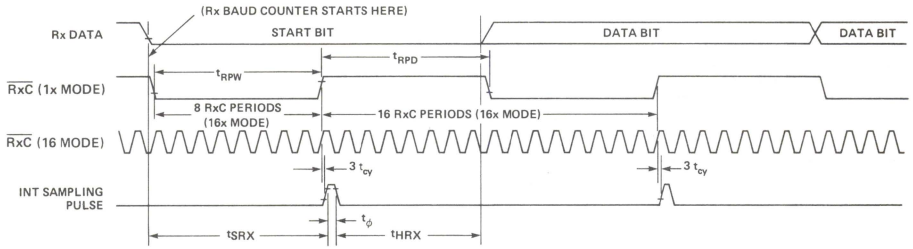
System Clock Input



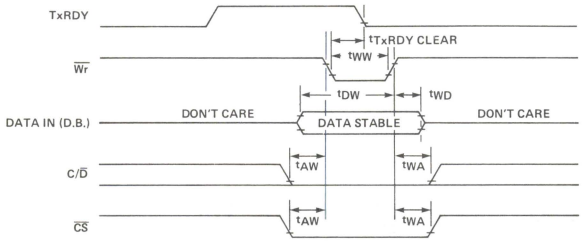
Transmitter Clock & Data



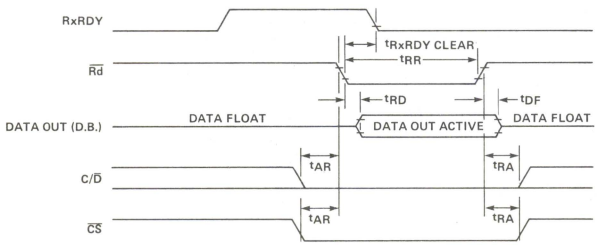
Receiver Clock & Data



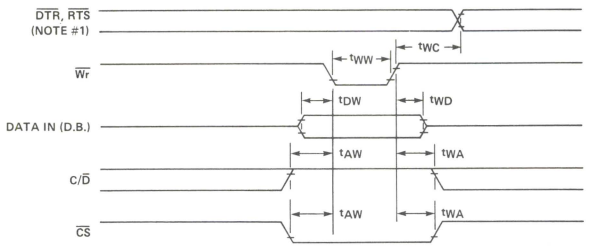
Write Data Cycle (CPU → USART)



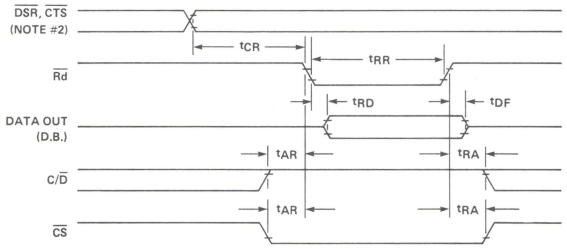
Read Data Cycle (CPU ← USART)



Write Control or Output Port Cycle (CPU → USART)

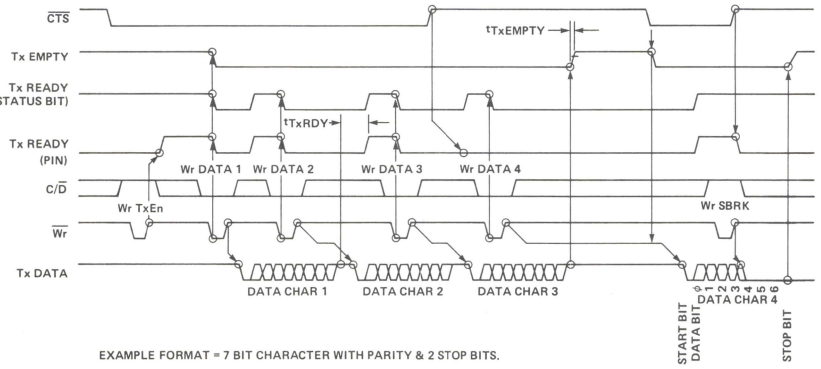


Read Control or Input Port (CPU ← USART)



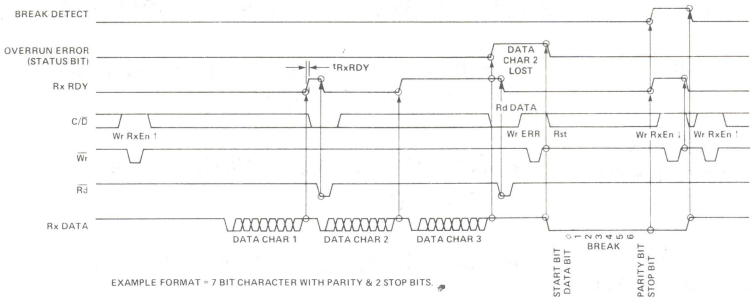
NOTE #1: T_{WC} INCLUDES THE RESPONSE TIMING OF A CONTROL BYTE.
NOTE #2: T_{CR} INCLUDES THE EFFECT OF CTS ON THE TxENBL CIRCUITRY.

Transmitter Control & Flag Timing (ASYNC Mode)

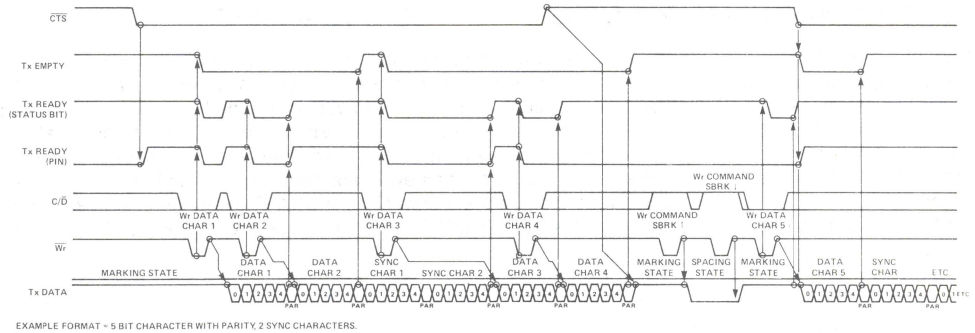


EXAMPLE FORMAT = 7 BIT CHARACTER WITH PARITY & 2 STOP BITS.

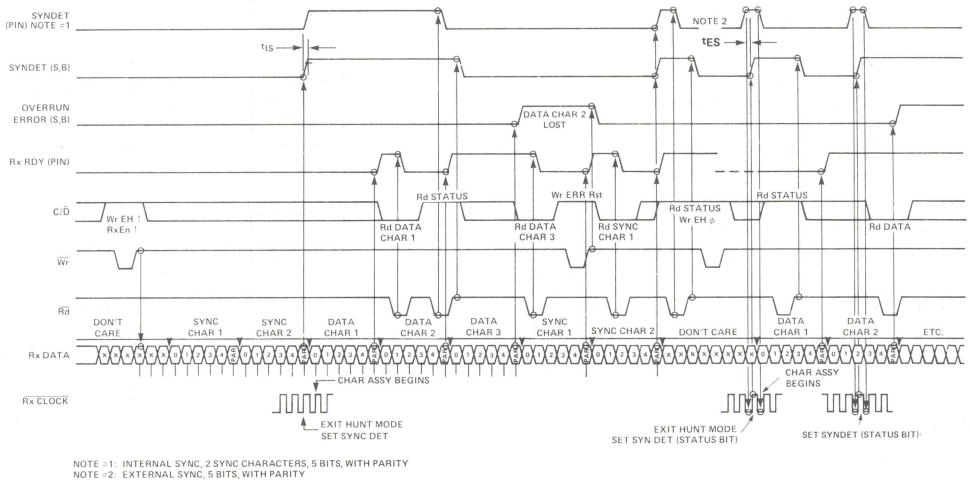
Receiver Control & Flag Timing (ASYNC Mode)



Transmitter Control & Flag Timing (SYNC Mode)



Receiver Control & Flag Timing (SYNC Mode)



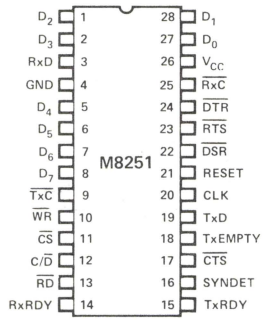
NOTE =1: INTERNAL SYNC, 2 SYNC CHARACTERS, 5 BITS, WITH PARITY
NOTE =2: EXTERNAL SYNC, 5 BITS, WITH PARITY

M8251
PROGRAMMABLE COMMUNICATION INTERFACE

- **Synchronous and Asynchronous Operation**
- **Synchronous — 5 8-Bit Characters; Internal or External Character Synchronization; Automatic Sync Insertion**
- **Asynchronous — 5 8-Bit Characters; Clock Rate — 1, 16, or 64 Times Baud Rate; Break Character Generation; 1, 1½, or 2-Stop Bits; False Start Bit Detection**
- **Baud Rate — DC to 56K Baud (Sync Mode), DC to 8.1K Baud (Async Mode)**
- **Full Duplex, Double Buffered Transmitter and Receiver**
- **Error Detection — Parity, Overrun, and Framing**
- **Fully Compatible with 8080 CPU**
- **All Inputs and Outputs TTL Compatible**
- **Full Military Temperature Range −55°C to +125°C**

The Intel® M8251 is a universal synchronous/asynchronous receiver/transmitter (USART) chip designed for data communications in microcomputer systems. The USART is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmissioin technique presently in use (including IBM "bi-sync"). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time. These include data transmission errors and control signals such as SYNDET, TxEMPT. The chip is constructed using N-channel silicon gate technology.

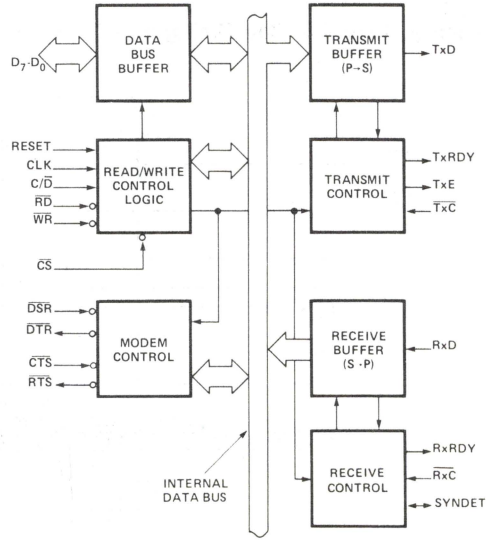
PIN CONFIGURATION



Pin Name	Pin Function
D_7-D_0	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
RD	Read Data Command
WR	Write Data or Control Command
CS	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
TxC	Transmitter Clock
TxD	Transmitter Data
RxC	Receiver Clock
RxD	Receiver Data
RxRDY	Receiver Ready (has character for 8080)
TxRDY	Transmitter Ready (ready for char. from 8080)

Pin Name	Pin Function
DSR	Data Set Ready
DTR	Data Terminal Ready
SYNDET	Sync Detect
RTS	Request to Send Data
CTS	Clear to Send Data
TxE	Transmitter Empty
V_{CC}	+5 Volt Supply
GND	Ground

BLOCK DIAGRAM



MPU PERIPHERALS

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . .–65°C to +150°C
Voltage On Any Pin
With Respect to GND . . . . . -0.5V to +7V
Power Dissipation . . . . . 1 Watt

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS*

T_A = -55°C to +125°C; V_{CC} = 5.0V ±10%; GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage					
V_{IH}	Input High Voltage					
V_{OL}	Output Low Voltage					
V_{OH}	Output High Voltage					
I_{DL}	Data Bus Leakage					
I_{LI}	Input Load Current					
I_{CC}	Power Supply Current					

Note: Military specifications have not yet been established.

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND.

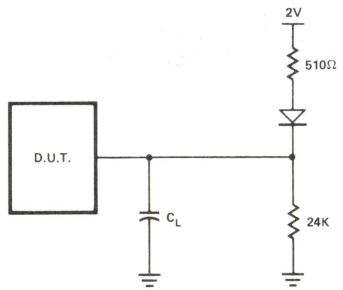


Figure 1. Test Load Circuit

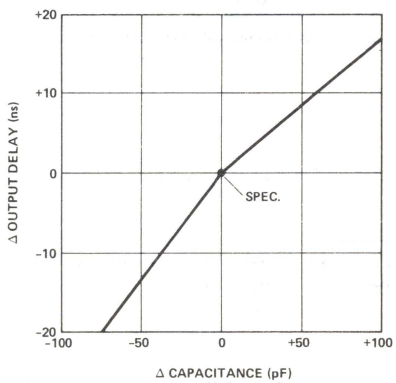


Figure 2. Typical Δ Output Delay vs. Δ Capacitance (dB)

A.C. CHARACTERISTICS*[2]

T_A = -55°C to +125°C; V_{CC} = 5.0V ±10%; GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{CY}	Clock Period					
$t_{\phi W}$	Clock Pulse Width					
t_R,t_F	Clock Rise and Fall Time					
t_{WR}	$\overline{WRITE}$ Pulse Width					
t_{DS}	Data Set-Up Time for $\overline{WRITE}$					
t_{DH}	Data Hold Time for $\overline{WRITE}$					
t_{AW}	Address Stable before $\overline{WRITE}$					
t_{WA}	Address Hold Time for $\overline{WRITE}$					
t_{RD}	READ Pulse Width					
t_{DD}	Data Delay from $\overline{READ}$					
t_{DF}	$\overline{READ}$ to Data Floating [3]					
t_{AR}	Address (CE, C/$\overline{D}$) Stable before $\overline{READ}$					
t_{RA}	Address (CE, C/$\overline{D}$) Hold Time for $\overline{READ}$					
t_{DTx}	TxD Delay from Falling Edge of TxC					
t_{SRx}	Rx Data Set-Up Time to Sampling Pulse					
t_{HRx}	Rx Data Hold Time to Sampling Pulse					
f_{Tx} [1]	Transmitter Clock Frequency 1X Baud Rate 16X and 64X Baud Rate					
f_{Rx} [1]	Receiver Clock Frequency 1X Baud Rate 16X and 64X Baud Rate					
t_{Tx}	TxRDY Delay from Center of Data Bit					
t_{Rx}	RxRDY Delay from Center of Data Bit					
t_{IS}	Internal Syndet Delay from Center of Data Bit					
t_{ES}	External Syndet Set-Up Time before Falling Edge of RxC					

*Military specifications have not yet been established.

Note 1: The TxC and RxC frequencies have the following limitation with respect to CLK.
For ASYNC Mode, t_{Tx} or $t_{Rx} \geq 4.5\ t_{CY}$
For SYNC Mode, t_{Tx} or $t_{Rx} \geq 30\ t_{CY}$
2. AC timings are measured at V_{OH} = 2.0V, V_{OL} = 0.8V, and load circuit of Figure 1.
3. Float timings are measured at V_{OH} = 2.48V, V_{OL} = 2.08V

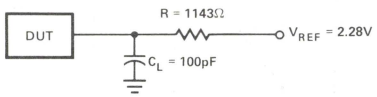


Figure 3. Test Load Circuit

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

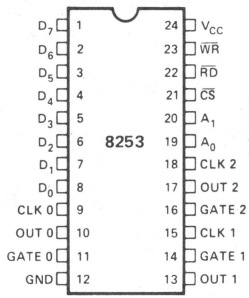
8253/8253-5
PROGRAMMABLE INTERVAL TIMER

- **MCS—85™ Compatible 8253-5**
- **3 Independent 16-Bit Counters**
- **DC to 2 MHz**
- **Programmable Counter Modes**
- **Count Binary or BCD**
- **Single +5V Supply**
- **24-Pin Dual In-Line Package**

The Intel® 8253 is a programmable counter/timer chip designed for use as an Intel microcomputer peripheral. It uses nMOS technology with a single +5V supply and is packaged in a 24-pin plastic DIP.

It is organized as 3 independent 16-bit counters, each with a count rate of up to 2 MHz. All modes of operation are software programmable.

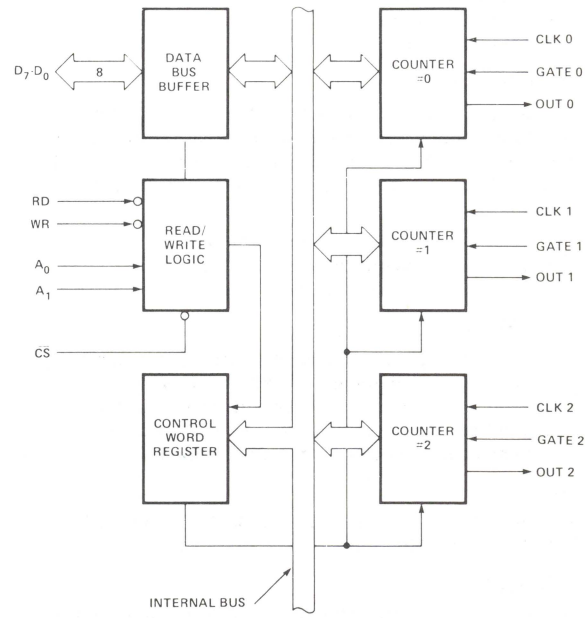
PIN CONFIGURATION



PIN NAMES

D_7-D_0	DATA BUS (8-BIT)
CLK N	COUNTER CLOCK INPUTS
GATE N	COUNTER GATE INPUTS
OUT N	COUNTER OUTPUTS
$\overline{RD}$	READ COUNTER
$\overline{WR}$	WRITE COMMAND OR DATA
$\overline{CS}$	CHIP SELECT
A_0-A_1	COUNTER SELECT
V_{CC}	+5 VOLTS
GND	GROUND

BLOCK DIAGRAM



MPU PERIPHERALS

FUNCTIONAL DESCRIPTION

General

The 8253 is a programmable interval timer/counter specifically designed for use with the Intel™ Microcomputer systems. Its function is that of a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.

The 8253 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in systems software, the programmer configures the 8253 to match his requirements, initializes one of the counters of the 8253 with the desired quantity, then upon command the 8253 will count out the delay and interrupt the CPU when it has completed its tasks. It is easy to see that the software overhead is minimal and that multiple delays can easily be maintained by assignment of priority levels.

Other counter/timer functions that are non-delay in nature but also common to most microcomputers can be implemented with the 8253.

- Programmable Rate Generator
- Event Counter
- Binary Rate Multiplier
- Real Time Clock
- Digital One-Shot
- Complex Motor Controller

Data Bus Buffer

This 3-state, bi-directional, 8-bit buffer is used to interface the 8253 to the system data bus. Data is transmitted or received by the buffer upon execution of INput or OUTput CPU instructions. The Data Bus Buffer has three basic functions.

1. Programming the MODES of the 8253.
2. Loading the count registers.
3. Reading the count values.

Read/Write Logic

The Read/Write Logic accepts inputs from the system bus and in turn generates control signals for overall device operation. It is enabled or disabled by CS so that no operation can occur to change the function unless the device has been selected by the system logic.

$\overline{RD}$ (Read)

A "low" on this input informs the 8253 that the CPU is inputting data in the form of a counters value.

$\overline{WR}$ (Write)

A "low" on this input informs the 8253 that the CPU is outputting data in the form of mode information or loading counters.

A0, A1

These inputs are normally connected to the address bus. Their function is to select one of the three counters to be operated on and to address the control word register for mode selection.

$\overline{CS}$ (Chip Select)

A "low" on this input enables the 8253. No reading or writing will occur unless the device is selected. The $\overline{CS}$ input has no effect upon the actual operation of the counters.

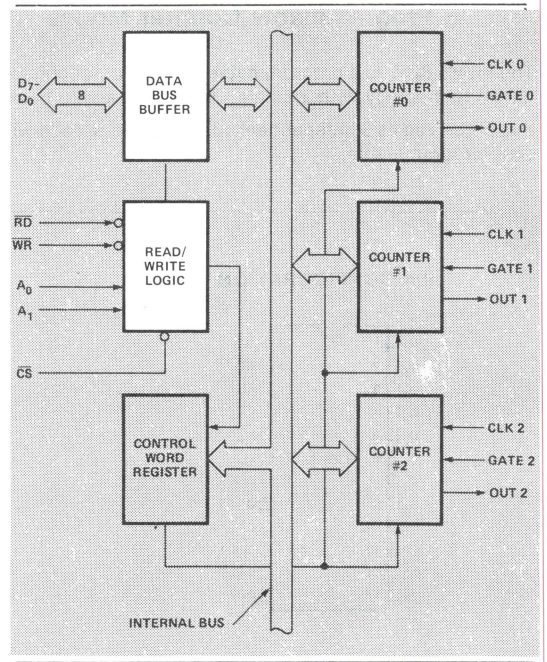


Figure 1. Block Diagram Showing Data Bus Buffer and Read/Write Logic Functions

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	
0	1	0	0	0	Load Counter No. 0
0	1	0	0	1	Load Counter No. 1
0	1	0	1	0	Load Counter No. 2
0	1	0	1	1	Write Mode Word
0	0	1	0	0	Read Counter No. 0
0	0	1	0	1	Read Counter No. 1
0	0	1	1	0	Read Counter No. 2
0	0	1	1	1	No-Operation 3-State
1	X	X	X	X	Disable 3-State
0	1	1	X	X	No-Operation 3-State

Control Word Register

The Control Word Register is selected when A0, A1 are 11. It then accepts information from the data bus buffer and stores it in a register. The information stored in this register controls the operational MODE of each counter, selection of binary or BCD counting and the loading of each count register.

The Control Word Register can only be written into; no read operation of its contents is available.

Counter #0, Counter #1, Counter #2

These three functional blocks are identical in operation so only a single Counter will be described. Each Counter consists of a single, 16-bit, pre-settable, DOWN counter. The counter can operate in either binary or BCD and its input, gate and output are configured by the selection of MODES stored in the Control Word Register.

The counters are fully independent and each can have separate Mode configuration and counting operation, binary or BCD. Also, there are special features in the control word that handle the loading of the count value so that software overhead can be minimized for these functions.

The reading of the contents of each counter is available to the programmer with simple READ operations for event counting applications and special commands and logic are included in the 8253 so that the contents of each counter can be read "on the fly" without having to inhibit the clock input.

8253 SYSTEM INTERFACE

The 8253 is a component of the Intel™ Microcomputer Systems and interfaces in the same manner as all other peripherals of the family. It is treated by the systems software as an array of peripheral I/O ports; three are counters and the fourth is a control register for MODE programming.

Basically, the select inputs A0, A1 connect to the A0, A1 address bus signals of the CPU. The $\overline{CS}$ can be derived directly from the address bus using a linear select method. Or it can be connected to the output of a decoder, such as an Intel® 8205 for larger systems.

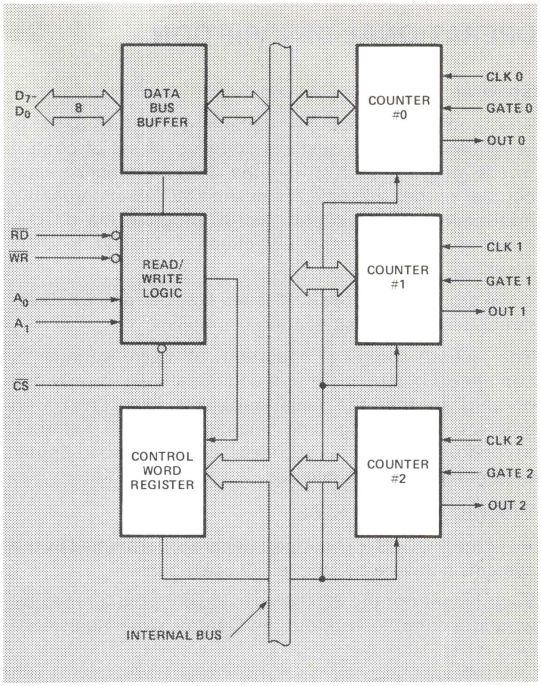


Figure 2. Block Diagram Showing Control Word Register and Counter Functions

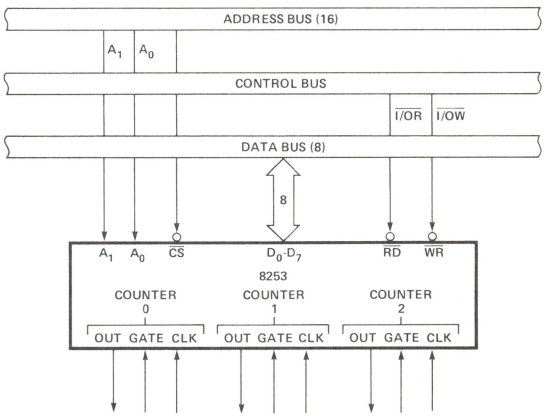


Figure 3. 8253 System Interface

OPERATIONAL DESCRIPTION

General

The complete functional definition of the 8253 is programmed by the systems software. A set of control words must be sent out by the CPU to initialize each counter of the 8253 with the desired MODE and quantity information. These control words program the MODE, Loading sequence and selection of binary or BCD counting.

Once programmed, the 8253 is ready to perform whatever timing tasks it is assigned to accomplish.

The actual counting operation of each counter is completely independent and additional logic is provided on-chip so that the usual problems associated with efficient monitoring and management of external, asynchronous events or rates to the microcomputer system have been eliminated.

Programming the 8253

All of the MODES for each counter are programmed by the systems software by simple I/O operations.

Each counter of the 8253 is individually programmed by writing a control word into the Control Word Register. (A0, A1 = 11)

Control Word Format

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

Definition of Control

SC — Select Counter:

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Illegal

RL — Read/Load:

RL1	RL0	
0	0	Counter Latching operation (see READ/WRITE Procedure Section)
1	0	Read/Load most significant byte only.
0	1	Read/Load least significant byte only.
1	1	Read/Load least significant byte first, then most significant byte.

M — MODE:

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD:

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

MODE Definition

MODE: Interrupt on Terminal Count. The output will be initially low after the mode set operation. After the count is loaded into the selected count register, the output will remain low and the counter will count. When terminal count is reached the output will go high and remain high until the selected count register is reloaded with the mode or a new count is loaded.

Reloading a counter register during counting results in the following:

(1) Load 1st byte stops the current counting.

(2) Load 2nd byte starts the new count.

MODE 1: Programmable One-Shot. The output will go low on the count following the rising edge of the gate input.

The output will go high on the terminal count. If a new count value is loaded while the output is low it will not affect the duration of the one-shot pulse until the succeeding trigger. The current count can be read at any time without affecting the one-shot pulse.

The one-shot is retriggerable, hence the output will remain low for the full count after any rising edge of the gate input.

MODE 2: Rate Generator. Divide by N counter. The output will be low for one period of the input clock. The period from one output pulse to the next equals the number of input counts in the count register. If the count register is reloaded between output pulses the present period will not be affected, but the subsequent period will reflect the new value.

The gate input, when low, will force the output high. When the gate input goes high, the counter will start from the initial count. Thus, the gate input can be used to synchronize the counter.

When this mode is set, the output will remain high until after the count register is loaded. The output then can also be synchronized by software.

MODE 3: Square Wave Rate Generator. Similar to MODE 2 except that the output will remain high until one half the count has been completed (for even numbers) and go low for the other half of the count. If the count is odd, the output will be high for (N + 1)/2 counts and low for (N – 1)/2 counts.

If the counter register is reloaded with a new value during counting, this new value will be reflected immediately after after the output transition of the current count.

MODE 4: Software Triggered Strobe. After the mode is set, the output will be high. When the count is loaded, the counter will begin counting. On terminal count, the output will go low for one input clock period, then will go high again.

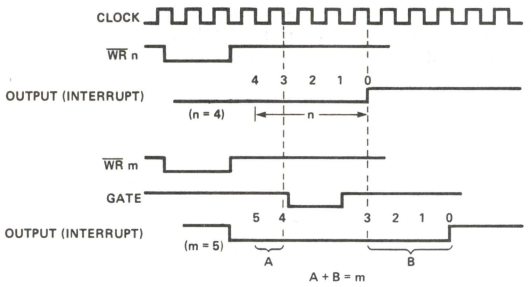
If the count register is reloaded between output pulses the present period will not be affected, but the subsequent period will reflect the new value. The count will be inhibited while the gate input is low. Reloading the counter register will restart counting beginning with the new number.

MODE 5: Hardware Triggered Strobe. The counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable. The output will not go low until the full count after the rising edge of any trigger.

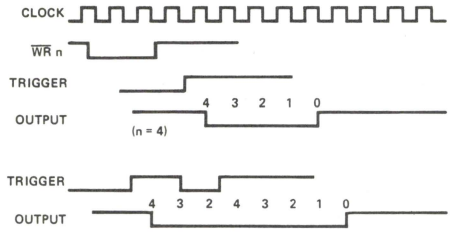
Modes \ Signal Status	Low Or Going Low	Rising	High
0	Disables counting	——	Enables counting
1	——	1) Initiates counting 2) Resets output after next clock	——
2	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
3	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
4	Disables counting	——	Enables counting
5	——	Initiates counting	——

Figure 4. Gate Pin Operations Summary

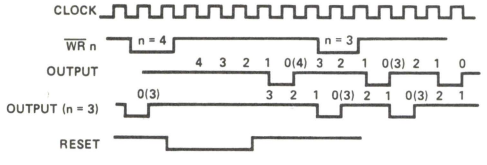
MODE 0



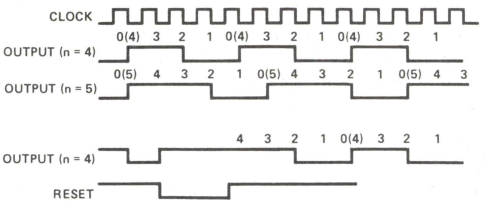
MODE 1



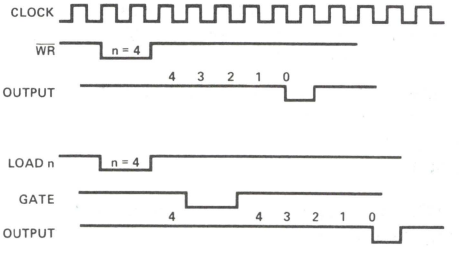
MODE 2



MODE 3



MODE 4



MODE 5

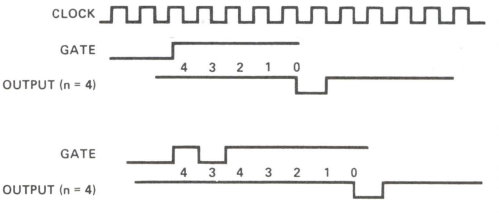


Figure 5. 8253 Timing Diagrams

8253 READ/WRITE PROCEDURE

Write Operations

The systems software must program each counter of the 8253 with the mode and quantity desired. The programmer must write out to the 8253 a MODE control word and the programmed number of count register bytes (1 or 2) prior to actually using the selected counter.

The actual order of the programming is quite flexible. Writing out of the MODE control word can be in any sequence of counter selection, e.g., counter #0 does not have to be first or counter #2 last. Each counter's MODE control word register has a separate address so that its loading is completely sequence independent. (SC0, SC1)

The loading of the Count Register with the actual count value, however, must be done in exactly the sequence programmed in the MODE control word (RL0, RL1). This loading of the counter's count register is still sequence independent like the MODE control word loading, but when a selected count register is to be loaded it must be loaded with the number of bytes programmed in the MODE control word (RL0, RL1). The one or two bytes to be loaded in the count register do not have to follow the associated MODE control word. They can be programmed at any time following the MODE control word loading as long as the correct number of bytes is loaded in order.

All counters are down counters. Thus, the value loaded into the count register will actually be decremented. Loading all zeroes into a count register will result in the maximum count (2^{16} for Binary or 10^4 for BCD). In MODE 0 the new count will not restart until the load has been completed. It will accept one of two bytes depending on how the MODE control words (RL0, RL1) are programmed. Then proceed with the restart operation.

	MODE Control Word Counter n
LSB	Count Register byte Counter n
MSB	Count Register byte Counter n

Note: Format shown is a simple example of loading the 8253 and does not imply that it is the only format that can be used.

Figure 6. Programming Format

			A1	A0
No. 1		MODE Control Word Counter 0	1	1
No. 2		MODE Control Word Counter 1	1	1
No. 3		MODE Control Word Counter 2	1	1
No. 4	LSB	Count Register Byte Counter 1	0	1
No. 5	MSB	Count Register Byte Counter 1	0	1
No. 6	LSB	Count Register Byte Counter 2	1	0
No. 7	MSB	Count Register Byte Counter 2	1	0
No. 8	LSB	Count Register Byte Counter 0	0	0
No. 9	MSB	Count Register Byte Counter 0	0	0

Note: The exclusive addresses of each counter's count register make the task of programming the 8253 a very simple matter, and maximum effective use of the device will result if this feature is fully utilized.

Figure 7. Alternate Programming Formats

Read Operations

In most counter applications it becomes necessary to read the value of the count in progress and make a computational decision based on this quantity. Event counters are probably the most common application that uses this function. The 8253 contains logic that will allow the programmer to easily read the contents of any of the three counters without disturbing the actual count in progress.

There are two methods that the programmer can use to read the value of the counters. The first method involves the use of simple I/O read operations of the selected counter. By controlling the A0, A1 inputs to the 8253 the programmer can select the counter to be read (remember that no read operation of the mode register is allowed A0, A1-11). The only requirement with this method is that in order to assure a stable count reading the actual operation of the selected counter must be inhibited either by controlling the Gate input or by external logic that inhibits the clock input. The contents of the counter selected will be available as follows:

first I/O Read contains the least significant byte (LSB).

second I/O Read contains the most significant byte (MSB).

Due to the internal logic of the 8253 it is absolutely necessary to complete the entire reading procedure. If two bytes are programmed to be read then two bytes must be read before any loading WR command can be sent to the same counter.

Read Operation Chart

A1	A0	RD	
0	0	0	Read Counter No. 0
0	1	0	Read Counter No. 1
1	0	0	Read Counter No. 2
1	1	0	Illegal

Reading While Counting

In order for the programmer to read the contents of any counter without effecting or disturbing the counting operation the 8253 has special internal logic that can be accessed using simple WR commands to the MODE register. Basically, when the programmer wishes to read the contents of a selected counter "on the fly" he loads the MODE register with a special code which latches the present count value into a storage register so that its contents contain an accurate, stable quantity. The programmer then issues a normal read command to the selected counter and the contents of the latched register is available.

MODE Register for Latching Count

A0, A1 = 11

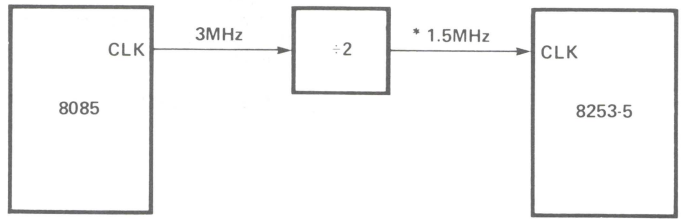
D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	0	0	X	X	X	X

SC1,SC0 — specify counter to be latched.

D5,D4 — 00 designates counter latching operation.

X — don't care.

The same limitation applies to this mode of reading the counter as the previous method. That is, it is mandatory to complete the entire read operation as programmed.



*If an 8085 clock output is to drive an 8253-5 clock input, it must be reduced to 2 MHz or less.

Figure 8. MCS-85™ Clock Interface*

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0° C to 70° C
Storage Temperature ..... −65° C to +150° C
Voltage On Any Pin
With Respect to Ground ..... −0.5 V to +7 V
Power Dissipation ..... 1 Watt

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ±5%)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.2	V_{CC}+.5V	V	
V_{OL}	Output Low Voltage		0.45	V	Note 1
V_{OH}	Output High Voltage	2.4		V	Note 2
I_{IL}	Input Load Current		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = V_{CC} to 0V
I_{CC}	V_{CC} Supply Current		140	mA	

Note 1: 8253, I_{OL} = 1.6 mA; 8253-5, I_{OL} = 2.2 mA.
Note 2: 8253, I_{OH} = −150 μA; 8253-5, I_{OH} = −400 μA.

CAPACITANCE T_A = 25°C; V_{CC} = GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	fc = 1 MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to V_{SS}

A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$; $V_{CC} = 5.0V \pm 5\%$; GND = 0V

Bus Parameters (Note 1)

Read Cycle:

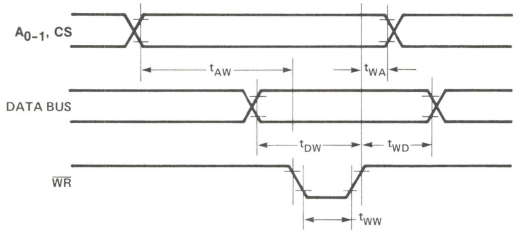
SYMBOL	PARAMETER	8253 MIN.	8253 MAX.	8253-5 MIN.	8253-5 MAX.	UNIT
t_{AR}	Address Stable Before $\overline{READ}$	50		50		ns
t_{RA}	Address Hold Time for $\overline{READ}$	5		5		ns
t_{RR}	$\overline{READ}$ Pulse Width	400		300		ns
t_{RD}	Data Delay From $\overline{READ}$[2]		300		200	ns
t_{DF}	$\overline{READ}$ to Data Floating	25	125	25	100	ns

Write Cycle:

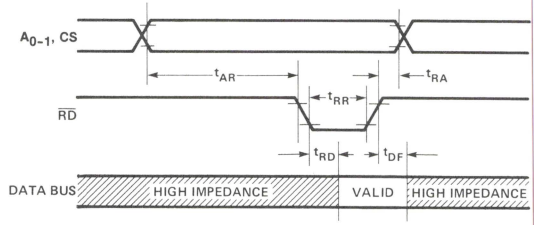
SYMBOL	PARAMETER	8253 MIN.	8253 MAX.	8253-5 MIN.	8253-5 MAX.	UNIT
t_{AW}	Address Stable Before $\overline{WRITE}$	50		50		ns
t_{WA}	Address Hold Time for $\overline{WRITE}$	30		30		ns
t_{WW}	$\overline{WRITE}$ Pulse Width	400		300		ns
t_{DW}	Data Set Up Time for $\overline{WRITE}$	300		250		ns
t_{WD}	Data Hold Time for $\overline{WRITE}$	40		30		ns
t_{RV}	Recovery Time Between $\overline{WRITES}$	1		1		μs

Notes: 1. AC timings measured at $V_{OH} = 2.2$, $V_{OL} = 0.8$
2. Test Conditions: 8253, $C_L = 100pF$; 8253-5: $C_L = 150pF$.

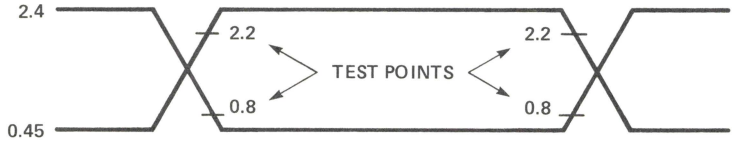
Write Timing:



Read Timing:



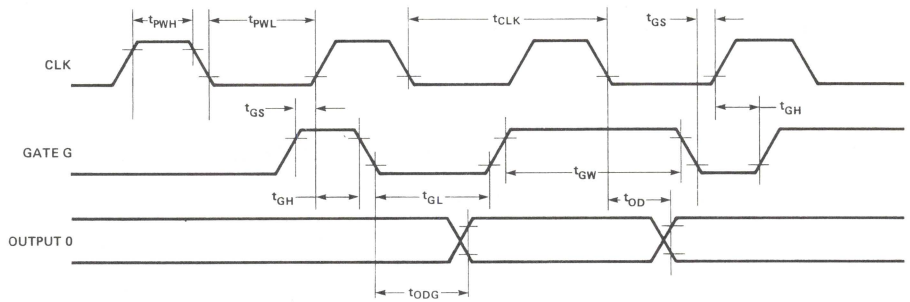
Input Waveforms for A.C. Tests:



Clock and Gate Timing:

SYMBOL	PARAMETER	8253		8253-5		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{CLK}	Clock Period	380	dc	380	dc	ns
t_{PWH}	High Pulse Width	230		230		ns
t_{PWL}	Low Pulse Width	150		150		ns
t_{GW}	Gate Width High	150		150		ns
t_{GL}	Gate Width Low	100		100		ns
t_{GS}	Gate Set Up Time to CLK↑	100		100		ns
t_{GH}	Gate Hold Time After CLK↑	50		50		ns
t_{OD}	Output Delay From CLK↓[1]		400		400	ns
t_{ODG}	Output Delay From Gate↓[1]		300		300	ns

Note 1: Test Conditions: 8253: C_L = 100pF; 8253-5: C_L = 150pF.



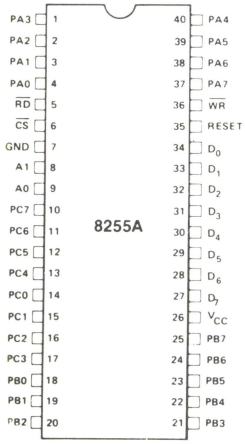
PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

8255A/8255A-5
PROGRAMMABLE PERIPHERAL INTERFACE

- MCS-85™ Compatible 8255A-5
- 24 Programmable I/O Pins
- Completely TTL Compatible
- Fully Compatible with Intel® Microprocessor Families
- Improved Timing Characteristics
- Direct Bit Set/Reset Capability Easing Control Application Interface
- 40-Pin Dual In-Line Package
- Reduces System Package Count
- Improved DC Driving Capability

The Intel® 8255A is a general purpose programmable I/O device designed for use with Intel® microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.

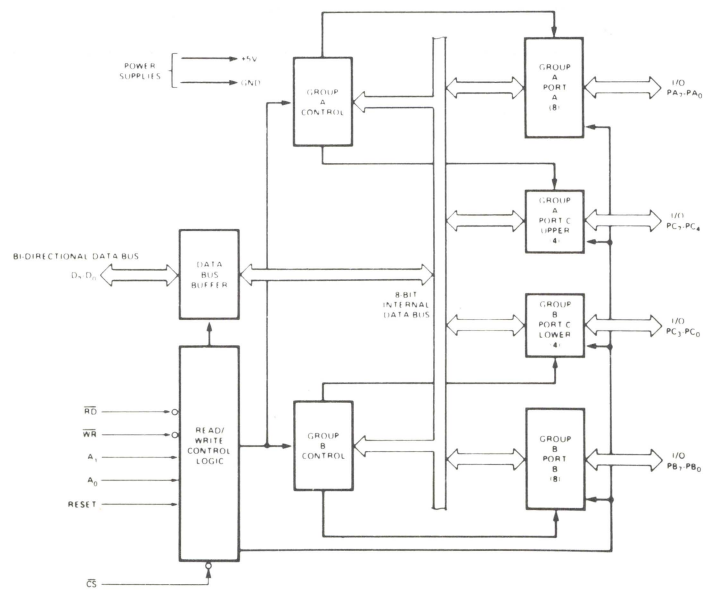
PIN CONFIGURATION



PIN NAMES

D_7–D_0	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	Ø VOLTS

8255A BLOCK DIAGRAM



MPU PERIPHERALS

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8255A FUNCTIONAL DESCRIPTION

General

The 8255A is a programmable peripheral interface (PPI) device designed for use in Intel® microcomputer systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the 8255A is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the 8255A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

($\overline{CS}$)

Chip Select. A "low" on this input pin enables the communiction between the 8255A and the CPU.

($\overline{RD}$)

Read. A "low" on this input pin enables the 8255A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the 8255A.

($\overline{WR}$)

Write. A "low" on this input pin enables the CPU to write data or control words into the 8255A.

(A_0 and A_1)

Port Select 0 and Port Select 1. These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word registers. They are normally connected to the least significant bits of the address bus (A_0 and A_1).

8255A BASIC OPERATION

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	INPUT OPERATION (READ)
0	0	0	1	0	PORT A ⇒ DATA BUS
0	1	0	1	0	PORT B ⇒ DATA BUS
1	0	0	1	0	PORT C ⇒ DATA BUS
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	DATA BUS ⇒ PORT A
0	1	1	0	0	DATA BUS ⇒ PORT B
1	0	1	0	0	DATA BUS ⇒ PORT C
1	1	1	0	0	DATA BUS ⇒ CONTROL
					DISABLE FUNCTION
X	X	X	X	1	DATA BUS ⇒ 3-STATE
1	1	0	1	0	ILLEGAL CONDITION
X	X	1	1	0	DATA BUS ⇒ 3-STATE

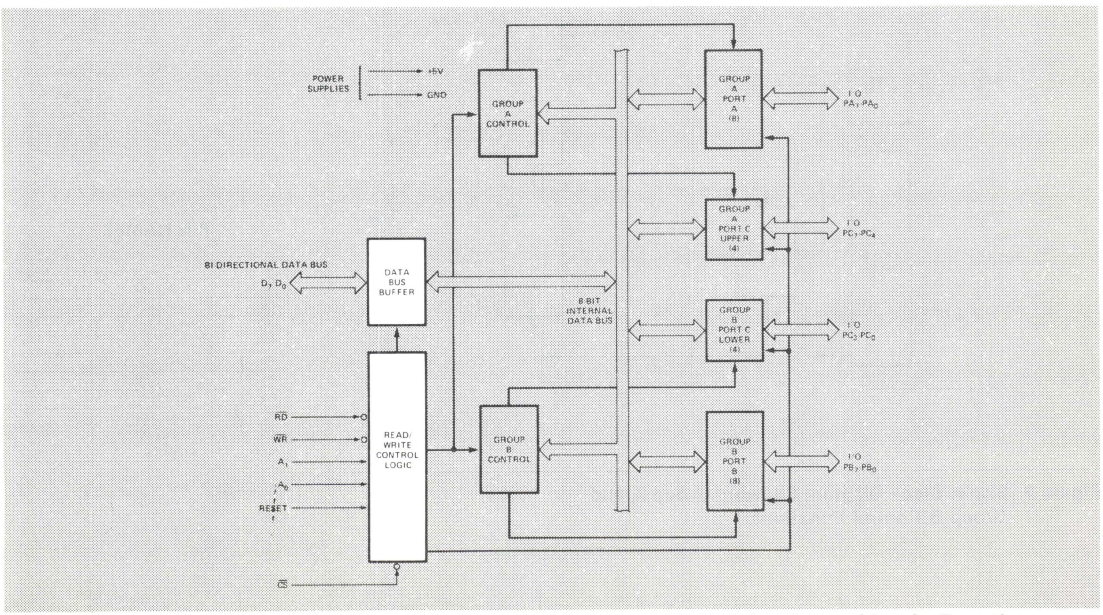


Figure 1. 8255A Block Diagram Showing Data Bus Buffer and Read/Write Control Logic Functions

(RESET)

Reset. A "high on this input clears the control register and all ports (A, C, C) are set to the input mode.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 8255A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 8255.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A – Port A and Port C upper (C7-C4)
Control Group B – Port B and Port C lower (C3-C0)

The Control Word Register can **Only** be written into. No Read operation of the Control Word Register is allowed.

Ports A, B, and C

The 8255A contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 8255A.

Port A. One 8-bit data output latch/buffer and one 8-bit data input latch.

Port B. One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C. One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.

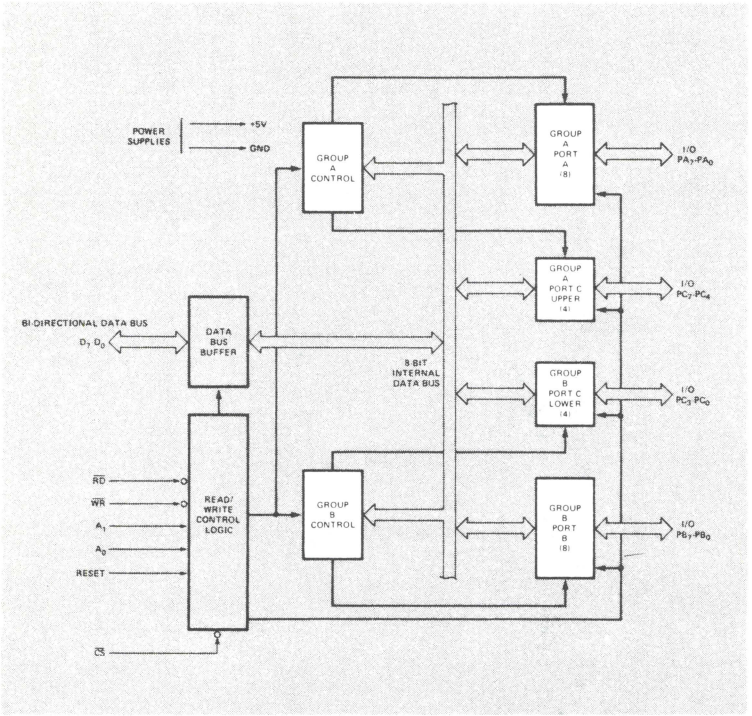
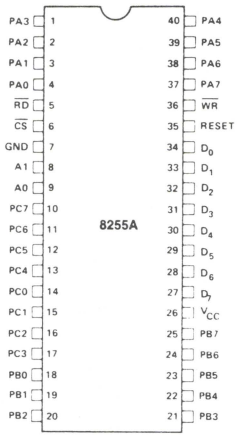


Figure 2. 8225A Block Diagram Showing Group A and Group B Control Functions

PIN CONFIGURATION



PIN NAMES

D_7-D_0	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	0 VOLTS

MPU PERIPHERALS

8255A OPERATIONAL DESCRIPTION

Mode Selection

There are three basic modes of operation that can be selected by the system software:

Mode 0 — Basic Input/Output
Mode 1 — Strobed Input/Output
Mode 2 — Bi-Directional Bus

When the reset input goes "high" all ports will be set to the input mode (i.e., all 24 lines will be in the high impedance state). After the reset is removed the 8255A can remain in the input mode with no additional initialization required. During the execution of the system program any of the other modes may be selected using a single output instruction. This allows a single 8255A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance; Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

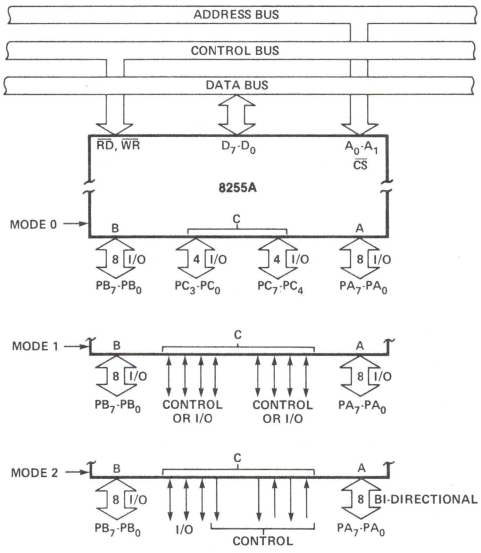


Figure 3. Basic Mode Definitions and Bus Interface

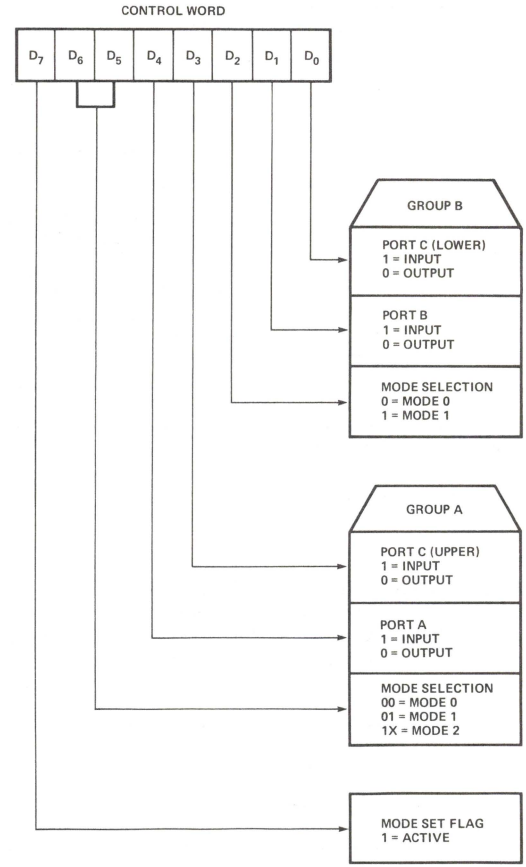


Figure 4. Mode Definition Format

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 8255A has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. This feature reduces software requirements in Control-based applications.

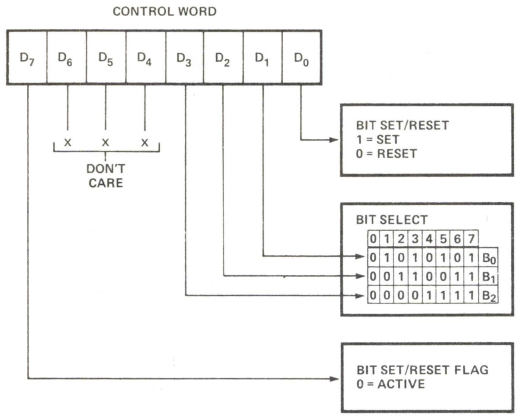


Figure 5. Bit Set/Reset Format

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

Interrupt Control Functions

When the 8255A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the Programmer to disallow or allow a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET) — INTE is SET — Interrupt enable
(BIT-RESET) — INTE is RESET — Interrupt disable

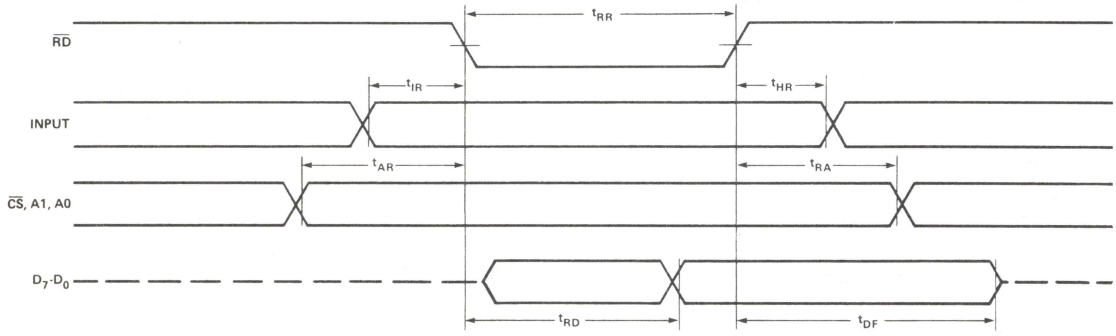
Note: All Mask flip-flops are automatically reset during mode selection and device Reset.

Operating Modes

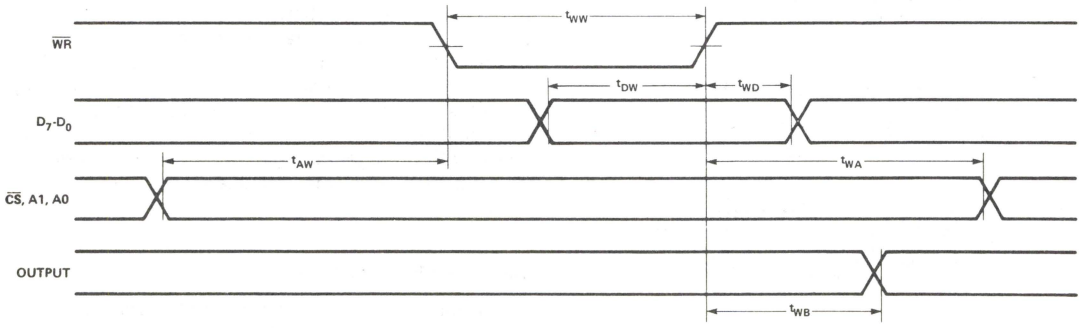
MODE 0 (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No "handshaking" is required, data is simply written to or read from a specified port.

Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports.
- Any port can be input or output.
- Outputs are latched.
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this Mode.



MODE 0 (Basic Input)



MODE 0 (Basic Output)

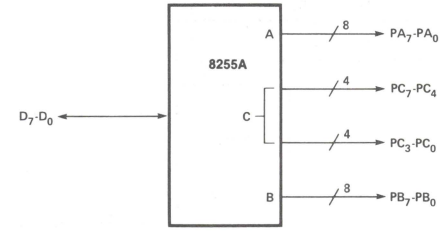
MODE 0 Port Definition

A		B		GROUP A			GROUP B	
D_4	D_3	D_1	D_0	PORT A	PORT C (UPPER)	#	PORT B	PORT C (LOWER)
0	0	0	0	OUTPUT	OUTPUT	0	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	1	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	2	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	3	INPUT	INPUT
0	1	0	0	OUTPUT	INPUT	4	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	5	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	6	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	7	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	8	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	9	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	10	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	11	INPUT	INPUT
1	1	0	0	INPUT	INPUT	12	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	13	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	14	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	15	INPUT	INPUT

MODE 0 Configurations

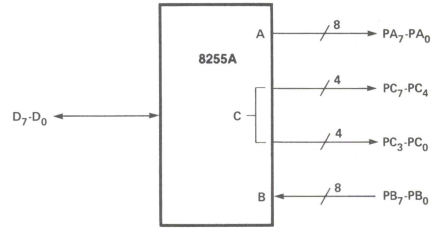
CONTROL WORD #0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	0	0



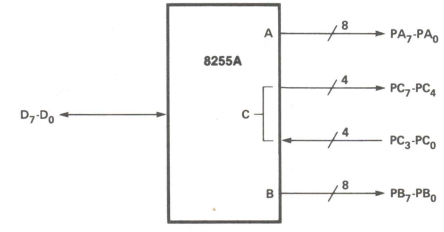
CONTROL WORD #2

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	1	0



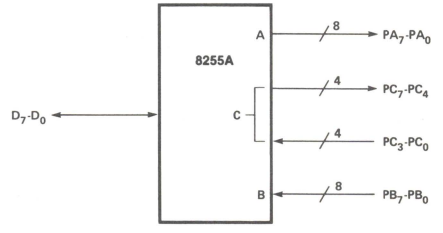
CONTROL WORD #1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	0	1



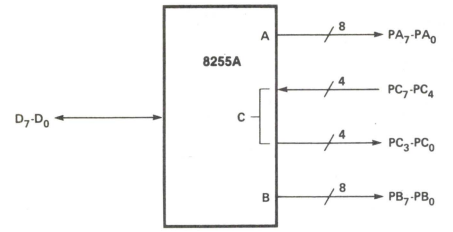
CONTROL WORD #3

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	1	1



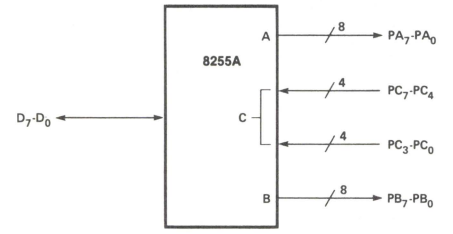
CONTROL WORD #4

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	0	0



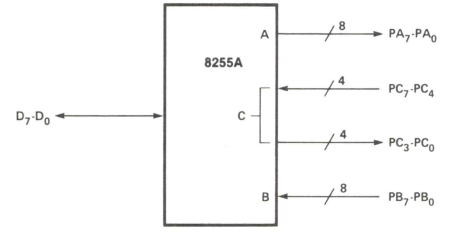
CONTROL WORD #5

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	0	1



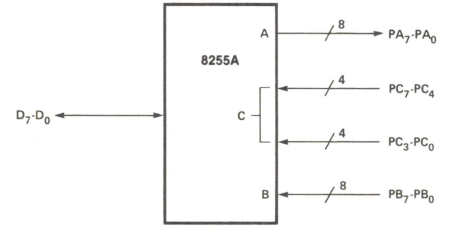
CONTROL WORD #6

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	1	0



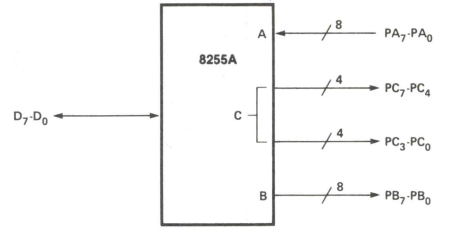
CONTROL WORD #7

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	1	1



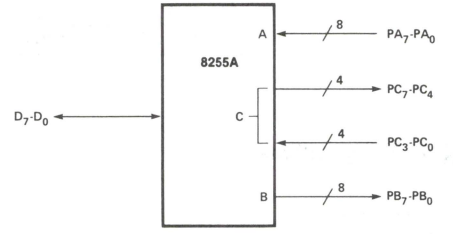
CONTROL WORD #8

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	0	0



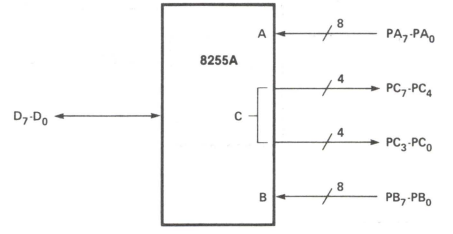
CONTROL WORD #9

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	0	1



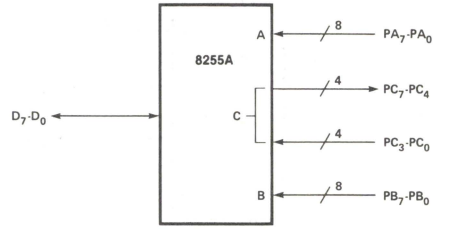
CONTROL WORD #10

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	1	0



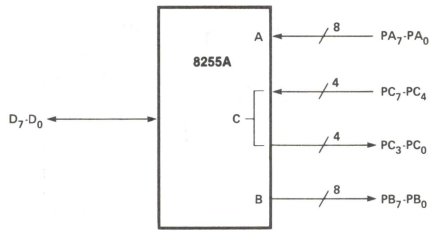
CONTROL WORD #11

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	1	1



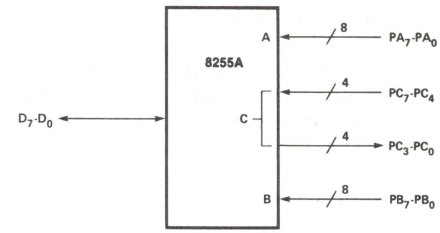
CONTROL WORD #12

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	1	0	0	0



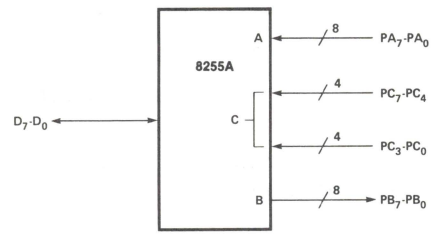
CONTROL WORD #14

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	1	0	1	0



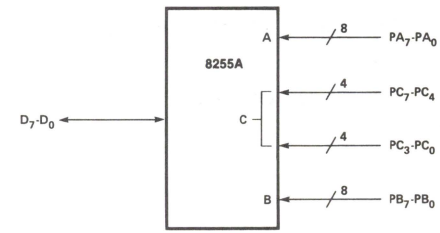
CONTROL WORD #13

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	1	0	0	1



CONTROL WORD #15

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	1	0	1	1



Operating Modes

MODE 1 (Strobed Input/Output). This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In mode 1, port A and Port B use the lines on port C to generate or accept these "handshaking" signals.

Mode 1 Basic Functional Definitions:

- Two Groups (Group A and Group B)
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

Input Control Signal Definition

STB (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. IBF is set by STB input being low and is reset by the rising edge of the RD input.

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the $\overline{STB}$ is a "one", IBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

Controlled by bit set/reset of PC_4.

INTE B

Controlled by bit set/reset of PC_2.

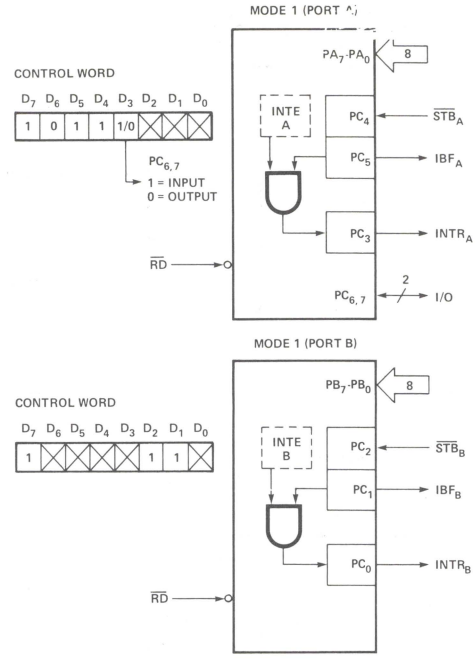


Figure 6. MODE 1 Input

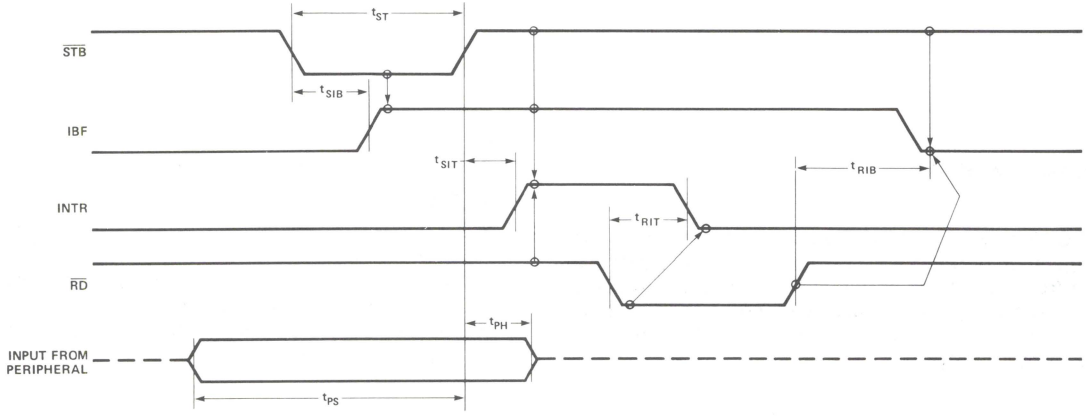


Figure 7. MODE 1 (Strobed Input)

Output Control Signal Definition

$\overline{OBF}$ (Output Buffer Full F/F). The OBF output will go "low" to indicate that the CPU has written data out to the specified port. The OBF F/F will be set by the rising edge of the WR input and reset by ACK Input being low.

$\overline{ACK}$ (Acknowledge Input). A "low" on this input informs the 8255A that the data from port A or port B has been accepted. In essence, a response from the peripheral device indicating that it has received the data output by the CPU.

INTR (Interrupt Request). A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when ACK is a "one", OBF is a "one" and INTE is a "one". It is reset by the falling edge of WR.

INTE A

Controlled by bit set/reset of PC_6.

INTE B

Controlled by bit set/reset of PC_2.

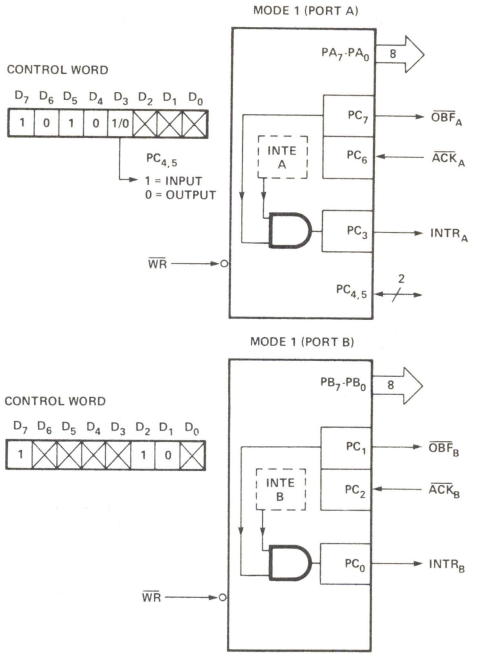


Figure 8. MODE 1 Output

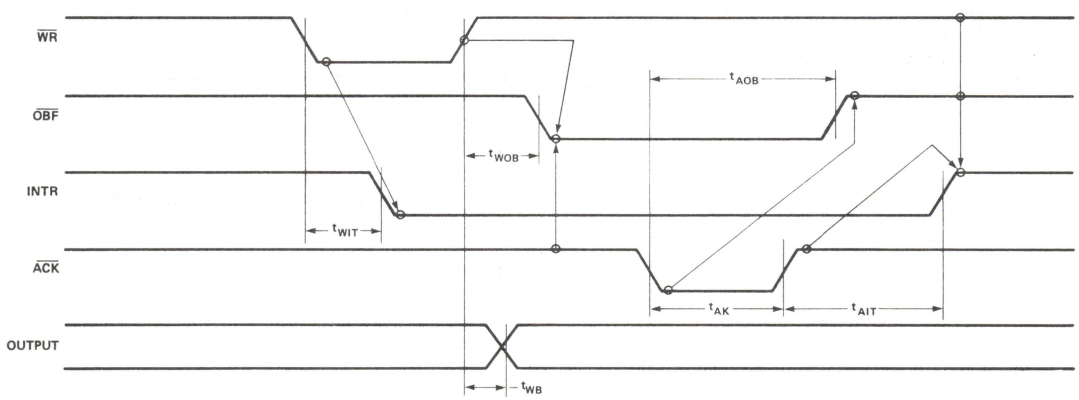


Figure 9. Mode 1 (Strobed Output)

Combinations of MODE 1

Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.

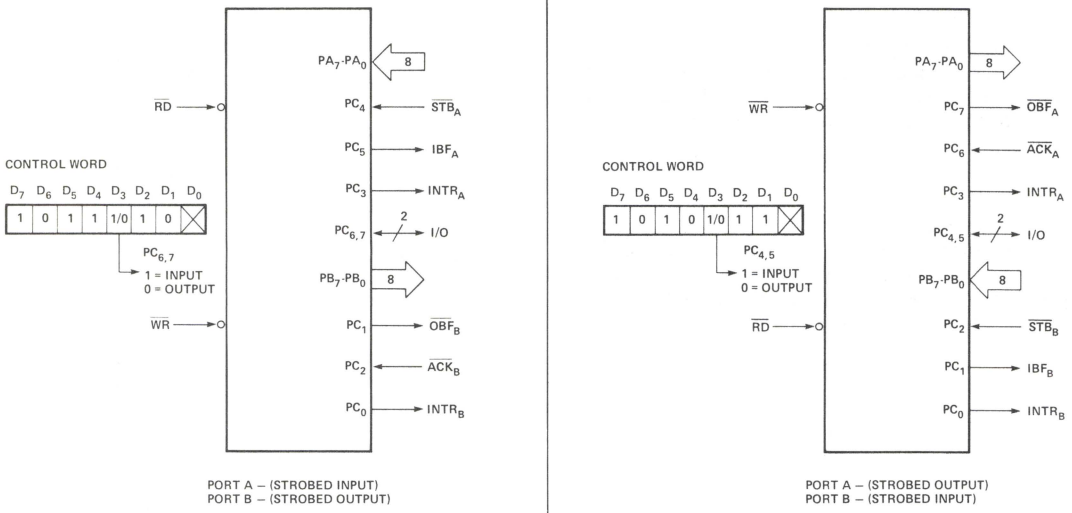


Figure 10. Combinations of MODE 1

Operating Modes

MODE 2 (Strobed Bidirectional Bus I/O). This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline in a similar manner to MODE 1. Interrupt generation and enable/disable functions are also available.

MODE 2 Basic Functional Definitions:

- Used in Group A only.
- One 8-bit, bi-directional bus Port (Port A) and a 5-bit control Port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A).

Bidirectional Bus I/O Control Signal Definition

INTR (Interrupt Request). A high on this output can be used to interrupt the CPU for both input or output operations.

Output Operations

$\overline{\text{OBF}}$ (Output Buffer Ful). The OBF output will go "low" to indicate that the CPU has written data out to port A.

$\overline{\text{ACK}}$ (Acknowledge). A "low" on this input enables the tri-state output buffer of port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 (The INTE Flip-Flop Associated with OBF). Controlled by bit set/reset of PC_6.

Input Operations

$\overline{\text{STB}}$ (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F). A "high" on this output indicates that data has been loaded into the input latch.

INTE 2 (The INTE Flip-Flop Associated with IBF). Controlled by bit set/reset of PC_4.

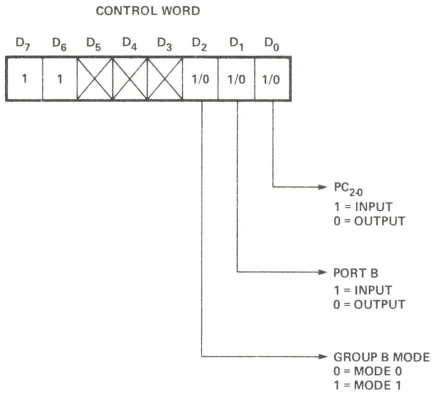


Figure 11. MODE Control Word

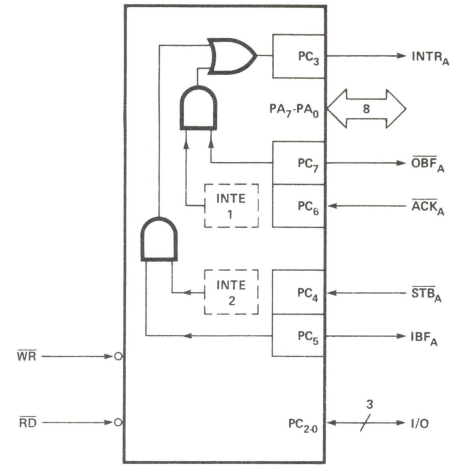


Figure 12. MODE 2

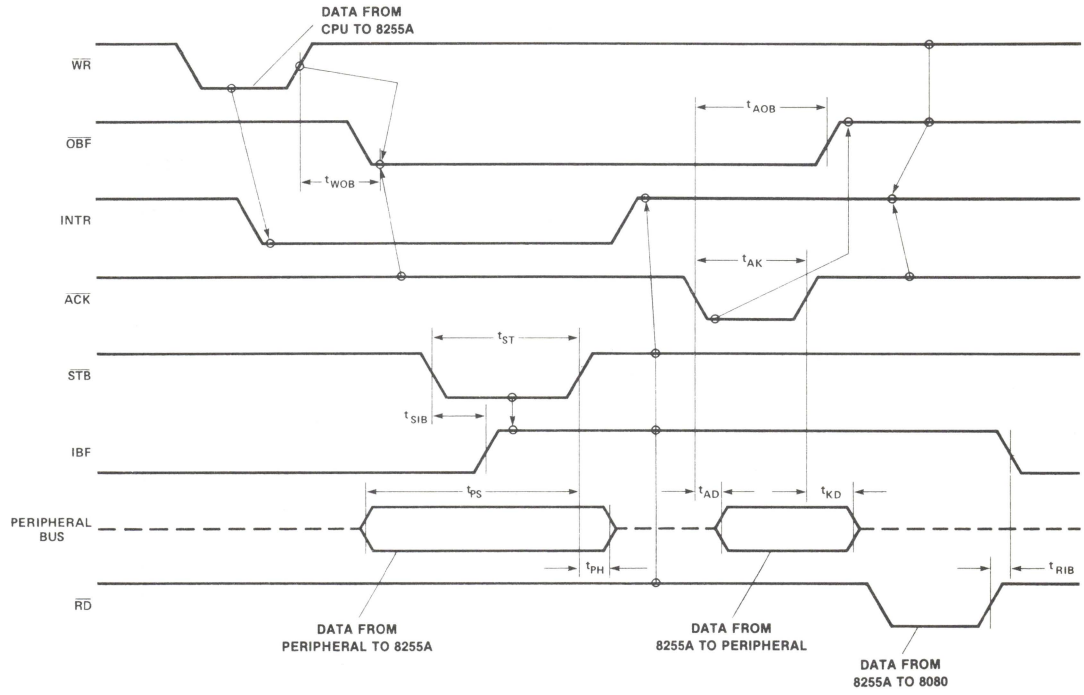


Figure 13. MODE 2 (Bidirectional)

NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
(INTR = IBF • $\overline{MASK}$ • $\overline{STB}$ • $\overline{RD}$ + $\overline{OBF}$ • $\overline{MASK}$ • $\overline{ACK}$ • $\overline{WR}$)

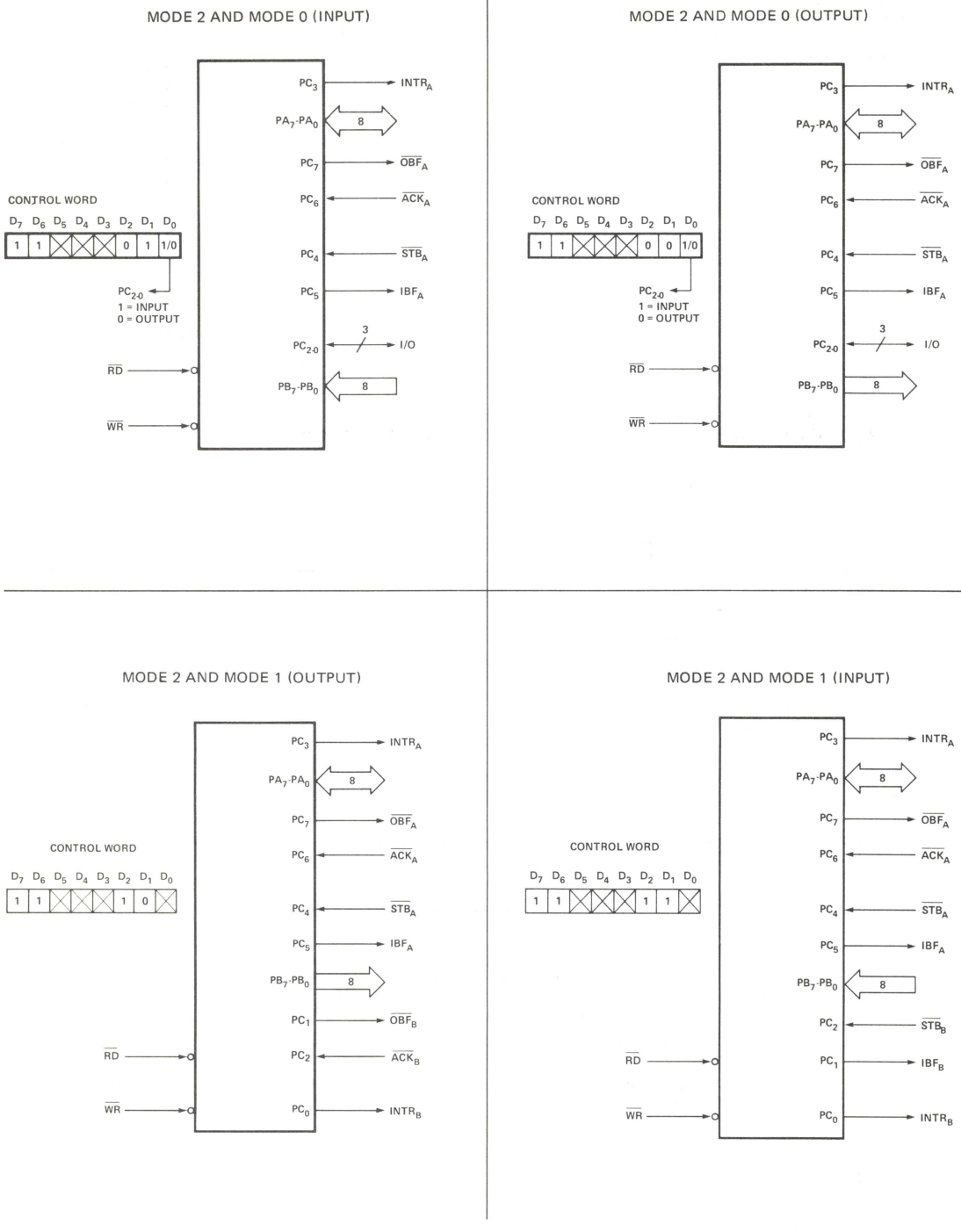


Figure 14. MODE 2 Combinations

Mode Definition Summary

	MODE 0		MODE 1		MODE 2	
	IN	OUT	IN	OUT	GROUP A ONLY	
PA_0	IN	OUT	IN	OUT	↔	
PA_1	IN	OUT	IN	OUT	↔	
PA_2	IN	OUT	IN	OUT	↔	
PA_3	IN	OUT	IN	OUT	↔	
PA_4	IN	OUT	IN	OUT	↔	
PA_5	IN	OUT	IN	OUT	↔	
PA_6	IN	OUT	IN	OUT	↔	
PA_7	IN	OUT	IN	OUT	↔	
PB_0	IN	OUT	IN	OUT	—	MODE 0 OR MODE 1 ONLY
PB_1	IN	OUT	IN	OUT	—	
PB_2	IN	OUT	IN	OUT	—	
PB_3	IN	OUT	IN	OUT	—	
PB_4	IN	OUT	IN	OUT	—	
PB_5	IN	OUT	IN	OUT	—	
PB_6	IN	OUT	IN	OUT	—	
PB_7	IN	OUT	IN	OUT	—	
PC_0	IN	OUT	$INTR_B$	$INTR_B$	I/O	
PC_1	IN	OUT	IBF_B	$\overline{OBF}_B$	I/O	
PC_2	IN	OUT	$\overline{STB}_B$	$\overline{ACK}_B$	I/O	
PC_3	IN	OUT	$INTR_A$	$INTR_A$	$INTR_A$	
PC_4	IN	OUT	$\overline{STB}_A$	I/O	$\overline{STB}_A$	
PC_5	IN	OUT	IBF_A	I/O	IBF_A	
PC_6	IN	OUT	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$	
PC_7	IN	OUT	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$	

Special Mode Combination Considerations

There are several combinations of modes when not all of the bits in Port C are used for control or status. The remaining bits can be used as follows:

If Programmed as Inputs –
All input lines can be accessed during a normal Port C read.

If Programmed as Outputs –
Bits in C upper (PC_7-PC_4) must be individually accessed using the bit set/reset function.

Bits in C lower (PC_3-PC_0) can be accessed using the bit set/reset function or accessed as a threesome by writing into Port C.

Source Current Capability on Port B and Port C

Any set of eight output buffers, selected randomly from Ports B and C can source 1mA at 1.5 volts. This feature allows the 8255 to directly drive Darlington type drivers and high-voltage displays that require such source current.

Reading Port C Status

In Mode 0, Port C transfers data to or from the peripheral device. When the 8255 is programmed to function in Modes 1 or 2, Port C generates or accepts "hand-shaking" signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

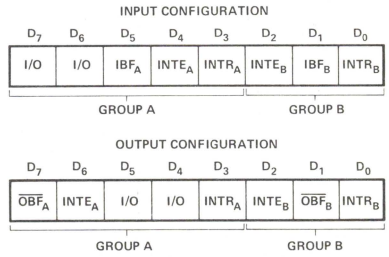


Figure 15. MODE 1 Status Word Format

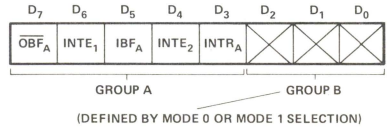


Figure 16. MODE 2 Status Word Format

APPLICATIONS OF THE 8255A

The 8255A is a very powerful tool for interfacing peripheral equipment to the microcomputer system. It represents the optimum use of available pins and is flexible enough to interface almost any I/O device without the need for additional external logic.

Each peripheral device in a microcomputer system usually has a "service routine" associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the 8255A is programmed by the I/O service routine and becomes an extension of the system software. By examining the I/O devices interface characteristics for both data transfer and timing, and matching this information to the examples and tables in the detailed operational description, a control word can easily be developed to initialize the 8255A to exactly "fit" the application. Figures 17 through 23 present a few examples of typical applications of the 8255A.

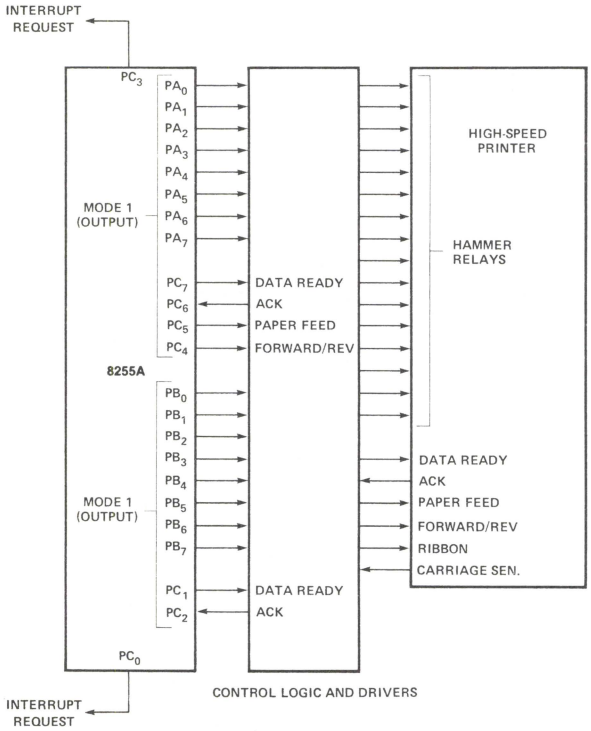


Figure 17. Printer Interface

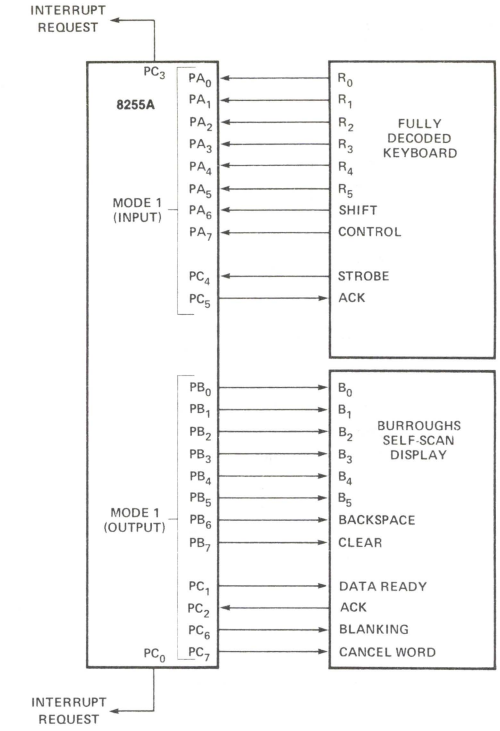


Figure 18. Keyboard and Display Interface

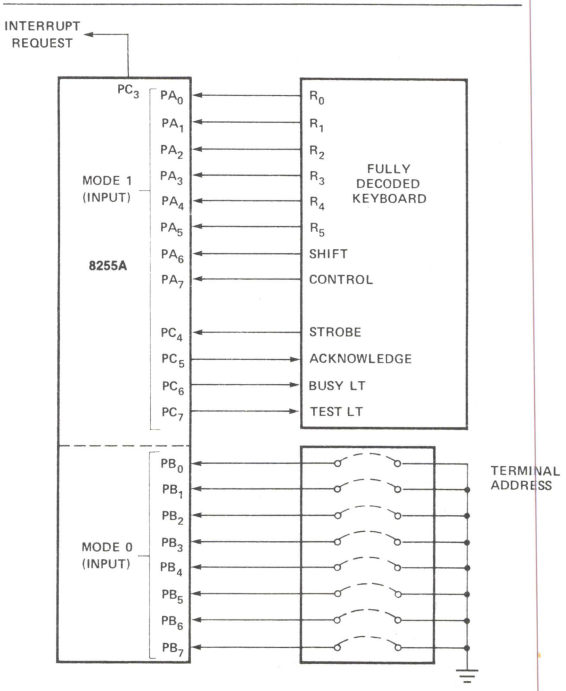


Figure 19. Keyboard and Terminal Address Interface

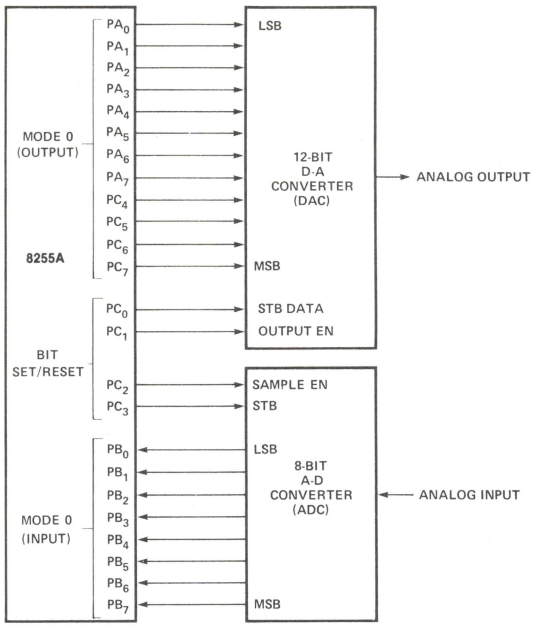


Figure 20. Digital to Analog, Analog to Digital

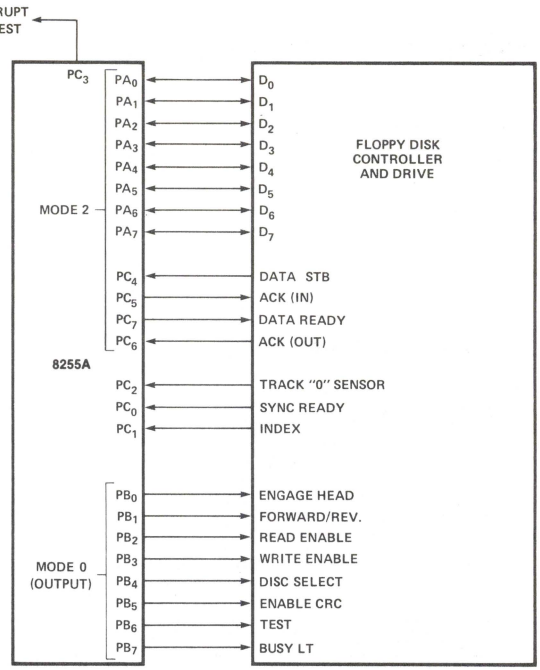


Figure 22. Basic Floppy Disc Interface

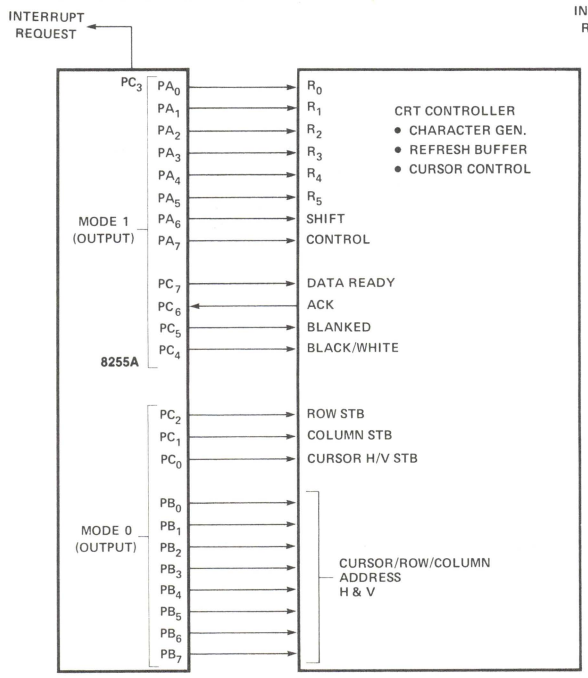


Figure 21. Basic CRT Controller Interface

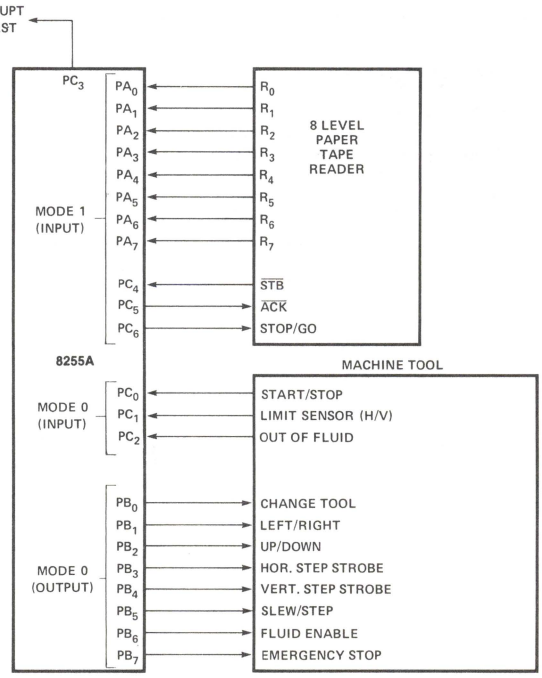


Figure 23. Machine Tool Controller Interface

MPU PERIPHERALS

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . 0°C to 70°C
Storage Temperature . . . . . –65°C to +150°C
Voltage on Any Pin
With Respect to Ground . . . . . –0.5V to +7V
Power Dissipation . . . . . 1 Watt

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ±5%; GND = 0V

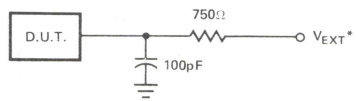
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL} (DB)	Output Low Voltage (Data Bus)		0.45	V	I_{OL} = 2.5mA
V_{OL}(PER)	Output Low Voltage (Peripheral Port)		0.45	V	I_{OL} = 1.7mA
V_{OH}(DB)	Output High Voltage (Data Bus)	2.4		V	I_{OH} = -400μA
V_{OH}(PER)	Output High Voltage (Peripheral Port)	2.4		V	I_{OH} = -200μA
I_{DAR}[1]	Darlington Drive Current	-1.0	-4.0	mA	R_{EXT} = 750Ω; V_{EXT} = 1.5V
I_{CC}	Power Supply Current		120	mA	
I_{IL}	Input Load Current		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = V_{CC} to 0V

Note 1: Available on any 8 pins from Port B and C.

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
C_{IN}	Input Capacitance			10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND



*V_{EXT} is set at various voltages during testing to guarantee the specification.

Figure 24. Test Load Circuit (for dB)

A.C. CHARACTERISTICS

T_A = 0°C to 70°C; V_{CC} = +5V ±5%; GND = 0V

NOTE:
The 8255A-5 specifications are not final. Some parametric limits are subject to change.

Bus Parameters

Read:

		8255A		8255A-5		
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	UNIT
t_{AR}	Address Stable Before READ	0		0		ns
t_{RA}	Address Stable After READ	0		0		ns
t_{RR}	READ Pulse Width	300		300		ns
t_{RD}	Data Valid From READ[1]		250		200	ns
t_{DF}	Data Float After READ	10	150	10	100	ns
t_{RV}	Time Between READs and/or WRITEs	850		850		ns

Write:

		8255A		8255A-5		
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	UNIT
t_{AW}	Address Stable Before WRITE	0		0		ns
t_{WA}	Address Stable After WRITE	20		20		ns
t_{WW}	WRITE Pulse Width	400		300		ns
t_{DW}	Data Valid to WRITE (T.E.)	100		100		ns
t_{WD}	Data Valid After WRITE	30		30		ns

Other Timings:

		8255A		8255A-5		
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	UNIT
t_{WB}	WR = 1 to Output[1]		350		350	ns
t_{IR}	Peripheral Data Before RD	0		0		ns
t_{HR}	Peripheral Data After RD	0		0		ns
t_{AK}	ACK Pulse Width	300		300		ns
t_{ST}	STB Pulse Width	500		500		ns
t_{PS}	Per. Data Before T.E. of STB	0		0		ns
t_{PH}	Per. Data After T.E. of STB	180		180		ns
t_{AD}	ACK = 0 to Output[1]		300		300	ns
t_{KD}	ACK = 1 to Output Float	20	250	20	250	ns
t_{WOB}	WR = 1 to OBF = 0[1]		650		650	ns
t_{AOB}	ACK = 0 to OBF = 1[1]		350		350	ns
t_{SIB}	STB = 0 to IBF = 1[1]		300		300	ns
t_{RIB}	RD = 1 to IBF = 0[1]		300		300	ns
t_{RIT}	RD = 0 to INTR = 0[1]		400		400	ns
t_{SIT}	STB = 1 to INTR = 1[1]		300		300	ns
t_{AIT}	ACK = 1 to INTR = 1[1]		350		350	ns
t_{WIT}	WR = 0 to INTR = 0[1]		850		850	ns

Notes: 1. Test Conditions: 8255A: C_L = 100pF; 8255A-5: C_L = 150pF.
2. Period of Reset pulse must be at least 50μs during or after power on. Subsequent Reset pulse can be 500 ns min.

Figure 25. Input Waveforms for A.C. Tests

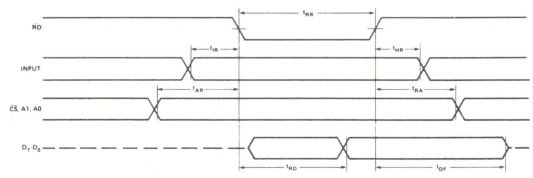


Figure 26. MODE 0 (Basic Input)

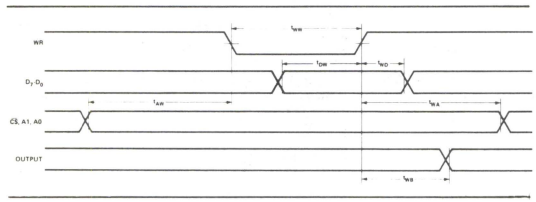


Figure 27. MODE 0 (Basic Input)

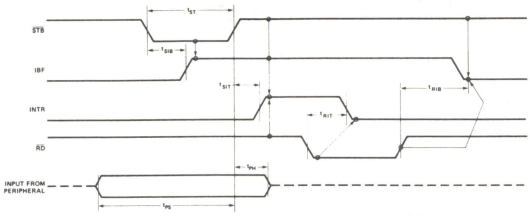


Figure 28. MODE 1 (Strobed Input)

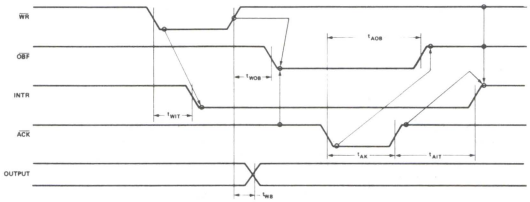
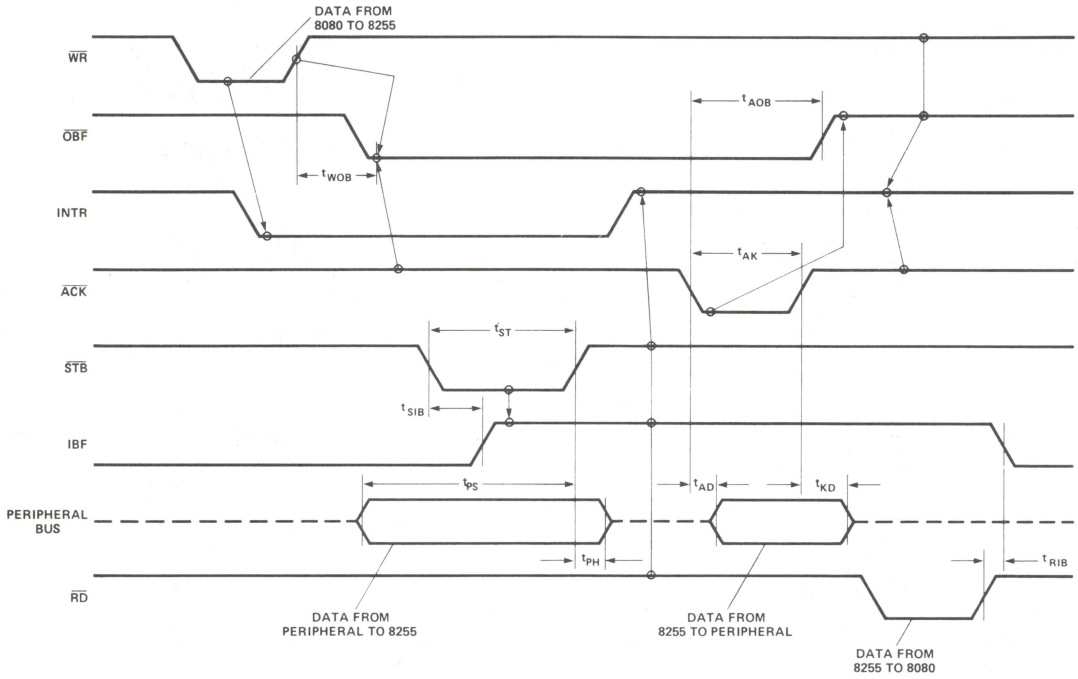


Figure 29. MODE 1 (Strobed Output)



NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
($INTR = IBF \cdot \overline{MASK} \cdot \overline{STB} \cdot \overline{RD} + \overline{OBF} \cdot \overline{MASK} \cdot \overline{ACK} \cdot \overline{WR}$)

Figure 30. MODE 2 (Bidirectional)

MPU PERIPHERALS

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

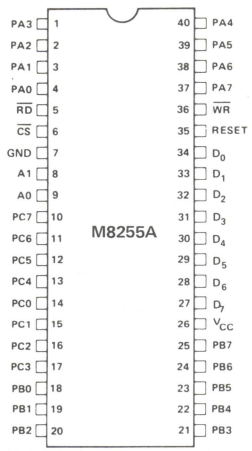
M8255A
PROGRAMMABLE PERIPHERAL INTERFACE

- 24 Programmable I/O PIns
- Completely TTL Compatible
- Fully Compatible with MCS-80™ Microprocessor Family
- Full Military Temperature Range −55°C to +125°C
- Direct Bit Set/Reset Capability Easing Control Application Interface
- 40-Pin Dual In-Line Package
- Reduces System Package Count
- ±10% Power Supply Tolerance

The Intel® M8255A is a general purpose programmable I/O device designed for use with microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.

Other features of the M8255A include bit set and reset capability and the ability to source 1 mA of current at 1.5 volts. This allows darlington transistors to be directly driven for applications such as printers and high voltage displays.

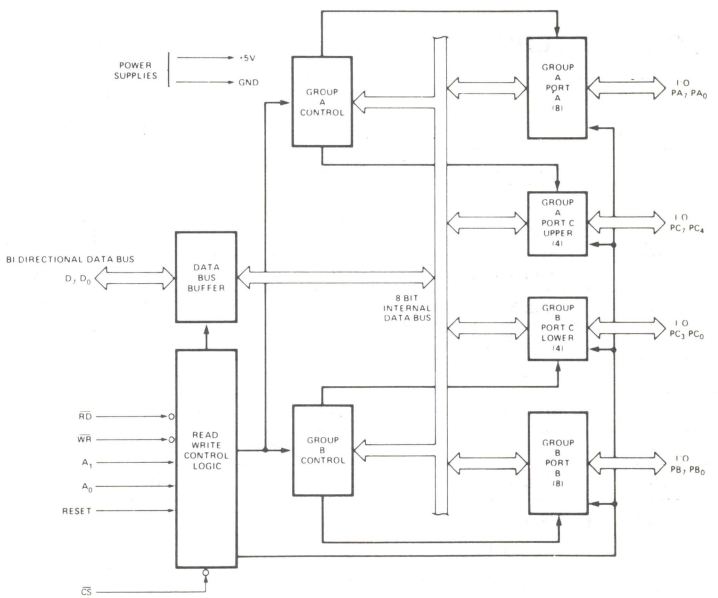
PIN CONFIGURATION



PIN NAMES

D_7–D_0	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	0 VOLTS

M8255A BLOCK DIAGRAM



MPU PERIPHERALS

PRELIMINARY
Mostek reserves the right to change parameters or limits contained herein without notice.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
Voltage On Any Pin
With Respect to GND . . . . . -0.5V to +7V
Power Dissipation . . . . . 1 Watt

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS T_A = -55°C to +125°C; V_{CC} = +5V ±10%; GND = 0V

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL} (DB)	Output Low Voltage (Data Bus)		0.45	V	I_{OL} = 2.5mA
V_{OL}(PER)	Output Low Voltage (Peripheral Port)		0.45	V	I_{OL} = 1.7mA
V_{OH}(DB)	Output High Voltage (Data Bus)	2.4		V	I_{OH} = -400μA
V_{OH}(PER)	Output High Voltage (Peripheral Port)	2.4		V	I_{OH} = -200μA
I_{DAR}[1]	Darlington Drive Current	-1.0	-4.0	mA	R_{EXT} = 750Ω; V_{EXT} = 1.5V
I_{CC}	Power Supply Current		120	mA	
I_{IL}	Input Load Current		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = V_{CC} to 0V

Note 1: Available on any 8 pins from Port B and C.

A.C. CHARACTERISTICS T_A = -55°C to +125°C, V_{CC} = +5V ±10%; GND = 0V

		8255A		8255A-5		
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	UNIT
t_{AR}	Address Stable Before READ	0		0		ns
t_{RA}	Address Stable After READ	0		0		ns
t_{RR}	READ Pulse Width	300		300		ns
t_{RD}	Data Valid From READ[1]		250		200	ns
t_{DF}	Data Float After READ	10	150	10	100	ns
t_{RV}	Time Between READs and/or WRITEs	850		850		ns
t_{AW}	Address Stable Before WRITE	0		0		ns
t_{WA}	Address Stable After WRITE	20		20		ns
t_{WW}	WRITE Pulse Width	400		300		ns
t_{DW}	Data Valid to WRITE (T.E.)	100		100		ns
t_{WD}	Data Valid After WRITE	30		30		ns
t_{WB}	WR = 1 to Output[1]		350		350	ns
t_{IR}	Peripheral Data Before RD	0		0		ns
t_{HR}	Peripheral Data After RD	0		0		ns
t_{AK}	ACK Pulse Width	300		300		ns
t_{ST}	STB Pulse Width	500		500		ns
t_{PS}	Per. Data Before T.E. of STB	0		0		ns

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

t_{PH}	Per. Data After T.E. of STB	180		180		ns
t_{AD}	ACK = 0 to Output[1]		300		300	ns
t_{KD}	ACK = 1 to Output Float	20	250	20	250	ns
t_{WOB}	WR = 1 to OBF = 0[1]		650		650	ns
t_{AOB}	ACK = 0 to OBF = 1[1]		350		350	ns
t_{SIB}	STB = 0 to IBF = 1[1]		300		300	ns
t_{RIB}	RD = 1 to IBF = 0[1]		300		300	ns
t_{RIT}	RD = 0 to INTR = 0[1]		400		400	ns
t_{SIT}	STB = 1 to INTR = 1[1]		300		300	ns
t_{AIT}	ACK = 1 to INTR = 1[1]		350		350	ns
t_{WIT}	WR = 0 to INTR = 0[1]		850		850	ns

CAPACITANCE $T_A = 25°C$, $V_{CC} = GND = 0V$

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
C_{IN}	Input Capacitance			10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND

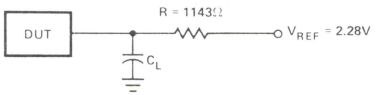


Figure 31. Test Load Circuit

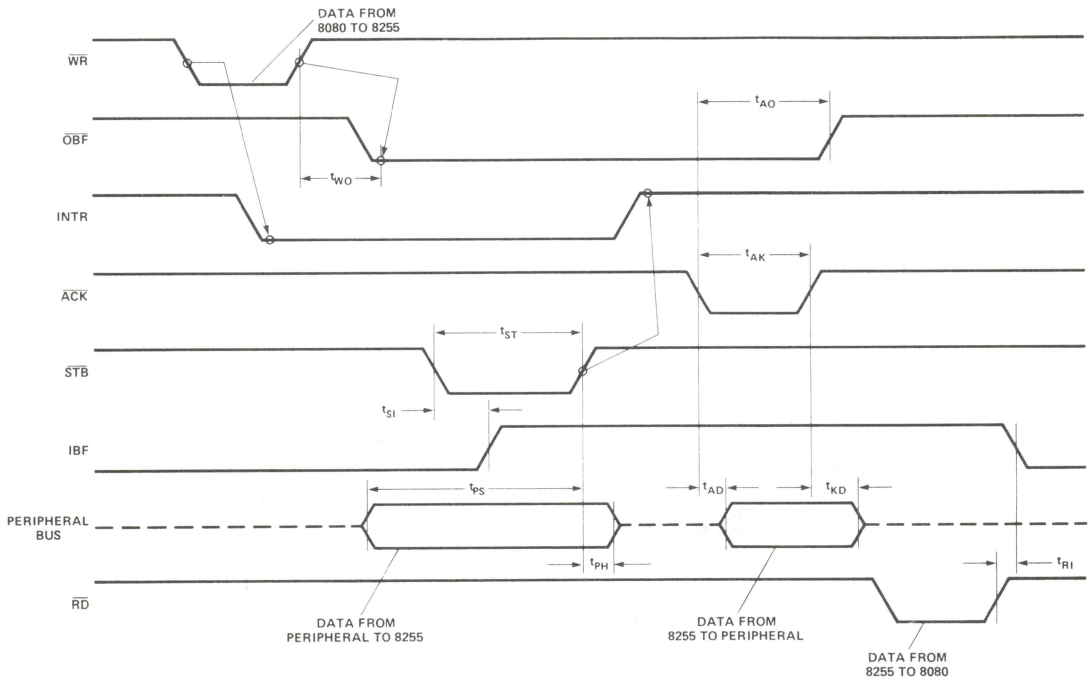


Figure 32. MODE 2 (Bidirectional)

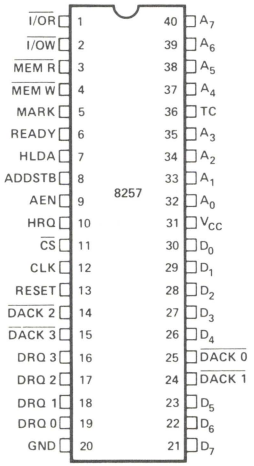
PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

8257/8257-5
PROGRAMMABLE DMA CONTROLLER

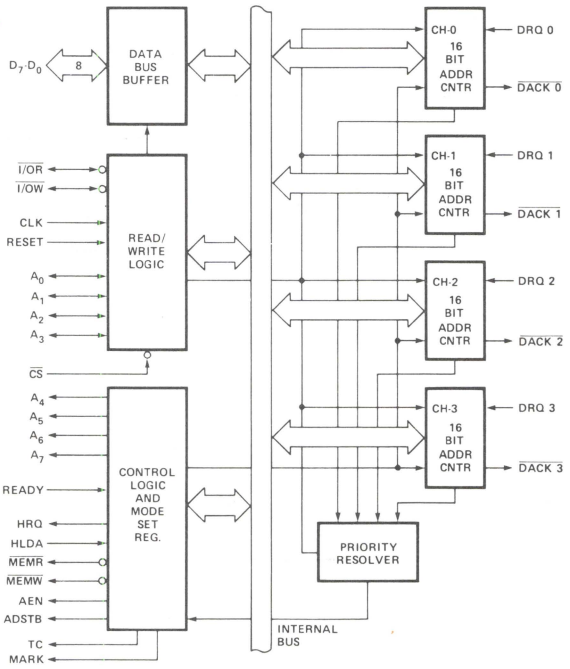
- MCS-85™ Compatible 8257-5
- 4-Channel DMA Controller
- Priority DMA Request Logic
- Channel Inhibit Logic
- Terminal Count and Modulo 128 Outputs
- Auto Load Mode
- Single TTL Clock
- Single +5V Supply
- Expandable
- 40-Pin Dual In-Line Package

The Intel® 8257 is a 4-channel direct memory access (DMA) controller. It is specifically designed to simplify the transfer of data at high speeds for the Intel® microcomputer systems. Its primary function is to generate, upon a peripheral request, a sequential memory address which will allow the peripheral to read or write data directly to or from memory. Acquisition of the system bus in accomplished via the CPU's hold function. The 8257 has priority logic that resolves the peripherals requests and issues a composite hold request to the CPU. It maintains the DMA cycle count for each channel and outputs a control signal to notify the peripheral that the programmed number of DMA cycles is complete. Other output control signals simplify sectored data transfers and expansion to other 8257 devices for systems that require more than 4 channels of DMA controlled transfer. The 8257 represents a significant savings in component count for DMA-based microcomputer systems and greatly simplifies the transfer of data at high speed between peripherals and memories.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

D_7-D_0	DATA BUS
A_7-A_0	ADDRESS BUS
$\overline{I/OR}$	I/O READ
$\overline{I/OW}$	I/O WRITE
$\overline{MEMR}$	MEMORY READ
$\overline{MEMW}$	MEMORY WRITE
CLK	CLOCK INPUT
RESET	RESET INPUT
READY	READY
HRQ	HOLD REQUEST (TO 8080A)
HLDA	HOLD ACKNOWLEDGE (FROM 8080A)

AEN	ADDRESS ENABLE
ADSTB	ADDRESS STROBE
TC	TERMINAL COUNT
MARK	MODULO 128 MARK
DRQ_3-DRQ_0	DMA REQUEST INPUT
$\overline{DACK_3}$-$\overline{DACK_0}$	DMA ACKNOWLEDGE OUT
$\overline{CS}$	CHIP SELECT
V_{CC}	+5 VOLTS
GND	GROUND

MPU PERIPHERALS

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FUNCTIONAL DESCRIPTION

General

The 8257 is a programmable, Direct Memory Access (DMA) device which, when coupled with a single Intel® 8212 I/O port device, provides a complete four-channel DMA controller for use in Intel® microcomputer systems. After being initialized by software, the 8257 can transfer a block of data, containing up to 16,384 bytes, between memory and a peripheral device directly, without further intervention required of the CPU. Upon receiving a DMA transfer request from an enabled peripheral, the 8257:

- Acquires control of the system bus.
- Acknowledges that requesting peripheral which is connected to the highest priority channel.
- Outputs the least significant eight bits of the memory address onto system address lines A_0-A_7, outputs the most significant eight bits of the memory address to the 8212 I/O port via the data bus (the 8212 places these address bits on lines A_8-A_{15}), and
- Generates the appropriate memory and I/O read/write control signals that cause the peripheral to receive or deposit a data byte directly from or to the addressed location in memory.

The 8257 will retain control of the system bus and repeat the transfer sequence, as long as a peripheral maintains its DMA request. Thus, the 8257 can transfer a block of data to/from a high speed peripheral (e.g., a sector of data on a floppy disk) in a single "burst". When the specified number of data bytes have been transferred, the 8257 activates its Terminal Count (TC) output, informing the CPU that the operation is complete.

The 8257 offers three different modes of operation: (1) DMA read, which causes data to be transferred from memory to a peripheral; (2) DMA write, which causes data to be transferred from a peripheral to memory; and (3) DMA verify, which does not actually involve the transfer of data. When an 8257 channel is in the DMA verify mode, it will respond the same as described for transfer operations, except that no memory or I/O read/write control signals will be generated, thus preventing the transfer of data. The 8257, however, will gain control of the system bus and will acknowledge the peripheral's DMA request for each DMA cycle. The peripheral can use these acknowledge signals to enable an internal access of each byte of a data block in order to execute some verification procedure, such as the accumulation of a CRC (Cyclic Redundancy Code) checkword. For example, a block of DMA verify cycles might follow a block of DMA read cycles (memory to peripheral) to allow the peripheral to verify its newly acquired data.

Block Diagram Description

1. DMA Channels

The 8257 provides four separate DMA channels (labeled CH-0 to CH-3). Each channel includes two sixteen-bit registers: (1) a DMA address register, and (2) a terminal count register. Both registers must be initialized before a channel is enabled. The DMA address register is loaded with the address of the first memory location to be accessed. The value loaded into the low-order 14-bits of the terminal count register specifies the number of DMA cycles minus one before the Terminal Count (TC) output is activated. For instance, a terminal count of 0 would cause the TC output to be active in the first DMA cycle for that channel. In general, if N = the number of desired DMA cycles, load the value N-1 into the low-order 14-bits of the terminal count register. The most significant two bits of the terminal count register specify the type of DMA operation for that channel:

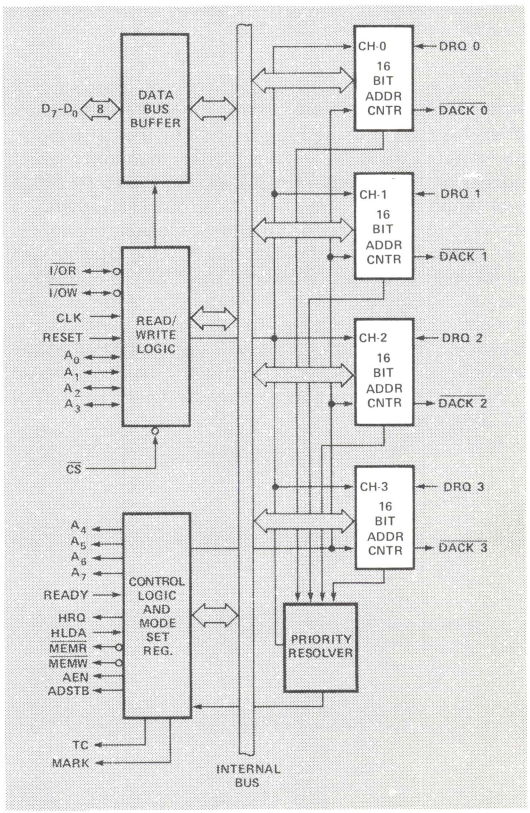

Figure 1. 8257 Block Diagram Showing DMA Channels

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These two bits are not modified during a DMA cycle, but can be changed between DMA blocks.

Each channel accepts a DMA Request (DRQn) input and provides a DMA Acknowledge (DACKn) output:

(DRQ 0-DRQ 3)

DMA Request: These are individual asynchronous channel request inputs used by the peripherals to obtain a DMA cycle. If not in the rotating priority mode then DRQ 0 has the highest priority and DRQ 3 has the lowest. A request can be generated by raising the request line and holding it high until DMA acknowledge. For multiple DMA cycles (Burst Mode) the request line is held high until the DMA acknowledge of the last cycle arrives.

($\overline{\text{DACK 0 - DACK 3}}$)

DMA Acknowledge: An active low level on the acknowledge output informs the peripheral connected to that channel that it has been selected for a DMA cycle.

BIT 15	BIT 14	TYPE OF DMA OPERATION
0	0	Verify DMA Cycle
0	1	Write DMA Cycle
1	0	Read DMA Cycle
1	1	(Illegal)

2. Data Bus Buffer

This three-state, bi-directional, eight bit buffer interfaces the 8257 to the system data bus:

(D_0-D_7)

Data Bus Lines: These are bi-directional three-state lines. When the 8257 is being programmed by the CPU, eight-bits of data for a DMA address register, a terminal count register or the Mode Set register are received on the data bus. When the CPU reads a DMA address register, a terminal count register or the Status register, the data is sent to the CPU over the data bus. During DMA cycles (when the 8257 is the bus master), the 8257 will output the most significant eight-bits of the memory address (from one of the DMA address registers) to the 8212 latch via the data bus. These address bits will be transferred at the beginning of the DMA cycle; the bus will then be released to handle the memory data transfer during the balance of the DMA cycle.

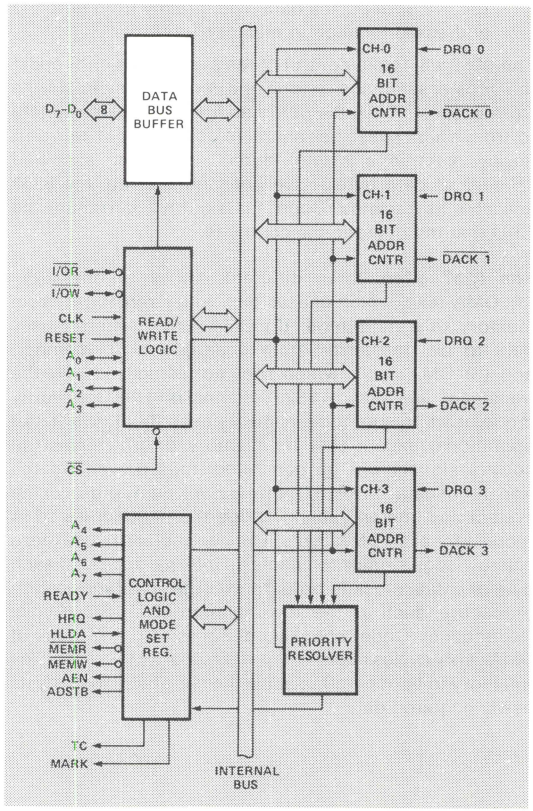

Figure 2. 8257 Block Diagram Showing Data Bus Buffer

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3. Read/Write Logic

When the CPU is programming or reading one of the 8257's register (i.e., when the 8257 is a "slave" device on the system bus), the Read/Write Logic accepts the I/O Read ($\overline{I/OR}$) or I/O Write ($\overline{I/OW}$) signal, decodes the least significant four address bits, (A_0-A_3), and either writes the contents of the data bus into the addressed register (if $\overline{I/OW}$ is true) or places the contents of the addressed register onto the data bus (if $\overline{I/OR}$ is true).

During DMA cycles (i.e., when the 8257 is the bus "master"), the Read/Write Logic generates the I/O read and memory write (DMA write cycle) or I/O Write and memory read (DMA read cycle) signals which control the data link with the peripheral that has been granted the DMA cycle.

Note that during DMA transfers Non-DMA I/O devices should be de-selected (disabled) using "AEN" signal to inhibit I/O device decoding of the memory address as an erroneous device address.

($\overline{I/OR}$)

I/O Read: An active-low, bi-directional three-state line. In the "slave" mode, it is an input which allows the 8-bit status register or the upper/lower byte of a 16-bit DMA address register or terminal count register to be read. In the "master" mode, $\overline{I/OR}$ is a control output which is used to access data from a peripheral during the DMA write cycle.

($\overline{I/OW}$)

I/O Write: An active-low, bi-directional three-state line. In the "slave" mode, it is an input which allows the contents of the data bus to be loaded into the 8-bit mode set register or the upper/lower byte of a 16-bit DMA address register or terminal count register. In the "master" mode, $\overline{I/OW}$ is a control output which allows data to be output to a peripheral during a DMA read cycle.

(CLK)

Clock Input: Generally from an Intel® 8224 Clock Generator device. (ϕ2 TTL)

(RESET)

Reset: An asynchronous input (generally from an 8224 device) which clears all control lines and disables all DMA channels by clearing the mode register.

(A_0-A_3)

Address Lines: These least significant four address lines are bi-directional. In the "slave" mode they are inputs which select one of the registers to be read or programmed. In the "master" mode, they are outputs which constitute the least significant four bits of the 16-bit memory address generated by the 8257.

($\overline{CS}$)

Chip Select: An active-low input which enables the I/O Read or I/O Write input when the 8257 is being read or programmed in the "slave" mode. In the "master" mode, $\overline{CS}$ is automatically disabled to prevent the chip from selecting itself while performing the DMA function.

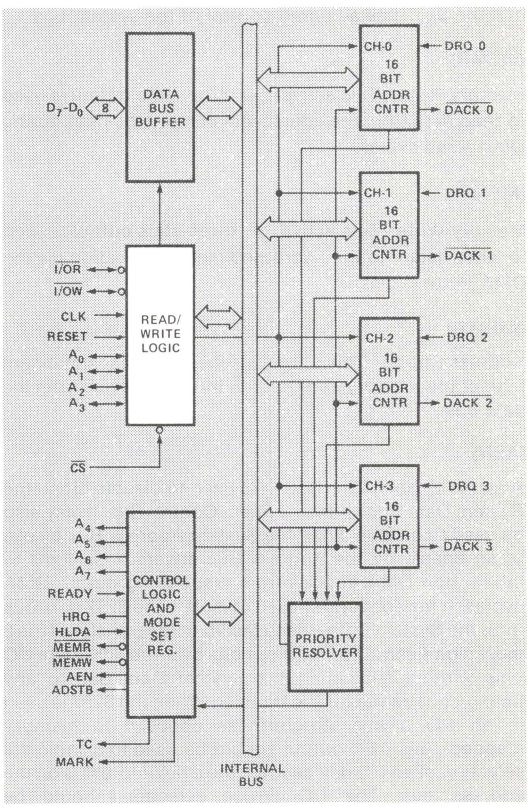

Figure 3. 8257 Block Diagram Showing Read/Write Logic Function

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4. Control Logic

This block controls the sequence of operations during all DMA cycles by generating the appropriate control signals and the 16-bit address that specifies the memory location to be accessed.

(A_4-A_7)

Address Lines: These four address lines are three-state outputs which constitute bits 4 through 7 of the 16-bit memory address generated by the 8257 during all DMA cycles.

(READY)

Ready: This asynchronous input is used to elongate the memory read and write cycles in the 8257 with wait states if the selected memory requires longer cycles.

(HRQ)

Hold Request: This output requests control of the system bus. In systems with only one 8257, HRQ will normally be applied to the HOLD input on the CPU.

(HLDA)

Hold Acknowledge: This input from the CPU indicates that the 8257 has acquired control of the system bus.

($\overline{\text{MEMR}}$)

Memory Read: This active-low three-state output is used to read data from the addressed memory location during DMA Read cycles.

($\overline{\text{MEMW}}$)

Memory Write: This active-low three-state output is used to write data into the addressed memory location during DMA Write cycles.

(ADSTB)

Address Strobe: This output strobes the most significant byte of the memory address into the 8212 device from the data bus.

(AEN)

Address Enable: This output is used to disable (float) the System Data Bus and the System Control Bus. It may also be used to disable (float) the System Address Bus by use of an enable on the Address Bus drivers in systems to inhibit non-DMA devices from responding during DMA cycles. It may be further used to isolate the 8257 data bus from the System Data Bus to facilitate the transfer of the 8 most significant DMA address bits over the 8257 data I/O pins without subjecting the System Data Bus to any timing constraints for the transfer. When the 8257 is used in an I/O device structure (as opposed to memory mapped), this AEN output should be used to disable the selection of an I/O device when the DMA address is on the address bus. The I/O device selection should be determined by the DMA acknowledge outputs for the 4 channels.

(TC)

Terminal Count: This output notifies the currently selected peripheral that the present DMA cycle should be the last cycle for this data block. If the TC STOP bit in the Mode Set register is set, the selected channel will be automatically disabled at the end of that DMA cycle. TC is activated when the 14-bit value in the selected channel's terminal count register equals zero. Recall that the low-order 14-bits of the terminal count register should be loaded with the values (n-1), where n = the desired number of the DMA cycles.

(MARK)

Modulo 128 Mark: This output notifies the selected peripheral that the current DMA cycle is the 128th cycle since the previous MARK output. MARK always occurs at 128 (and all multiples of 128) cycles from the end of the data block. Only if the total number of DMA cycles (n) is evenly divisable by 128 (and the terminal count register was loaded with n-1), will MARK occur at 128 (and each succeeding multiple of 128) cycles from the beginning of the data block.

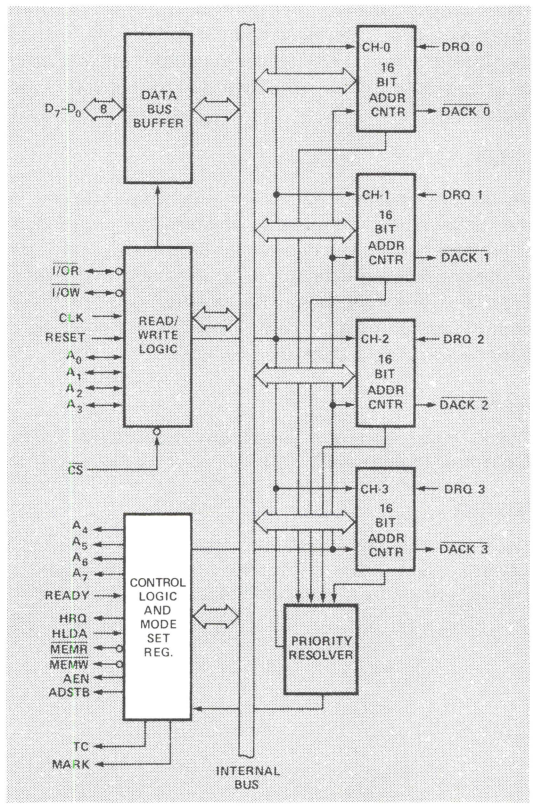

Figure 4. 8257 Block Diagram Showing Control Logic and Mode Set Register

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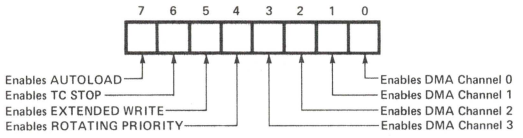
5. Mode Set Register

When set, the various bits in the Mode Set register enable each of the four DMA channels, and allow four different options for the 8257:

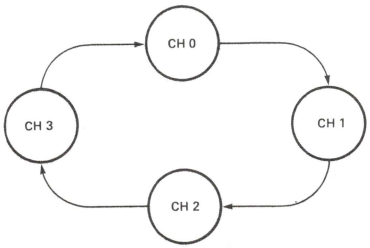


The Mode Set register is normally programmed by the CPU after the DMA address register(s) and terminal count register(s) are initialized. The Mode Set Register is cleared by the RESET input, thus disabling all options, inhibiting all channels, and preventing bus conflicts on power-up. A channel should not be left enabled unless its DMA address and terminal count registers contain valid values; otherwise, an inadvertent DMA request (DRQn) from a peripheral could initiate a DMA cycle that would destroy memory data.

The various options which can be enabled by bits in the Mode Set register are explained below:

Rotating Priority Bit 4

In the Rotating Priority Mode, the priority of the channels has a circular sequence. After each DMA cycle, the priority of each channel changes. The channel which had just been serviced will have the lowest priority.



If the ROTATING PRIORITY bit is not set (set to a zero), each DMA channel has a fixed priority. In the fixed priority mode, Channel 0 has the highest priority and Channel 3 has the lowest priority. If the ROTATING PRIORITY bit is set to a one, the priority of each channel changes after each DMA cycle (not each DMA request). Each channel moves up to the next highest priority assignment, while the channel which has just been serviced moves to the lowest priority assignment:

	CHANNEL → JUST SERVICED	CH-0	CH-1	CH-2	CH-3
Priority → Assignments	Highest	CH-1	CH-2	CH-3	CH-0
	↑	CH-2	CH-3	CH-0	CH-1
	↓	CH-3	CH-0	CH-1	CH-2
	Lowest	CH-0	CH-1	CH-2	CH-3

Note that rotating priority will prevent any one channel from monopolizing the DMA mode; consecutive DMA cycles will service different channels if more than one channel is enabled and requesting service. All DMA operations began with Channel 0 initially assigned to the highest priority for the first DMA cycle.

Extended Write Bit 5

If the EXTENDED WRITE bit is set, the duration of both the $\overline{\text{MEMW}}$ and $\overline{\text{I/OW}}$ signals is extended by activating them earlier in the DMA cycle. Data transfers within microcomputer systems proceed asynchronously to allow use of various types of memory and I/O devices with different access times. If a device cannot be accessed within a specific amount of time it returns a "not ready" indication to the 8257 that causes the 8257 to insert one or more wait states in its internal sequencing. Some devices are fast enough to be accessed without the use of wait states, but if they generate their READY response with the leading edge of the $\overline{\text{I/OW}}$ or $\overline{\text{MEMW}}$ signal (which generally occurs late in the transfer sequence), they would normally cause the 8257 to enter a wait state because it does not receive READY in time. For systems with these types of devices, the Extended Write option provides alternative timing for the I/O and memory write signals which allows the devices to return an early READY and prevents the unnecessary occurrence of wait states in the 8257, thus increasing system throughput.

TC Stop Bit 6

If the TC STOP bit is set, a channel is disabled (i.e., its enable bit is reset) after the Terminal Count (TC) output goes true, thus automatically preventing further DMA operation on that channel. The enable bit for that channel must be re-programmed to continue or begin another DMA operation. If the TC STOP bit is not set, the occurrence of the TC output has no effect on the channel enable bits. In this case, it is generally the responsibility of the peripheral to cease DMA requests in order to terminate a DMA operation.

Auto Load Bit 7

The Auto Load mode permits Channel 2 to be used for repeat block or block chaining operations, without immediate software intervention between blocks. Channel 2 registers are initialized as usual for the first data block; Channel 3 registers, however, are used to store the block re-initialization parameters (DMA starting address, terminal count and DMA transfer mode). After the first block of DMA cycles is executed by Channel 2 (i.e., after the TC output goes true), the parameters stored in the Channel 3 registers are transferred to Channel 2 during an "update" cycle. Note that the TC STOP feature, described above, has no effect on Channel 2 when the Auto Load bit is set.

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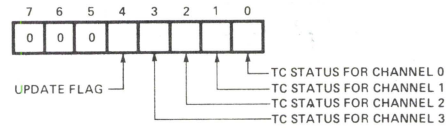
If the Auto Load bit is set, the initial parameters for Channel 2 are automatically duplicated in the Channel 3 registers when Channel 2 is programmed. This permits repeat block operations to be set up with the programming of a single channel. Repeat block operations can be used in applications such as CRT refreshing. Channels 2 and 3 can still be loaded with separate values if Channel 2 is loaded before loading Channel 3. Note that in the Auto Load mode, Channel 3 is still available to the user if the Channel 3 enable bit is set, but use of this channel will change the values to be auto loaded into Channel 2 at update time. All that is necessary to use the Auto Load feature for chaining operations is to reload Channel 3 registers at the conclusion of each update cycle with the new parameters for the next data block transfer.

Each time that the 8257 enters an update cycle, the update flag in the status register is set and parameters in Channel 3 are transferred to Channel 2, non-destructively for Channel 3. The actual re-initialization of Channel 2 occurs at the beginning of the next channel 2 DMA cycle after the TC cycle. This will be the first DMA cycle of the new data block for Channel 2. The update flag is cleared at the conclusion of this DMA cycle. For chaining operations, the update flag in the status register can be monitored by the CPU to determine when the re-initialization process has been completed so that the next block parameters can be safely loaded into Channel 3.

6. Status Register

The eight-bit status register indicates which channels have reached a terminal count condition and includes the update flag described previously.



The TC status bits are set when the Terminal Count (TC) output is activated for that channel. These bits remain set until the status register is read or the 8257 is reset. The UPDATE FLAG, however, is not affected by a status register read operation. The UPDATE FLAG can be cleared by resetting the 8257, by changing to the non-auto load mode (i.e., by resetting the AUTO LOAD bit in the Mode Set register) or it can be left to clear itself at the completion of the update cycle. The purpose of the UPDATE FLAG is to prevent the CPU from inadvertently skipping a data block by overwriting a starting address or terminal count in the Channel 3 registers before those parameters are properly auto-loaded into Channel 2.

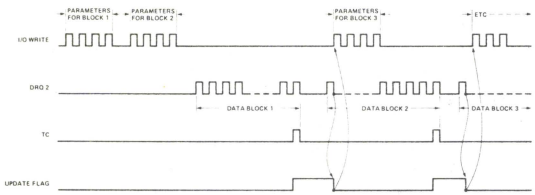


Figure 5. Autoload Timing

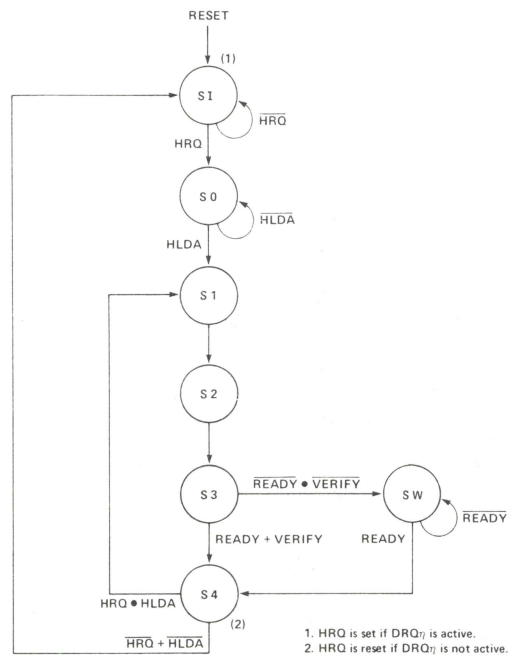


Figure 6. DMA Operation State Diagram

8257 Register Selection

REGISTER	BYTE	ADDRESS INPUTS A3	A2	A1	A0	F/L	*BI-DIRECTIONAL DATA BUS D7	D6	D5	D4	D3	D2	D1	D0
CH-0 DMA Address	LSB	0	0	0	0	0	A7	A6	A5	A4	A3	A2	A1	A0
	MSB	0	0	0	0	1	A15	A14	A13	A12	A11	A10	A9	A8
CH-0 Terminal Count	LSB	0	0	0	1	0	C7	C6	C5	C4	C3	C2	C1	C0
	MSB	0	0	0	1	1	Rd	Wr	C13	C12	C11	C10	C9	C8
CH-1 DMA Address	LSB	0	0	1	0	0	Same as Channel 0							
	MSB	0	0	1	0	1								
CH-1 Terminal Count	LSB	0	0	1	1	0								
	MSB	0	0	1	1	1								
CH-2 DMA Address	LSB	0	1	0	0	0	Same as Channel 0							
	MSB	0	1	0	0	1								
CH-2 Terminal Count	LSB	0	1	0	1	0								
	MSB	0	1	0	1	1								
CH-3 DMA Address	LSB	0	1	1	0	0	Same as Channel 0							
	MSB	0	1	1	0	1								
CH-3 Terminal Count	LSB	0	1	1	1	0								
	MSB	0	1	1	1	1								
MODE SET (Program only)	—	1	0	0	0	0	AL	TCS	EW	RP	EN3	EN2	EN1	EN0
STATUS (Read only)	—	1	0	0	0	0	0	0	0	UP	TC3	TC2	TC1	TC0

*A_7-A_{15}: DMA Starting Address, C_7-C_{13}: Terminal Count value (N-1), Rd and Wr: DMA Verify (00), Write (01) or Read (10) cycle selection, AL: Auto Load, TCS: TC STOP, EW: EXTENDED WRITE, RP: ROTATING PRIORITY, EN3-EN0: CHANNEL ENABLE MASK, UP: UPDATE FLAG, TC3-TC0: TERMINAL COUNT STATUS BITS.

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Programming and Reading the 8257 Registers

There are four pairs of "channel registers": each pair consisting of a 16-bit DMA address register and a 16-bit terminal count register (one pair for each channel). The 8257 also includes two "general registers": one 8-bit Mode Set register and one 8-bit Status register. The registers are loaded or read when the CPU executes a write or read instruction that addresses the 8257 device and the appropriate register within the 8257. The 8228 generates the appropriate read or write control signal (generally I/OR or I/OW while the CPU places a 16-bit address on the system address bus, and either outputs the data to be written onto the system data bus or accepts the data being read from the data bus. All or some of the most significant 12 address bits A_4-A_{15} (depending on the systems memory, I/O configuration) are usually decoded to produce the chip select ($\overline{CS}$) input to the 8257. An I/O Write input (or Memory Write in memory mapped I/O configurations, described below) specifies that the addressed register is to be programmed, while an I/O Read input (or Memory Read) specifies that the addressed register is to be read. Address bit 3 specifies whether a "channel register" ($A_3 = 0$) or the Mode Set (program only)/Status (read only) register ($A_3 = 1$) is to be accessed.

The least significant three address bits, A_0-A_2, indicate the specific register to be accessed. When accessing the Mode Set or Status register, A_0-A_2 are all zero. When accessing a channel register bit A_0 differentiates between the DMA address register ($A_0 = 0$) and the terminal count register ($A_0 = 1$), while bits A_1 and A_2 specify one of the four channels. Because the "channel registers" are 16-bits, two program instruction cycles are required to load or read an entire register. The 8257 contains a first/last (F/L) flip flop which toggles at the completion of each channel program or read operation. The F/L flip flop determines whether the upper or lower byte of the register is to be accessed. The F/L flip flop is reset by the RESET input and whenever the Mode Set register is loaded. To maintain proper synchronization when accessing the "channel registers" all channel command instruction operations should occur in pairs, with the lower byte of a register always being accessed first. Do not allow $\overline{CS}$ to clock while either $\overline{I/OR}$ or $\overline{I/OW}$ is active, as this will cause an erroneous F/L flip flop state. In systems utilizing an interrupt structure, interrupts should be disabled prior to any paired programming operations to prevent an interrupt from splitting them. The result of such a split would leave the F/L F/F in the wrong state. This problem is particularly obvious when other DMA channels are programmed by an interrupt structure.

CONTROL INPUT	$\overline{CS}$	$\overline{I/OW}$	$\overline{I/OR}$	A_3
Program Half of a Channel Register	0	0	1	0
Read Half of a Channel Register	0	1	0	0
Program Mode Set Register	0	0	1	1
Read Status Register	0	1	0	1

DMA Operation

Internal 8257 operations may proceed through seven different states. The duration of a state is defined by the clock input. When the 8257 is not executing a DMA cycle, it is in the idle state, S_I. A DMA cycle begins when one or more DMA Request (DRQn) lines become active. The 8257 then enters state S_0, sends a Hold Request (HRQ) to the CPU and waits for as many S_0 states as are necessary for the CPU to return a Hold Acknowledge (HLDA). For each S_0 state, the DMA Request lines are again sampled and DMA priority is resolved (according to the fixed or rotating priority scheme). When HLDA is received, the DMA Acknowledge ($\overline{DACKn}$) line for the highest priority requesting channel is activated, thus selecting that channel and its peripheral for the DMA cycle. The 8257 then proceeds to state S_1. Note that the DMA Request (DRQn) input should remain high until either $\overline{DACKn}$ is received for a single DMA cycle service, or until both the $\overline{DACKn}$ and TC outputs are received when transferring an entire data block in a "burst" mode. If the 8257 should lose control of the system bus (i.e., if HLDA goes false), the DMA Acknowledge will be removed after the current DMA cycle is completed and no more DMA cycles will occur until the 8257 again acquires control of the system bus.

Each DMA cycle will consist of at least four internal states: S_1, S_2, S_3, and S_4. If the access time for the memory or I/O devices involved is not fast enough to return the required READY response and complete a byte transfer within the specified amount of time, one or more wait states (SW) are inserted between states S_3 and S_4. Recall that in certain cases the Extended Write option can eliminate the need for a wait state. Note that a READY response is not required during DMA verify cycles. Specified minimum/maximum values for READY setup time (t_{RS}), write data setup time (t_{DW}), read data access time (t_{RD}) and HLDA setup time (t_{QS}) are listed under A.C. CHARACTERISTICS and are illustrated in the accompanying timing diagrams.

During DMA write cycles, the I/O Read ($\overline{I/OR}$) output is generated at the beginning of state S_2 and the Memory Write ($\overline{MEMW}$) output is generated at the beginning of S_3. During DMA read cycles, the Memory Read ($\overline{MEMR}$) output is generated at the beginning of state S_2 and the I/O Write (I/OW) output goes true at the beginning of of state S_3. Recall that no read or write control signals are generated during DMA verify cycles. Extended $\overline{WR}$ for MEM and I/O will be generated in S_2.

Memory Mapped I/O Configurations

The 8257 can be connected to the system bus as a memory device instead of as an I/O device for memory mapped I/O configurations by connecting the system memory control lines to the 8257's I/O control lines and the system I/O control lines to the 8257's memory control lines.

This configuration permits use of the 8080's considerably larger repertoire of memory instructions when reading or loading the 8257's registers. Note that with this connection, the programming of the Read (bit 15) and Write (bit 14) bits in the terminal count register will have a different meaning:

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

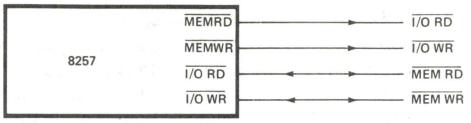


Figure 7. System Interface for Memory Mapped I/O

BIT 15 READ	BIT 14 WRITE	
0	0	DMA Verify Cycle
0	1	DMA Read Cycle
1	0	DMA Write Cycle
1	1	Illegal

Figure 8. TC Register for Memory Mapped I/O Only

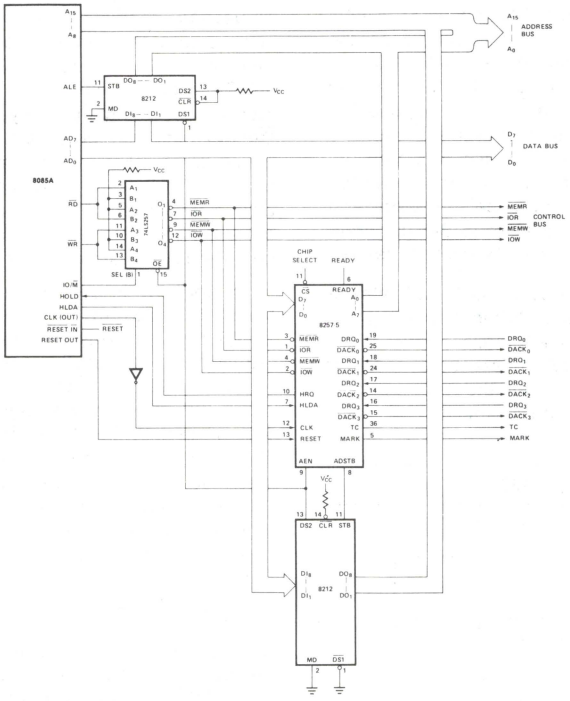


Figure 9. Detailed System Interface Schematic

SYSTEM APPLICATION EXAMPLES

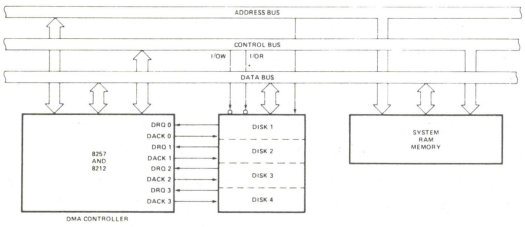


Figure 10. Floppy Disk Controller (4 Drives)

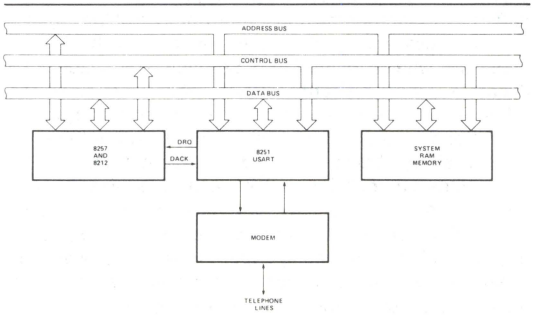


Figure 11. High-Speed Communication Controller

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . 0°C to 70°C
Storage Temperature . . . . . .–65°C to +150°C
Voltage on Any Pin
With Respect to Ground . . . . . –0.5V to +7V
Power Dissipation . . . . . 1 Watt

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ± 5%, GND = 0V

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	Volts	
V_{IH}	Input High Voltage	2.0	V_{CC}+.5	Volts	
V_{OL}	Output Low Voltage		0.45	Volts	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage	2.4	V_{CC}	Volts	I_{OH}=-150μA for AB, DB and AEN I_{OH}=-80μA for others
V_{HH}	HRQ Output High Voltage	3.3	V_{CC}	Volts	I_{OH} = -80μA
I_{CC}	V_{CC} Current Drain		120	mA	
I_{IL}	Input Leakage		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Leakage During Float		±10	μA	V_{OUT} = V_{CC} to 0V

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
C_{IN}	Input Capacitance			10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

A.C. CHARACTERISTICS: PRIPHERAL (SLAVE) MODE

T_A = 0°C to 70°C, V_{CC} = 5.0V ±5%; GND = 0V (Note 1).

8080 Bus Parameters

Read Cycle:

Symbol	Parameter	8257 Min.	8257 Max.	8257-5 Min.	8257-5 Max.	Unit	Test Conditions
T_{AR}	Adr or $\overline{CS}\downarrow$ Setup to $\overline{RD}\downarrow$	0		0		ns	
T_{RA}	Adr or $\overline{CS}\uparrow$ Hold from $\overline{RD}\uparrow$	0		0		ns	
T_{RD}	Data Access from $\overline{RD}\downarrow$	0	300	0	200	ns	(Note 2)
T_{DF}	DB→Float Delay from $\overline{RD}\uparrow$	20	150	20	100	ns	
T_{RR}	$\overline{RD}$ Width	250		250		ns	

Write Cycle:

Symbol	Parameter	8257 Min.	8257 Max.	8257-5 Min.	8257-5 Max.	Unit	Test Conditions
T_{AW}	Adr Setup to $\overline{WR}\downarrow$	20		20		ns	
T_{WA}	Adr Hold from $\overline{WR}\uparrow$	0		0		ns	
T_{DW}	Data Setup to $\overline{WR}\uparrow$	200		200		ns	
T_{WD}	Data Hold from $\overline{WR}\uparrow$	0		0		ns	
T_{WW}	$\overline{WR}$ Width	200		200		ns	

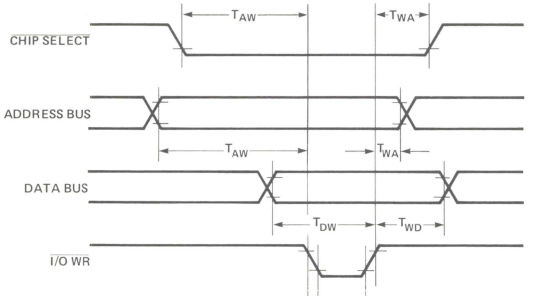
Other Timing:

Symbol	Parameter	8257 Min.	8257 Max.	8257-5 Min.	8257-5 Max.	Unit	Test Conditions
T_{RSTW}	Reset Pulse Width	300		300		ns	
T_{RSTD}	Power Supply↑ (V_{CC}) Setup to Reset↓	500		500		μs	
T_r	Signal Rise Time		20		20	ns	
T_f	Signal Fall Time		20		20	ns	
T_{RSTS}	Reset to First $\overline{IOWR}$	2		2		t_{CY}	

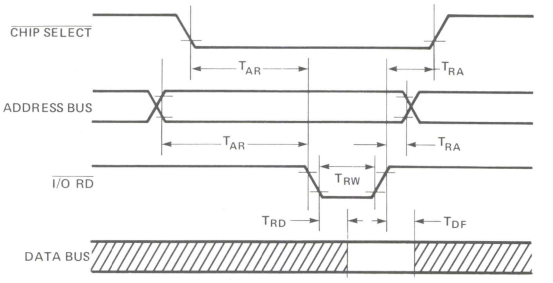
Notes: 1. All timing measurements are made at the following reference voltages unless specified otherwise: Input "1" at 2.0V, "0" at 0.8V
Output "1" at 2.0V, "0" at 0.8V
2. 8257: C_L = 100pF, 8257-5: C_L = 150pF.

8257 PERIPHERAL MODE TIMING DIAGRAMS

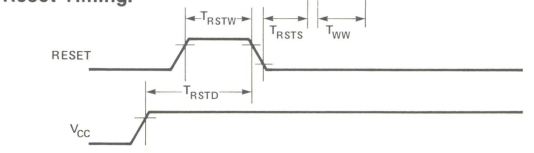
Write Timing:



Read Timing:



Reset Timing:



Input Waveform for A.C. Tests:

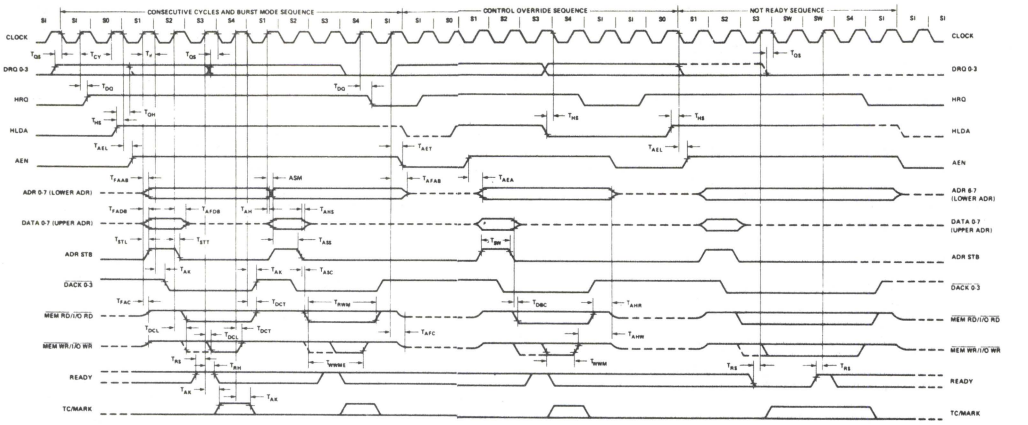
PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

A.C. CHARACTERISTICS: DMA (MASTER) MODE $T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 5\%$, GND = 0V

SYMBOL	PARAMETER	8257		8257-5		UNIT
		MIN.	MAX.	MIN.	MAX.	
T_{CY}	Cycle Time (Period)	0.320	4	320	4	μs
$T\theta$	Clock Active (High)	120	$.8T_{CY}$	80	$.8T_{CY}$	ns
T_{QS}	DRQ↑ Setup to θ↓(SI,S4)	120		120		
T_{QH}	DRQ↓ Hold from HLDA↑[4]	0		0		
T_{DQ}	HRQ↑ or ↓Delay from θ↑(SI,S4) (measured at 2.0V)[1]		160		160	ns
T_{DQ1}	HRQ↑ or ↓Delay from θ↑(SI,S4) (measured at 3.3V)[3]		250		250	ns
T_{HS}	HLDA↑ or ↓Setup to θ↓(SI,S4)	100		100		ns
T_{AEL}	AEN↑ Delay from θ↓(S1)[1]		300		300	ns
T_{AET}	AEN↓ Delay from θ↑(SI)[1]		200		200	ns
T_{AEA}	Adr(AB)(Active) Delay from AEN↑(S1)[4]	20		20		ns
T_{FAAB}	Adr(AB)(Active) Delay from θ↑(S1)[2]		250		250	ns
T_{AFAB}	Adr(AB)(Float) Delay from θ↑(SI)[2]		150		150	ns
T_{ASM}	Adr(AB)(Stable) Delay from θ↑(S1)[2]		250		250	ns
T_{AH}	Adr(AB)(Stable) Hold from θ↑(S1)[2]	$T_{ASM}-50$		$T_{ASM}-50$		
T_{AHR}	Adr(AB)(Valid) Hold from $\overline{Rd}$↑(S1,SI)[4]	60		60		ns
T_{AHW}	Adr(AB)(Valid) Hold from $\overline{Wr}$↑(S1,SI)[4]	300		300		ns
T_{FADB}	Adr(DB)(Active) Delay from θ↑(S1)[2]		300		300	ns
T_{AFDB}	Adr(DB)(Float) Delay from θ↑(S2)[2]	$T_{STT}+20$	250	$T_{STT}+20$	170	ns
T_{ASS}	Adr(DB) Setup to AdrStb↓(S1-S2)[4]	100		100		ns
T_{AHS}	Adr(DB)(Valid) Hold from AdrStb↓(S2)[4]	50		50		ns
T_{STL}	AdrStb↑ Delay from θ↑(S1)[1]		200		200	ns
T_{STT}	AdrStb↓ Delay from θ↑(S2)[1]		140		140	ns
T_{SW}	AdrStb Width (S1-S2)[4]	$T_{CY}-100$		$T_{CY}-100$		ns
T_{ASC}	$\overline{Rd}$↓ or $\overline{Wr}$(Ext)↓ Delay from AdrStb↓(S2)[4]	70		70		ns
T_{DBC}	$\overline{Rd}$↓ or $\overline{Wr}$(Ext)↓ Delay from Adr(DB) (Float)(S2)[4]	20		20		ns
T_{AK}	DACK↑ or ↓Delay from θ↓(S2,S1) and TC/Mark↑ Delay from θ↑(S3) and TC/Mark↓ Delay from θ↑(S4)[1,5]		250		250	ns
T_{DCL}	$\overline{Rd}$↓ or $\overline{Wr}$(Ext)↓ Delay from θ↑(S2) and $\overline{Wr}$↓ Delay from θ↑(S3)[2,6]		200		200	ns
T_{DCT}	$\overline{Rd}$↑ Delay from θ↓(S1,SI) and $\overline{Wr}$↑ Delay from θ↑(S4)[2,7]		200		200	ns
T_{FAC}	$\overline{Rd}$ or $\overline{Wr}$ (Active) from θ↑(S1)[2]		300		300	ns
T_{AFC}	$\overline{Rd}$ or $\overline{Wr}$ (Float) from θ↑(SI)[2]		150		150	ns
T_{RWM}	$\overline{Rd}$ Width (S2-S1 or SI)[4]	$2T_{CY}+T_\theta-50$		$2T_{CY}+T_\theta-50$		ns
T_{WWM}	$\overline{Wr}$ Width (S3-S4)[4]	$T_{CY}-50$		$T_{CY}-50$		ns
T_{WWME}	$\overline{Wr}$(Ext) Width (S2-S4)[4]	$2T_{CY}-50$		$2T_{CY}-50$		ns
T_{RS}	READY Set Up Time to θ↑ (S3, Sw)	30		30		ns
T_{RH}	READY Hold Time from θ↑ (S3, Sw)	20		20		ns

Notes: 1. Load = 1 TTL. 2. Load = 1 TTL + 50pF. 3. Load = 1 TTL + (R_L = 3.3K), V_{OH} = 3.3V. 4. Tracking Specification. 5. $\Delta T_{AK} < 50$ ns. 6. $\Delta T_{DCL} < 50$ ns. 7. $\Delta T_{DCT} < 50$ ns.

DMA MODE WAVEFORMS



PRELIMINARY
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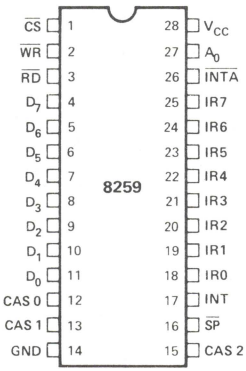
8259/8259-5
PROGRAMMABLE INTERRUPT CONTROLLER

- MCS-85™ Compatible 8259-5
- 8-Level Priority Controller
- Expandable to 64 Levels
- Programmable Interrupt Modes
- Individual Request Mask Capability
- Single +5V Supply (No Clocks)
- 28-Pin Dual In-Line Package

The Intel® 8259 handles up to 8 vectored priority interrupts for the CPU. It is cascadable for up to 64 vectored priority interrupts, without additional circuitry. It will be packaged in a 28-pin plastic DIP, uses nMOS technology and requires a single +5V supply. Circuitry is static, requiring no clock input.

The 8259 is designed to minimize the software and real time overhead in handling multi-level priority interrupts. It has several modes, permitting optimization for a variety of system requirements.

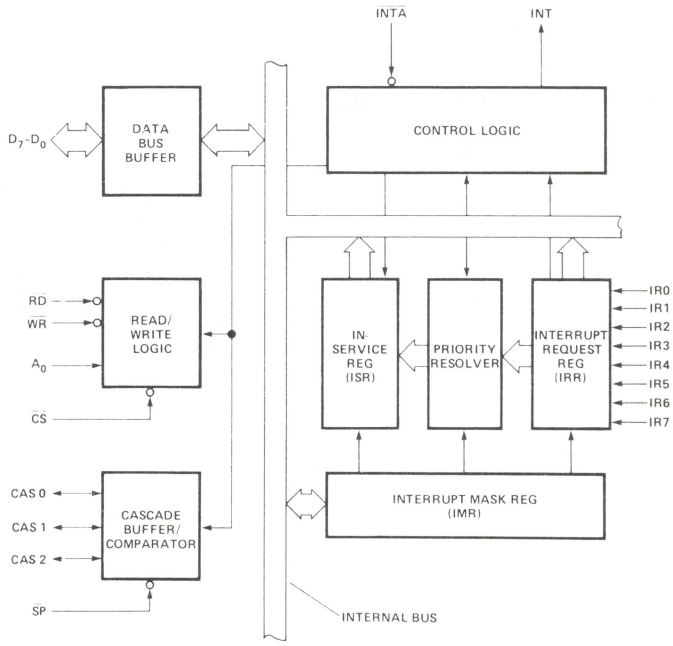
PIN CONFIGURATION



PIN NAMES

D_7-D_0	DATA BUS (BI-DIRECTIONAL)
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A_0	COMMAND SELECT ADDRESS
$\overline{CS}$	CHIP SELECT
CAS1-CAS0	CASCADE LINES
$\overline{SP}$	SLAVE PROGRAM INPUT
INT	INTERRUPT OUTPUT
$\overline{INTA}$	INTERRUPT ACKNOWLEDGE INPUT
IR0-IR7	INTERRUPT REQUEST INPUTS

BLOCK DIAGRAM



MPU PERIPHERALS

INTRODUCTION TO THE USE OF INTERRUPTS IN MICROCOMPUTER SYSTEMS

Microcomputer system design requires that I/O devices such as keyboards, displays, sensors and other components receive servicing in an efficient method so that large amounts of the total system tasks can be assumed by the microcomputer with little or no effect on throughput.

The most common method of servicing such devices is the **Polled** approach. This is where the processor must test each device in sequence and in effect "ask" each one if it needs servicing. It is easy to see that a large portion of the main program is looping through this continuence polling cycle and that such a method would have a serious, detrimental effect on system throughput thus limiting the tasks that could be assumed by the microcomputer and reducing the cost effectiveness of using such devices.

A more desireable method would be one that would allow the microprocessor to be executing its main program and only stop to service peripheral devices when it is told to do so by the device itself. In effect, the method would provide an external asynchronous input that would inform the processor that it should complete whatever instruction that is currently being executed and fetch a new routine that will service the requesting device. Once this servicing is complete however the processor would resume exactly where it left off.

This method is called **Interrupt**. It is easy to see that system throughput would drastically increase, and thus more tasks could be assumed by the microcomputer to further enhance its cost effectiveness.

The Programmable Interrupt Controller (PIC) functions as an overall manager in an Interrupt-Driven system environment. It accepts requests from the peripheral equipment, determines which of the incoming requests is of the highest importance (priority), ascertains whether the incoming request has a higher priority value than the level currently being serviced and issues an Interrupt to the CPU based on this determination.

Each peripheral device or structure usually has a special program or "routine" that is associated with its specific functional or operational requirements; this is referred to as a "service routine". The PIC, after issuing an Interrupt to the CPU, must somehow input information into the CPU that can "point" the Program Counter to the service routine associated with the requesting device. The PIC does this by providing the CPU with a 3-byte CALL instruction.

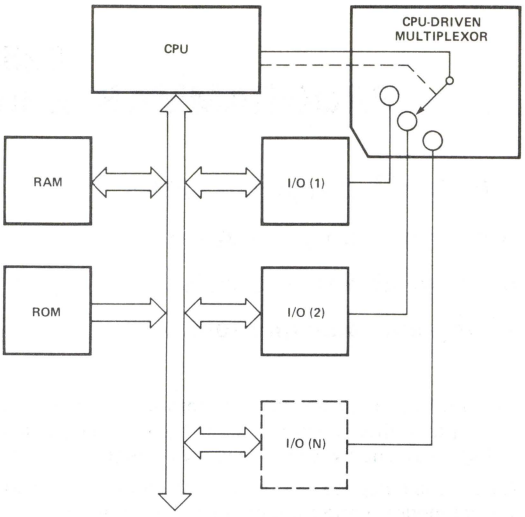


Figure 1. Polled Method

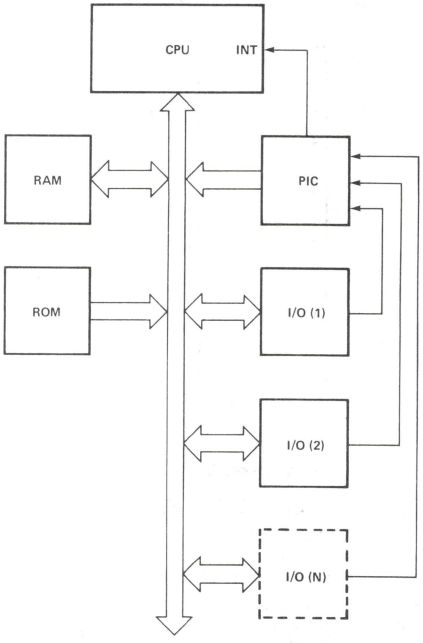


Figure 2. Interrupt Method

Data Bus Buffer

This 3-state, bi-directional, 8-bit buffer is used to interface the 8259 to the system Data Bus. Control words and status information are transferred through the Data Bus Buffer.

Read/Write Control Logic

The function of this block is to accept OUTput commands from the CPU. It contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers which store the various control formats for device operation. This function block also allows the status of the 8259 to be transferred onto the Data Bus.

$\overline{CS}$ (Chip Select)

A "low" on this input enables the 8259. No reading or writing of the chip will occur unless the device is selected.

$\overline{WR}$ (Write)

A "low" on this input enables the CPU to write control words (ICWs and OCWs) to the 8259.

$\overline{RD}$ (Read)

A "low" on this input enables the 8259 to send the status of the Interrupt Request Register (IRR), In Service Register (ISR), the Interrupt Mask Register (IMR) or the BCD of the Interrupt level on to the Data Bus.

A_0

This input signal is used in conjunction with $\overline{WR}$ and $\overline{RD}$ signals to write commands into the various command registers as well as reading the various status registers of the chip. This line can be tied directly to one of the address lines.

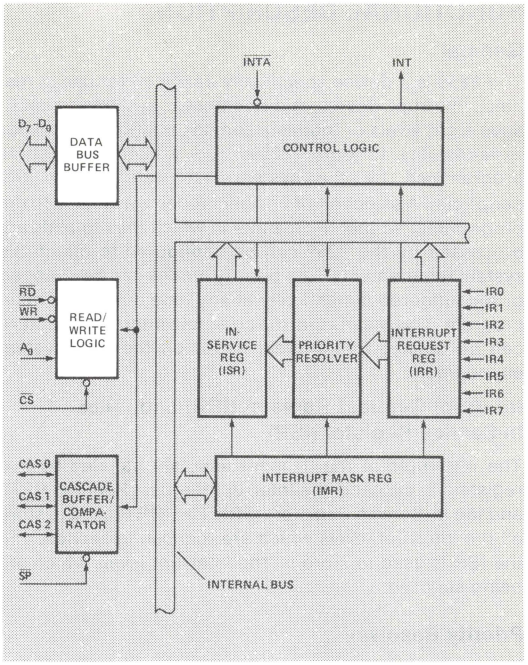


Figure 3. 8259 Block Diagram Showing Data Bus Buffer and Read/Write Logic Functions

A_0	D_4	D_3	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	INPUT OPERATION (READ)
0			0	1	0	IRR, ISR or Interrupting Level ⇒ DATA BUS (Note 1)
1			0	1	0	IMR ⇒ DATA BUS
						OUTPUT OPERATION (WRITE)
0	0	0	1	0	0	DATA BUS ⇒ OCW2
0	0	1	1	0	0	DATA BUS ⇒ OCW3
0	1	X	1	0	0	DATA BUS ⇒ ICW1
1	X	X	1	0	0	DATA BUS ⇒ OCW1, ICW2, ICW3 (Note 2)
						DISABLE FUNCTION
X	X	X	1	1	0	DATA BUS ⇒ 3-STATE
X	X	X	X	X	1	DATA BUS ⇒ 3-STATE

Note 1: Selection of IRR, ISR or Interrupting Level is based on the content of OCW3 written before the READ operation.
Note 2: On-chip sequencer logic queues these commands into proper sequence.

Figure 4. 8259 Basic Operation

FUNCTIONAL DESCRIPTION

General

The 8259 is a device specifically designed for use in real time, interrupt driven, microcomputer systems. It manages eight levels or requests and has built-in features for expandability to other 8259s (up to 64 levels). It is programmed by the system's software as an I/O peripheral. A selection of priority modes is available to the programmer so that the manner in which the requests are processed by the 8259 can be configured to match his system requirements. The priority modes can be changed or reconfigured dynamically at any time during the main program. This means that the complete interrupt structure can be defined as required, based on the total system environment.

Interrupt Request Register (IRR) and rice In-Service Register (ISR)

The interrupts at the IR input lines are handled by two registers in cascade, the Interrupt Request Register (IRR) and the In-Service Register (ISR). The IRR is used to store all the interrupt levels which are requesting service; and the ISR is used to store all the interrupt levels which are being serviced.

Priority Resolver

This logic block determines the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during $\overline{INTA}$ pulse.

INT (Interrupt)

This output goes directly to the CPU interrupt input. The V_{OH} level on this line is designed to be fully compatible with the 8080 input level.

$\overline{INTA}$ (Interrupt Acknowledge)

Three $\overline{INTA}$ pulses will cause the 8259 to release a 3-byte CALL instruction onto the Data Bus.

Interrupt Mask Register (IMR)

The IMR stores the bits of the interrupt lines to be masked. The IMR operates on the ISR. Masking of a higher priority input will not affect the interrupt request lines of lower priority.

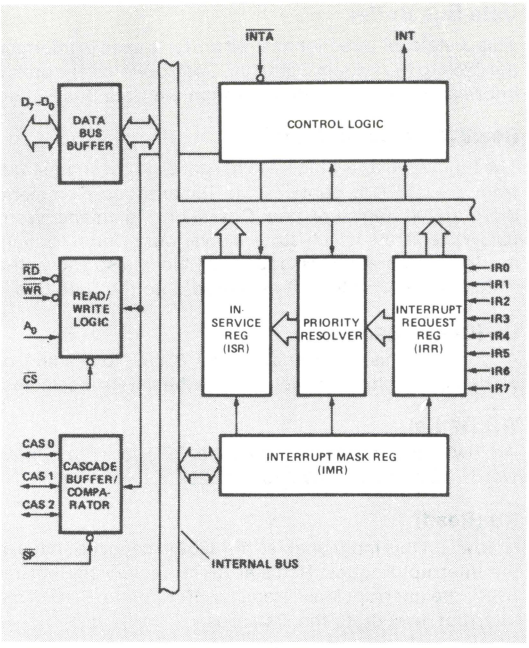


Figure 5. 8259 Block Diagram Showing Basic Interrupt Functions

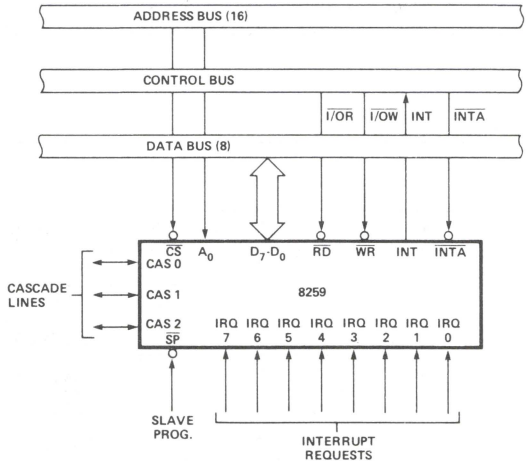


Figure 6. 8259 Interface to Standard System Bus

SP (Slave Program)

More than one 8259 can be used in the system to expand the priority interrupt scheme up to 64 levels. In such case, one 8259 acts as the master, and the others act as slaves. A "high" on the $\overline{SP}$ pin designates the 8259 as the master, a "low" designates it as a slave.

The Cascade/Buffer/Comparator

This function block stores and compares the IDs of all 8259 used in the system. The associated three I/O pins ($\overline{CAS0}$-2) are outputs when the 8259 is used as a master ($\overline{SP}$ = 1), and are inputs when the 8259 is used as a slave ($\overline{SP}$ = 0). As a master, the 8259 sends the ID of the interrupting slave device onto the $\overline{CAS0}$-2 lines. The slave thus selected will send its preprogrammed subroutine addressed onto the Data Bus during next two consecutive $\overline{INTA}$ pulses. (See section "Cascading the 8259".)

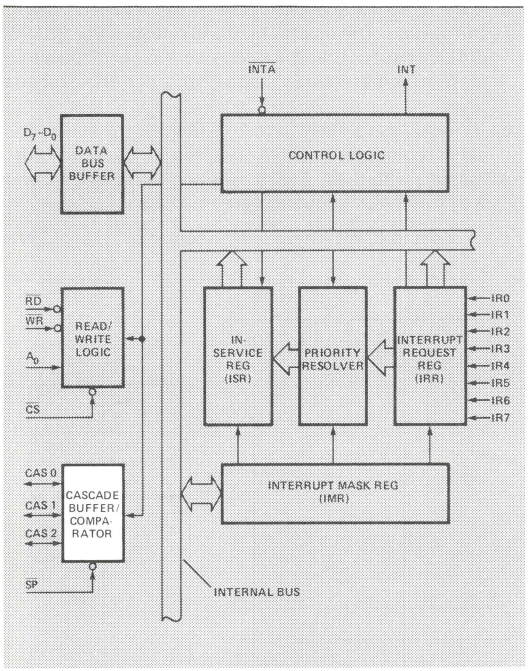


Figure 7. 8259 Block Diagram Showing Cascading Function

OPERATIONAL DESCRIPTION

General

The powerful features of the 8259 in a microcomputer system are its programmability and its utilization of the CALL instruction to jump into any address in the memory map. The normal sequence of events that the 8259 interacts with the CPU is as follows:

1. One or more of the INTERRUPT REQUEST lines (IR7-0) are raised high, setting the corresponding IRR bit(s).
2. The 8259 accepts these requests, resolves the priorities, and sends an INT to the CPU.
3. The CPU acknowledges the INT and responds with an $\overline{INTA}$ pulse.
4. Upon receiving an $\overline{INTA}$ from the CPU group, the highest priority ISR bit is set, and the corresponding IRR bit is reset. The 8259 will also release a CALL instruction code (11001101) onto the 8-bit Data Bus through its D7-0 pins.
5. This CALL instruction will initiate two more $\overline{INTA}$ pulses to be sent to the 8259 from the CPU group.
6. These two $\overline{INTA}$ pulses allow the 8259 to release its preprogrammed subroutine address onto the Data Bus. The lower 8-bit address is released at the first $\overline{INTA}$ pulse and the higher 8-bit address is released at the second $\overline{INTA}$ pulse.
7. This completes the 3-byte CALL instruction released by the 8259. ISR bit is not reset until the end of the subroutine when an EOI (End of interrupt) command is issued to the 8259.

Programming The 8259

The 8259 accepts two types of command words generated by the CPU:

1. Initialization Command Words (ICWs):
   Before normal operation can begin, each 8259 in the system must be brought to a starting point — by a sequence of 2 or 3 bytes timed by $\overline{WR}$ pulses. This sequence is described in Figure 1.
2. Operation Command Words (OCWs):
   These are the command words which command the 8259 to operate in various interrupt modes. These modes are:
   a. Fully nested mode
   b. Rotating priority mode
   c. Special mask mode
   d. Polled mode

The OCWs can be written into the 8259 at anytime after initialization.

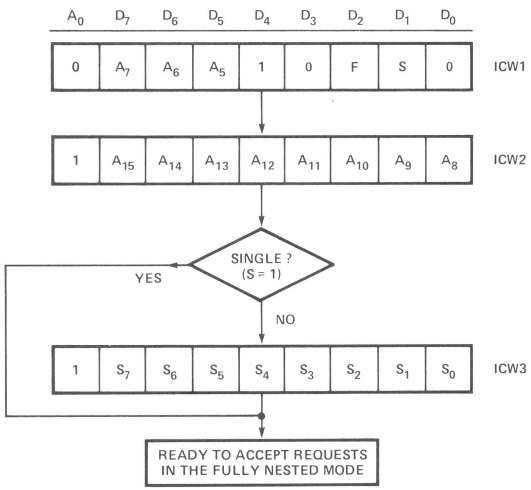


Figure 8. Initialization Sequence

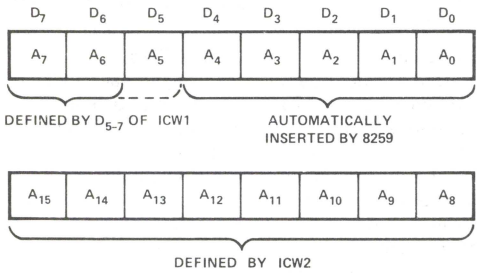
Initialization Command Words 1 and 2 (ICW1 and ICW2)

Whenever a command is issued with A0 = 0 and D4 = 1, this is interpreted as Initialization Command Word 1 (ICW1), and initiates the initialization sequence. During this sequence, the following occur automatically:

a. The edge sense circuit is reset, which means that following initialization, an interrupt request (IR) input must make a low to high transition to generate an interrupt.
b. The interrupt Mask Register is cleared.
c. IR 7 input is assigned priority 7.
d. Special Mask Mode Flip-flop and status Read Flip-flop are reset.

The 8 requesting devices have 8 addresses equally spaced in memory. The addresses can be programmed at intervals of 4 or 8 bytes; the 8 routines thus occupying a page of 32 or 64 bytes respectively in memory.

The address format is:



A0-4 are automatically inserted by the 8259, while A15-6 are programmed by ICW1 and ICW2. When interval = 8, A5 is fixed by the 8259. If interval = 4, A5 is programmed in ICW1. Thus, the interrupt service routines can be located anywhere in the memory space. The 8 byte interval will maintain compatibility with current 8080 RESTART instruction software, while the 4 byte interval is best for compact jump table.

The address format inserted by the 8259 is described in Table 1.

The bits F and S are defined by ICW1 as follows:

F: Call address interval. F = 1, then interval = 4; F = 0, then interval = 8.

S: Single. S = 1 means that this is the only 8259 in the system. It avoids the necesity of programming ICW3.

	INTERVAL = 4 LOWER MEMORY ROUTINE ADDRESS								INTERVAL = 8							
	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
IR 7	A7	A6	A5	1	1	1	0	0	A7	A6	1	1	1	0	0	0
IR 6	A7	A6	A5	1	1	0	0	0	A7	A6	1	1	0	0	0	0
IR 5	A7	A6	A5	1	0	1	0	0	A7	A6	1	0	1	0	0	0
IR 4	A7	A6	A5	1	0	0	0	0	A7	A6	1	0	0	0	0	0
IR 3	A7	A6	A5	0	1	1	0	0	A7	A6	0	1	1	0	0	0
IR 2	A7	A6	A5	0	1	0	0	0	A7	A6	0	1	0	0	0	0
IR 1	A7	A6	A5	0	0	1	0	0	A7	A6	0	0	1	0	0	0
IR 0	A7	A6	A5	0	0	0	0	0	A7	A6	0	0	0	0	0	0

Table 1. 8259 Address Format

Example of Interrupt Acknowledge Sequence

Assume the 8259 is programmed with F = 1 (CALL address interval = 4), and IR5 is the interrupting level. The 3 byte sequence released by the 8259 timed by the $\overline{INTA}$ pulses is as follows:

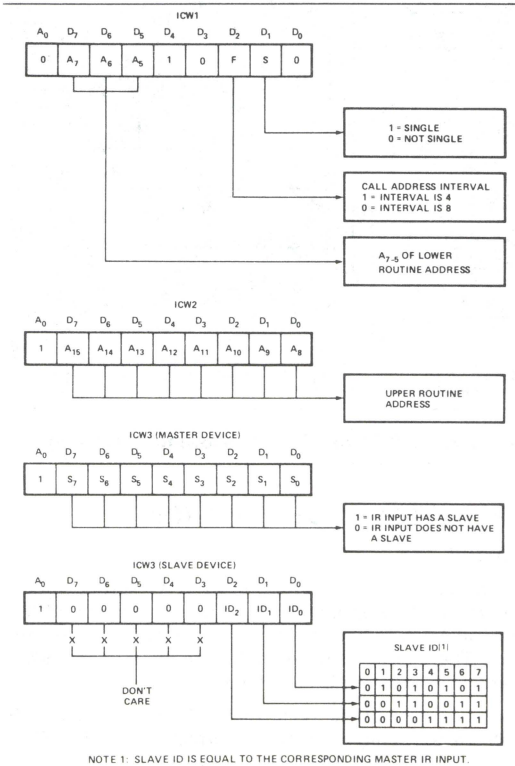
	D7	D6	D5	D4	D3	D2	D1	D0	
1st $\overline{INTA}$	1	1	0	0	1	1	0	1	CALL CODE
2nd $\overline{INTA}$	A7	A6	A5	1	0	1	0	0	LOWER ROUTINE ADDRESS
3rd $\overline{INTA}$	A15	A14	A13	A12	A11	A10	A9	A8	HIGHER ROUTINE ADDRESS

Initialization Command Word 3 (ICW3)

This will load the 8-bit slave register. The functions of this register are as follows:

a. If the 8259 is the master, a "1" is set for each slave in the system. The master then will release byte 1 of the CALL sequence and will enable the corresponding slave to release bytes 2 and 3, through the cascade lines.
b. If the 8259 is a slave, bits 2 - 0 identify the slave. The slave compares its CAS0-2 inputs (sent by the master) with these bits. If they are equal, bytes 2 and 3 of the CALL sequence are released.

If bit S is set in ICW1, there is no need to program ICW3.



NOTE 1: SLAVE ID IS EQUAL TO THE CORRESPONDING MASTER IR INPUT.

Figure 9. Initialization Command Word Format

Operation Command Words (OCWs)

After the Initialization Command Words (ICWs) are programmed into the 8259, the chip is ready to accept interrupt requests at its input lines. However, during the 8259 operation, a selection of algorithms can command the 8259 to operate in various modes through the Operation Command Words (OCWs). These various modes and their associated OCWs are described below.

Interrupt Masks

Each Interrupt Request input can be masked individually by the Interrupt Masked Register (IMR) programmed through OCW1.

The IMR operates on the In-Service Register. Note that if an interrupt is already acknowledged by the 8259 (an $\overline{\text{INTA}}$ pulse has occurred), then the Interrupting level, although masked, will inhibit the lower priorities. To enable these lower priority interrupts, one can do one of two things: (1) Write an End of Interrupt (EOI) command (OCW2) to reset the ISR bit or (2) Set the special mask mode using OCW3 (as will be explained later in the special mask mode.)

Fully Nested Mode

The 8259 will operate in the fully nested mode after the execution of the initialization sequence without any OCW being written. In this mode, the interrupt requests are ordered in priorities from 0 through 7. When an interrupt is acknowledged, the highest priority request is determined and its address vector placed on the bus. In addition, a bit of the Interrupt service register (IS 7-0) is set. This bit remains set until the CPU issues an End of Interrupt (EOI) command immediately before returning from the service routine. While the IS bit is set, all further interrupts of lower priority are inhibited, while higher levels will be able to generate an interrupt (which will only be acknowledged if the CPU has enabled its own interrupt input through software).

After the Initialization sequence, IR0 has the highest priority and IR7 the lowest. Priorities can be changed, as will be explained in the rotating priority mode.

Rotating Priority Commands

There are two variations of rotating priority: auto rotate and specific rotate.

1. Auto Rotate — Executing the Rotate-at-EOI (Auto) command, resets the highest priority ISR bit and assigns that input the lowest priority. Thus, a device requesting an interrupt will have to wait, in the worst case, until 7 other devices are serviced at most once each, i.e., if the priority and "in-service" status is:

BEFORE ROTATE	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
"IS" STATUS	0	1	0	1	0	0	0	0
	LOWEST PRIORITY						HIGHEST PRIORITY	
PRIORITY STATUS	7	6	5	4	3	2	1	0

AFTER ROTATE	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
"IS" STATUS	0	1	0	0	0	0	0	0
	LOWEST PRIORITY						HIGHEST PRIORITY	
PRIORITY STATUS	4	3	2	1	0	7	6	5

In this example, the In-Service FF corresponding to line 4 (the highest priority FF set) was reset and line 4 became the lowest priority, while all the other priorities rotated correspondingly.

The Rotate command is issued in OCW2, where: R = 1, EOI = 1, SEOI = 0.

2. Specific Rotate — The programmer can change priorities by programming the bottom priority, and by doing this, to fix the highest priority: i.e., if IR5 is programmed as the bottom priority device, the IR6 will have the highest one. This command can be used with or without resetting the selected ISR bit.

The Rotate command is issued in OCW2 where: R = 1, SEOI = 1. L2, L1, L0 are the BCD priority level codes of the bottom priority device. If EOI = 1 also, the ISR bit selected by L2-L0 is reset.

Observe that this mode is independent of the End of Interrupt Command and priority changes can be executed during EOI command or independently from the EOI command.

End of Interrupt (EOI) and Specific End of Interrupt (SEOI)

An End of Interrupt command word must be issued to the 8259 before returning from a service routine, to reset the appropriate IS bit.

There are two forms of EOI command: Specific and non-Specific. When the 8259 is operated in modes which preserve the fully nested structure, it can determine which IS bit to reset on EOI. When a non-Specific EOI command is issued the 8259 will automatically reset the highest IS bit of those that are set, since in the nested mode, the highest IS level was necessarily the last level acknowledged and will necessarily be the next routine level returned from.

However, when a mode is used which may disturb the fully nested structure, such as in the rotating priority case, the 8259 may no longer be able to determine the last level acknowledged. In this case, a specific EOI (SEOI) must be issued which includes the IS level to be reset as part of the command. The End of the Interrupt is issued whenever EOI = "1" in OCW2. For specific EOI, SEOI = "1", and EOI = 1. L2, L1, L0 is then the BCD level to be reset. As explained in the Rotate Mode earlier, this can also be the bottom priority code. Note that although the Rotate command can be issued during an EOI = 1, it is not necessarily tied to it.

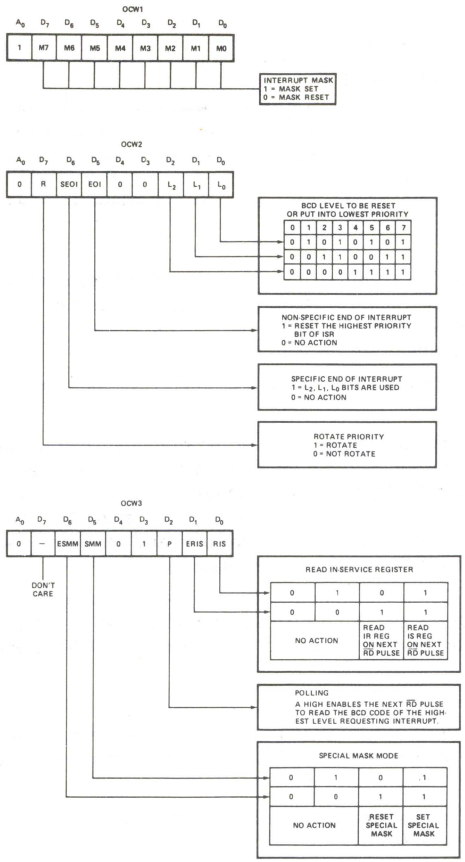


Figure 10. Operation Command Word Format

	A0	D4	D3		
OCW1	1			M7-M0	IMR (Interrupt Mask Register). $\overline{WR}$ will load it while status can be read with $\overline{RD}$.
OCW2	0	0	0	R SEOI EOI	
				0 0 0	No Action.
				0 0 1	Non-specific End of Interrupt.
				0 1 0	No Action.
				0 1 1	Specific End of Interrupt. L2, L1, L0 is the BCD level to be reset.
				1 0 0	No Action.
				1 0 1	Rotate priority at EOI. (Auto Mode)
				1 1 0	Rotate priority, L2, L1, L0 becomes bottom priority without Ending of Interrupt.
				1 1 1	Rotate priority at EOI (Specific Mode), L2, L1, L0 becomes bottom priority, and its corresponding IS FF is reset.
OCW3	0	0	1	ESMM SMM	
				0 0	Special Mask not Affected.
				0 1	
				1 0	Reset Special Mask.
				1 1	Set Special Mask.
				ERIS RIS	
				0 0	No Action.
				0 1	
				1 0	Read IR Register Status.
				1 1	Read IS Register Status.

Note: The CPU interrupt input must be disabled during:
1. Initialization sequence for all the 8259 in the system.
2. Any control command execution.

Figure 11. Summary of Operation Word Programming

Special Mask Mode (SMM)

This mode is useful when some bit(s) are set (masked) by the Interrupt Mask Register (IMR) through OCW1. If, for some reason, we are currently in an interrupt service routine which is masked (this could happen when the subroutine intentionally mask itself off), it is still possible to enable the lower priority lines by setting the Special Mask mode. In this mode the lower priority lines are enabled until the SMM is reset. The higher priorities are not affected.

The special mask mode FF is set by OCW3 where ESMM = 1, SMM = 1, and reset where: ESSM = 1 and SMM = 0.

Polled Mode

In this mode, the CPU must disable its interrupt input. Service to device is achieved by programmer initiative by a Poll command.

The poll command is issued by setting P = "1" in OCW3 during a $\overline{WR}$ pulse.

The 8259 treats the next $\overline{RD}$ pulse as an interrupt acknowledge, sets the appropriate IS Flip-flop, if there is a request, and reads the priority level.

For polling operation, an OCW3 must be written before every read.

The word enabled onto the data bus during $\overline{RD}$ is:

D7	D6	D5	D4	D3	D2	D1	D0
I	–	–	–	–	W2	W1	W0

W0 — 2: BCD code of the highest priority level requesting service.

I: Equal to a "1" if there is an interrupt.

This mode is useful if there is a routine common to several levels — so that the $\overline{INTA}$ sequence is not needed (and this saves ROM space). Another application is to use the poll mode to expand the number of priority levels to more than 64.

Reading 8259 Status

The input status of several internal registers can be read to update the user information on the system. The following registers can be read by issuing a suitable OCW3 and reading with $\overline{RD}$.

Interrupt Requests Register (IRR): 8-bit register which contains the levels requesting an interrupt to be acknowledged. The highest request level is reset from the IRR when an interrupt is acknowledged. (Not affected by IMR).

In Service Register (ISR): 8-bit register which contains the priority levels that are being serviced. The ISR is updated when an End of Interrupt command is issued.

Interrupt Mask Register: 8-bit register which contains the interrupt request lines which are masked.

The IRR can be read when prior to the $\overline{RD}$ pulse, an $\overline{WR}$ pulse is issued with OCW3, and ERIS = 1, RIS = 0.

The ISR can be read in a similar mode, when ERIS = 1, RIS = 1.

There is no need to write an OCW3 before every status read operation as long as the status read corresponds with the previous one, i.e. the 8259 "remembers" whether the IRR or ISR has been previously selected by the OCW3.

For reading the IMR, a $\overline{WR}$ pulse is not necessary to preceed the $\overline{RD}$. The output data bus will contain the IMR whenever $\overline{RD}$ is active and A0 = 1.

Polling overrides status read when P = 1, ERIS = 1 in OCW3.

Cascading

The 8259 can be easily interconnected in a system of one master with up to eight slaves to handle up to 64 priority levels.

A typical system is shown in Figure 2. The master controls, through the 3 line cascade bus, which one of the slaves will release the corresponding address.

As shown in Figure 2, the slaves interrupt outputs are connected to the master interrupt request inputs. When a slave request line is activated and later acknowledged, the master releases the 8080 CALL code during the first $\overline{INTA}$ pulse. From the trailing edge of this first $\overline{INTA}$ pulse until the trailing edge of the third pulse, the CAS lines will contain the slave address code. Thus, the corresponding slave is enabled to release the two-byte service routine address during the second and third $\overline{INTA}$ pulses.

Note that since the CAS lines default to 000, no slave should be connected with IR0 on the master unless all other master request inputs (IR1-IR7) are connected to slaves. Otherwise, the slave on IR0 will attempt to drive the data bus in conflict with a non-slave interrupt request on the master.

It is obvious that each 8259 in the system must follow a separate initialization sequence and can be programmed to work in a different mode. An EOI command must be issued twice: once for the master and once for the corresponding slave. An address decoder is required to activate the Chip Select ($\overline{CS}$) input of each 8259. The slave program pin ($\overline{SP}$) must be at a "low" level for a slave (and then the cascade lines are inputs) and at a "high" level for a master (and then the cascade lines are outputs).

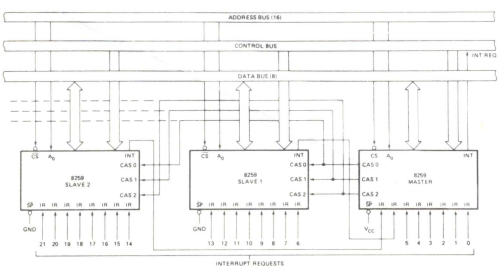


Figure 12. Cascading the 8259

INST. NO.		A0	D7	D6	D5	D4	D3	D2	D1	D0	OPERATION DESCRIPTION
1	ICW1 A	0	A7	A6	A5	1	0	1	1	0	Byte 1 initialization, format = 4, single.
2	ICW1 B	0	A7	A6	A5	1	0	1	0	0	Byte 1 initialization, format = 4, not single.
3	ICW1 C	0	A7	A6	A5	1	0	0	1	0	Byte 1 initialization, format = 8, single.
4	ICW1 D	0	A7	A6	A5	1	0	0	0	0	Byte 1 initialization, format = 8, not single.
5	ICW2	1	A15	A14	A13	A12	A11	A10	A9	A8	Byte 2 initialization (Address No. 2)
6	ICW3 M	1	S7	S6	S5	S4	S3	S2	S1	S0	Byte 3 initialization – master.
7	ICW3 S	1	0	0	0	0	0	S2	S1	S0	Byte 3 initialization – slave.
8	OCW1	1	M7	M6	M5	M4	M3	M2	M1	M0	Load mask reg, read mask reg.
9	OCW2 E	0	0	0	1	0	0	0	0	0	Non specific EOI.
10	OCW2 SE	0	0	1	1	0	0	L2	L1	L0	Specific EOI. L2, L1, L0 code of IS FF to be reset.
11	OCW2 RE	0	1	0	1	0	0	0	0	0	Rotate at EOI (Auto Mode).
12	OCW2 RSE	0	1	1	1	0	0	L2	L1	L0	Rotate at EOI (Specific Mode). L2, L1, L0, code of line to be reset and selected as bottom priority.
13	OCW2 RS	0	1	1	0	0	0	L2	L1	L0	L2, L1, L0 code of bottom priority line.
14	OCW3 P	0	–	0	0	0	1	1	0	0	Poll mode.
15	OCW3 RIS	0	–	0	0	0	1	0	1	1	Read IS register.
16	OCW3 RR	0	–	0	0	0	1	0	1	0	Read requests register.
17	OCW3 SM	0	–	1	1	0	1	0	0	0	Set special mask mode.
18	OCW3 RSM	0	–	1	0	0	1	0	0	0	Reset special mask mode.

Notes:
1. In the master mode $\overline{SP}$ pin = 1, in slave mode $\overline{SP}$ = 0.
2. (–) = do not care.

Figure 13. 8259 Instruction Set

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0° C to 70° C
Storage Temperature ..... −65° C to +150° C
Voltage On Any Pin
With Respect to Ground ..... −0.5 V to +7 V
Power Dissipation ..... 1 Watt

*COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS

(T_A = 0°C to 70°C; V_{CC} = 5V ±5%)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	-.5	.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+.5V	V	
V_{OL}	Output Low Voltage		.45	V	I_{OL} = 2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400 μA
V_{OH-INT}	Interrupt Output High Voltage	2.4 3.5		V V	I_{OH} = -400 μA I_{OH} = -50 μA
$I_{IL(IR_{0-7})}$	Input Leakage Current for IR_{0-7}		-300 10	μA μA	V_{IN} = 0V V_{IN} = V_{CC}
I_{IL}	Input Leakage Current for Other Inputs		10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = 0.45V to V_{CC}
I_{CC}	V_{CC} Supply Current		100	mA	

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
C_{IN}	Input Capacitance			10	pF	fc = 1 MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to V_{SS}

A.C. CHARACTERISTICS

(T_A = 0°C to 70°C; V_{CC} = +5V ±5%, GND = 0V)

Bus Parameters

Read:

SYMBOL	PARAMETER	8259 MIN.	8259 MAX.	8259-5 MIN.	8259-5 MAX.	UNIT
t_{AR}	$\overline{CS}/A_0$ Stable Before $\overline{RD}$ or $\overline{INTA}$	50		50		ns
t_{RA}	$\overline{CS}/A_0$ Stable After $\overline{RD}$ or $\overline{INTA}$	5		30		ns
t_{RR}	$\overline{RD}$ Pulse Width	420		300		ns
t_{RD}	Data Valid From $\overline{RD}/\overline{INTA}$[1]		300		200	ns
t_{DF}	Data Float After $\overline{RD}/\overline{INTA}$	20	200	20	100	ns

Write:

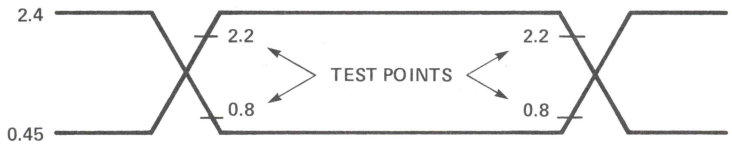
SYMBOL	PARAMETER	8259 MIN.	8259 MAX.	8259-5 MIN.	8259-5 MAX.	UNIT
t_{AW}	A_0 Stable Before $\overline{WR}$	50		50		ns
t_{WA}	A_0 Stable After $\overline{WR}$	20		30		ns
t_{WW}	$\overline{WR}$ Pulse Width	400		300		ns
t_{DW}	Data Valid to $\overline{WR}$ (T.E.)	300		250		ns
t_{WD}	Data Valid After $\overline{WR}$	40		30		ns

Other Timings:

SYMBOL	PARAMETER	8259 MIN.	8259 MAX.	8259-5 MIN.	8259-5 MAX.	UNIT
t_{IW}	Width of Interrupt Request Pulse	100		100		ns
t_{INT}	INT ↑ After IR ↑	400		350		ns
t_{IC}	Cascade Line Stable After $\overline{INTA}$ ↑	400		400		ns

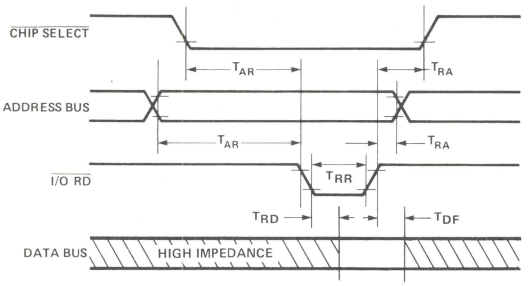
Note 1: 8259: C_L = 100pF, 8259-5: C_L = 150pF.

Input Waveforms for A.C. Tests

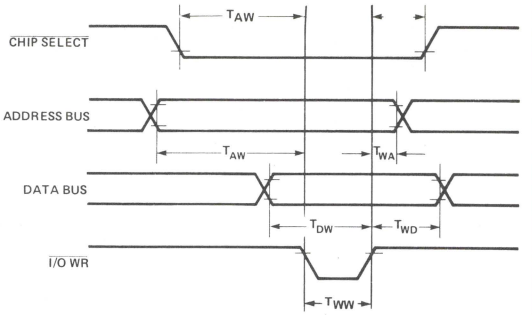


WAVEFORMS

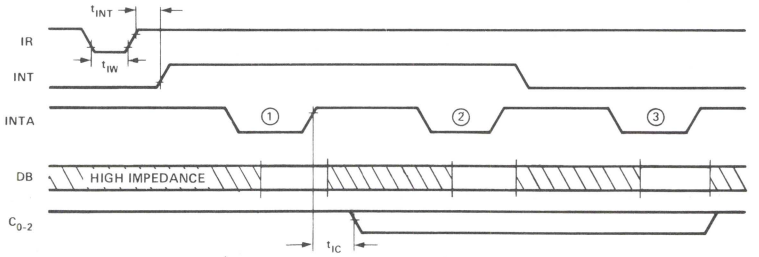
Read Timing



Write Timing

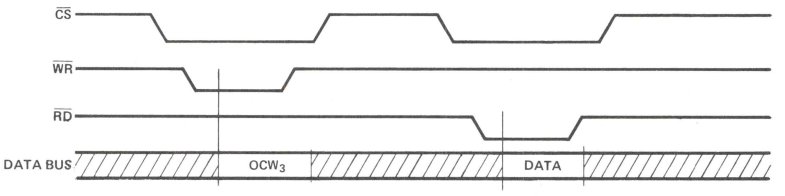


Other Timing



Note: Interrupt Request must remain "HIGH" (at least) until leading edge of first INTA.

Read Status/Poll Mode



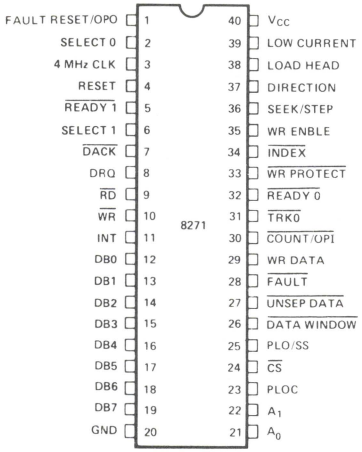
PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

8271
PROGRAMMABLE FLOPPY DISK CONTROLLER

- Supports Standard or Mini-Floppy Drives
- IBM 3740 Soft Sectored Format Compatible
- Programmable Record Lengths
- Multi-Sector Capability
- Maintains Dual Drives with Minimum Software Overhead Expandable to 4 Drives
- Automatic Read/Write Head Positioning and Verification
- Internal CRC Generation and Checking
- Programmable Step Rate, Settle-Time, Head Load Time, Head Unload Index Count
- Fully MCS-80 and MCS-85 Compatible
- Single +5V Supply
- 40-Pin Package

The Intel® 8271 Programmable Floppy Disk Controller (FDC) is an LSI component designed to interface one to four floppy disk drives to an 8-bit microcomputer system. Its powerful control functions minimize both hardware and software overhead normally associated with floppy disk controllers.

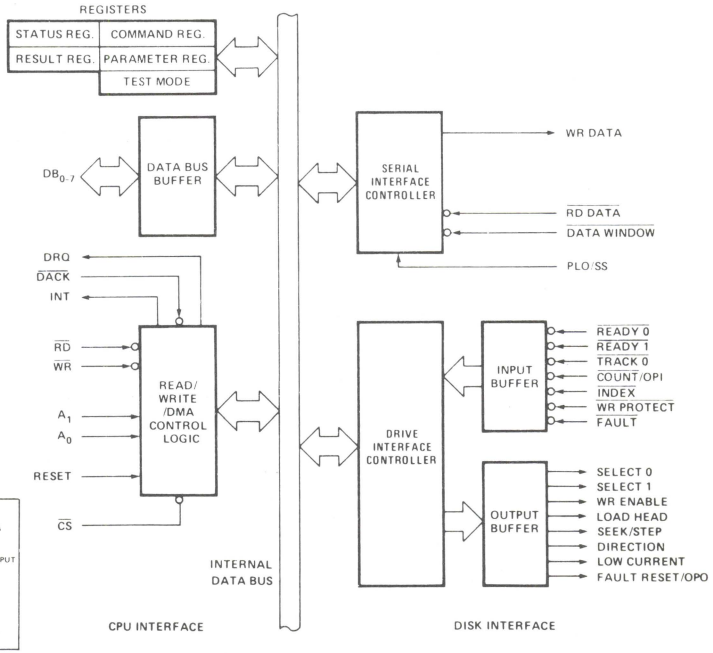
PIN CONFIGURATION



PIN NAMES

$DB_7 - DB_0$	DATA BUS (BI DIRECTIONAL)	PLO/SS	PLO/SINGLE SHOT
CLK	CLOCK INPUT (TTL)	DATA WINDOW	DATA WINDOW
SELECT 1, 0	SELECT 1, 0	UNSEP DATA	UNSEPARATED DATA
FAULT RESET/OPO	FAULT RESET/OPTIONAL OUTPUT	FAULT	FAULT
RESET	CHIP RESET	WR DATA	WRITE DATA
READY 1, 0	READY 1, 0	COUNT/OPI	COUNT/OPTIONAL INPUT
DACK	DMA ACKNOWLEDGE	TRK 0	TRACK 0
DRQ	DMA REQUEST	WR PROTECT	WRITE PROTECT
RD	CPU READ INPUT	INDEX	INDEX
WR	CPU WRITE INPUT	WR ENABLE	WRITE ENABLE
INT	INTERRUPT	SEEK/STEP	SEEK/STEP
$A_{1,0}$	REGISTER SELECT	DIRECTION	DIRECTION
INSYNC	READ DATA INSYNC	LOAD HEAD	LOAD HEAD
CS	CHIP SELECT	LOW CURRENT	LOW CURRENT

BLOCK DIAGRAM



MPU PERIPHERALS

IBM DISKETTE GENERAL FORMAT INFORMATION

The IBM Flexible Diskette used for data storage and retrieval is organized into concentric circular paths or TRACKS. There are 77 tracks on either one or both sides (surfaces) of the diskette. On double-sided diskettes, the corresponding top and bottom tracks are referred to as a CYLINDER. Each track is further divided into fixed length sections or SECTORS. The number of sectors per track — 26, 15 or 8 — is determined when a track is formatted and is dependent on the sector length — 128, 256 or 512 bytes respectively — specified.

All tracks on the diskette are referenced to a physical index mark (a small hole in the diskette). Each time the hole passes a photodetector cell (one revolution of the diskette), an Index pulse is generated to indicate the logical beginning of a track. This index pulse is used to initiate a track formatting operation.

Track Format

Each Diskette Surface is divided into 77 tracks with each track divided into fixed length sectors. A sector can hold a whole record or a part of a record. If the record is shorter than the sector length, the unused bytes are filled with binary zeros. If a record is longer than the sector length, the record is written over as many sectors as its length requires. The sector size that provides the most efficient use of diskette space can be chosen depending upon the record length required.

Tracks are numbered from 00 (outer-most) to 76 (inner-most) and are used as follows:

TRACK 00 reserved as System Label Track
TRACKS 01 through 74 used for data
TRACKS 75 and 76 used as alternates.

Each sector consists of an ID field (which holds a unique address for the sector) and a data field.

The ID field is seven bytes long and is written for each sector when the track is formatted. Each ID field consists of an ID field Address Mark, a Cylinder Number byte which identifies the track number, a Head Number byte which specifies the head used (top or bottom) to access the sector, a Record Number byte identifying the sector number (1 through 26 for 128 byte sectors), an N-byte specifying the byte length of the sector and two CRC (Cyclic Redundancy Check) bytes.

The Gaps separating the index mark and the ID and data fields are written on a track when it is formatted. These gaps provide both an interval for switching the drive electronics from reading or writing and compensation for rotational speed and other diskette-to-diskette and drive-to-drive manufacturing tolerances to ensure that data written on a diskette by one system can be read by another (diskette interchangeability).

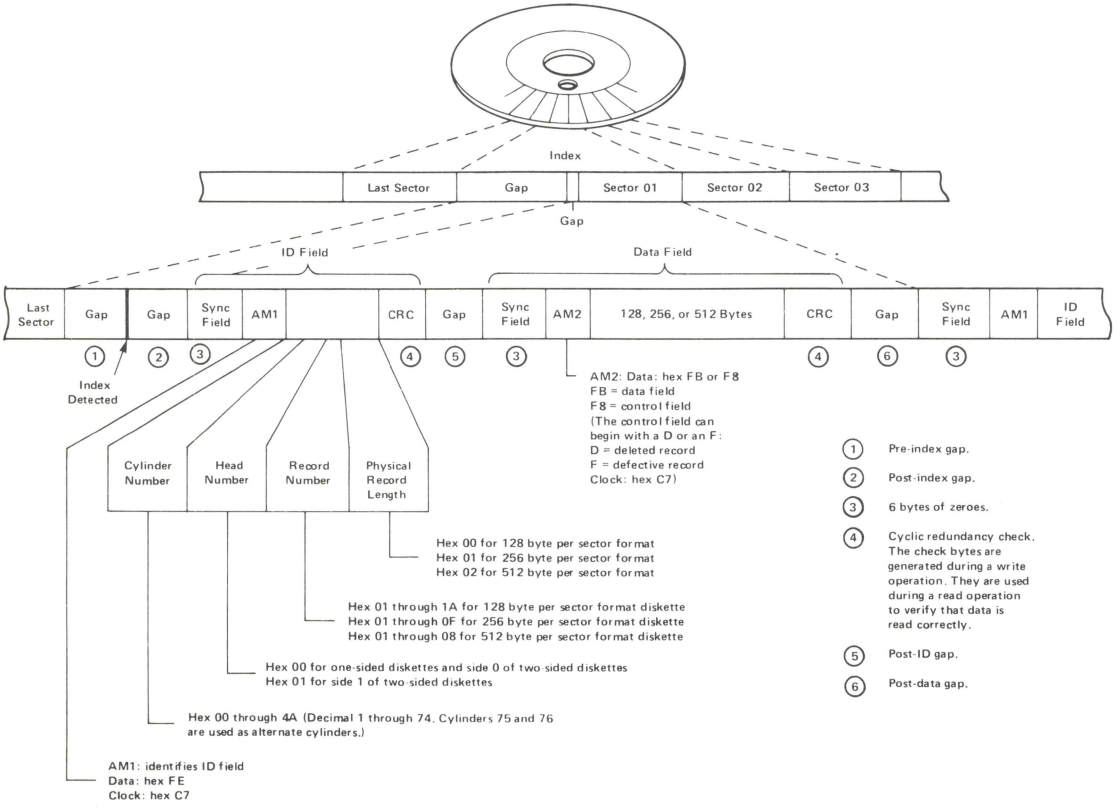


Figure 1. Track Format

FUNCTIONAL DESCRIPTION

General

The 8271 Floppy Disk Controller (FDC) interfaces either two single or one dual floppy drive to an eight bit microprocessor and is fully compatible with Intel's new high performance MCS-85 microcomputer system. With minimum external circuitry, this innovative controller supports most standard, commonly-available flexible disk drives including the mini-floppy.

The 8271 FDC supports a comprehensive soft sectored format which is IBM 3740 compatible and includes provision for the designating and handling of bad tracks. It is a high level controller that relieves the CPU (and user) of many of the control tasks associated with implementing a floppy disk interface. The FDC supports a variety of high level instructions which allow the user to store and retrieve data on a floppy disk without dealing with the low level details of disk operation.

In addition to the standard read/write commands, a scan command is supported. The scan command allows the user program to specify a data pattern and instructs the FDC to search for that pattern on a track. Any application that is required to search the disk for information (such as point of sale price lookup, disk directory search, etc.), may use the scan command to reduce the CPU overhead. Once the scan operation is initiated, no CPU intervention is required.

Hardware Description

The 8271 is packaged in a 40 pin DIP. The following is a functional description of each pin.

Pin Name	Pin No.	I/O	Description
V_{CC}	(40)		+5V supply
GND	(20)		Ground
Clock	(3)	I	A square wave clock
Reset	(1)	I	A high signal on the reset input forces the 8271 to an idle state. The 8271 remains idle until a command is issued by the CPU. The drive interface output signals are forced low.
$\overline{CS}$	(24)	I	The I/O Read and I/O Write inputs are enabled by the chip select signal.
DB_7-DB_0	(19-12)	I/O	The Data Bus lines are bidirectional, three-state lines (8080 data bus compatible).
$\overline{WR}$	(10)	I	The Write signal is used to signal the control logic that a transfer of data from the data bus to the 8271 is required.
$\overline{RD}$	(9)	I	The Read signal is used to signal the control logic that a transfer of data from the 8271 to the data bus is required.
INT	(11)	O	The interrupt signal indicates that the 8271 requires service.
A_1-A_0	(22-21)	I	These two lines are CPU Interface Register select lines.
DRQ	(8)	O	The DMA request signal is used to request a transfer of data between the 8271 and memory.
$\overline{DACK}$	(7)	I	The DMA acknowledge signal notifies the 8271 that a DMA cycle has been granted.
Select 1– Select 0	(6) (2)	O	These lines are used to specify the selected drive.
Fault Reset/ OPO	(1)	O	The optional fault reset output line is used to reset an error condition which is latched by the drive.
Write Enable	(35)	O	This signal enables the drive write logic.
Seek/Step	(36)	O	This multi-function line is used during drive seeks.
Direction	(37)	O	The direction line specifies the seek direction. A high level on this pin steps the R/W head toward the spindle (step-in), a low level steps the head away from the spindle (step-out).
Load Head	(38)	O	The load head line causes the drive to load the Read/Write head against the diskette.
Low Current	(39)	O	This line notifies the drive that track 43 or greater is selected.
$\overline{Ready\ 1}$, $\overline{Ready\ 0}$	(5) (32)	I	These two lines indicate that the specified drive is ready.
$\overline{Fault}$	(28)	I	This line is used by the drive to specify a file unsafe condition.
$\overline{Count/OPI}$	(30)	I	If the optional seek/direction/count seek mode is selected, the count pin is pulsed to step the R/W head to the desired track.
$\overline{Write\ Protect}$	(33)	I	This signal specifies that the diskette inserted is write protected.
$\overline{TRK0}$	(31)	I	This signal indicates when the R/W head is positioned over track zero.
$\overline{Index}$	(34)	I	The index signal gives an indication of the relative position of the diskette.
PLO/SS	(25)	I	This pin is used to specify the type of data separator used.
Write Data	(29)	O	Composite write data.
$\overline{Unseparated\ Data}$	(27)	I	This input is the unseparated data and clocks.
$\overline{Data\ Window}$	(26)	I	This is a data window established by a single-shot or phase-locked oscillator data separator.
INSYNC	(23)	O	This line is high when 8271 has attained input data synchronization, by detecting 2 bytes of zeros followed by an expected Address Mark. It will stay high until the end of the ID or data field.

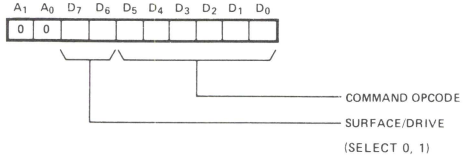
CPU Interface Description

This interface minimizes CPU involvement by supporting a set of high level commands and both DMA and non-DMA type data transfers and by providing hierarchical status information regarding the result of command execution.

The CPU utilizes the control interface (see the Block diagram) to specify the FDC commands and to determine the result of an executed command. This interface is supported by five Registers which are addressed by the CPU via the A_1, A_0, $\overline{RD}$ and $\overline{WR}$ signals. If an 8080 based system is used, the $\overline{RD}$ and $\overline{WR}$ signals can be driven by the 8228's $\overline{I/OR}$ and $\overline{I/OW}$ signals. The registers are defined as follows:

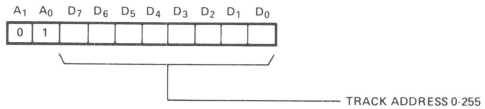
Command Register

The CPU loads an appropriate command into the Command Register which has the following format:



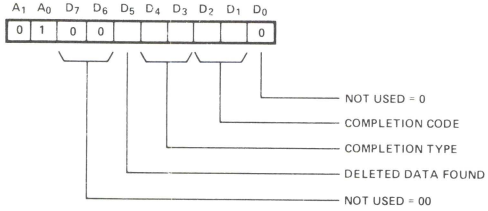
Parameter Register

Accepts parameters of commands that require further description; up to five parameters may be required, example:



Result Register

The Result Register is used to supply the outcome of FDC command execution (such as a good/bad completion) to the CPU. The standard Result byte format is:



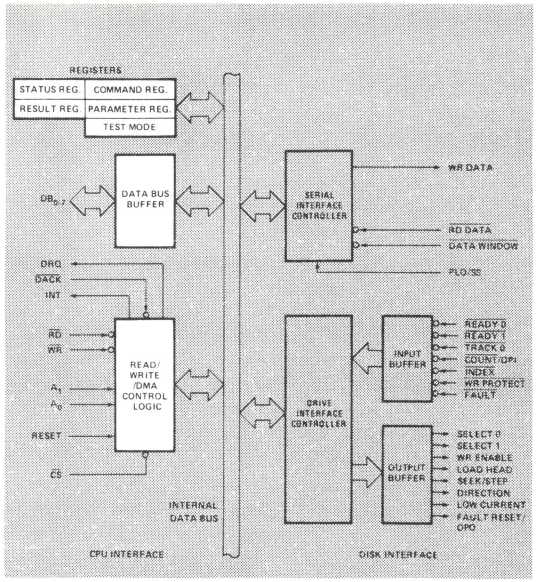
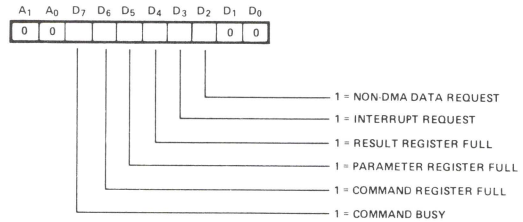


Figure 2. 8271 Block Diagram Showing CPU Interface Functions

Status Register

Reflects the state of the FDC.



Test Mode

Allows the 8271 to be reset by the program.

INT (Interrupt Line)

Another element of the control interface is the Interrupt line (INT). This line is used to signal the CPU that an FDC operation has been completed. It remains active until the result register is read.

DMA Operation

The 8271 can transfer data in either DMA or non DMA mode. The data transfer rate of a floppy disk drive is high enough (one byte every 32 µsec) to justify DMA transfer. In DMA mode the elements of the DMA interface are:

DRQ: DMA Request:
The DMA request signal is used to request a transfer of data between the 8271 and memory.

$\overline{\text{DACK}}$: DMA Acknowledge:
The DMA acknowledge signal notifies the 8271 that a DMA cycle has been granted.

$\overline{\text{RD}}$, $\overline{\text{WR}}$: Read, Write
The read and write signals are used to specify the direction of the data transfer.

DMA transfers require the use of a DMA controller such as the Intel®8257. The function of the DMA controller is to provide sequential addresses and timing for the transfer at a starting address determined by the CPU. Counting of data block lengths is performed by the FDC.

To request a DMA transfer, the FDC raises DRQ. DACK and RD enable DMA data onto the bus (independently of CHIP SELECT). DACK and WR transfer DMA data to the FDC. If a data transfer request (read or write) is not serviced within 31 µsec, the command is cancelled, a late DMA status is set, and an interrupt is generated. In DMA mode, an interrupt is generated at the completion of the data block transfer.

When configured to transfer data in non-DMA mode, the CPU must pass data to the FDC in response to the non-DMA data requests indicated by the status word. The data is passed to and from the chip by asserting the DACK and the RD or WR signals.

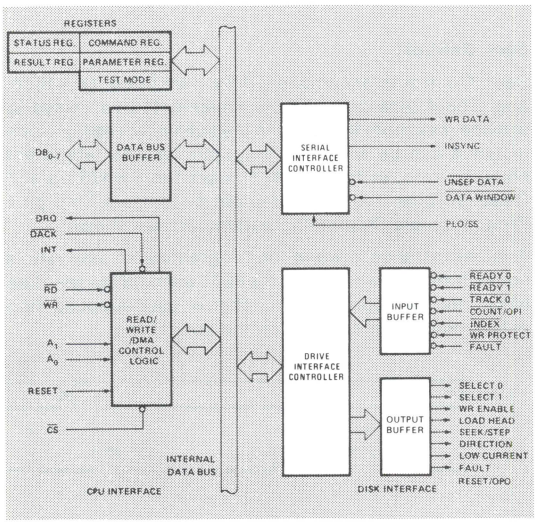


Figure 3. 8271 Block Diagram Showing Disk Interface Functions

Disk Drive Interface

The 8271 disk drive interface supports the high level command structure described in the Command Description section. The 8271 maintains the location of bad tracks and the current track location for two drives. However, with minor software support, this interface can support four drives by expanding the two drive select lines (select 0, select 1) with the addition of minimal support hardware.

The FDC Disk Drive Interface has the following major functions.

READ FUNCTIONS

Utilize the user supplied data window to obtain the clock and data patterns from the unseparated read data.

Establish byte synchronization.

Compute and verify the ID and data field CRCs.

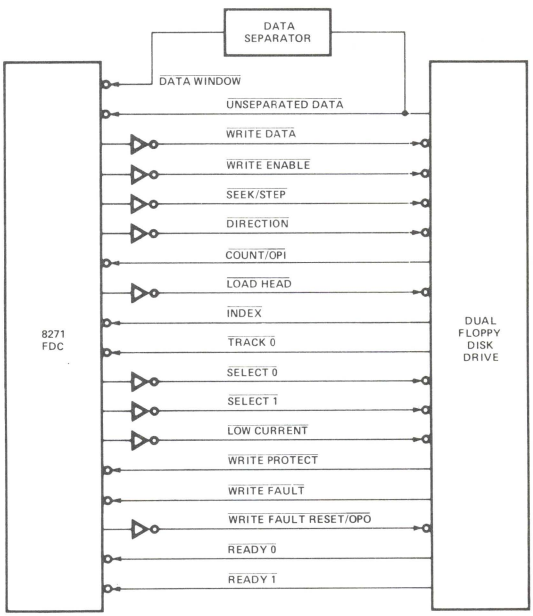
WRITE FUNCTIONS

Encode composite write data.

Compute the ID and data field CRCs and append them to their respective fields.

CONTROL FUNCTIONS

Generate the programmed step rate, head load time, head settling time, head unload delay, and monitor drive functions.



NOTE: INPUTS TO CHIP MAY REQUIRE RECEIVERS (AT LEAST PULL UP/DOWN PAIRS).

Figure 4. 8271 Disk Drive Interface

Data Separation

The 8271 needs only a data window to separate the data from the composite read data, as well as detect missing clocks in the Address Marks.

The window generation logic may be implemented using either a single shot or a phase-locked oscillator.

Single-Shot Separator

The single shot approach is the lowest cost solution.

The FDC samples the value of Data Window on the leading edge of Unseparated Data and determines whether the delay from the previous pulse was a half or full bit-cell (high input = full bit-cell, low input = half bit-cell). PLO/SS should be tied to Ground.

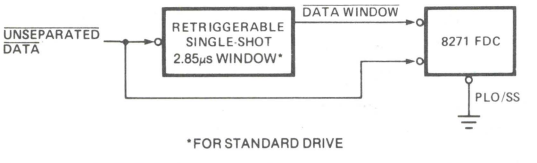


Figure 6. Single-Shot Data Separator Block Diagram

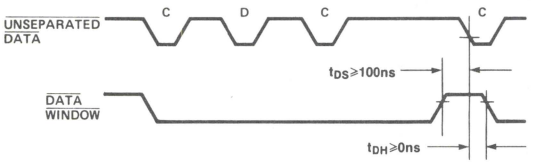


Figure 7. Single-Shot Data Window Timing

Phase-Locked Oscillator Separator

The FDC samples the value of Data Window on the leading edge of Unseparated Data and determines whether the pulse represents a Clock or Data Pulse.

PLO/SS should be tied to V_{CC} (+5V).

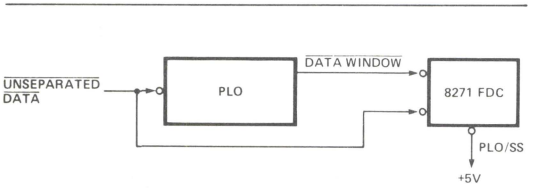


Figure 8. PLO Data Separator Block Diagram

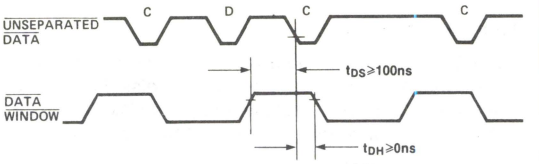


Figure 9. PLO Data Window Timing

Disk Drive Control Interface

The disk drive control interface performs the high level and programmable flexible disk drive operations. It customizes many varied drive performance parameters such as the step rate, settle time, head load time, and head unload index count. The following is the description of the control interface.

Write Enable

The Write Enable controls the read write functions of a flexible disk drive. When Write Enable is a logical one, it enables the drive write electronics to pass current through the Read/Write head. When Write Enable is a logical zero the drive Write circuitry is disabled and the Read/Write head detects the magnetic flux transitions recorded on a diskette. The write current turn-on is as follows.

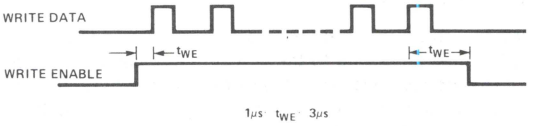
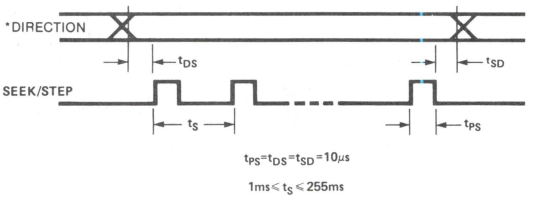


Figure 10. Write Enable Timing

Seek Control

Seek Control is accomplished by Seek/Step, Direction, and Count pins and can be implemented two ways to provide maximum flexibility in the subsystem design. One instance can be when the programmed step rate is not equal to zero; in this the 8271 uses the Seek/Step and Direction pins (the Seek/Step pin becomes a Step pin). Programmable Step timing parameters are shown.

Another instance is when the programmable step rate is equal to zero; in which case the 8271 will hold the seek line high until the appropriate number of user-supplied step pulses have been counted on the count input pin.



*WHEN DIRECTION PIN IS HIGH THE HEAD MOVES TOWARD THE SPINDLE.

Figure 11. Seek Timing

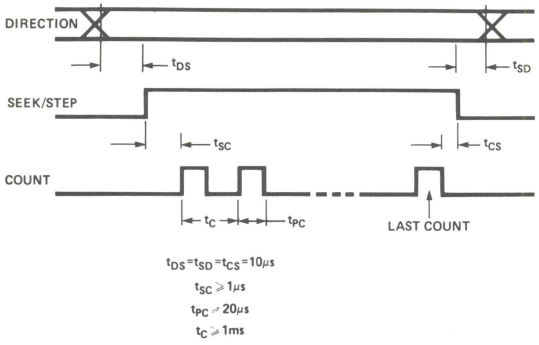


Figure 12. Seek/Step/Count Timing

Head Settle

The 8271 allows the head settle time to be programmed from 0 to 255 ms, in increments of 1 ms.

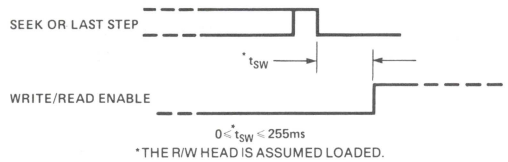


Figure 13. Head Settle Timing

Load Head

The Load Head output pin must become active prior to any read or write operation and remain active for a programmable number (0-14) of disk revolutions after termination of each operation. When frequent disk accesses are made, the Head Load settling delay is eliminated.

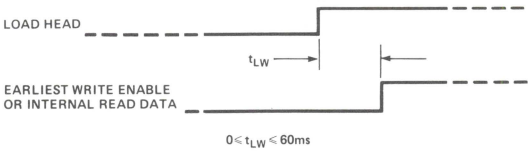


Figure 14. Head Load to Read/Write Timing

Index

The Index input is used to determine "Sector not found" status, to initiate format track/read ID commands and head unload Index and Count operations.

Track 0

This input pin indicates that the diskette is at track 0. During any seek operation, the stepping out of the actuator will cease when the track 0 pin becomes active.

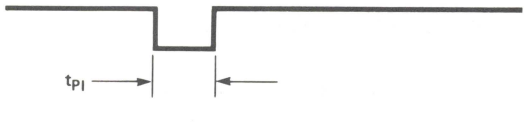


Figure 15. Index Timing

Select 1, 0

Only one drive may be selected at a time. The Input/Output pins that must be externally qualified with select 0 and select 1 are:

Unseparated Data
Data Window
Write Enable
Seek/Step
Count/User Optional Input
Load Head
Track 0
Low Current
Write Protect
Write Fault
Fault Reset/User Optional Output
Index

Low Current

This output pin is active whenever the physical track location of the selected drive is greater than 43. Generally this signal may be used to enable compensation for lower velocity while recording on the inner tracks by adjusting the current in a Read/Write head.

Write Protect

The 8271 will not write to a disk when this input pin is active and will interrupt the CPU if a Write attempt is made. Operations marked check Write Protect will be aborted if Write Protect line is active.

This signal normally comes from a sensor which detects the presence or absence of a Write Protect hole in a diskette envelope.

Write Fault and Write Fault Reset

Write Fault input is normally latched by the drive and indicates any condition which could endanger data integrity if writing is attempted. The 8271 interrupts the CPU anytime Write Fault is detected during an operation and will immediately reset the Write Enable, Seek/Step, Direction, and Low Current signals. The Write Fault is reset through the user specified optional output pin.

Ready 1, 0

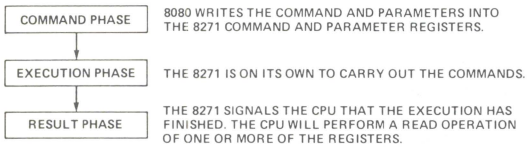
These two pins indicate the functional status of the flexible disk drives. Whenever an operation is attempted on a drive which is not ready, an interrupt is generated. Whenever a drive becomes not ready, this condition is latched by the 8271. The Not Ready condition is reset by the execution of a Read Drive Status command.

PRINCIPLES OF OPERATION

As an 8080 peripheral device, the 8271 accepts commands from the CPU, executes them and provides a RESULT back to the 8080 CPU at the end of the execution. The communication with the CPU is established by the activation of $\overline{CS}$, $\overline{RD}$, $\overline{WR}$. The A_1, A_0 select the appropriate registers on the chip:

A_1	A_0	CS RD	CS WR
0	0	Status Reg	Command Reg
0	1	Result Reg	Parameter Reg
1	0	—	Test Mode
1	1	—	—

The FDC chip operation is composed of the following sequence of events.



The Command Phase

The software writes a command to the command register. As a function of the command issued, from zero to five parameters are written to the parameter register. Refer to diagram showing a flow chart of the command phase. Note that the flow chart shows that a command may not be issued if the FDC status register indicates that the device is busy. Issuing a command while another command is in progress is illegal. The flow chart also shows a parameter buffer full check. The FDC status indicates the state of the parameter buffer. If a parameter is issued while the parameter buffer is full, the previous parameter will be over written and lost.

The Execution Phase

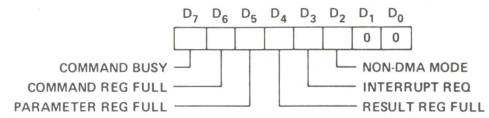
During the execution phase the operation specified during the command phase is performed. During this phase there is no CPU involvement if the system utilizes DMA for the data transfers. The execution phase of each command is discussed within the detailed command descriptions. The following table summarizes many of the basic execution phase characteristics.

The Result Phase

During the Result Phase, the FDC chip notified the CPU of the outcome of the command execution. This phase may be initiated by:

1. The successful completion of an operation.
2. An error detected during an operation.

In the Result Phase, the CPU Reads the Status Register which provides the following information:



Bit 7: Command Busy

The command busy bit is set on writing to the command port. Whenever the FDC is busy processing a command the command busy bit is set to a one. This bit is set to zero after the command is completed.

Bit 6: Command Full

The command full bit is set on writing to the command buffer and cleared when the FDC begins processing the command.

Bit 5: Parameter Full

This bit indicates the state of a parameter buffer. This bit is set when a parameter is written to the FDC and reset after the FDC has accepted the parameter.

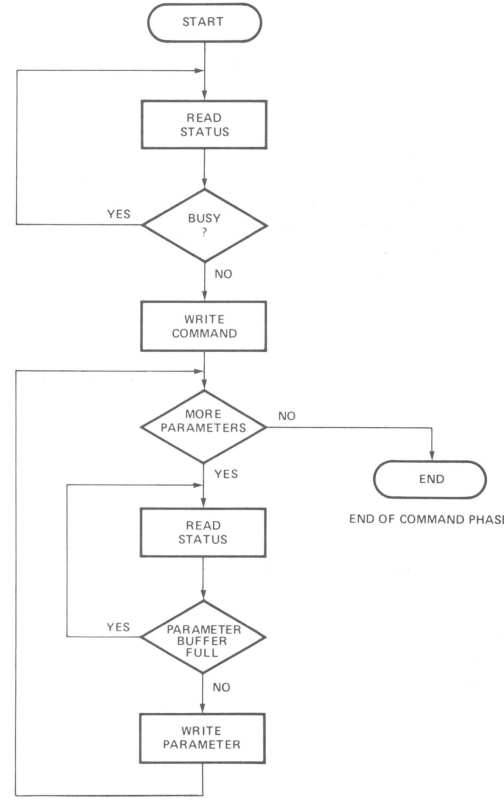


Figure 5. Command Phase Sequence

Bit 4: Result Full

This bit indicates the state of the result buffer. This bit is set when the FDC has a result byte and reset after the result byte is read by the CPU. The data in the result buffer is valid only after the FDC has completed a command. Reading the result buffer while a command is in progress will yield no useful information.

Bit 3: Interrupt Request

This bit reflects the state of the FDC INT pin.

Bit 2: Non-DMA Data Request

When the FDC is utilized without a DMA controller, this bit is used to indicate FDC data requests.

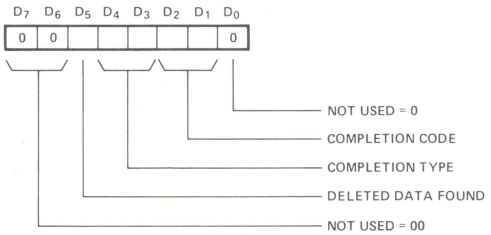
Bits 1 and 0

Not used.

After reading the Status Register, the CPU then Reads the Result Register for more information.

The Result Register

The standard result byte format is:



(D5)

Deleted Data Found: This bit is set when deleted data is encountered during a transaction.

(D4-D3)

Completion Type	Event
00	Good Completion — No Error
01	System Error — recoverable errors
10	Operator intervention probably required for recovery
11	Command/Drive Error — either a program error or drive hardware failure.

(D2-D1)

Completion Code: The completion code field provides more detailed information about the completion type.

Completion Type	Completion Code	Event
00	00	Good Completion
00	01	Scan Met Equal
00	10	Scan Met Not Equal
00	11	——
01	00	Clock Error
01	01	Late DMA
01	10	ID CRC Error
01	11	Data CRC Error
10	00	Drive not ready
10	01	Write Protect
10	10	Recalibrate Error
10	11	Write Fault
11	00	Record Not Found
11	01	——
11	10	——
11	11	——

It is important to note the hierarchical structure of the result byte. In very simple systems where only a GO-NO GO result is required the user may simply branch on a zero result (a zero result is a good completion). The next level of complexity is at the completion type interface. The completion type supplies enough information so that the software may distinguish between fatal and non-fatal errors. If a completion type 01 occurs, ten retries should be performed before the error is considered unrecoverable.

The Completion Type/Completion Code interface supplies the greatest detail about each type of completion. This interface is used when detailed information about the transaction completion is required.

EXECUTION PHASE BASIC CHARACTERISTICS

The following table summarizes the various commands with corresponding execution phase characteristics.

COMMANDS	1 Deleted Data	2 Head	3 Ready	4 Write/ Protect	5 Seek	6 Seek Check	7 Result	8 Completion Interrupt
SCAN DATA	SKIP	LOAD	√	x	YES	YES	YES	YES
SCAN DATA AND DEL DATA	XFER	LOAD	√	x	YES	YES	YES	YES
WRITE DATA	x	LOAD	√	√	YES	YES	YES	YES
WRITE DEL DATA	x	LOAD	√	√	YES	YES	YES	YES
READ DATA	SKIP	LOAD	√	x	YES	YES	YES	YES
READ DATA AND DEL DATA	XFER	LOAD	√	x	YES	YES	YES	YES
READ ID	x	LOAD	√	x	YES	NO	YES	YES
VERIFY DATA AND DEL DATA	XFER	LOAD	√	x	YES	YES	YES	YES
FORMAT TRACK	x	LOAD	√	√	YES	NO	YES	YES
SEEK	x	LOAD	y	x	YES	NO	YES	YES
READ DRIVE STAT	x	–	x	x	NO	NO	YES	NO
SPECIFY	x	–	x	x	NO	NO	NO	NO
RESET	x	UNLOAD	x	x	NO	NO	NO	NO
R/W SP REGISTERS	x	–	x	x	NO	NO	NO	NO

Note: 1. "x" → DON'T CARE 2. "√" → check 3. "–" → No change 4. "y" → Check at end of operation

Table 1. Execution Phase Basic Characteristics

Explanation of the execution phase characteristics table.

1. Deleted Data Processing

   If deleted data is encountered during an operation that is marked skip in the table, the deleted data record is not transferred into memory, but the record is counted. For example, if the command and parameters specify a read of five records and one of the records was written with a deleted data mark, four records are transferred to memory. The deleted data flag is set in the result byte. However, if the operation is marked transfer, all data is transferred to memory regardless of the type of data mark.

2. Head

   The Head column in the table specifies whether the Read/Write head will be loaded or not. If the table specifies load, the head is loaded after it is positioned over the track. The head loaded by a command remains loaded until the user specified number of index pulses have occurred.

3. Ready

   The Ready column indicates if the ready line (Ready 1, Ready 0) associated with the selected drive is checked. A not ready state is latched by the 8271 until the user executes a read status command.

4. Write Protect

   The operations that are marked check Write Protect are immediately aborted if Write Protect line is active at the beginning of an operation.

5. Seek

   Many of the 8271 commands cause a seek to the desired track. A current track register is maintained for each drive or surface.

6. Seek Check

   Operations that perform Seek Check verify that selected data in the ID field is correct before the 8271 accesses the data field.

DETAILED COMMAND DESCRIPTION

Many of the interface characteristics of the FDC are specified by the systems software. Prior to initiating any drive operation command, the software must execute the specify command. There are two types of specify commands selectable by the parameter issued.

First Parameter	Specify Type
$0D_H$	Initialization
10_H	Load bad Tracks Surface '0'
18_H	Load bad Tracks Surface '1'

Specify Command

The Specify command is used prior to performing any diskette operation (including formatting of a diskette) to define the drive's inherent operating characteristics and also is used following a formatting operation or installation of another diskette to define the locations of bad tracks. Since the Specify command only loads internal registers within the 8271 and does not involve an actual diskette operation, command processing is limited to only Command Phase. Note that once the operating characteristics and bad tracks have been specified for a given drive and diskette, redefining these values need only be done if a diskette with unique bad tracks is to be used or if the system is powered down.

Initialization:

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	0	0	1	1	0	1	0	1
PAR:	0	1	0	0	0	0	1	1	0	1
PAR:	0	1	STEP RATE*							
PAR:	0	1	HEAD SETTLING TIME*							
PAR:	0	1	INDEX CNT BEFORE HEAD UNLOAD*				HEAD LOAD TIME*			

*Note: Mini-floppy parameters are doubled.

Parameter 0 — $0D_H$ = Select Specify Initialization.
Parameter 1 — D_7-D_0 = Step Rate (0-255ms in 1ms steps).
Parameter 2 — D_7-D_0 = Head Settling Time (0-255ms in 1 ms steps).
Parameter 3 — D_7-D_4 = Index Count — Specifies the number of Revolutions (0-14) which are to occur before the FDC automatically unloads the R/W head. If 15 is specified, the head remains loaded.
D_3-D_0 = Head Load Time (0-60ms in steps of 4ms).

Load Bad Tracks

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	0	0	1	1	0	1	0	1
PAR:	0	1	0	0	0	1	1/0	0	0	0
PAR:	0	1	BAD TRACK NO. 1							
PAR:	0	1	BAD TRACK NO. 2							
PAR:	0	1	CURRENT TRACK							

Parameter 0: 10_H = Load Surface zero bad tracks
18_H = Load Surface one bad track

Parameter 1:
Bad track address number 1 (Physical Address).

Parameter 2:
Bad track address number 2 (Physical Address).

Parameter 3:
Current track address (Physical Address).

Conditions:
1. Bad track number one must be numerically less than bad track number two.
2. If no bad tracks are present, set the parameter to FF_H.

Reset Command

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
PAR:	1	0	0	0	0	0	0	0	0	1
PAR:	1	0	0	0	0	0	0	0	0	0

Function: The Reset command emulates the action of the reset pin. It is issued by outputting a one followed by a zero to the Test Mode Register.

1. The drive control signals are forced low.
2. An in-progress command is aborted.
3. The FDC status register flags are cleared.
4. The FDC enters an idle state until the next command is issued.

Special Drive Commands

The special drive commands are used to explicitly position the drive read/write head or to interrogate the drive status.

Command Seek Function

The seek command moves the head to the specified track without loading the head or verifying the track.

The seek operation uses the specified bad tracks to compute the physical track address. This feature insures that the seek operation positions the head over the correct track.

When a seek to track zero is specified (bad track registers are not used), the FDC steps the head until the track 00 signal is detected.

If the track 00 signal is not detected within $(FF)_H$ steps, a track 0 not found error status is returned.

A seek to track zero is used to position the read/write head when the current head position is unknown (such as after a power up).

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	SEL 1	SEL 0	1	0	1	0	0	1
PAR:	0	1	TRACK ADDRESS 0-255							

Seek operations are not verified. A subsequent read or write operation must be performed to determine if the correct track is located.

Read Drive Status Command

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	SEL 1	SEL 0	1	0	1	1	0	0

RESULT: EACH BIT INDICATES CURRENT STATE OF INPUT PINS.

A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	——	RDY 1	WR FAULT	INDEX	WR PROT	RDY 0	TRACK 0	CNT / OPI

IF A DRIVE NOT READY RESULT IS RETURNED, THE READ STATUS MUST BE ISSUED TO CLEAR THE CONDITION.

Read/Write Special Register

This command is used to access special registers within the 8271.

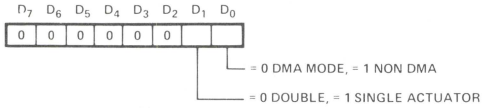
Command code:

3D$_H$ Read Special Register
3A$_H$ Write Special Register

For both commands, the first parameter is the register address; for Write command a second parameter specifies data to be written. Only the Read Special Register command supplies the result.

Description	Register Address in Hex	Comment
Scan Sector Number	06	See Scan Description
Scan MSB of Count	14	See Scan Description
Scan LSB of Count	13	See Scan Description
Surface 0 Current Track	12	
Surface 1 Current Track	1A	
Mode Register	17	See Description
Drive Control Output Port	23	See Description
Drive Control Input Port	22	See Read Status Description

Mode Register Write Parameter Format



Bits 7-2

Not used. Must be set to zero.

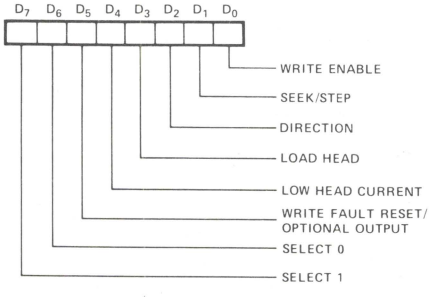
Bit 1

Double/Single Actuator: Selects single or double actuator mode. If the single actuator mode is selected the FDC will assume that the physical track location of both disks is always the same. This mode facilitates control of a drive which has a single actuator mechanism which moves two heads.

Bit 0

Data Transfer Mode: This bit selects the data transfer mode. If this bit is a zero the FDC operates in the DMA mode (DMA Request/ACK). If this bit is a one the FDC operates in non-DMA mode. When the FDC is operating in DMA mode interrupts are generated at the completion of commands. If the non-DMA mode is selected the FDC will generate an interrupt for every data byte transferred.

Drive Control Output Port Format



Each of these signals correspond to the chip pin of the same name.

Data Processing Commands

128 byte single record format.

A_1	A_0	D_7	D_6	D_5 D_4 D_3 D_2 D_1 D_0
0	0	SEL 1	SEL 0	COMMAND OPCODE
0	1	TRACK ADDR 0-255		
0	1	SECTOR 0-255		

Commands	Opcode
READ DATA	12
READ DATA AND DELETED DATA	16
WRITE DATA	0A
WRITE DELETED DATA	0E
VERIFY DATA AND DELETED DATA	1E

Variable Length/Multi-Record

A_1	A_0	D_7	D_6	D_5 D_4 D_3 D_2 D_1 D_0
0	0	SEL 1	SEL 0	COMMAND OPCODE
0	1	TRACK ADDR 0-255		
0	1	SECTOR 0-255		
0	1	LENGTH		NO. OF SECTORS

D_7-D_5 of Parameter 2 determine the length of the disk record.

0 0 0	128 Bytes
0 0 1	256 Bytes
0 1 0	512 Bytes
0 1 1	1024 Bytes
1 0 0	2048 Bytes
1 0 1	4096 Bytes
1 1 0	8192 Bytes
1 1 1	16,384 Bytes

Commands	Opcode
READ DATA	13
READ DATA AND DELETED DATA	17
WRITE DATA	0B
WRITE DELETED DATA	0F
VERIFY DATA AND DELETED DATA	1F
SCAN DATA	00
SCAN DATA AND DELETED DATA	04

Commands

Read Data, Read Data and Deleted Data.

Function

The read command transfers data from a specified disk record or group of records to memory. The operation of this command is outlined in execution phase table.

Commands

Write Data, Write Deleted Data.

Function

The write command transfers data from memory to a specified disk record or group of records.

Commands

Verify Data and Deleted Data.

Function

The verify command is identical to the read data and deleted data command except that the data is not transferred to memory. This command is used to check that a record or group of records have been written correctly through verifying the CRC character.

Scan

The Scan command is used to search fields within disk records for a specified pattern. It compares a sector image in memory with a sector or multiple sectors on disk.

A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	SEL 1	SEL 0	0	0	0	S.DATA S.DELD	0	0
0	1	TRACK ADDR 0-255							
0	1	SECTOR 0-255							
0	1	LENGTH		NO. OF SECTORS					
0	1	SCAN TYPE		STEP SIZE					
0	1	FIELD LENGTH							

Command $D_2 = 0$ Scan Data
$D_2 = 1$ Scan Data and Deleted Data

Parameters 0, 1, 2 are same as the Read Command

Parameter 3

D7-D6: Indicate scan type

00-EQ Scan for each character within the field length equal to the corresponding character within the disk sector.

01-GE Scan for each character within the disk sector greater than or equal to the corresponding character within the field length.

10-LE Scan for each character within the disk sector less than or equal to corresponding character within the field length.

D5-D0: Step Size: The Step Size field specifies the offset to the next record in a multirecord scan. In this case, the next record address is generated by adding the Step Size to the current record address.

Parameter 4, Field Length

The Field Length is the number of characters to be included in each scan comparison group.

More detailed information about the completion of the scan command may be obtained through the Read Special Registers command discussed previously.

Read Special Register

Parameter (Hex) Results

06 Record number in which the scan condition was met.

14 Count MSB — The MSB of the count is decremented every 128 characters.

13 Count LSB — The LSB of the count is set to 128 and decremented every time a character is compared.

Notes: 1. The character (from memory) $(FF)_H$ is not compared.
2. The image in memory must be supplied to the FDC multiple times during the scan operation. Usually this will be performed through the use of the 8257 DMA controller auto load mode.

Commands That Process Special Data

Read ID

The Read ID command will transfer the specified number of ID fields into memory (beginning with the first ID field after Index). The CRC character is checked but not transferred.

A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	SEL 1	SEL 0	0	1	1	0	1	1
0	1	TRACK ADDRESS							
0	1	0	0	0	0	0	0	0	0
0	1	NUMBER OF ID FIELDS							

Format Track

A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	SEL 1	SEL 0	1	0	0	0	1	1
0	1	TRACK ADDRESS							
0	1	GAP 3 SIZE MINUS 6							
0	1	LENGTH			NO. OF SECTORS/TRACK				
0	1	GAP 5 SIZE MINUS 6							
0	1	GAP 1 SIZE MINUS 6							

The format command can be used to initialize a disk track compatible with the IBM 3740 format. A Shugart "IBM Type" mini-floppy format may also be generated.

When a format track command is issued, the user must supply a list of the ID fields in memory. As the command is processed, the ID fields (cylinder address, head address, sector address, record length) are read from memory and transferred to the disk. Parameter 2, D_7-D_5 specify record length; bits coded the same as in Read Data Command.

The following is the gap size and description summary:

Gap 1 Programmable
Gap 2 17 Bytes
Gap 3 Programmable
Gap 4 Variable
Gap 5 Programmable

The last six bytes of gaps 1,2,3 and 5 are $[00]_H$, all other bytes in the gaps are $[FF]_H$. The Gaps 1,3,5 counts specified by the user are the counts of the number of bytes of $[FF]_H$. Gap 4 is written until the leading edge of the index pulse. If a Gap 5 size of zero is specified, the Index Mark is not written.

IBM Format Implementation Summary

Track Format

The disk has 77 tracks, numbered physically from 00 to 76, with track 00 being the outermost track. There are logically 75 data tracks and two alternate tracks. Any two tracks may be initialized as bad tracks. The data tracks are numbered logically in sequence from 00 to 74, skipping over bad tracks (alternate tracks replace bad tracks). Note: In IBM format track 00 cannot be a bad track.

Sector Format

Eack track is divided into 26, 15, or 8 sectors of 128, 256, or 512 bytes length respectively. The first sector is numbered 01, and is physically the first sector after the physical index mark. The logical sequence of the remaining sectors may be nonsequential physically. The location of these is determined at initialization by CPU software.

Each sector consists of an ID field and a data field. All fields are separated by gaps. The beginning of each field is indicated by 6 bytes of $(00)_H$ followed by one byte mark.

Address Marks

Address Marks are unique bit patterns one byte in length which are used to identify the beginning of ID and Data fields and to synchronize the deserializing circuitry with the first byte of each field. Address Mark bytes are unique from all other data bytes in that certain bit cells do not contain a clock bit (all other data bytes have clock bits in every bit cell.) There are four different types of Address Marks used. Each of these is used to identify different types of fields.

Index Address Mark

The Index Address Mark is located at the beginning of each track and is a fixed number of bytes in front of the first record.

ID Address Mark

The ID Address Mark byte is located at the beginning of each ID field on the diskette.

Data Address Mark

The Data Address Mark byte is located at the beginning of each non-deleted Data Field on the diskette.

Deleted Data Address Mark

The Deleted Data Address Mark byte is located at the beginning of each deleted Data Field on the diskette.

Address Mark Summary	Clock Pattern	Data Pattern
Index Address Mark	D7	FC
ID Address Mark	C7	FE
Data Address Mark	C7	FB
Deleted Data Address Mark	C7	F8
Bad Track ID Address Mark	C7	FE

ID Field

MARK	C	H	R	N	CRC	CRC

C = Cylinder (Track) Address, 00-74
H = Head Address
R = Record (Sector) Address, 01-26
N = Record (Sector) Length, 00-02
Note: Sector Length = $128 \times (2^N - 1)$
CRC = 16 Bit CRC Character (See Below)

Data Field

MARK	DATA	CRC	CRC

Data is 128, 256, or 512 bytes long.

Note: All marks, data, ID characters and CRC characters are recorded and read most significant bit first.

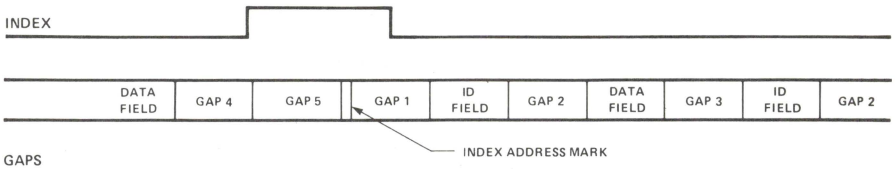
CRC Character

The 16-bit CRC character is generated using the generator polynomial $X^{16} + X^{12} + X^5 + 1$, normally initialized to $(FF)_H$. It is generated including all characters except the CRC in the ID or data field, including the data (not the clocks) in the mark. It is recorded and read most significant bit first.

Bad Track Format

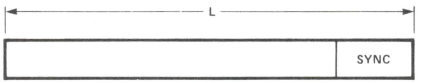
The Bad Track Format is the same as the good track format except that the bad track ID field is initialized as follows:

$C = H = R = N = (FF)_H$

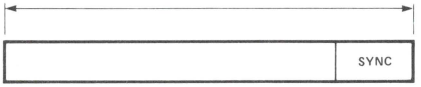


GAPS

GAP 1: POST INDEX GAP



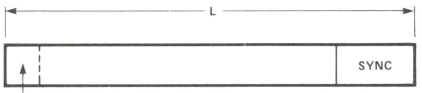
GAP 2: POST ID FIELD GAP



WRITE GATE TURN-ON FOR UPDATE OF NEXT DATA FIELD.

NOTE: THE WRITE GATE TURN-ON SHOULD BE TIMED TO WITHIN ± 1 BIT BY COUNTING THE BYTES IN THE GAP UNTIL 1 BYTE BEFORE THE TURN-ON.

GAP 3: POST DATA FIELD GAP

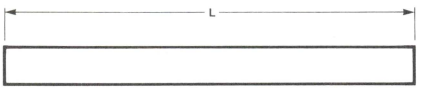


WRITE GATE TURN-OFF FROM UPDATE OF PREVIOUS DATA FIELD.

NOTE: IBM FORMAT REQUIRES AT LAT 2 BINARY "1" BITS AS A DATA FIELD POSTAMBLE.

2-BITS

GAP 4: FINAL GAP



GAP 5: INITIAL GAP

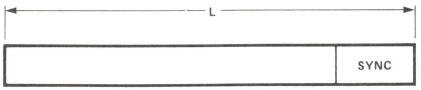
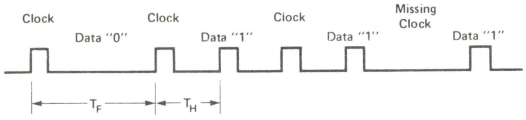


Figure 6. Track Format

Data Format

Data is written (general case) in the following manner:



T_F = Full Bit Time = Nominally 4μs
T_H = Half Bit Time = Nominally 2μs

References

"The IBM Diskette for Standard Data Interchange", IBM Document GA21-9182-0. "System 32", Chapter 8, IBM Document GA21-9176-0.

Data Track Gap Lengths

Data Field Length (Bytes)	Gap 1	Gap 2*	Gap 3*	Gap 4**	Gap 5
128	32	17	33	274	46
256	32	17	48	197	46
512	32	17			46

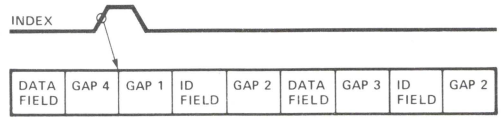
*Nominal after data written.
**Nominal after initialization.

Notes:
1. L is the gap length in bytes.
2. SYNC consists of 6 bytes of (00)H.
3. All other bytes in the gaps are (FF)H.
4. All gaps except Gap 4 are fixed at initialization. Gap 3 length is nominal after writing data.

Mini-floppy Disk Format

The mini-floppy disk format display differs from the standard disk format in the following ways:

1. Gap 5 and the Index Address mark have been eliminated.
2. There are fewer sectors/track.



Gaps

Gap 1 = 16 bytes of FF Hex followed by 6 bytes of zeros.
Gap 2 = 11 bytes of FF Hex followed by 6 bytes of zeros.
Gap 3 size is a function of the record size. For 128 byte records Gap 3 = 27 bytes of FF Hex followed by 6 bytes of zeros.
Gap 4 is a final gap and is whatever is left over.

The ID field format marks, and CRC used are the same as in the standard disk format.

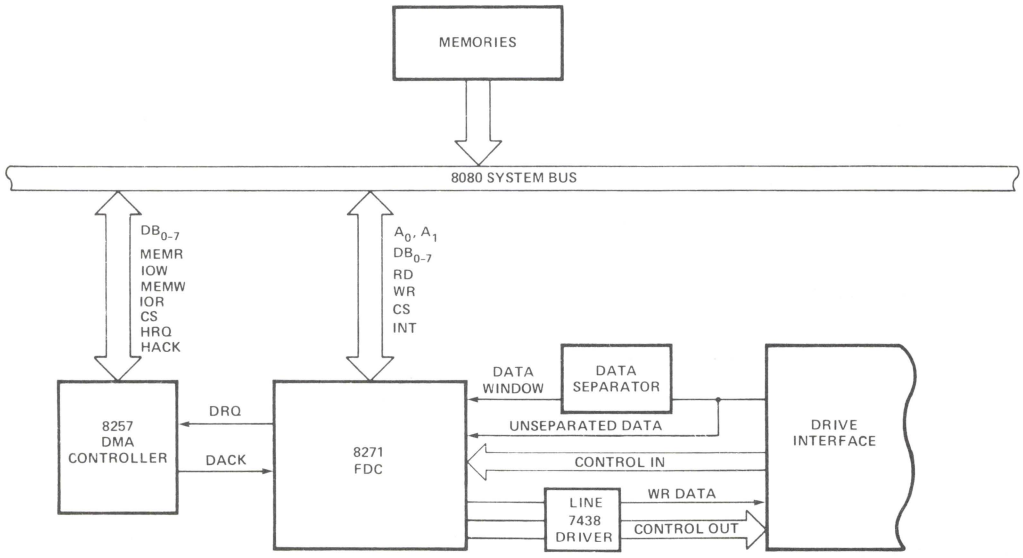


Figure 7. 8271 System Diagram

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 50°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin With Respect to Ground ..... -0.5V to +7V
Power Dissipation ..... 1 Watt

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to 50°C, V_{CC} = +5.0V ±5%

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	Volts	
V_{IH}	Input High Voltage	2.0	(V_{CC} + 0.5)	Volts	
V_{OL}	Output Low Voltage		0.45	Volts	I_{OL} = 2.0mA
V_{OH}	Output High Voltage	2.4		Volts	I_{OH} = -200μA
I_{IL}	Input Load Current		±10	μA	V_{IN} = V_{CC} to 0V
I_{OZ}	Off-State Output Current		±10	μA	V_{OUT} = V_{CC} to 0V
I_{CC}	V_{CC} Supply Current		160	mA	

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	t_c = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured Pins Returned to GND

A.C. CHARACTERISTICS

T_A = 0°C to 50°C, V_{CC} = +5.0V ±5%

Read Cycle

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{AC}	Select Setup to $\overline{RQ}$	0		ns	
t_{CA}	Select Hold from $\overline{RD}$	0		ns	
t_{RR}	$\overline{RD}$ Pulse Width	250		ns	
t_{AD}	Data Delay from Address		200	ns	
t_{RD}	Data Delay from $\overline{RD}$		150	ns	C_L = 150pF
t_{DF}	Output Float Delay	20	100	ns	C_L = 20pF for Minimum; 150pF for Maximum

Write Cycle

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{AC}	Select Setup to $\overline{WR}$	0		ns	
t_{CA}	Select Hold from $\overline{WR}$	0		ns	
t_{WW}	$\overline{WR}$ Pulse Width	250		ns	
t_{DW}	Data Setup to $\overline{WR}$	150		ns	
t_{WD}	Data Hold from $\overline{WR}$	-20		ns	

DMA

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{CQ}	Request Hold from $\overline{WR}$ or $\overline{RD}$ (for Non-Burst Mode)		150	ns	

Other Timing

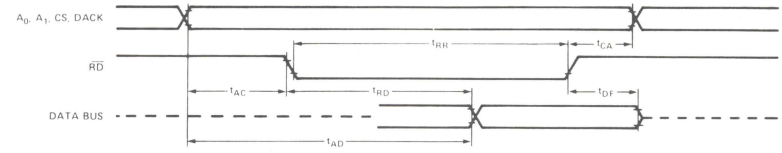
Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{RSTW}	Reset Pulse Width	10		t_{CY}	
t_r	Input Signal Rise Time		20	ns	
t_f	Input Signal Fall Time		20	ns	
t_{RSTS}	Reset to First $\overline{IOWR}$	2		t_{CY}	
t_{CY}	Clock Period	250			See Note 3
t_{CL}	Clock Low Period	T_{BS}			See Note 2
t_{CH}	Clock High Period	T_{BS}			See Note 2

Notes:

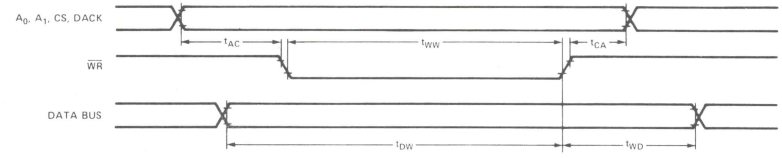
1. All timing measurements are made at the following reference voltages unless specified otherwise:
   Input "1" at 2.0V, "0" at 0.8V
   Output "1" at 2.0V, "0" at 0.8V
2. To be specified
3. Standard Floppy: T_{CY} = 250ns ± 0.4%
   Mini-Floppy: T_{CY} = 500ns ± 0.4%

WAVEFORMS

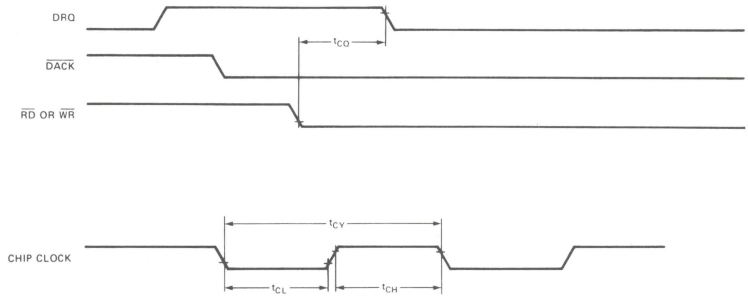
Read Waveforms

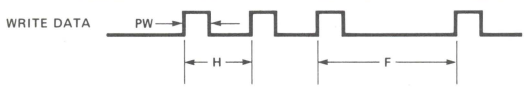


Write Waveforms



DMA Waveforms





	* t_{CY} = 250ns ± 0.4%	** t_{CY} = 500ns ± 0.4%
PULSE WIDTH PW = t_{CY} ± 30ns.	250ns ± 30ns	500ns ± 30ns
H(HALF BIT CELL) = 8 t_{CY}	2.0 sec ± 8ns	4.0μsec ± 16ns
F(FULL BIT CELL) = 16 t_{CY}	4.0 sec ± 16ns	8.0μsec ± 32ns

Figure 18. Write Data

	* t_{CY} = 250ns	** t_{CY} = 500ns
F(MINIMUM FULL BIT-CELL) ≥ 8t_{CY}	2.0μsec	4.0μsec
H(MINIMUM HALF BIT-CELL) ≥ 4t_{CY}	1.0μsec	2.0μsec

* Standard flexible disk drive timing.
** Minifloppy timing.

Figure 19. Read Data

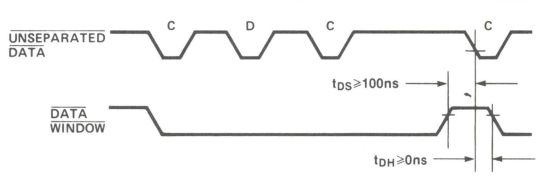


Figure 20. Single-Shot Data Separator

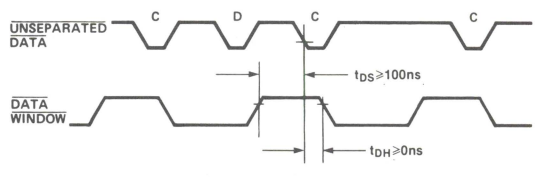


Figure 21. Data Separator

MPU PERIPHERALS

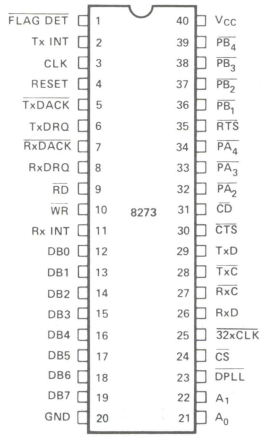
PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

8273
PROGRAMMABLE HDLC/SDLC PROTOCOL CONTROLLER

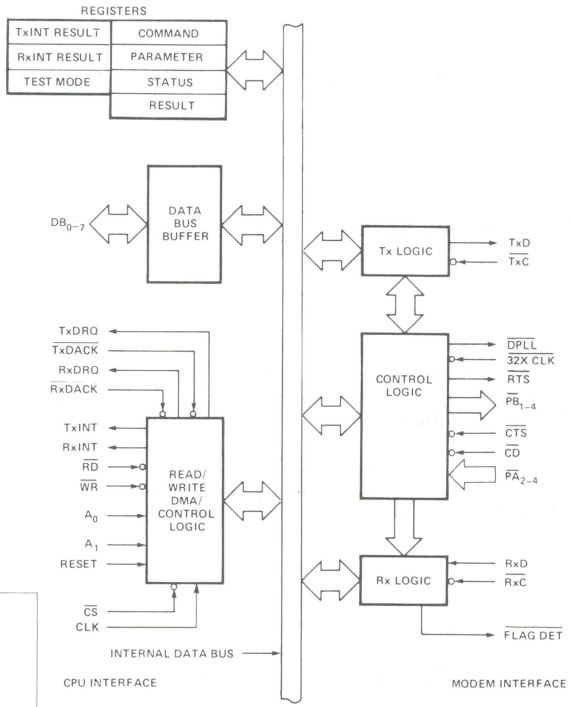
- HDLC/SDLC Compatible
- Frame Level Commands
- Full Duplex, Half Duplex, or Loop SDLC Operation
- Up to 64K Baud Transfers
- Two User Programmable Modem Control Ports
- Automatic FCS (CRC) Generation and Checking
- Programmable NRZI Encode/Decode
- N-Bit Reception Capability
- Digital Phase Locked Loop Clock Recovery
- Minimum CPU Overhead
- Fully Compatible with 8080/8085 CPUs
- Single +5V Supply
- 40-Pin Package

The Intel® 8273 Programmable HDLC/SDLC Protocol Controller is a dedicated device designed to support the ISO/C-CITT's HDLC and IBM's SDLC communication line protocols. It is fully compatible with Intel's new high performance microcomputer systems such as the MCS-85™. A frame level command set is achieved by a unique microprogrammed dual processor chip architecture. The processing capability supported by the 8273 relieves the system CPU of the low level real-time tasks normally associated with controllers.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

DB0–DB7	DATA BUS (8 BITS)	$\overline{CS}$	CHIP SELECT
FLAG DET	FLAG DETECT	32xCLK	32 TIMES CLOCK
TxINT	TRANSMITTER INTERRUPT	Rx D	RECEIVER DATA
CLK	CLOCK INPUT	Rx C	RECEIVER CLOCK
RESET	RESET	Tx C	TRANSMITTER CLOCK
Tx DACK	TRANSMITTER DMA ACKNOWLEDGE	Tx D	TRANSMITTER DATA
TxDRQ	TRANSMITTER DMA REQUEST	CTS	CLEAR TO SEND
RD	READ INPUT	CD	CARRIER DETECT
WR	WRITE INPUT	PA_2–PA_4	GP INPUT PORTS
Rx DACK	RECEIVER DMA ACKNOWLEDGE	PB_1–PB_4	GP OUTPUT PORTS
Rx DRQ	RECEIVER DMA REQUEST	RTS	REQUEST TO SEND
Rx INT	RECEIVER INTERRUPT	V_{CC}	+5 VOLT SUPPLY
A0–A1	COMMAND REGISTER SELECT ADDRESS	GND	GROUND
DPLL	DIGITAL PHASE LOCKED LOOP		

MPU PERIPHERALS

A BRIEF DESCRIPTION OF HDLC/SDLC PROTOCOLS

General

The High Level Data Link Control (HDLC) is a standard communication link protocol established by International Standards Organization (ISO). HDLC is the discipline used to implement ISO X.25 packet switching systems.

The Synchronous Data Link Control (SDLC) is an IBM communication link protocol used to implement the System Network Architecture (SNA). Both the protocols are bit oriented, code independent, and ideal for full duplex communication. Some common applications include terminal to terminal, terminal to CPU, CPU to CPU, satellite communication, packet switching and other high speed data links. In systems which require expensive cabling and interconnect hardware, any of the two protocols could be used to simplify interfacing (by going serial), thereby reducing interconnect hardware costs. Since both the protocols are speed independent, reducing interconnect hardware could become an important application.

Network

In both the HDLC and SDLC line protocols, according to a pre-assigned hierarchy, a PRIMARY (Control) STATION controls the overall network (data link) and issues commands to the SECONDARY (Slave) STATIONS. The latter comply with instructions and respond by sending appropriate RESPONSES. Whenever a transmitting station must end transmission prematurely it sends an ABORT character. Upon detecting an abort character, a receiving station ignores the transmission block called a FRAME. Time fill between frames can be accomplished by transmitting either continuous frame preambles called FLAGS or an abort character. A time fill within a frame is not permitted. Whenever a station receives a string of more that fifteen consecutive ones, the station goes into an IDLE state.

Frames

A single communication element is called a FRAME which can be used for both Link Control and data transfer purposes. The elements of a frame are the beginning eight bit FLAG (F) consisting of one zero, six ones, and a zero, an eight bit ADDRESS FIELD (A), an eight bit CONTROL FIELD (C), a variable (N-bit) INFORMATION FIELD (I), a sixteen bit FRAME CHECK SEQUENCE (FCS), and an eight bit end FLAG (F), having the same bit pattern as the beginning flag. In HDLC the Address (A) and Control (C) bytes are extendable. The HDLC and the SDLC use three types of frames; an Information Frame is used to transfer data, a Supervisory Frame is used for control purposes, and a Non-sequenced Frame is used for initialization and control of the secondary stations.

Frame Characteristics

An important characteristic of a frame is that its contents are made code transparent by use of a zero bit insertion and deletion technique. Thus, the user can adopt any format or code suitable for his system — it may even be a computer word length or a "memory dump". The frame is bit oriented that is, bits, not characters in each field, have specific meanings. The Frame Check Sequence (FCS) is an error detection scheme similar to the Cyclic Redundancy Checkword (CRC) widely used in magnetic disk storage devices. The Command and Response information frames contain sequence numbers in the control fields identifying the sent and received frames. The sequence numbers are used in Error Recovery Procedures (ERP) and as implicit acknowledgement of frame communication, enhancing the true full-duplex nature of the HDLC/SDLC protocols.

In contrast, BISYNC is basically half-duplex (two way alternate) because of necessity to transmit immediate acknowledgement frames. HDLC/SDLC therefore saves propagation delay times and have a potential of twice the throughput rate of BISYNC.

It is possible to use HDLC or SDLC over half duplex lines but there is a corresponding loss in throughput because both are primarily designed for full-duplex communication. As in any synchronous system, the bit rate is determined by the clock bits supplied by the modem, protocols themselves are speed independent.

A byproduct of the use of zero-bit insertion-deletion technique is the non-return-to-zero invert (NRZI) data transmission/reception compatibility. The latter allows HDLC/SDLC protocols to be used with asynchronous data communication hardware in which the clocks are derived from the NRZI encoded data.

References

IBM Synchronous Data Link Control General Information, IBM, GA27-3093-1.

Standard Network Access Protocol Specification, DATAPAC, Trans-Canada Telephone System CCG111

Recommendation X.25, ISO/CCITT March 2, 1976.

IBM 3650 Retail Store System Loop Interface OEM Information, IBM, GA 27-3098-0

Guidebook to Data Communications, Training Manual, Hewlett-Packard 5955-1715

IBM Introduction to Teleprocessing, IBM, GC 20-8095-02

System Network Architecture, Technical Overview, IBM, GA 27-3102

System Network Architecture Format and Protocol, IBM GA 27-3112

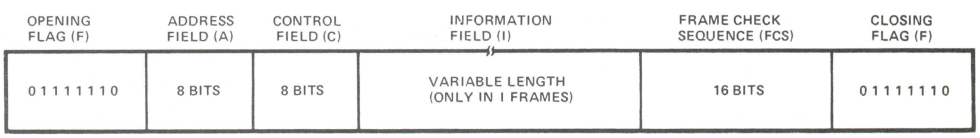


Figure 1. Frame Format

FUNCTIONAL DESCRIPTION

General

The Intel® 8273 HDLC/SDLC controller is a microcomputer peripheral device which supports the International Standards Organization (ISO) High Level Data Link Control (HDLC), and IBM Synchronous Data Link Control (SDLC) communications protocols. This controller minimizes CPU software by supporting a comprehensive frame-level instruction set and by hardware implementation of the low level tasks associated with frame assembly/disassembly and data integrity. The 8273 can be used in either synchronous or asynchronous applications. In asynchronous applications the data can be programmed to be encoded/decoded in NRZI code. The clock is derived from the NRZI data using a digital phase locked loop. The data transparency is achieved by using a zero-bit insertion/deletion technique. The frames are automatically checked for errors during reception by verifying the Frame Check Sequence (FCS); the FCS is automatically generated and appended before the final flag in transmit.

The 8273 recognizes and can generate flags (01111110), Abort, Idle, and GA (EOP) characters.

The 8273 can assume either a primary (control) or a secondary (slave) role. It can therefore be readily implemented in an SDLC loop configuration as typified by the IBM 3650 Retail Store System by programming the 8273 into a one-bit delay mode. In such a configuration, a two wire pair can be effectively used for data transfer between controllers and loop stations. The digital phase locked loop output pin can be used by the loop station without the presence of an accurate Tx clock.

Hardware Description

The 8273 is packaged in a 40 pin DIP. The following is a functional description of each pin.

Pin Name (No.)	I/O	Description
V_{CC} (40)		+5V Supply
GND (20)		Ground
RESET (4)	I	A high signal on this pin will force the 8273 to an idle state. The 8273 will remain idle until a command is issued by the CPU. The modem interface output signals are forced high. Reset must be true for a minimum of 10 TCY.
$\overline{CS}$ (24)	I	The $\overline{RD}$ and $\overline{WR}$ inputs are enabled by the chip select input.
DB_7-DB_0 (19-12)	I/O	The Data Bus lines are bidirectional three-state lines which interface with the system Data Bus.
$\overline{WR}$ (10)	I	The Write signal is used to control the transfer of either a command or data from CPU to the 8273.
$\overline{RD}$ (9)	I	The Read signal is used to control the transfer of either a data byte or a status word from the 8273 to the CPU.
TxINT (2)	O	The Transmitter interrupt signal indicates that the transmitter logic requires service.
RxINT (11)	O	The Receiver interrupt signal indicates that the Receiver logic requires service.
TxDRQ (6)	O	Requests a transfer of data between memory and the 8273 for a transmit operation.
RxRDQ (8)	O	Requests a transfer of data between the 8273 and memory for a receive operation.
$\overline{TxDACK}$ (5)	I	The Transmitter DMA acknowledge signal notifies the 8273 that the TxDMA cycle has been granted.
$\overline{RxDACK}$ (7)	I	The Receiver DMA acknowledge signal notifies the 8273 that the RxDMA cycle has been granted.
A_1-A_0 (22-21)	I	These two lines are CPU Interface Register Select lines.
TxD (29)	O	This line transmits the serial data to the communication channel.
$\overline{TxC}$ (28)	I	The transmitter clock is used to synchronize the transmit data.
RxD (26)	I	This line receives serial data from the communication channel.
$\overline{RxC}$ (27)	I	The Receiver Clock is used to synchronize the receive data.
$\overline{32X\ CLK}$ (25)	I	The 32X clock is used to provide clock recovery when an asynchronous modem is used. In loop configuration the loop station can run without an accurate 1X clock by using the 32X CLK in conjunction with the DPLL output. (This pin must be grounded when not used).
$\overline{DPLL}$ (23)	O	Digital Phase Locked Loop output can be tied to RxC and/or TxC when 1X clock is not available. DPLL is used with 32X CLK.
$\overline{FLAG\ DET}$ (1)	O	Flag Detect signals that a flag (01111110) has been received by an active receiver.
$\overline{RTS}$ (35)	O	Request to Send signals that the 8273 is ready to transmit data.
$\overline{CTS}$ (30)	I	Clear to Send signals that the modem is ready to accept data from the 8273.
$\overline{CD}$ (31)	I	Carrier Detect signals that the line transmission has started and the 8273 may begin to sample data on RxD line.
$\overline{PA_{2-4}}$ (32-34)	I	General purpose input ports. The logic levels on these lines can be Read by the CPU through the Data Bus Buffer.
$\overline{PB_{1-4}}$ (36-39)	O	General purpose output ports. The CPU can write these output lines through Data Bus Buffer.
CLK (3)	I	A square wave TTL clock.

CPU Interface

The CPU interface is optimized for the MCS-80/85™ bus with an 8257 DMA controller. However, the interface is flexible, and allows either DMA or non-DMA data transfers, interrupt or non-interrupt driven. It further allows maximum line utilization by providing early interrupt mechanism for buffered (only the information field can be transferred to memory) Tx command overlapping. It also provides separate Rx and Tx interrupt output channels for efficient operation. The 8273 keeps the interrupt request active until all the associated interrupt results have been read.

The CPU utilizes the CPU interface to specify commands and transfer data. It consists of seven registers addressed via $\overline{CS}$, A_1, A_0, $\overline{RD}$ and $\overline{WR}$ signals and two independent data registers for receive data and transmit data. A_1, A_0 are generally derived from two low order bits of the address bus. If an 8080 based CPU is utilized, the $\overline{RD}$ and $\overline{WR}$ signals may be driven by the 8228 $\overline{I/OR}$ and $\overline{I/OW}$. The table shows the seven register select decoding:

Address Inputs		Control Logic Inputs	
A1	A0	$\overline{CS} \cdot \overline{RD}$	$\overline{CS} \cdot \overline{WR}$
0	0	Status	Command
0	1	Result	Parameter
1	0	TxINT Result	Test Mode
1	1	RxINT Result	—

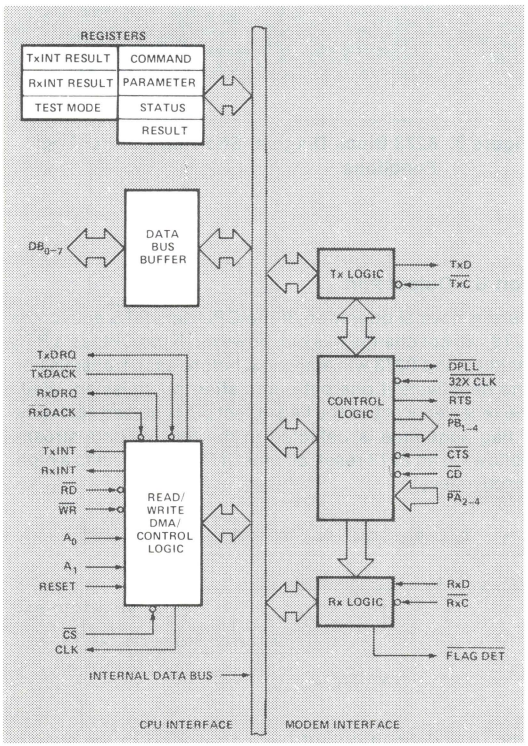


Figure 2. 8273 Block Diagram Showing CPU Interface Functions

Register Description

Command

Operations are initiated by writing an appropriate command in the Command Register.

Parameter

Parameters of commands that require additional information are written to this register.

Result

Contains an immediate result describing an outcome of an executed command.

Transmit Interrupt Result

Contains the outcome of 8273 transmit operation (good/bad completion).

Receive Interrupt Result

Contains the outcome of 8273 receive operation (good/bad completion), followed by additional results which detail the reason for interrupt.

Status

The status register reflects the state of the 8273 CPU Interface.

DMA Data Transfers

The 8273 CPU interface supports two independent data interfaces: receive data and transmit data. At high data transmission speeds the data transfer rate of the 8273 is great enough to justify the use of direct memory access (DMA) for the data transfers. When the 8273 is configured in DMA mode, the elements of the DMA interfaces are:

TxDRQ: Transmit DMA Request

Requests a transfer of data between memory and the 8273 for a transmit operation.

$\overline{TxDACK}$: Transmit DMA Acknowledge

The $\overline{TxDACK}$ signal notifies the 8273 that a transmit DMA cycle has been granted.

RxDRQ: Receive DMA Request

Requests a transfer of data between the 8273 and memory for a receive operation.

$\overline{\text{RxDACK}}$: Receive DMA Acknowledge

The $\overline{\text{RxDACK}}$ signal notifies the 8273 that a receive DMA cycle has been granted.

$\overline{\text{RD}}$, $\overline{\text{WR}}$: Read, Write

The $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals are used to specify the direction of the data transfer.

DMA transfers require the use of a DMA controller such as the Intel 8257. The function of the DMA controller is to provide sequential addresses and timing for the transfer, at a starting address determined by the CPU. Counting of data block lengths is performed by the 8273.

To request a DMA transfer the 8273 raises the appropriate DMA REQUEST. DMA ACKNOWLEDGE and READ enables DMA data onto the bus (independently of CHIP SELECT). DMA ACKNOWLEDGE and WRITE transfers DMA data to the 8273 (independent of CHIP SELECT).

It is also possible to configure the 8273 in the non-DMA data transfer mode. In this mode the CPU module must pass data to the 8273 in response to non-DMA data requests indicated by the status word.

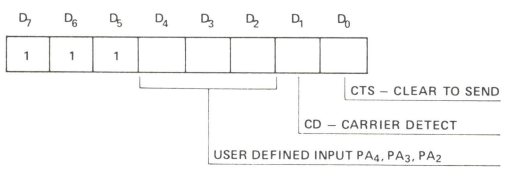
Modem Interface

The 8273 Modem interface provides both dedicated and user defined modem control functions. All the signals are active low so that EIA RS-232C inverting drivers (MC 1488) and inverting receivers (MC 1489) may be used to interface to standard modems. For asynchronous operation, this interface supports programmable NRZI data encode/decode, a digital phase locked loop for efficient clock extraction from NRZI data, and modem control ports with automatic $\overline{\text{CTS}}$, $\overline{\text{CD}}$ monitoring and $\overline{\text{RTS}}$ generation. This interface also allows the 8273 to operate in PRE-FRAME SYNC mode in which the 8273 prefixes 16 transitions to a frame to synchronize idle lines before transmission of the first flag.

It should be noted that all the 8273 port operations deal with logical values, for instance, bit D0 of Port A will be a one when $\overline{\text{CTS}}$ (Pin 30) is a physical zero (logical one).

Port A — Input Port

During operation, the 8273 interrogates input pins $\overline{\text{CTS}}$ (Clear to Send) and $\overline{\text{CD}}$ (Carrier Detect). $\overline{\text{CTS}}$ is used to condition the start of a transmission. If during transmission $\overline{\text{CTS}}$ is lost the 8273 generates an interrupt. During reception, if $\overline{\text{CD}}$ is lost, the 8273 generates an interrupt.



The user defined input bits correspond to the 8273 PA_4, PA_3 and PA_2 pins. The 8273 does not interrogate or manipulate these bits.

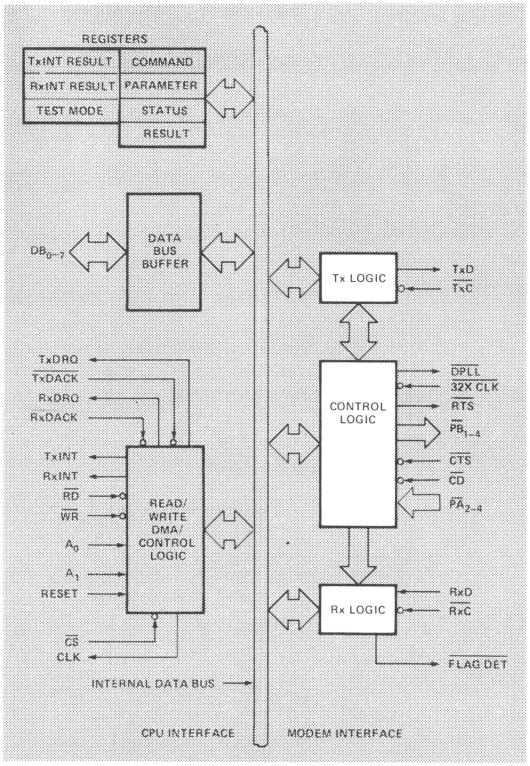
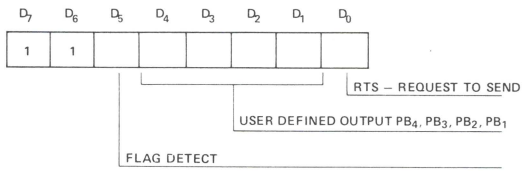


Figure 3. 8273 Block Diagram Showing Control Logic Functions

Port B - Output Port

During normal operation, if the CPU sets $\overline{\text{RTS}}$ active, the 8273 will not change this pin; however, if the CPU sets $\overline{\text{RTS}}$ inactive, the 8273 will activate it before each transmission and deactivate it one byte time after transmission. While the receiver is active the flag detect pin is pulsed each time a flag sequence is detected in the receive data stream. Following an 8273 reset, all pins of Port B are set to a high, inactive level.



The user defined output bits correspond to the state of PB_4-PB_1 pins. The 8273 does not interrogate or manipulate these bits.

Serial Data Logic

The Serial data is synchronized by the user transmit ($\overline{TxC}$) and receive ($\overline{RxC}$) clocks. The leading edge of $\overline{TxC}$ generates new transmit data and the trailing edge of $\overline{RxC}$ is used to capture receive data. The NRZI encoding/decoding of the receive and transmit data is programmable.

The diagnostic features included in the Serial Data logic are programmable loop back of data and selectable clock for the receiver. In the loop-back mode, the data presented to the TxD pin is internally routed to the receive data input circuitry in place of the RxD pin, thus allowing a CPU to send a message to itself to verify operation of the 8273.

In the selectable clock diagnostic feature, when the data is looped back, the receiver may be presented incorrect sample timing by the external circuitry. The user may select to substitute the $\overline{TxC}$ pin for the $\overline{RxC}$ input on-chip so that the clock used to generate the loop back data is used to sample it. Since TxD is generated off the leading edge of $\overline{TxC}$ and RxD is sampled on the trailing edge, the selected clock allows bit synchronism.

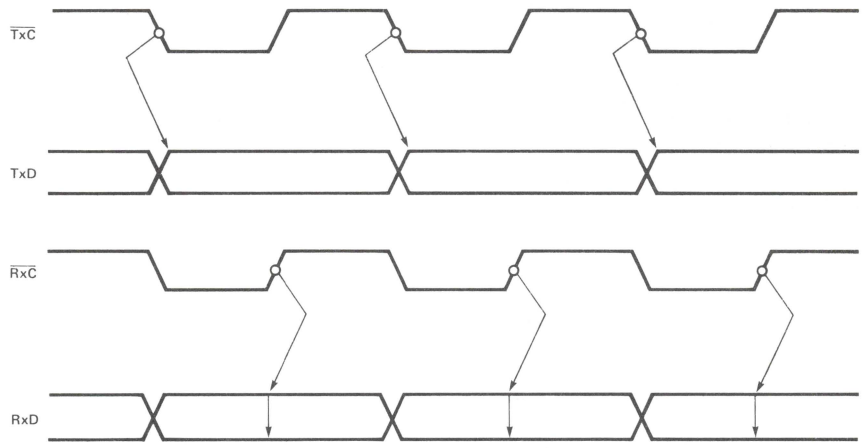


Figure 4. Transmit/Receive Timing

Asynchronous Mode Interface

Although the 8273 is fully compatible with the HDLC/SDLC communication line protocols, which are primarily designed for synchronous communication, the 8273 can also be used in asynchronous applications by using this interface. The interface employs a digital phase locked loop (DPLL) for clock recovery from a receive data stream and programmable NRZI encoding and decoding of data. The use of NRZI coding with SDLC transmission guarantees that within a frame, data transitions will occur at least every five bit times — the longest sequence of ones which may be transmitted without zero-bit insertion. The DPLL should be used only when NRZI coding is used since the NRZI coding will transmit zero sequence as line transitions. The digital phase locked loop also facilitates full-duplex and half-duplex asynchronous implementation with, or without modems.

Digital Phase Locked Loop

In asynchronous applications, the clock is derived from the receiver data stream by the use of the digital phase locked loop (DPLL). The DPLL requires a clock input at 32 times the required baud rate. The receive data (RxD) is sampled with this $\overline{32X\ CLK}$ and the 8273 DPLL supplies a sample pulse nominally centered on the RxD bit cells. The DPLL has a built-in "stiffness" which reduces sensitivity to line noise and bit distortion. This is accomplished by making phase error adjustments in discrete increments. Since the nominal pulse is made to occur at 32 counts of the $\overline{32X\ CLK}$, these counts are subtracted or added to the nominal, depending upon which quadrant of the four error quadrants the data edge occurs in. For example if an RxD edge is detected in quadrant A1, it is apparent that the $\overline{DPLL}$ sample "A" was placed too close to the trailing edge of the data cell; sample "B" will then be placed at T = ($T_{nominal}$ - 2 counts) = 30 counts of the $\overline{32X\ CLK}$ to move the sample pulse "B" toward the nominal center of the next bit cell. A data edge occuring in quadrant B1 would cause a smaller adjustment of phase with T = 31 counts of the $\overline{32X\ CLK}$. Using this technique the $\overline{DPLL}$ pulse will converge to nominal bit center within 12 data bit times, worst case, with constant incoming RxD edges.

A method of attaining bit synchronism following a line idle is to use PRE-FRAME SYNC mode of transmission.

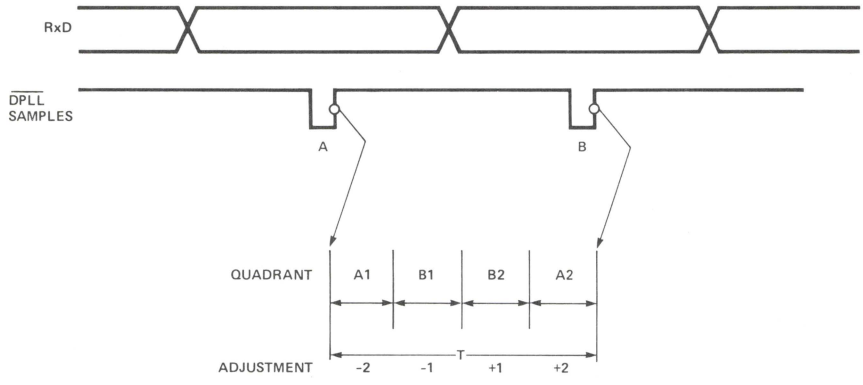
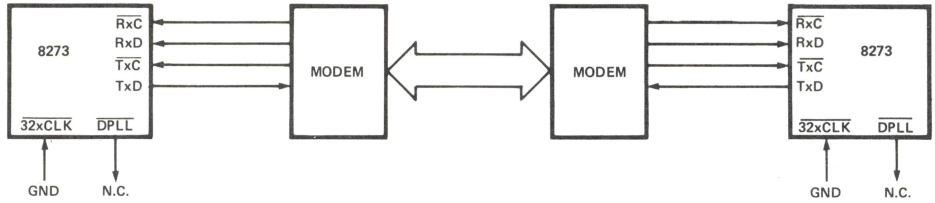
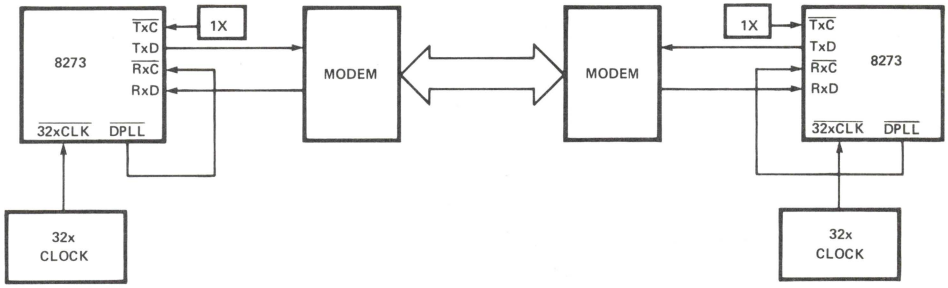


Figure 5. DPLL Sample Timing

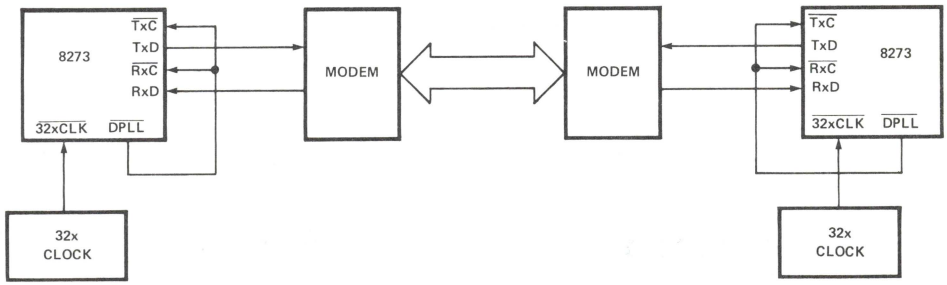
Synchronous Modem — Duplex or Half Duplex Operation



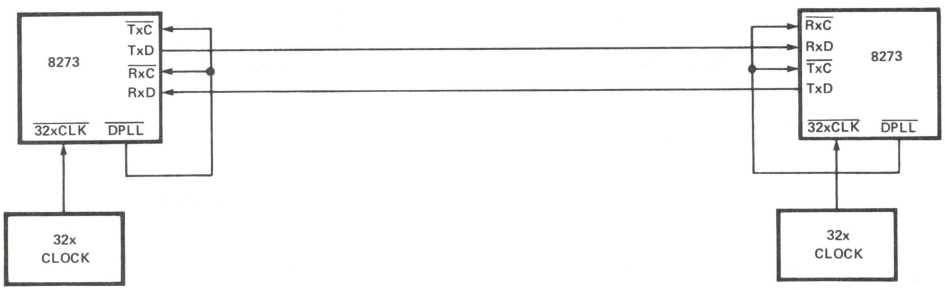
Asynchronous Modems — Duplex Operation



Asynchronous Modems — Half Duplex Operation



Asynchronous — No Modems — Duplex or Half Duplex



SDLC Loop

The DPLL simplifies the SDLC loop station implementation. In this application, each secondary station on a loop data link is a repeater set in one-bit delay mode. The signals sent out on the loop by the loop controller (primary station) are relayed from station to station then, back to the controller. Any secondary station finding its address in the A field captures the frame for action at that station. All received frames are relayed to the next station on the loop.

Loop stations are required to derive bit timing from the incoming NRZI data stream. The DPLL generates sample Rx clock timing for reception and uses the same clock to implement Tx clock timing.

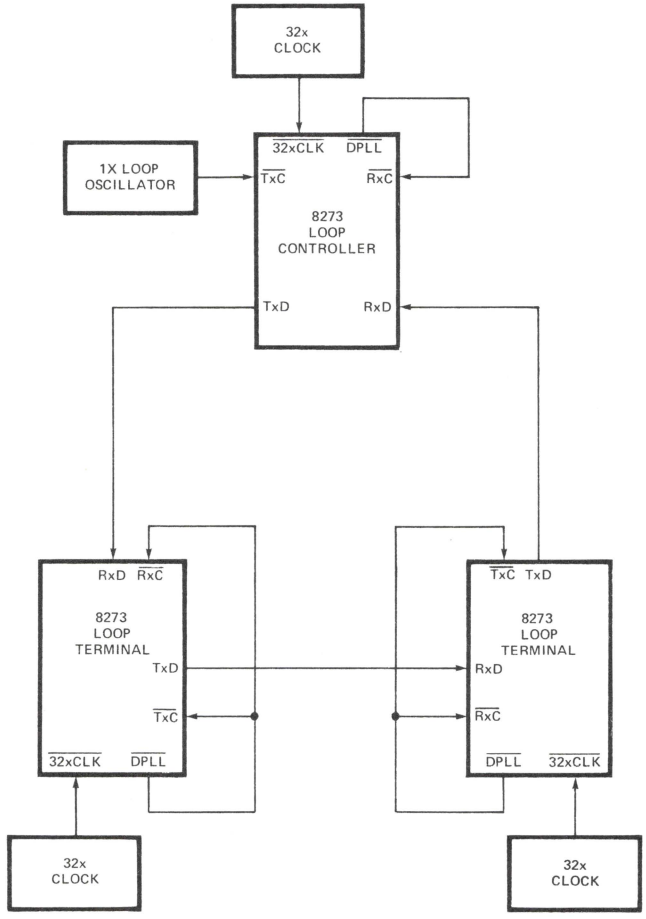
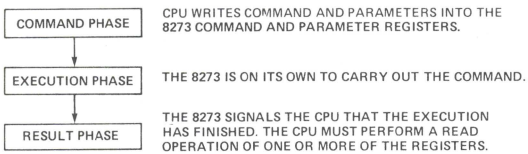


Figure 6. SDLC Loop Application

PRINCIPLES OF OPERATION

The 8273 is an intelligent peripheral controller which relieves the CPU of many of the rote tasks associated with constructing and receiving frames. It is fully compatible with the MCS-80/85™ system bus. As a peripheral device, it accepts commands from a CPU, executes these commands and provides an Interrupt and Result back to the CPU at the end of the execution. The communication with the CPU is done by activation of $\overline{CS}$, $\overline{RD}$, $\overline{WR}$ pins, while the A_1, A_0 select the appropriate registers on the chip as described in the Hardware Description Section.

The 8273 operation is composed of the following sequence of events:



The Command Phase

During the command phase, the software writes a command to the command register. The command bytes provide a general description of the type of operation requested. Many commands require more detailed information about the command. In such a case up to four parameters are written into the parameter register. The flowchart of the command phase indicates that a command may not be issued if the Status Register indicates that the device is busy. Similarly if a parameter is issued when the Parameter Buffer shows full, incorrect operation will occur.

The 8273 is a duplex device and both transmitter and receiver may each be executing a command or passing results at any given time. For this reason separate interrupt pins are provided. However, the command register must be used for one command sequence at a time.

Status Register

The status register contains the status of the 8273 activity. The description is as follows.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CBSY	CBF	CPBF	CRBF	RxINT	TxINT	RxIRA	TxIRA

Bit 7 CBSY (Command Busy)

Indicates in-progress command, set for CPU poll when Command Register is full, reset upon command phase completion. It is improper to write a command when CBSY is set; it results in incorrect operation.

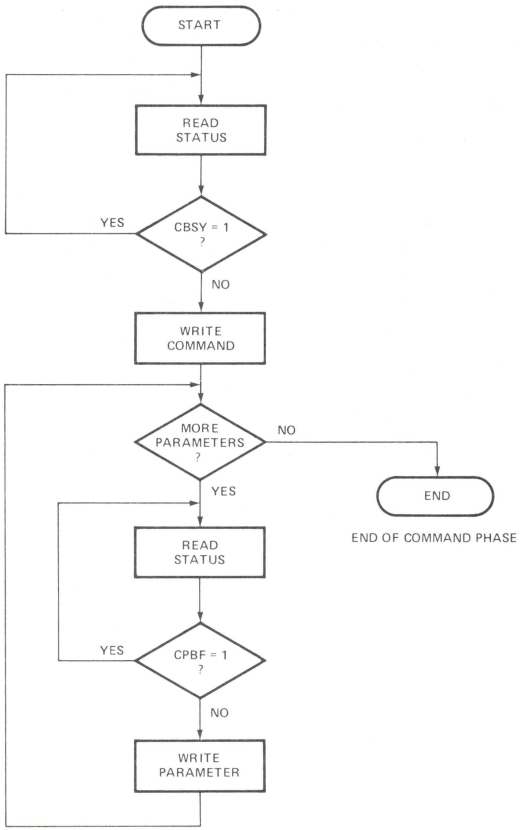


Figure 7. Command Phase Flowchart

Bit 6 CBF (Command Buffer Full)

Indicates that the command register is full, it is reset when the 8273 accepts the command byte but does not imply that execution has begun.

Bit 5 CPBF (Command Parameter Buffer Full)

CPBF is set when the parameter buffer is full, and is reset by the 8273 when it accepts the parameter. The CPU may poll CPBF to determine when additional parameters may be written.

Bit 4 CRBF (Command Result Buffer Full)

Indicates that an executed command immediate result is present in the Result Register. It is set by 8273 and reset when CPU reads the result.

Bit 3 RxINT (Receiver Interrupt)

RxINT indicates that the receiver requires CPU attention. It is identical to RxINT (pin 11) and is set by the 8273 either upon good/bad completion of a specified command or by Non-DMA data transfer. It is reset only after the CPU has read the result byte or has received a data byte from the 8273 in a Non-DMA data transfer.

Bit 2 TxINT (Transmitter Interrupt)

The TxINT indicates that the transmitter requires CPU attention. It is identical to TxINT (pin 2). It is set by 8273 either upon good/bad completion of a specified command or by Non-DMA data transfer. It is reset only after the CPU has read the result byte or has transferred transmit data byte to the 8273 in a Non-DMA transfer.

Bit 1 RxIRA (Receiver Interrupt Result Available)

The RxIRA is set by the 8273 when an interrupt result byte is placed in the RxIRA register. It is reset after the CPU has read the RxIRA register.

Bit 0 TxIRA (Transmitter Interrupt Result Available)

The TxIRA is set by the 8273 when an interrupt result byte is placed in the TxIRA register. It is reset when the CPU has read the TxIRA register.

The Execution Phase

Upon accepting the last parameter, the 8273 enters into the Execution Phase. The execution phase may consist of a DMA or other activity, and may or may not require CPU intervention. The CPU intervention is elliminated in this phase if the system utilizes DMA for the data transfers, otherwise, for non-DMA data transfers, the CPU is interrupted by the 8273 via TxINT and RxINT pins, for each data byte request.

The Result Phase

During the result phase, the 8273 notifies the CPU of the execution outcome of a command. This phase is initiated by:

1. The successful completion of an operation
2. An error detected during an operation.

To facilitate quick network software decisions, two types of execution results are provided:

1. An Immediate Result
2. A Non-Immediate Result

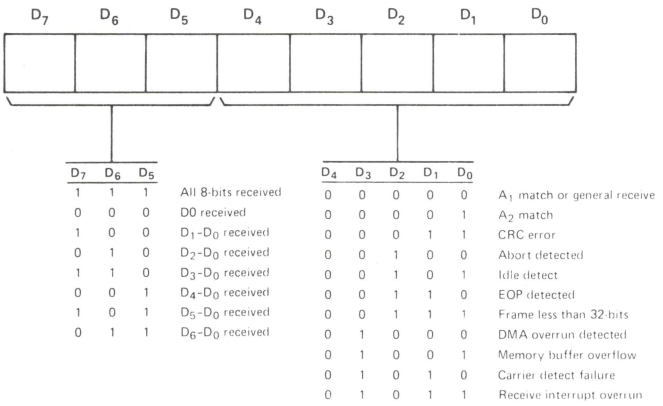


Figure 8. Rx Interrupt Result Byte Format

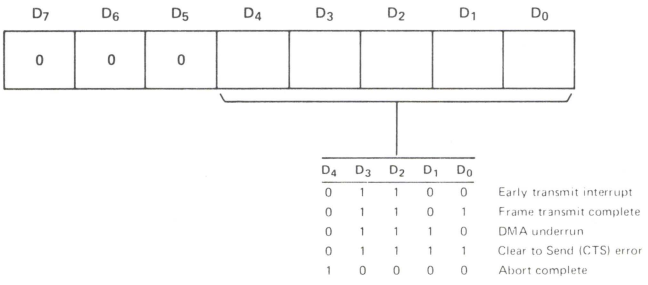


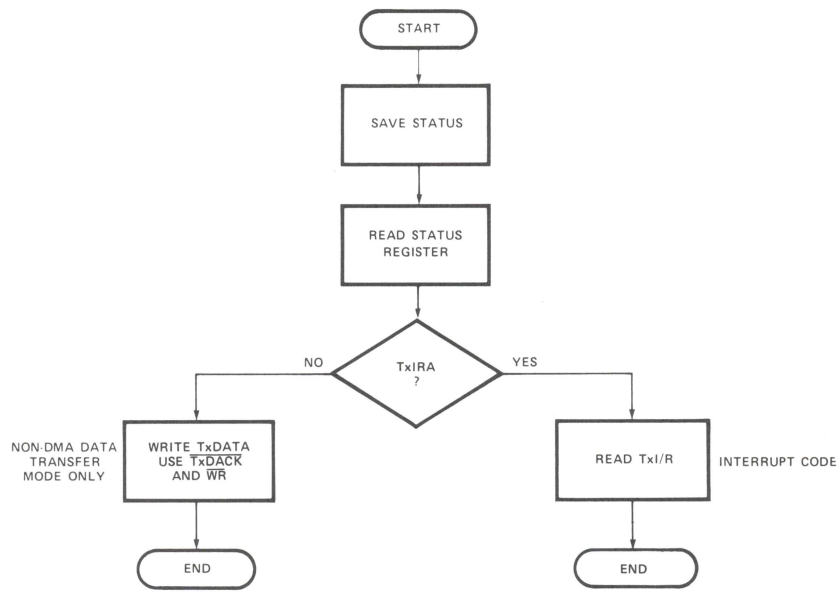
Figure 9. Tx Interrupt Result Byte Format

Immediate result is provided by the 8273 for commands such as Read Port A and Read Port B which have information ($\overline{CTS}$, $\overline{CD}$, $\overline{RTS}$, etc.) that the network software needs to make quick operational decisions.

A command which cannot provide an immediate result will generate an interrupt to signal the beginning of the Result phase. The immediate results are provided in the Result Register; all non-immediate results are available upon device interrupt, through Tx Interrupt Result Register TxI/R or Rx Interrupt Result Register RxI/R. The result may consist of a one-byte interrupt code indicating the condition for the interrupt and, if required, one or more bytes which detail the condition.

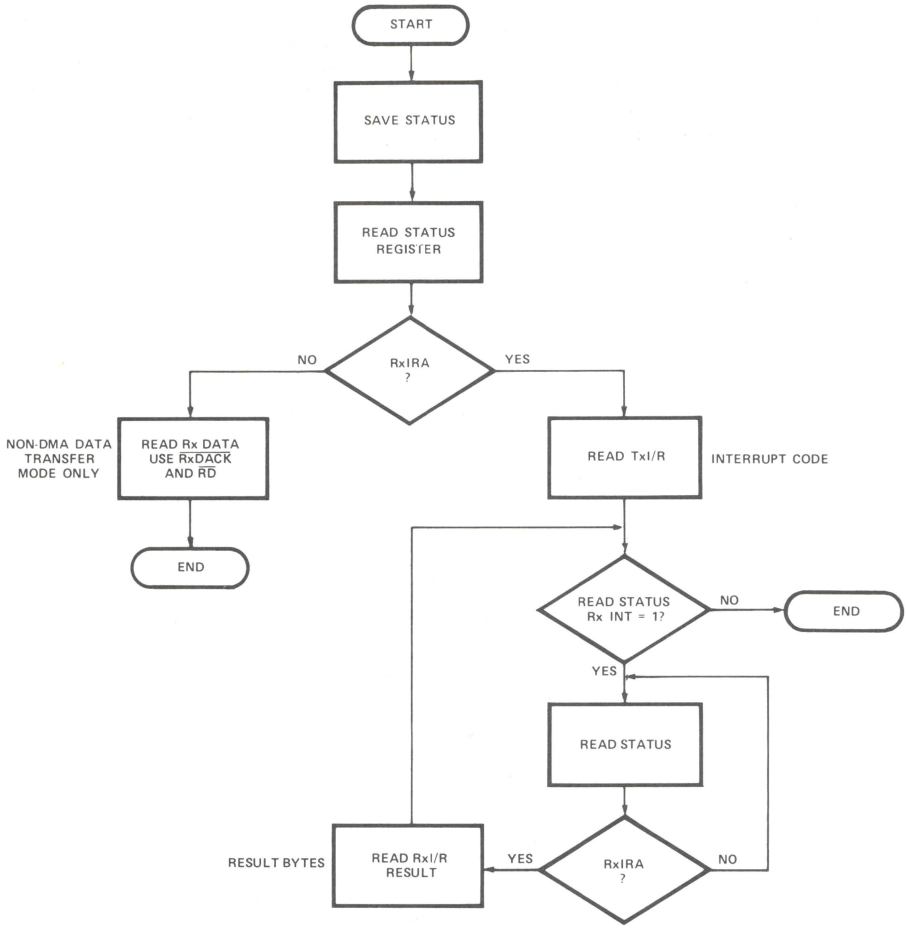
Tx and Rx Interrupt Result Registers

The Result Registers have a result code, the three high order bits D_7-D_5 of which are set to zero for all but the receive command. This command result contains a count that indicates the number of bits received in the last byte. If a partial byte is received, the high order bits of the last data byte are indeterminate.

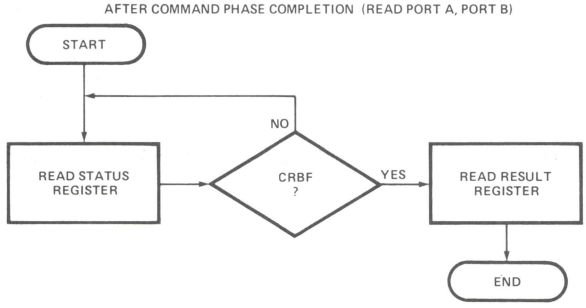


RESULT PHASE FLOWCHART — Tx INTERRUPT RESULTS

Figure 10. Tx Interrupt Service



RESULT PHASE FLOWCHART — INTERRUPT RESULTS



RESULT PHASE FLOWCHART — IMMEDIATE RESULTS

Figure 11. Rx Interrupt Service

DETAILED COMMAND DESCRIPTION

General

The 8273 HDLC/SDLC controller supports a comprehensive set of high level commands which allows the 8273 to be readily used in full-duplex, half-duplex, synchronous, asynchronous and SDLC loop configuration, with or without modems. These frame-level commands minimize CPU and software overhead. The 8273 has address and control byte buffers which allow the receive and transmit commands to be used in buffered or non-buffered modes.

In buffered transmit mode, the 8273 transmits a flag automatically, reads the Address and Control buffer registers and transmits the fields, then via DMA, it fetches the information field. The 8273, having transmitted the information field, automatically appends the Frame Check Sequence (FCS) and the end flag. Correspondingly, in buffered read mode, the Address and Control fields are stored in their respective buffer registers and only Information Field is transferred to memory.

In non-buffered transmit mode, the 8273 transmits the beginning flag automatically, then fetches and transmits the Address, Control and Information fields from the memory, appends the FCS character and an end flag. In the non-buffered receive mode the entire contents of a frame are sent to memory with the exception of the flags and FCS.

HDLC Implementation

HDLC Address and Control field are extendable. The extension is selected by setting the low order bit of the field to be extended to a one, a zero in the low order bit indicates the last byte of the respective field.

Since Address/Control field extension is normally done with software to maximize extension flexibility, the 8273 does not create or operate upon contents of the extended HDLC Address/Control fields. Extended fields are transparently passed by the 8273 to user as either interrupt results or data transfer requests. Software must assemble the fields for transmission and interrogate them upon reception.

However, the user can take advantage of the powerful 8273 commands to minimize CPU/Software overhead and simplify buffer management in handling extended fields. For instance buffered mode can be used to separate the first two bytes, then interrogate the others from buffer. Buffered mode is perfect for a two byte address field.

The 8273 when programmed, recognizes protocol characters unique to HDLC such as Abort, which is a string of seven or more ones (01111111). Since Abort character is the same as the GA (EOP) character used in SDLC Loop applications, Loop Transmit and Receive commands are not recommended to be used in HDLC. HDLC does not support Loop mode.

Initialization Set/Reset Commands

These commands are used to manipulate data within the 8273 registers. The Set commands have a single parameter which is a mask that corresponds to the bits to be set. (They perform a logical-OR of the specified register with the mask provided as a parameter). The Register commands have a single parameter which is a mask that has a zero in the bit positions that are to be reset. (They perform a logical-AND of the specified register with the mask).

Set One-Bit Delay (CMD Code A4)

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	1	0	1	0	0	1	0	0
PAR:	0	1	1	0	0	0	0	0	0	0

When one bit delay is set, 8273 retransmits the received data stream one bit delayed. This mode is entered at a receiver character boundary, and should only be used by Loop Stations.

Reset One-Bit Delay (CMD Code 64)

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	0	1	1	0	0	1	0	0
PAR:	0	1	0	1	1	1	1	1	1	1

The 8273 stops the one bit delayed retransmission mode.

Set Data Transfer Mode (CMD Code 97)

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	1	0	0	1	0	1	1	1
PAR:	0	1	0	0	0	0	0	0	0	1

When the data transfer mode is set, the 8273 will interrupt when data bytes are required for transmission or are available from a receive. If a transmit interrupt occurs and the status indicates that there is no Transmit Result (TxIRA = 0), the interrupt is a transmit data request. If a receive interrupt occurs and the status indicates that there is no receive result (RxIRA = 0), the interrupt is a receive data request.

Reset Data Transfer Mode (CMD Code 57)

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	0	1	0	1	0	1	1	1
PAR:	0	1	1	1	1	1	1	1	1	0

If the Data Transfer Mode is reset, the 8273 data transfers are performed through the DMA requests without interrupting the CPU.

Set Operating Mode (CMD Code 91)

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	1	0	0	1	0	0	0	1
PAR:	0	1	0	0						

1 = FLAG STREAM MODE
1 = PREFRAME SYNC MODE
1 = BUFFERED MODE
1 = EARLY INTERRUPT MODE
1 = EOP INTERRUPT MODE
1 = HDLC MODE

Reset Operating Mode (CMD Code 51)

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	0	1	0	1	0	0	0	1
PAR:	0	1	1	1						

Any mode switches set in CMD code 91 can be reset using this command by placing zeros in the appropriate positions.

(D5) HDLC Mode

In HDLC mode, a bit sequence of seven ones (01111111) is interpreted as an abort character. Otherwise, eight ones (011111111) signal an abort.

(D4) EOP Interrupt Mode

In EOP interrupt mode, an interrupt is generated whenever an EOP character (01111111) is detected by an active receiver. This mode is useful for the implementation of an SDLC loop controller in detecting the end of a message stream after a loop poll.

(D3) Transmitter Early Interrupt Mode (Tx)

The early interrupt mode is specified to indicate when the 8273 should generate an end of frame interrupt. When set, an early interrupt is generated when the last data character has been passed to the 8273. If the user software responds with another transmit command before the final flag is sent, the final flag interrupt will not be generated and a new frame will immediately begin when the current frame is complete. This permits frames to be separated by a single flag. If no additional Tx commands are provided, a final interrupt will follow.

If this bit is zero, the interrupt will be generated only after the final flag has been transmitted.

(D2) Buffered Mode

If the buffered mode bit is set to a one, the first two bytes (normally the address (A) and control (C) fields) of a frame are buffered by the 8273. If this bit is a zero the address and control fields are passed to and from memory.

(D1) Preframe Sync Mode

If this bit is set to a one the 8273 will transmit two characters before the first flag of a frame.
To guarantee sixteen line transitions, the 8273 sends two bytes of data $(00)_H$ if NRZI is set or data $(55)_H$ if NRZI is not set.

(D0) Flag Stream Mode

If this bit is set to a one, the following table outlines the operation of the transmitter.

TRANSMITTER STATE	ACTION
Idle	Send Flags immediately.
Transmit or Transmit-Transparent Active	Send Flags after the transmission complete
Loop Transmit Active	Ignore command.
1 Bit Delay Active	Ignore command.

If this bit is reset to zero the following table outlines the operation of the transmitter.

TRANSMITTER STATE	ACTION
IDLE	Send Idles on next character boundary.
Transmit or Transmit-Transparent Active	Send Idles after the transmission is complete.
Loop Transmit Active	Ignore command.
1 Bit Delay Active	Ignore command.

Set Serial I/O Mode (CMD Code A0)

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	1	0	1	0	0	0	0	0
PAR:	0	1	0	0	0	0	0			

1 = NRZ1 MODE
1 = TxC → RxC
1 = LOOP BACK TxD → RxD

Reset Serial I/O Mode (CMD Code 60)

This command allows bits set in CMD code A0 to be reset by placing zeros in the appropriate positions.

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	0	1	1	0	0	0	0	0
PAR:	0	1	1	1	1	1	1			

(D2) Loop Back

If this bit is set to a one, the transmit data is internally routed to the receive data circuitry.

(D1) TxC → RxC

If this bit is set to a one, the transmit clock is internally routed to the receive clock circuitry. It is normally used with the loop back bit (D2).

(D0) NRZI Mode

If this bit is set to a one, NRZI encoding and decoding of transmit and receive data is provided. If this bit is a zero, the transmit and receive data is treated as a normal positive logic bit stream.

NRZI encoding specifies that a zero causes a change in the polarity of the transmitted signal and a one causes no polarity change. NRZI is used in all asynchronous operations. Refer to IBM document GA27-3093 for details.

Reset Device Command

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
TMR:	1	0	0	0	0	0	0	0	0	1
TMR:	1	0	0	0	0	0	0	0	0	0

An 8273 reset command is executed by outputing a $(01)_H$ followed by $(00)_H$ to the test mode register (TMR). See 8273 AC timing characteristics for Reset pulse specifications.

The reset command emulates the action of the reset pin.

1. The modem control signals are forced high (inactive level).
2. The 8273 status register flags are cleared.
3. Any commands in progress are terminated immediately.
4. The 8273 enters an idle state until the next command is issued.
5. The Serial I/O and Operating Mode registers are set to zero and DMA data register transfer mode is selected.
6. The device assumes a non-loop SDLC terminal role.

Receive Commands

The 8273 supports three receive commands: General Receive, Selective Receive, and Selective Loop Receive.

General Receive (CMD Code C0)

General receive is a receive mode in which frames are received regardless of the contents of the address field.

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	1	1	0	0	0	0	0	0
PAR:	0	1	LEAST SIGNIFICANT BYTE OF THE RECEIVE BUFFER LENGTH (B0)							
PAR:	0	1	MOST SIGNIFICANT BYTE OF RECEIVE BUFFER LENGTH (B1)							

NOTES:

1. If buffered mode is specified, the R0, R1 receive frame length (result) is the number of data bytes received.
2. If non-buffered mode is specified, the R0, R1 receive frame length (result) is the number of data bytes received plus two (the count includes the address and control bytes).
3. The frame check sequence (FCS) is not transferred to memory.
4. Frames with less than 32 bits between flags are ignored (no interrupt generated) if the buffered mode is specified.
5. In the non-buffered mode an interrupt is generated when a less than 32 bit frame is received, since data transfer requests have occurred.
6. The 8273 receiver is always disabled when an Idle is received after a valid frame. The CPU module must issue a receive command to re-enable the receiver.
7. The intervening ABORT character between a final flag and an IDLE does not generate an interrupt.
8. If an ABORT Character is not preceded by a flag and is followed by an IDLE, an interrupt will be generated for the ABORT followed by an IDLE interrupt one character time later. The reception of an ABORT will disable the receiver.

Selective Receive (CMD Code C1)

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	1	1	0	0	0	0	0	1
PAR:	0	1	LEAST SIGNIFICANT BYTE OF THE RECEIVE BUFFER LENGTH (B0)							
PAR:	0	1	MOST SIGNIFICANT BYTE OF RECEIVE BUFFER LENGTH (B1)							
PAR:	0	1	RECEIVE FRAME ADDRESS MATCH FIELD ONE (A1)							
PAR:	0	1	RECEIVE FRAME ADDRESS MATCH FIELD TWO (A2)							

Selective receive is a receive mode in which frames are ignored unless the address field matches any one of two address fields given to the 8273 as parameters.

When selective receive is used in HDLC the 8273 looks at the first character, if extended, software must then decide if the message is for this unit.

Selective Loop Receive (CMD Code C2)

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	1	1	0	0	0	0	1	0
PAR:	0	0	LEAST SIGNIFICANT BYTE OF THE RECEIVE BUFFER LENGTH (B0)							
PAR:	0	1	MOST SIGNIFICANT BYTE OF RECEIVE BUFFER LENGTH (B1)							
PAR:	0	1	RECEIVE FRAME ADDRESS MATCH FIELD ONE (A1)							
PAR:	0	1	RECEIVE FRAME ADDRESS MATCH FIELD TWO (A2)							

Selective loop receive operates like selective receive except that the transmitter is placed in flag stream mode automatically after detecting an EOP (01111111) following a valid received frame. The one bit delay mode is also reset at the end of a selective loop receive.

Receive Disable (CMD Code C5)

Terminates an active receive command immediately.

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	1	1	0	0	0	1	0	1
PAR: NONE										

Transmit Commands

The 8273 supports three transmit commands: Transmit Frame, Loop Transmit, Transmit Transparent.

Transmit Frame (CMD Code C8)

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	1	1	0	0	1	0	0	0
PAR:	0	1	LEAST SIGNIFICANT BYTE OF FRAME LENGTH (L0)							
PAR:	0	1	MOST SIGNIFICANT BYTE OF FRAME LENGTH (L1)							
PAR:	0	1	ADDRESS FIELD OF TRANSMIT FRAME (A)							
PAR:	0	1	CONTROL FIELD OF TRANSMIT FRAME (C)							

Transmits one frame including: initial flag, frame check sequence, and the final flag.

If the buffered mode is specified, the L0, L1, frame length provided as a parameter is the length of the information field and the address and control fields must be input.

In unbuffered mode the frame length provided must be the length of the information field plus two and the address and control fields must be the first two bytes of data. Thus only the frame length bytes are required as parameters.

Loop Transmit (CMD Code CA)

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	1	1	0	0	1	0	1	0
PAR:	0	1	LEAST SIGNIFICANT BYTE OF FRAME LENGTH (L0)							
PAR:	0	1	MOST SIGNIFICANT BYTE OF FRAME LENGTH (L1)							
PAR:	0	1	ADDRESS FIELD OF TRANSMIT FRAME (A)							
PAR:	0	1	CONTROL FIELD OF TRANSMIT FRAME (C)							

Transmits one frame in the same manner as the transmit frame command except:

1. This command should be given only in one-bit delay mode.
2. If the flag stream mode is not active transmission will begin after a received EOP has been converted to a flag.
3. If the flag stream mode is active transmission will begin at the next flag boundary for buffered mode or at the third flag boundary for non-buffered mode.
4. At the end of a loop transmit the one-bit delay mode is entered and the flag stream mode is reset.

Transmit Transparent (CMD Coded C9)

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	1	1	0	0	1	0	0	1
PAR:	0	1	LEAST SIGNIFICANT BYTE OF FRAME LENGTH (L0)							
PAR:	0	1	MOST SIGNIFICANT BYTE OF FRAME LENGTH (L1)							

The 8273 will transmit a block of raw data without protocol, i.e., no zero bit insertion, flags, or frame check sequences.

Abort Transmit Commands

An abort command is supported for each type of transmit command. The abort commands are ignored if a transmit command is not in progress.

Abort Transmit Frame (CMD Code CC)

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	1	1	0	0	1	1	0	0

PAR: NONE

After an abort character (eight contiguous ones) is transmitted, the transmitter reverts to sending flags or idles as a function of the flag stream mode specified.

Abort Loop Transmit (CMD Code CE)

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	1	1	0	0	1	1	1	0

PAR: NONE

After a flag is transmitted the transmitter reverts to one bit delay mode.

Abort Transmit Transparent (CMD Code CD)

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	1	1	0	0	1	1	0	1

PAR: NONE

The transmitter reverts to sending flags or idles as a function of the flag stream mode specified.

Modem Control Commands

The modem control commands are used to manipulate the modem control ports.

When read Port A or Port B commands are executed the result of the command is returned in the result register. The Bit Set Port B command requires a parameter that is a mask that corresponds to the bits to be set. The Bit Reset Port B command requires a mask that has a zero in the bit positions that are to be reset.

Read Port A (CMD Code 22)

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	0	0	1	0	0	0	1	0

PAR: NONE

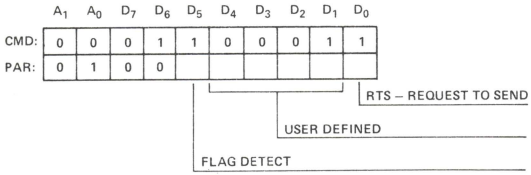
Read Port B (CMD Code 23)

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	0	0	1	0	0	0	1	1

PAR: NONE

Set Port B Bits (CMD Code A3)

This command allows user defined Port B pins to be set.



(D_5) Flag Detect

This bit can be used to set the flag detect pin. However, it will be reset when the next flag is detected.

(D_4-D_1) User Defined Outputs

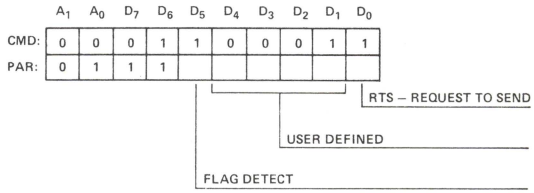
These bits correspond to the state of the PB_4-PB_1 output pins.

(D_0) Request to Send

This is a dedicated 8273 modem control signal, and reflects the same logical state of RTS pin.

Reset Port B Bits (CMD Code 63)

This command allows Port B user defined bits to be reset.



This command allows Port B (D_4-D_1) user defined bits to be reset. These bits correspond to Output Port pins (PB_4-PB_1).

8273 Command Summary

Command Description	Command (HEX)	Parameter	Results	Result Port	Completion Interrupt
Set One Bit Delay	A4	Set Mask	None	—	No
Reset One Bit Delay	64	Reset Mask	None	—	No
Set Data Transfer Mode	97	Set Mask	None	—	No
Reset Data Transfer Mode	57	Reset Mask	None	—	No
Set Operating Mode	91	Set Mask	None	—	No
Reset Operating Mode	51	Reset Mask	None	—	No
Set Serial I/O Mode	A0	Set Mask	None	—	No
Reset Serial I/O Mode	60	Reset Mask	None	—	No
General Receive	C0	B0,B1	IC,R0,R1,A,C	RXI/R	Yes
Selective Receive	C1	B0,B1,A1,A2	IC,R0,R1,A,C	RXI/R	Yes
Selective Loop Receive	C2	B0,B1,A1,A2	IC,R0,R1,A,C	RXI/R	Yes
Receive Disable	C5	None	None	—	No
Transmit Frame	C8	L0,L1,A,C	IC	TXI/R	Yes
Loop Transmit	CA	L0,L1,A,C	IC	TXI/R	Yes
Transmit Transparent	C9	L0,L1	IC	TXI/R	Yes
Abort Transmit Frame	CC	None	IC	TXI/R	Yes
Abort Loop Transmit	CE	None	IC	TXI/R	Yes
Abort Transmit Transparent	CD	None	IC	TXI/R	Yes
Read Port A	22	None	Port Value	Result	No
Read Port B	23	None	Port Value	Result	No
Set Port B Bit	A3	Set Mask	None	—	No
Reset Port B Bit	63	Reset Mask	None	—	No

8273 Command Summary Key

B0 — Least significant byte of the receive buffer length.
B1 — Most significant byte of the receive buffer length.
L0 — Least significant byte of the Tx frame length.
L1 — Most significant byte of the Tx frame length.
A1 — Receive frame address match field one.
A2 — Receive frame address match field two.
A — Address field of received frame. If non-buffered mode is specified, this result is not provided.
C — Control field of received frame. If non-buffered mode is specified this result is not provided.
RXI/R — Receive interrupt result register.
TXI/R — Transmit interrupt result register.
R0 — Least significant byte of the length of the frame received.
R1 — Most significant byte of the length of the frame received.
IC — Interrupt result code (see table).

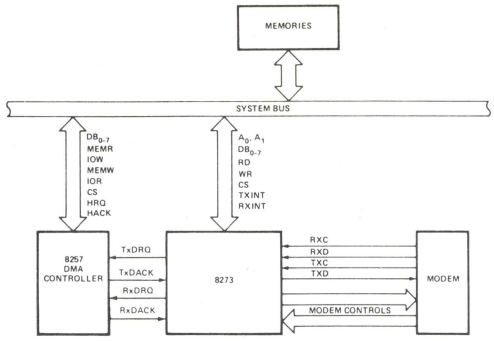


Figure 14. 8273 System Diagram

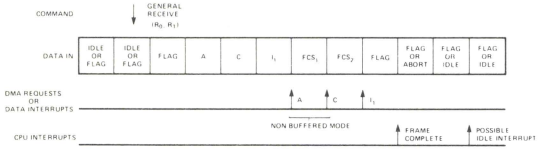


Figure 12. Typical Frame Reception

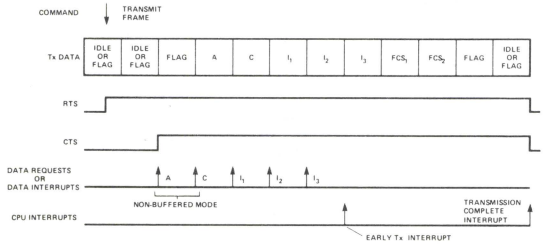


Figure 13. Typical Frame Transmission

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin With Respect to Ground ..... -0.5V to +7V
Power Dissipation ..... 1 Watt

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5.0V ±5%

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	Volts	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	Volts	
V_{OL}	Output Low Voltage		0.45	Volts	I_{OL} = 2.0mA
V_{OH}	Output High Voltage	2.4		Volts	I_{OH} = -200μA
I_{IL}	Input Load Current		±10	μA	V_{IN} = V_{CC} to 0V
I_{OZ}	Off-State Output Current		±10	μA	V_{OUT} = V_{CC} to 0V
I_{CC}	V_{CC} Supply Current		160	mA	

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	t_c = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured Pins Returned to GND

A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5.0V ±5%

Read Cycle

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{AC}	Select Setup to $\overline{RQ}$	0		ns	
t_{CA}	Select Hold from $\overline{RD}$	0		ns	
t_{RR}	$\overline{RD}$ Pulse Width	250		ns	
t_{AD}	Data Delay from Address		200	ns	
t_{RD}	Data Delay from $\overline{RD}$		150	ns	C_L = 150pF
t_{DF}	Output Float Delay	20	100	ns	C_L = 20pF for Minimum; 150pF for Maximum

Write Cycle

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{AC}	Select Setup to $\overline{WR}$	0		ns	
t_{CA}	Select Hold from $\overline{WR}$	0		ns	
t_{WW}	$\overline{WR}$ Pulse Width	250		ns	
t_{DW}	Data Setup to $\overline{WR}$	150		ns	
t_{WD}	Data Hold from $\overline{WR}$	-20		ns	

DMA

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{CQ}	Request Hold from $\overline{WR}$ or $\overline{RD}$ (for Non-Burst Mode)		150	ns	

Other Timing

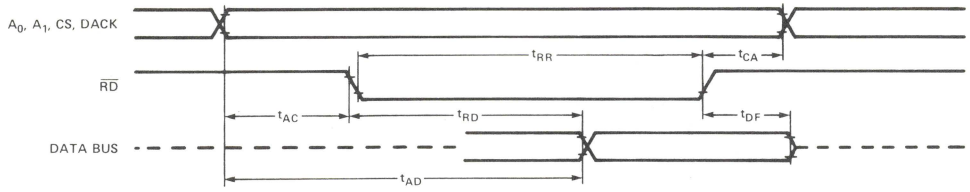
Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{RSTW}	Reset Pulse Width	10		t_{CY}	
t_r	Input Signal Rise Time		20	ns	
t_f	Input Signal Fall Time		20	ns	
t_{RSTS}	Reset to First $\overline{IOWR}$	2		t_{CY}	
t_{CY}	Clock	250			Note 3
t_{CL}	Clock Low	T_{BS}			Note 2
t_{CH}	Clock High	T_{BS}			Note 2
t_{DCL}	Data Clock Low				
t_{DCH}	Data Clock High	200		ns	
t_{DCY}	Data Clock	15625		ns	Note 3
t_{TD}	Transmit Data Delay		100	ns	
t_{DS}	Data Setup Time	100		ns	
t_{DH}	Data Hold Time	0		ns	
t_{DPLL}	$\overline{DPLL}$ Output Low	200		ns	
t_{FLD}	$\overline{FLAG\ DET}$ Output Low	$8 \cdot t_{CY} \pm 50$		ns	

NOTES:

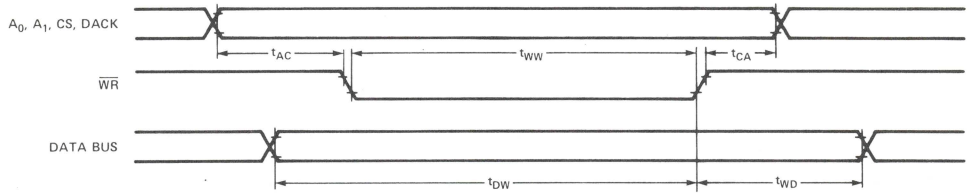
1. All timing measurements are made at the reference voltages unless otherwise specified:
   Input "1" at 2.0V, "0" at 0.8V
   Output "1" at 2.0V, "0" at 0.8V
2. To be specified.
3. 64K baud maximum operating rate.

WAVEFORMS

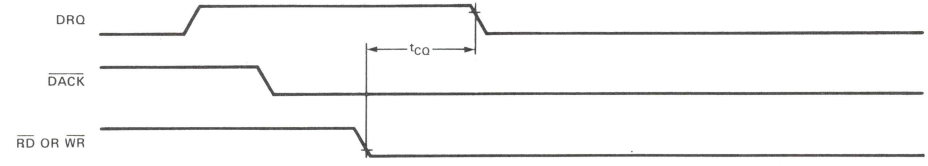
Read Waveforms

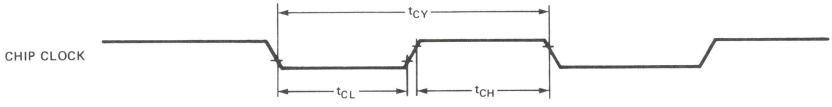


Write Waveforms

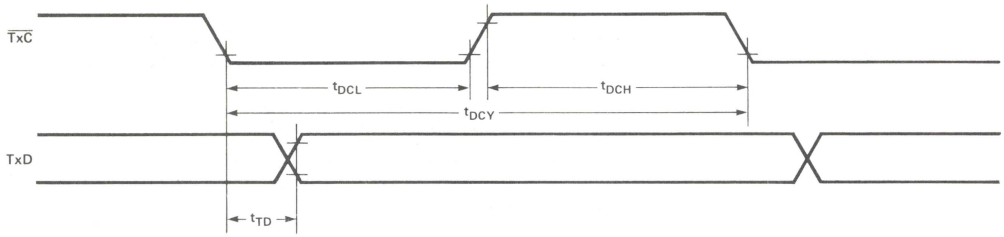


DMA Waveforms

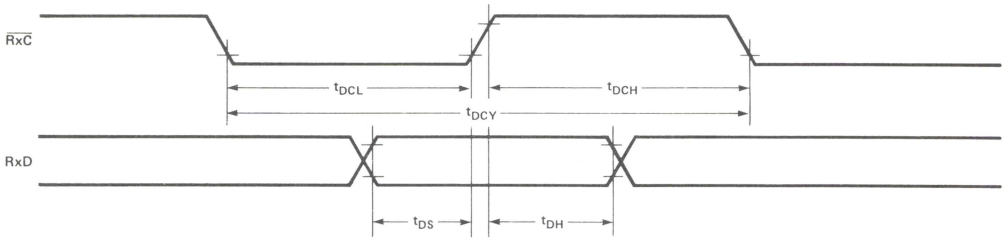




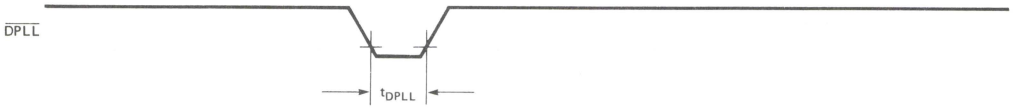
Transmit Data Waveforms



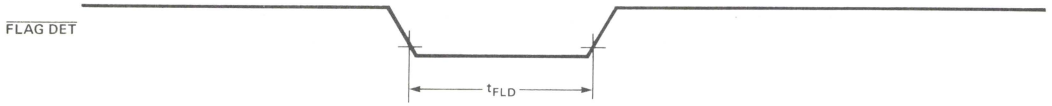
Receive Data Waveforms



DPLL Output Waveform



Flag Detect Output Waveform



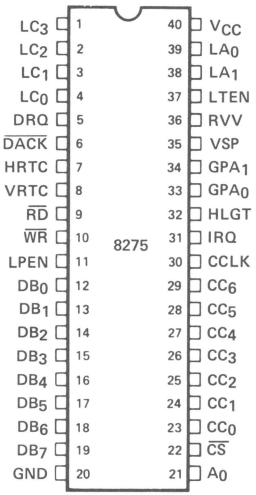
PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

8275
PROGRAMMABLE CRT CONTROLLER

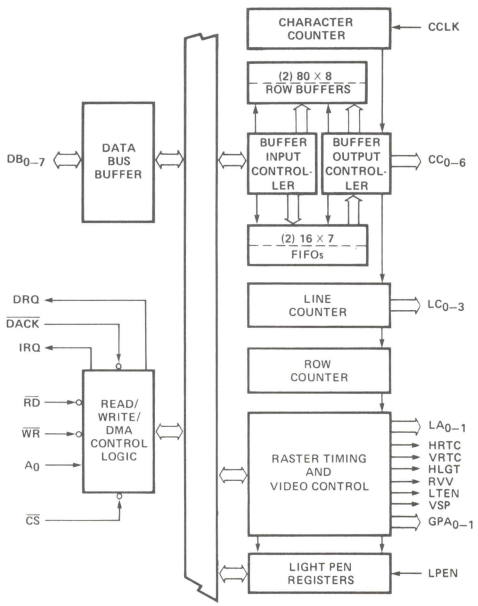
- Programmable Screen and Character Format
- 6 Independent Visual Field Attributes
- 11 Visual Character Attributes (Graphic Capability)
- Cursor Control (4 Types)
- Light Pen Detection and Registers
- Fully MCS-80™ and MCS-85™ Compatible
- Dual Row Buffers
- Programmable DMA Burst Mode
- Single +5V Supply
- 40-Pin Package

The Intel® 8275 Programmable CRT Controller is a single chip device to interface CRT raster scan displays with Intel® microcomputer systems. Its primary function is to refresh the display by buffering the information from main memory and keeping track of the display position of the screen. The flexibility designed into the 8275 will allow simple interface to almost any raster scan CRT display with a minimum of external hardware and software overhead.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

DB_{0-1}	B1–DIRECTIONAL DATA BUS	LC_{0-3}	LINE COUNTER OUTPUTS
DRQ	DMA REQUEST OUTPUT	LA_{0-1}	LINE ATTRIBUTE OUTPUTS
$\overline{DACK}$	DMA ACKNOWLEDGE INPUT	HRTC	HORIZONTAL RETRACE OUTPUT
IRQ	INTERRUPT REQUEST OUTPUT	VRTC	VERTICAL RETRACE OUTPUT
$\overline{RD}$	READ STROBE INPUT	HLGT	HIGHLIGHT OUTPUT
$\overline{WR}$	WRITE STROBE INPUT	RVV	REVERSE VIDEO OUTPUT
A_0	REGISTER ADDRESS INPUT	LTEN	LIGHT ENABLE OUTPUT
$\overline{CS}$	CHIP SELECT INPUT	VSP	VIDEO SUPPRESS OUTPUT
CCLK	CHARACTER CLOCK INPUT	GPA_{0-1}	GENERAL PURPOSE ATTRIBUTE OUTPUTS
CC_{0-6}	CHARACTER CODE OUTPUTS	LPEN	LIGHT PEN INPUT

MPU PERIPHERALS

PIN DESCRIPTIONS

Pin #	Pin Name	I/O	Pin Description
1	LC_3	O	Line count. Output from the line counter which is used to address the character generator for the line positions on the screen.
2	LC_2		
3	LC_1		
4	LC_0		
5	DRQ	O	DMA request. Output signal to the 8257 DMA controller requesting a DMA cycle.
6	$\overline{DACK}$	I	DMA acknowledge. Input signal from the 8257 DMA controller acknowledging that the requested DMA cycle has been granted.
7	HRTC	O	Horizontal retrace. Output signal which is active during the programmed horizontal retrace interval. During this period the VSP output is high and the LTEN output is low.
8	VRTC	O	Vertical retrace. Output signal which is active during the programmed vertical retrace interval. During this period the VSP output is high and the LTEN output is low.
9	$\overline{RD}$	I	Read input. A control signal to read registers.
10	$\overline{WR}$	I	Write input. A control signal to write commands into the control registers or write data into the row buffers during a DMA cycle.
11	LPEN	I	Light pen. Input signal from the CRT system signifying that a light pen signal has been detected.
12	DB_0	I/O	Bi-directional three-state data bus lines. The outputs are enabled during a read of the C or P ports.
13	DB_1		
14	DB_2		
15	DB_3		
16	DB_4		
17	DB_5		
18	DB_6		
19	DB_7		
20	Ground		Ground
40	V_{CC}		+5V power supply
39	LA_0	O	Line attribute codes. These attribute codes have to be decoded externally by the dot/timing logic to generate the horizontal and vertical line combinations for the graphic displays specified by the character attribute codes.
38	LA_1		
37	LTEN	O	Light enable. Output signal used to enable the video signal to the CRT. This output is active at the programmed underline cursor position, and at positions specified by attribute codes.
36	RVV	O	Reverse video. Output signal used to indicate the CRT circuitry to reverse the video signal. This output is active at the cursor position if a reverse video block cursor is programmed or at the positions specified by the field attribute codes.
35	VSP	O	Video suppression. Output signal used to blank the video signal to the CRT. This output is active: — during the horizontal and vertical retrace intervals. — at the top and bottom lines of rows if underline is programmed to be number 8 or greater. — when an end of row or end of screen code is detected. — When a DMA underrun occurs. — at regular intervals (1/16 frame frequency for cursor, 1/32 frame frequency for character and field attributes) — to create blinking displays as specified by cursor, character attribute, or field attribute programming.
34	GPA_1	O	General purpose attribute codes. Outputs which are enabled by the general purpose field attribute codes.
33	GPA_0		
32	HLGT	O	Highlight. Output signal used to intensify the display at particular positions on the screen as specified by the character attribute codes or field attribute codes.
31	IRQ	O	Interrupt request.
30	CCLK	I	Character clock (from dot/timing logic).
29	CC_6	O	Character codes. Output from the row buffers used for character selection in the character generator.
28	CC_5		
27	CC_4		
26	CC_3		
25	CC_2		
24	CC_1		
23	CC_0		
22	$\overline{CS}$	I	Chip select. The read and write are enabled by $\overline{CS}$.
21	A_0	I	Port address. A high input on A_0 selects the "C" port or command registers and a low input selects the "P" port or parameter registers.

PRELIMINARY

FUNCTIONAL DESCRIPTION

Data Bus Buffer

This 3-state, bidirectional, 8-bit buffer is used to interface the 8275 to the system Data Bus.

This functional block accepts inputs from the System Control Bus and generates control signals for overall device operation. It contains the Command, Parameter, and Status Registers that store the various control formats for the device functional definition.

A_0	OPERATION	REGISTER
0	Read	PREG
0	Write	PREG
1	Read	SREG
1	Write	CREG

$\overline{RD}$ (Read)

A "low" on this input informs the 8275 that the CPU is reading data or status information from the 8275.

$\overline{WR}$ (Write)

A "low" on this input informs the 8275 that the CPU is writing data or control words to the 8275.

$\overline{CS}$ (Chip Select)

A "low" on this input selects the 8275. No reading or writing will occur unless the device is selected. When $\overline{CS}$ is high, the Data Bus in the float state and $\overline{RD}$ and $\overline{WR}$ will have no effect on the chip.

DRQ (DMA Request)

A "high" on this output informs the DMA Controller that the 8275 desires a DMA transfer.

$\overline{DACK}$ (DMA Acknowledge)

A "low" on this input informs the 8275 that a DMA cycle is in progress.

IRQ (Interrupt Request)

A "high" on this output informs the CPU that the 8275 desires interrupt service.

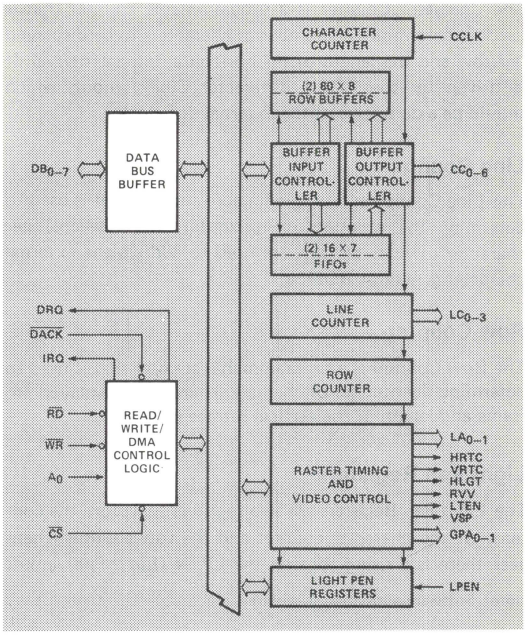


Figure 1. 8275 Block Diagram Showing Data Bus Buffer and Read/Write Functions

A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	Write 8275 Parameter
0	1	0	0	Read 8275 Parameter
1	0	1	0	Write 8275 Command
1	1	0	0	Read 8275 Status
X	1	1	0	Three-State
X	X	X	1	Three-state

PRELIMINARY
Notice: This is not a final specification
Intel Corporation reserves the right to change this

Character Counter

The Character Counter is a programmable counter that is used to determine the number of characters to be displayed per row and the length of the horizontal retrace interval. It is driven by the CCLK (Character Clock) input, which should be a derivative of the external dot clock.

Line Counter

The Line Counter is a programmable counter that is used to determine the number of horizontal lines (Sweeps) per character row. Its outputs are used to address the external character generator ROM.

Row Counter

The Row Counter is a programmable counter that is used to determine the number of character rows to be displayed per frame and length of the vertical retrace interval.

Light Pen Registers

The Light Pen Registers are two registers that store the contents of the character counter and the row counter whenever there is a rising edge on the LPEN (Light Pen) input.

Note: Software correction is required.

Raster Timing and Video Controls

The Raster Timing circuitry controls the timing of the HRTC (Horizontal Retrace) and VRTC (Vertical Retrace) outputs. The Video Control circuitry controls the generation of LA_{0-1} (Line Attribute), HGLT (Highlight), RVV (Reverse Video), LTEN (Light Enable), VSP (Video Suppress), and GPA_{0-1} (General Purpose Attribute) outputs.

Row Buffers

The Row Buffers are two 80 character buffers. They are filled from the microcomputer system memory with the character codes to be displayed. While one row buffer is displaying a row of characters, the other is being filled with the next row of characters.

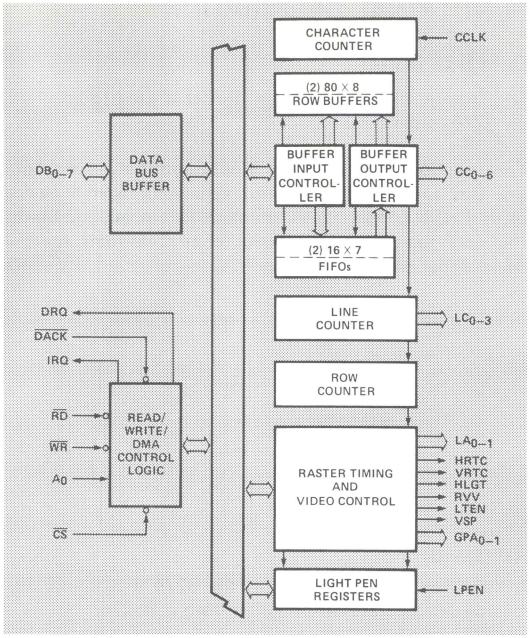


Figure 2. 8275 Block Diagram Showing Counter and Register Functions

FIFOs

There are two 16 character FIFOs in the 8275. They are used to provide extra row buffer length in the Transparent Attribute Mode (see Detailed Operation section).

Buffer Input/Output Controllers

The Buffer Input/Output Controllers decode the characters being placed in the row buffers. If the character is a character attribute, field attribute or special code, these controllers control the appropriate action. (Examples: An "End of Screen–Stop DMA" special code will cause the Buffer Input Controller to stop further DMA requests. A "Highlight" field attribute will cause the Buffer Output Controller to activate the HGLT output.)

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

SYSTEM OPERATION

The 8275 is programmable to a large number of different display formats. It provides raster timing, display row buffering, visual attribute decoding, cursor timing, and light pen detection.

It is designed to interface with the 8257 DMA Controller and standard character generator ROMs for dot matrix decoding. Dot level timing must be provided by external circuitry.

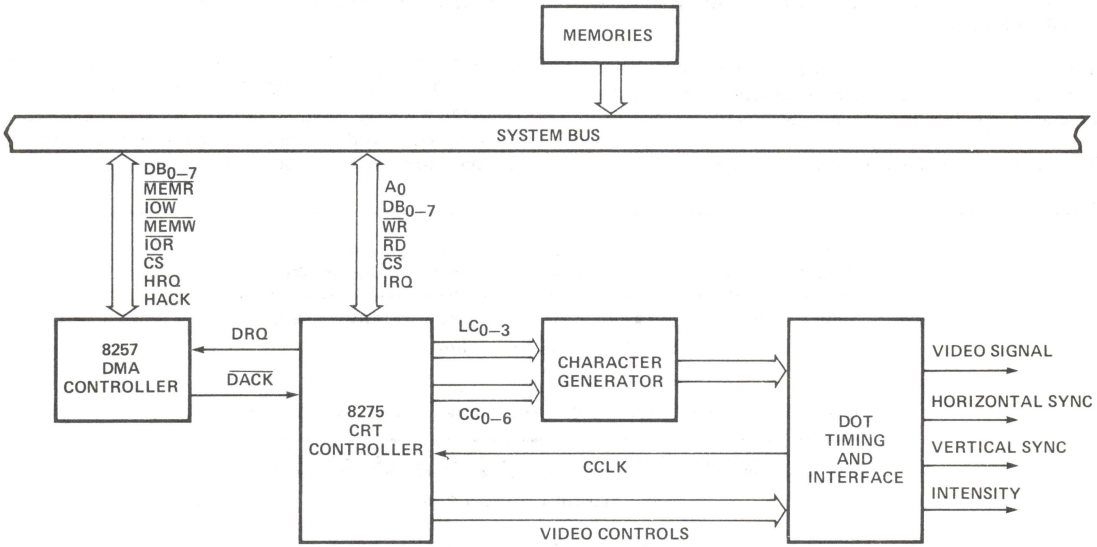


Figure 3. 8275 Systems Block Diagram Showing Systems Operation

PRELIMINARY

General Systems Operational Description

The 8275 provides a "window" into the microcomputer system memory.

Display characters are retrieved from memory and displayed on a row by row basis. The 8275 has two row buffers. While one row buffer is being used for display, the other is being filled with the next row of characters to be displayed. The number of display characters per row and the number of character rows per frame are software programmable, providing easy interface to most CRT displays. (See Programming Section.)

The 8275 requests DMA to fill the row buffer that is not being used for display. DMA burst length and spacing is programmable. (See Programming Section.)

The 8275 displays character rows one line at a time.

The number of lines per character row, the underline position, and blanking of top and bottom lines are programmable. (See Programming Section.)

The 8275 provides special Control Codes which can be used to minimize DMA or software overhead. It also provides Visual Attribute Codes to cause special action or symbols on the screen without the use of the character generator (see Visual Attributes Section).

The 8275 also controls raster timing. This is done by generating Horizontal Retrace (HRTC) and Vertical Retrace (VRTC) signals. The timing of these signals is programmable.

The 8275 can generate a cursor. Cursor location and format are programmable. (See Programming Section.)

The 8275 has a light pen input and registers. The light pen input is used to load the registers. Light pen registers can be read on command. (See Programming Section.)

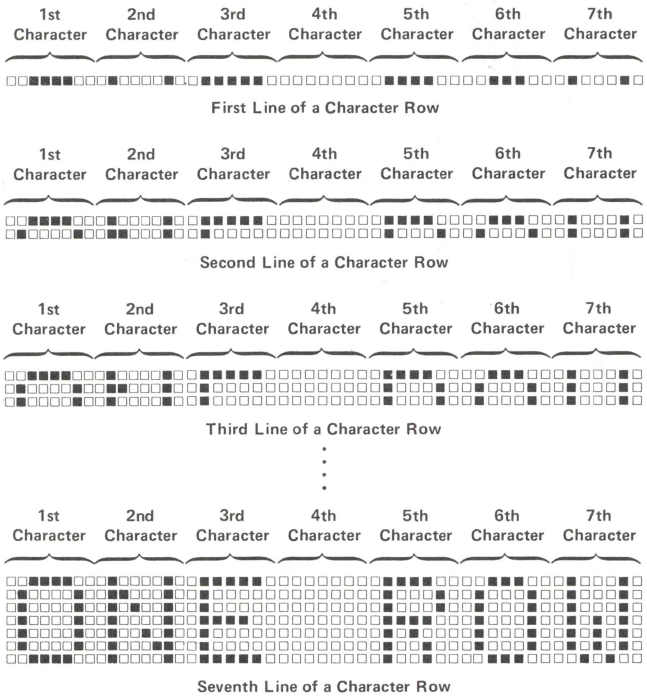


Figure 4. Display of a Character Row

PRELIMINARY
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This is not a final specification. Some parametric limits are subject to change.

Display Row Buffering

Before the start of a frame, the 8275 requests DMA and one row buffer is filled with characters.

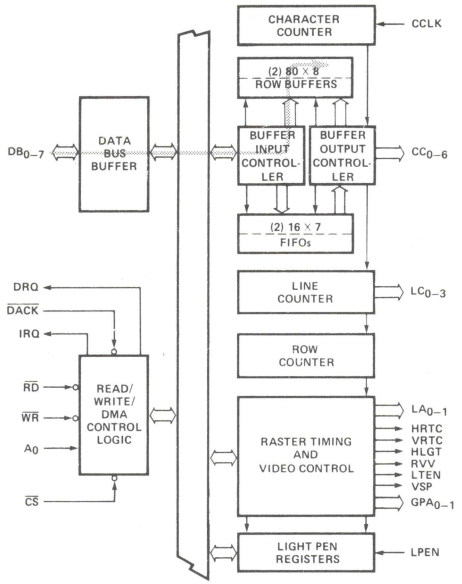


Figure 5. First Row Buffer Filled

When the first horizontal sweep is started, character codes are output to the character generator from the row buffer just filled. Simultaneously, DMA begins filling the other row buffer with the next row of characters.

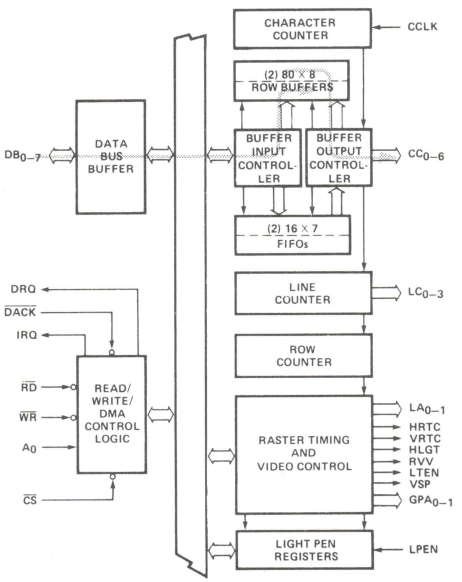


Figure 6. Second Buffer Filled, First Row Displayed

After all the lines of the character row are scanned, the roles of the two row buffers are reversed and the same procedure is followed for the next row.

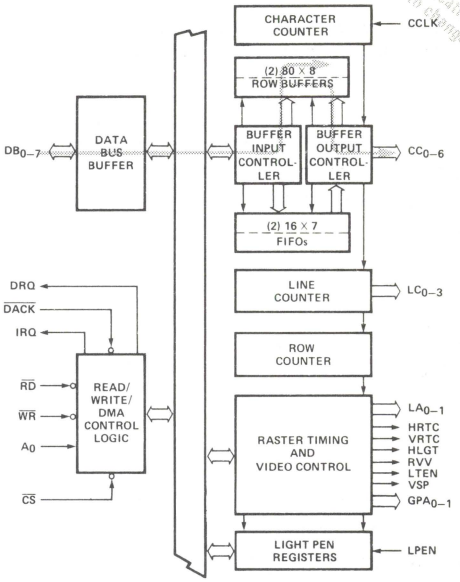


Figure 7. First Buffer Filled with Third Row, Second Row Displayed

This is repeated until all of the character rows are displayed.

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

Display Format

Screen Format

The 8275 can be programmed to generate from 1 to 80 characters per row, and from 1 to 64 rows per frame.

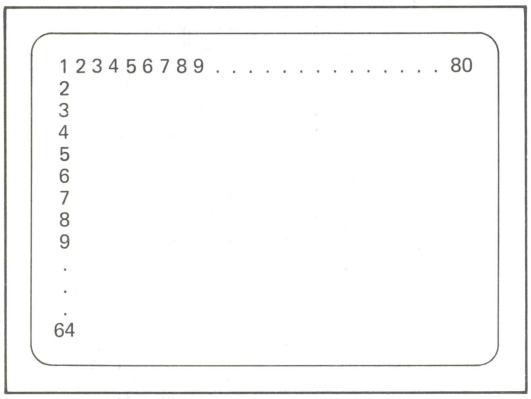


Figure 8. Screen Format

The 8275 can also be programmed to blank alternate rows. In this mode, the first row is displayed, the second blanked, the third displayed, etc. DMA is not requested for the blanked rows.

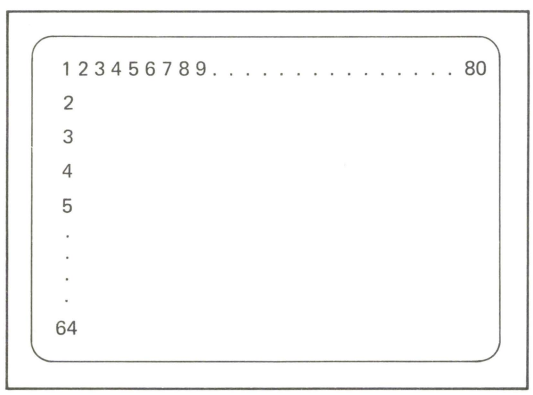


Figure 9. Blank Alternate Rows Mode

Row Format

The 8275 is designed to hold the line count stable while outputting the appropriate character codes during each horizontal sweep. The line count is incremented during horizontal retrace and the whole row of character codes are output again during the next sweep. This is continued until the whole character row is displayed.

The number of lines (horizontal sweeps) per character row is programmable from 1 to 16.

The output of the line counter can be programmed to be in one of two modes.

In mode 0, the output of the line *counter* is the same as the line *number*.

In mode 1, the line *counter* is offset by one from the line *number*.

Note: In mode 1, while the *first* line (line number 0) is being displayed, the *last* count is output by the line counter (see examples).

Line Number		Line Counter Mode 0	Line Counter Mode 1
0	□ □ □ □ □ □ □ □	0000	1111
1	□ □ □ □ ■ □ □ □	0001	0000
2	□ □ □ ■ □ ■ □ □	0010	0001
3	□ □ ■ □ □ □ ■ □	0011	0010
4	□ ■ □ □ □ □ ■ □	0100	0011
5	□ ■ □ □ □ □ ■ □	0101	0100
6	□ ■ ■ ■ ■ ■ ■ □	0110	0101
7	□ ■ □ □ □ □ ■ □	0111	0110
8	□ ■ □ □ □ □ ■ □	1000	0111
9	□ ■ □ □ □ □ ■ □	1001	1000
10	□ □ □ □ □ □ □ □	1010	1001
11	□ □ □ □ □ □ □ □	1011	1010
12	□ □ □ □ □ □ □ □	1100	1011
13	□ □ □ □ □ □ □ □	1101	1100
14	□ □ □ □ □ □ □ □	1110	1101
15	□ □ □ □ □ □ □ □	1111	1110

Figure 10. Example of a 16-Line Format

Line Number		Line Counter Mode 0	Line Counter Mode 1
0	□ □ □ □ □ □ □	0000	1001
1	□ □ □ ■ □ □ □	0001	0000
2	□ □ ■ □ ■ □ □	0010	0001
3	□ ■ □ □ □ ■ □	0011	0010
4	□ ■ □ □ □ ■ □	0100	0011
5	□ ■ ■ ■ ■ ■ □	0101	0100
6	□ ■ □ □ □ ■ □	0110	0101
7	□ ■ □ □ □ ■ □	0111	0110
8	□ □ □ □ □ □ □	1000	0111
9	□ □ □ □ □ □ □	1001	1000

Figure 11. Example of a 10-Line Format

Mode 0 is useful for character generators that leave address zero blank and start at address 1. Mode 1 is useful for character generators which start at address zero.

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

Underline placement is also programmable (from line *number* 0 to 15). This is independent of the line *counter* mode.

If the line *number* of the underline is greater than 7 (line *number* MSB = 1), then the top and bottom lines will be blanked.

Line Number		Line Counter Mode 0	Line Counter Mode 1
0	□ □ □ □ □ □ □ □ □	0000	1011
1	□ □ □ □ ■ □ □ □ □	0001	0000
2	□ □ □ ■ □ ■ □ □ □	0010	0001
3	□ □ ■ □ □ □ ■ □ □	0011	0010
4	□ ■ □ □ □ □ □ ■ □	0100	0011
5	□ ■ □ □ □ □ □ ■ □	0101	0100
6	□ ■ ■ ■ ■ ■ ■ ■ □	0110	0101
7	□ ■ □ □ □ □ □ ■ □	0111	0110
8	□ ■ □ □ □ □ □ ■ □	1000	0111
9	□ ■ □ □ □ □ □ ■ □	1001	1000
10	■ ■ ■ ■ ■ ■ ■ ■ ■	1010	1001
11	□ □ □ □ □ □ □ □ □	1011	1010

Top and Bottom Lines are Blanked

Figure 12. Underline in Line Number 10

If the line *number* of the underline is less than or equal to 7 (line *number* MSB = 0), then the top and bottom lines will *not* be blanked.

Line Number		Line Counter Mode 0	Line Counter Mode 1
0	□ □ □ ■ □ □ □	0000	0111
1	□ □ ■ □ ■ □ □	0001	0000
2	□ ■ □ □ □ ■ □	0010	0001
3	□ ■ □ □ □ ■ □	0011	0010
4	□ ■ ■ ■ ■ ■ □	0100	0011
5	□ ■ □ □ □ ■ □	0101	0100
6	□ ■ □ □ □ ■ □	0110	0101
7	■ ■ ■ ■ ■ ■ ■	0111	0110

Top and Bottom Lines are not Blanked

Figure 13. Underline in Line Number 7

If the line *number* of the underline is greater than the maximum number of lines, the underline will not appear.

Blanking is accomplished by the VSP (Video Suppression) signal. Underline is accomplished by the LTEN (Light Enable) signal.

Dot Format

Dot width and character width are dependent upon the external timing and control circuitry.

Dot level timing circuitry should be designed to accept the parallel output of the character generator and shift it out serially at the rate required by the CRT display.

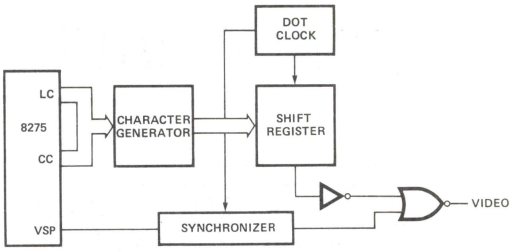


Figure 14. Typical Dot Level Block Diagram

Dot width is a function of dot clock frequency.

Character width is a function of the character generator width.

Horizontal character spacing is a function of the shift register length.

Note: Video control and timing signals must be synchronized with the video signal due to the character generator access delay.

PRELIMINARY
Notice: This is a product specification. Some parameters may be subject to change.

Raster Timing

The character counter is driven by the character clock input (CCLK). It counts out the characters being displayed (programmable from 1 to 80). It then causes the line counter to increment, and it starts counting out the horizontal retrace interval (programmable from 2 to 32). This is constantly repeated.

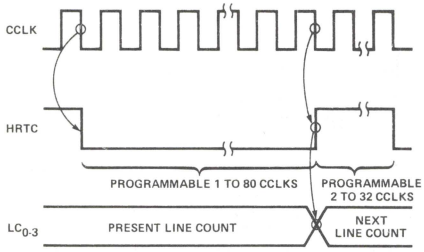


Figure 15. Line Timing

The line counter is driven by the character counter. It is used to generate the line address outputs (LC_{0-3}) for the character generator. After it counts all of the lines in a character row (programmable from 1 to 16), it increments the row counter, and starts over again. (See Character Format Section for detailed description of Line Counter functions.)

The row counter is an internal counter driven by the line counter. It controls the functions of the row buffers and counts the number of character rows displayed.

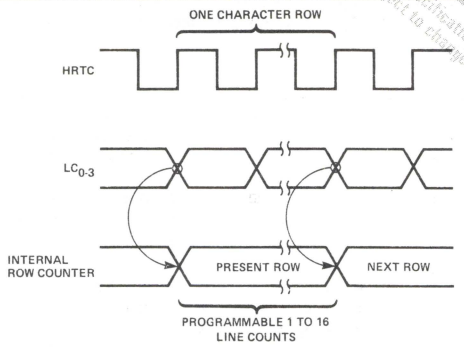


Figure 16. Row Timing

After the row counter counts all of the rows in a frame (programmable from 1 to 64), it starts counting out the vertical retrace interval (programmable from 1 to 4).

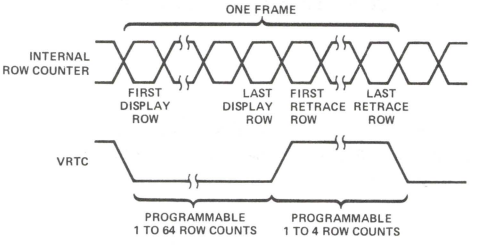


Figure 17. Frame Timing

The Video Suppression Output (VSP) is active during horizontal and vertical retrace intervals.

Dot level timing circuitry must synchronize these outputs with the video signal to the CRT Display.

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

DMA Timing

The 8275 can be programmed to request burst DMA transfers of 1 to 8 characters. The interval between bursts is also programmable (from 0 to 55 character clock periods ±1). This allows the user to tailor his DMA overhead to fit his system needs.

The first DMA request of the frame occurs one *row time* before the end of vertical retrace. DMA requests continue as programmed, until the row buffer is filled. If the row buffer is filled in the middle of a burst, the 8275 terminates the burst and resets the burst counter. No more DMA requests will occur until the *beginning* of the *next* row. At that time, DMA requests are activated as programmed until the other buffer is filled.

If, for any reason, there is a DMA underrun, a flag in the status word will be set.

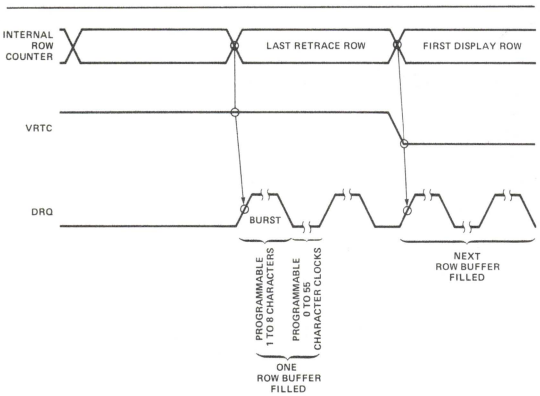


Figure 18. DMA Timing

The DMA controller is typically initialized for the next frame at the end of the current frame.

Interrupt Timing

The 8275 can be programmed to generate an interrupt request at the end of each frame. This can be used to reinitialize the DMA controller. If the 8275 interrupt enable flag is set, an interrupt request will occur at the *beginning* of the *last display row*.

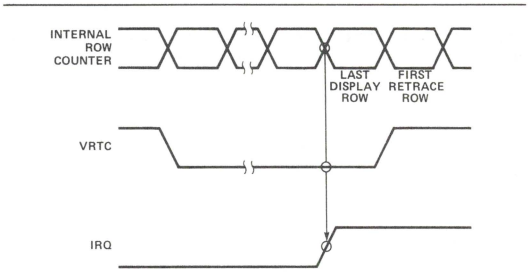


Figure 19. Beginning of Interrupt Request

IRQ will go inactive after the status register is read.

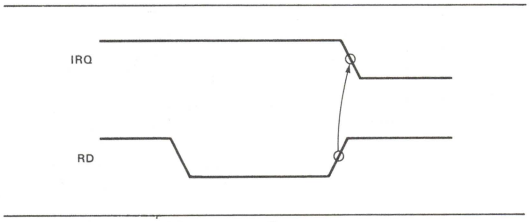


Figure 20. End of Interrupt Request

A reset command will also cause IRQ to go inactive, but this is not recommended during normal service.

Another method of reinitializing the DMA controller is to have the DMA controller itself interrupt on terminal count. With this method, the 8275 interrupt enable flag should not be set.

Note: Upon power-up, the 8275 Interrupt Enable Flag may be set. As a result, the user's cold start routine should write a reset command to the 8275 before system interrupts are enabled.

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

VISUAL ATTRIBUTES AND SPECIAL CODES

The characters processed by the 8275 are 8-bit quantities. The character code outputs provide the character generator with 7 bits of address. The Most Significant Bit is the extra bit and it is used to determine if it is a normal display character (MSB = 0), or if it is a Visual Attribute or Special Code (MSB = 1).

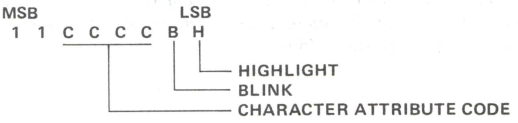
There are two types of Visual Attribute Codes. They are Character Attributes and Field Attributes.

Character Attribute Codes

Character attribute codes are codes that can be used to generate graphics symbols without the use of a character generator. This is accomplished by selectively activating the Line Attribute outputs (LA_{0-1}), the Video Suppression output (VSP), and the Light Enable output. The dot level timing circuitry can use these signals to generate the proper symbols.

Character attributes can be programmed to blink or be highlighted individually. Blinking is accomplished with the Video Suppression output (VSP). Blink frequency is equal to the screen refresh frequency divided by 32. Highlighting is accomplished by activating the Highlight output (HGLT).

Character Attributes



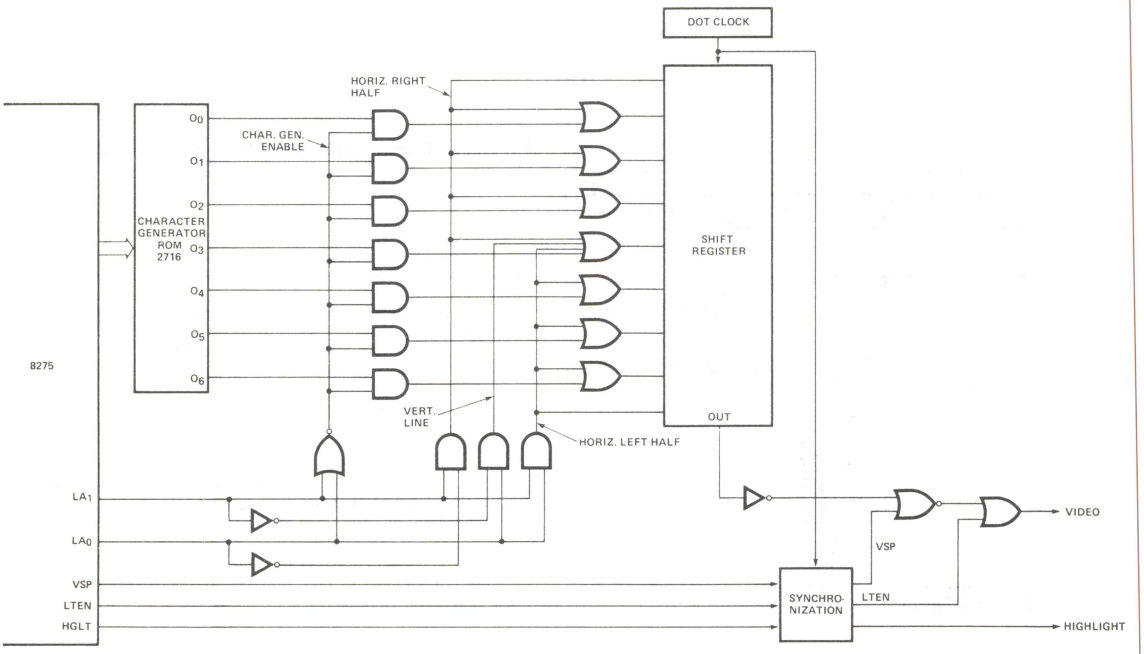


Figure 21. Typical Character Attribute Logic

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

Character attributes were designed to produce the following graphics:

CHARACTER ATTRIBUTE CODE "CCCC"		OUTPUTS LA_1	OUTPUTS LA_0	OUTPUTS VSP	OUTPUTS LTEN	SYMBOL	DESCRIPTION
0000	Above Underline	0	0	1	0		Top Left Corner
	Underline	1	0	0	0		
	Below Underline	0	1	0	0		
0001	Above Underline	0	0	1	0		Top Right Corner
	Underline	1	1	0	0		
	Below Underline	0	1	0	0		
0010	Above Underline	0	1	0	0		Bottom Left Corner
	Underline	1	0	0	0		
	Below Underline	0	0	1	0		
0011	Above Underline	0	1	0	0		Bottom Right Corner
	Underline	1	1	0	0		
	Below Underline	0	0	1	0		
0100	Above Underline	0	0	1	0		Top Intersect
	Underline	0	0	0	1		
	Below Underline	0	1	0	0		
0101	Above Underline	0	1	0	0		Right Intersect
	Underline	1	1	0	0		
	Below Underline	0	1	0	0		
0110	Above Underline	0	1	0	0		Left Intersect
	Underline	1	0	0	0		
	Below Underline	0	1	0	0		
0111	Above Underline	0	1	0	0		Bottom Intersect
	Underline	0	0	0	1		
	Below Underline	0	0	1	0		
1000	Above Underline	0	0	1	0		Horizontal Line
	Underline	0	0	0	1		
	Below Underline	0	0	1	0		
1001	Above Underline	0	1	0	0		Vertical Line
	Underline	0	1	0	0		
	Below Underline	0	1	0	0		
1010	Above Underline	0	1	0	0		Crossed Lines
	Underline	0	0	0	1		
	Below Underline	0	1	0	0		
1011	Above Underline	0	0	0	0		Not Recommended *
	Underline	0	0	0	0		
	Below Underline	0	0	0	0		
1100	Above Underline	0	0	1	0		Special Codes
	Underline	0	0	1	0		
	Below Underline	0	0	1	0		
1101	Above Underline						Illegal
	Underline		Undefined				
	Below Underline						
1110	Above Underline						Illegal
	Underline		Undefined				
	Below Underline						
1111	Above Underline						Illegal
	Underline		Undefined				
	Below Underline						

*Character Attribute Code 1011 is not recommended for normal operation. Since none of the attribute outputs are active, the character Generator will not be disabled, and an indeterminate character will be generated.

Character Attribute Codes 1101, 1110, and 1111 are illegal.

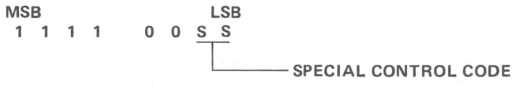
Blinking is active when B = 1.

Highlight is active when H = 1.

Special Codes

Four special codes are available to help reduce memory, software, or DMA overhead.

Special Control Character



S S	FUNCTION
0 0	End of Row
0 1	End of Row-Stop DMA
1 0	End of Screen
1 1	End of Screen-Stop DMA

The End of Row Code (00) activates VSP and holds it to the end of the line.

The End of Row-Stop DMA Code (01) causes the DMA Control Logic to stop DMA for the rest of the row when it is written into the Row Buffer. It affects the display in the same way as the End of Row Code (00).

The End of Screen Code (10) activates VSP and holds it to the end of the frame.

The End of Screen-Stop DMA Code (11) causes the DMA Control Logic to stop DMA for the rest of the frame when it is written into the Row Buffer. It affects the display in the same way as the End of Screen Code (10).

If the Stop DMA feature is not used, all characters after an End of Row character are ignored, except for the End of Screen character, which operates normally. All characters after an End of Screen character are ignored.

Note: If a Stop DMA character is not the last character in a burst or row, DMA is not stopped until after the next character is read. In this situation, a dummy character must be placed in memory after the Stop DMA character.

Field Attributes

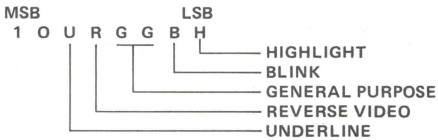
The field attributes are control codes which affect the visual characteristics for a field of characters, starting at the character following the code up to, and including, the character which precedes the *next* field attribute code, or up to the end of the frame. The field attributes are reset during the vertical retrace interval.

There are six field attributes:

1. *Blink* — Characters following the code are caused to blink by activating the Video Suppression output (VSP). The blink frequency is equal to the screen refresh frequency divided by 32.
2. *Highlight* — Characters following the code are caused to be highlighted by activating the Highlight output (HGLT).
3. *Reverse Video* — Characters following the code are caused to appear with reverse video by activating the Reverse Video output (RVV).
4. *Underline* — Characters following the code are caused to be underlined by activating the Light Enable output (LTEN).

5,6. *General Purpose* — There are two additional 8275 outputs which act as general purpose, independently programmable field attributes. GPA_{0-1} are active high outputs.

Field Attribute Code



H = 1 FOR HIGHLIGHTING
B = 1 FOR BLINKING
R = 1 FOR REVERSE VIDEO
U = 1 FOR UNDERLINE
GG = GPA_1, GPA_0

PRELIMINARY
Notice: This is not a final specification. Some parameter limits are subject to change.

The 8275 can be programmed to provide visible or invisible field attribute characters.

If the 8275 is programmed in the visible field attribute mode, all field attributes will occupy a position on the screen. They will appear as blanks caused by activation of the Video Suppression output (VSP). The chosen visual attributes are activated after this blanked character.

Figure 22. Example of the Visible Field Attribute Mode (Underline Attribute)

If the 8275 is programmed in the invisible field attribute mode, the 8275 FIFO is activated.

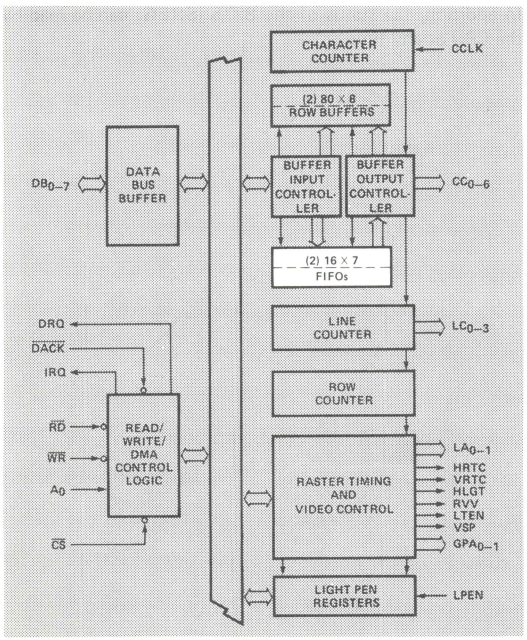


Figure 23. Block Diagram Showing FIFO Activation

Each row buffer has a corresponding FIFO. These FIFOs are 16 characters by 7 bits in size.

When a field attribute is placed in the row buffer during DMA, the buffer input controller recognizes it and places the *next* character in the proper FIFO.

When a field attribute is placed in the Buffer Output Controller during display, it causes the controller to immediately put a character from the FIFO on the Character Code outputs (CC_{0-6}). The chosen Visual Attributes are also activated.

Since the FIFO is 16 characters long, no more than 16 field attribute characters may be used per line in this mode. If more are used, a bit in the status word is set and the first characters in the FIFO are written over and lost.

Note: Since the FIFO is 7 bits wide, the MSB of any characters put in it are stripped off. Therefore, a Visual Attribute or Special Code must *not* immediately follow a field attribute code. If this situation does occur, the Visual Attribute or Special Code will be treated as a normal display character.

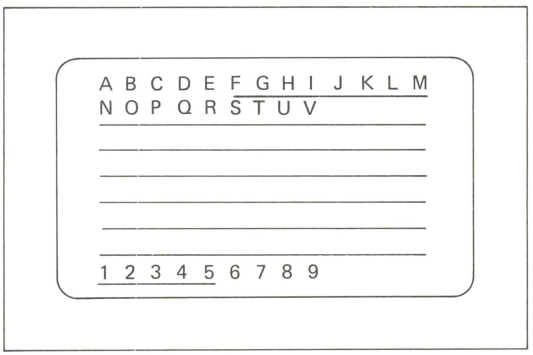


Figure 24. Example of the Invisible Field Attribute Mode (Underline Attribute)

Field and Character Attribute Interaction

Character Attribute Symbols are affected by the Reverse Video (RRV) and General Purpose (GPA_{0-1}) field attributes. They are not affected by Underline, Blink or Highlight field attributes; however, these characteristics can be programmed *individually* for Character Attribute Symbols.

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

Cursor Timing

The cursor location is determined by a cursor row register and a character position register which are loaded by command to the controller. The cursor can be programmed to appear on the display as:

1. a blinking underline
2. a blinking reverse video block
3. a non-blinking underline
4. a non-blinking reverse video block

The cursor blinking frequency is equal to the screen refresh frequency divided by 16.

If a non-blinking reverse video *cursor* appears in a non-blinking reverse video *field*, the cursor will appear as a normal video block.

If a non-blinking underline *cursor* appears in a non-blinking underline *field*, the cursor will not be visible.

Light Pen Detection

A light pen consists of a micro switch and a tiny light sensor. When the light pen is pressed against the CRT screen, the micro switch enables the light sensor. When the raster sweep reaches the light sensor, it triggers the light pen output.

If the output of the light pen is presented to the 8275 LPEN input, the row and character position coordinates are stored in a pair of registers. These registers can be read on command. A bit in the status word is set, indicating that the light pen signal was detected. The LPEN input must be a 0 to 1 transition for proper operation.

Note: Due to internal and external delays, the character position coordinate will be off by at least three character positions. This has to be corrected in software.

Device Programming

The 8275 has two programming registers, the Command Register (CREG) and the Parameter Register (PREG). It also has a Status Register (SREG). The Command Register can only be written into and the Status Registers can only be read from. They are addressed as follows:

A_0	OPERATION	REGISTER
0	Read	PREG
0	Write	PREG
1	Read	SREG
1	Write	CREG

The 8275 expects to receive a command and a sequence of 0 to 4 parameters, depending on the command. If the proper number of parameter bytes are not received before another command is given, a status flag is set, indicating an improper command.

Instruction Set

The 8275 instruction set consists of 8 commands.

COMMAND	NO. OF PARAMETER BYTES
Reset	4
Start Display	0
Stop Display	0
Read Light Pen	2
Load Cursor	2
Enable Interrupt	0
Disable Interrupt	0
Preset Counters	0

In addition, the status of the 8275 (SREG) can be read by the CPU at any time.

PRELIMINARY
Notice: This is not a final specification. Some parameter limits are subject to change.

1. Reset Command:

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB							LSB
Command	Write	1	Reset Command	0	0	0	0	0	0	0	0
Parameters	Write	0	Screen Comp Byte 1	S	H	H	H	H	H	H	H
	Write	0	Screen Comp Byte 2	V	V	R	R	R	R	R	R
	Write	0	Screen Comp Byte 3	U	U	U	U	L	L	L	L
	Write	0	Screen Comp Byte 4	M	F	C	C	Z	Z	Z	Z

Action — After the reset command is written, DMA requests stop, 8275 interrupts are disabled, and the VSP output is used to blank the screen. HRTC and VRTC continue to run. HRTC and VRTC timing are random on power-up.

As parameters are written, the screen composition is defined.

Parameter — S Spaced Rows

S	FUNCTIONS
0	Normal Rows
1	Spaced Rows

Parameter — HHHHHHH Horizontal Characters/Row

H	H	H	H	H	H	H	NO. OF CHARACTERS PER ROW
0	0	0	0	0	0	0	1
0	0	0	0	0	0	1	2
0	0	0	0	0	1	0	3
			.				.
			.				.
			.				.
1	0	0	1	1	1	1	80
1	0	1	0	0	0	0	Undefined
			.				.
			.				.
			.				.
1	1	1	1	1	1	1	Undefined

Parameter — VV Vertical Retrace Row Count

V	V	NO. OF ROW COUNTS PER VRTC
0	0	1
0	1	2
1	0	3
1	1	4

Parameter — RRRRRR Vertical Rows/Frame

R	R	R	R	R	R	NO. OF ROWS/FRAME
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
			.			.
			.			.
			.			.
1	1	1	1	1	1	64

Parameter — UUUU Underline Placement

U	U	U	U	LINE NUMBER OF UNDERLINE
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
		.		.
		.		.
		.		.
1	1	1	1	16

Parameter — LLLL Number of Lines per Character Row

L	L	L	L	NO. OF LINES/ROW
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
		.		.
		.		.
		.		.
1	1	1	1	16

Parameter — M Line Counter Mode

M	LINE COUNTER MODE
0	Mode 0 (Non-Offset)
1	Mode 1 (Offset by 1 Count)

Parameter — F Field Attribute Mode

F	FIELD ATTRIBUTE MODE
0	Transparent
1	Non-Transparent

Parameter — CC Cursor Format

C	C	CURSOR FORMAT
0	0	Blinking reverse video block
0	1	Blinking underline
1	0	Nonblinking reverse video block
1	1	Nonblinking underling

Parameter — ZZZZ Horizontal Retrace Count

Z	Z	Z	Z	NO. OF CHARACTER COUNTS PER HRTC
0	0	0	0	2
0	0	0	1	4
0	0	1	0	6
		.		.
		.		.
		.		.
1	1	1	1	32

Note: uuuu MSB determines blanking of top and bottom lines (1 = blanked, 0 = not blanked).

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

2. Start Display Command:

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB							LSB
Command	Write	1	Start Display	0	0	1	S	S	S	B	B
No parameters											

S S S BURST SPACE CODE

S S S	NO. OF CHARACTER CLOCKS BETWEEN DMA REQUESTS
0 0 0	0
0 0 1	7
0 1 0	15
0 1 1	23
1 0 0	31
1 0 1	39
1 1 0	47
1 1 1	55

B B BURST COUNT CODE

B B	NO. OF DMA CYCLES PER BURST
0 0	1
0 1	2
1 0	4
1 1	8

Action – 8275 interrupts are enabled, DMA requests begin, video is enabled, Interrupt Enable and Video Enable status flags are set.

3. Stop Display Command:

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB							LSB
Command	Write	1	Stop Display	0	1	0	0	0	0	0	0
No parameters											

Action – Disables video, interrupts remain enabled, HRTC and VRTC continue to run, Video Enable status flag is reset, and the "Start Display" command must be given to re-enable the display.

4. Read Light Pen Command

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB							LSB
Command	Write	1	Read Light Pen	0	1	1	0	0	0	0	0
Parameters	Read	0	Char. Number	(Char. Position in Row)							
	Read	0	Row Number	(Row Number)							

Action – The 8275 is conditioned to supply the contents of the light pen position registers in the next two read cycles of the parameter register. Status flags are not affected.

Note: Software correction of light pen position is required.

5. Load Cursor Position:

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB							LSB
Command	Write	1	Load Cursor	1	0	0	0	0	0	0	0
Parameters	Write	0	Char. Number	(Char. Position in Row)							
	Write	0	Row Number	(Row Number)							

Action – The 8275 is conditioned to place the next two parameter bytes into the cursor position registers. Status flags not affected.

6. Enable Interrupt Command:

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB							LSB
Command	Write	1	Enable Interrupt	1	0	1	0	0	0	0	0
No parameters											

Action – The interrupt enable status flag is set and interrupts are enabled.

7. Disable Interrupt Command:

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB							LSB
Command	Write	1	Disable Interrupt	1	1	0	0	0	0	0	0
No parameters											

Action – Interrupts are disabled and the interrupt enable status flag is reset.

8. Preset Counters Command:

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB							LSB
Command	Write	1	Preset Counters	1	1	1	0	0	0	0	0
No parameters											

Action – The internal timing counters are preset, corresponding to a screen display position at the top left corner. Two character clocks are required for this operation. The counters will remain in this state until any other command is given.

This command is useful for system debug and synchronization of clustered CRT displays on a single CPU.

Status Flags

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB	LSB
Command	Read	1	Status Word	0 IE IR LP IC VE OU F0	

IE – (Interrupt Enable) Set or reset by command. It enables vertical retrace interrupt. It is automatically set by a "Start Display" command and reset with the "Reset" command.

IR – (Interrupt Request) This flag is set at the beginning of display of the last row of the frame if the interrupt enable flag is set. It is reset after a status read operation.

LP – This flag is set when the light pen input (LPEN) is activated and the light pen registers have been loaded. This flag is automatically reset after a status read.

IC – (Improper Command) This flag is set when a command parameter string is too long or too short. The flag is automatically reset after a status read.

VE – (Video Enable) This flag indicates that video operation of the CRT is enabled. This flag is set on a "Start Display" command, and reset on a "Stop Display" or "Reset" command.

DU – (DMA Underrun) This flag is set whenever a data underrun occurs during DMA transfers. Upon detection of DU, the DMA operation is stopped and the screen is blanked until after the vertical retrace interval. This flag is reset after a status read.

FO – (FIFO Overrun) This flag is set whenever the FIFO is overrun. It is reset on a status read.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . 0°C to 70°C
Storage Temperature . . . . . –65°C to +150°C
Voltage On Any Pin
With Respect to Ground . . . . . –0.5V to +7V
Power Dissipation . . . . . 1 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$; $V_{CC} = 5V \pm 5\%$

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	–0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5V	V	
V_{OL}	Output Low Voltage		0.45	V	$I_{OL} = 2.2$ mA
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400\ \mu A$
I_{IL}	Input Load Current		±10	μA	$V_{IN} = V_{CC}$ to 0V
I_{OFL}	Output Float Leakage		±10	μA	$V_{OUT} = V_{CC}$ to 0V
I_{CC}	V_{CC} Supply Current		160	mA	

CAPACITANCE

$T_A = 25°C$; $V_{CC} = GND = 0V$

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
C_{IN}	Input Capacitance		10	pF	$f_c = 1$ MHz
$C_{I/O}$	I/O Capacitance		20	pF	Unmeasured pins returned to V_{SS}.

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

A.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$; $V_{CC} = 5.0V \pm 5\%$; GND = 0V

Bus Parameters (Note 1)

Read Cycle:

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
t_{AR}	Address Stable Before READ	0		ns	
t_{RA}	Address Hold Time for READ	0		ns	
t_{RR}	READ Pulse Width	250		ns	
t_{RD}	Data Delay from READ		200	ns	C_L = 150 pF
t_{DF}	READ to Data Floating	20	100	ns	

Write Cycle:

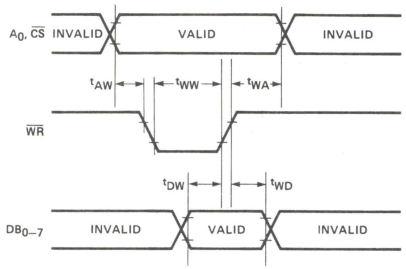
SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
t_{AW}	Address Stable Before WRITE	0		ns	
t_{WA}	Address Hold Time for WRITE	0		ns	
t_{WW}	WRITE Pulse Width	250		ns	
t_{DW}	Data Setup Time for WRITE	150		ns	
t_{WD}	Data Hold Time for WRITE	0		ns	

Clock Timing:

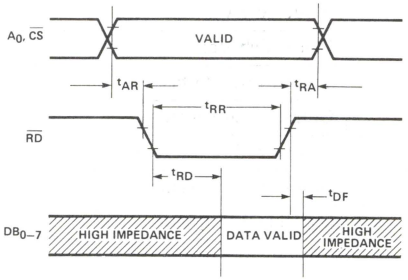
SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
t_{CLK}	Clock Period	320		ns	
t_{KH}	Clock High	120		ns	
t_{KL}	Clock Low	120		ns	
t_{KR}	Clock Rise	5	30	ns	
t_{KF}	Clock Fall	5	30	ns	

Note 1: AC timings measured at V_{OH} = 2.0, V_{OL} = 0.8

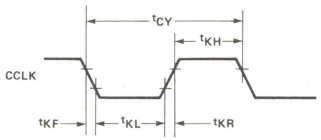
Write Timing



Read Timing



Clock Timing



Input Waveforms (For A.C. Tests)

MPU PERIPHERALS

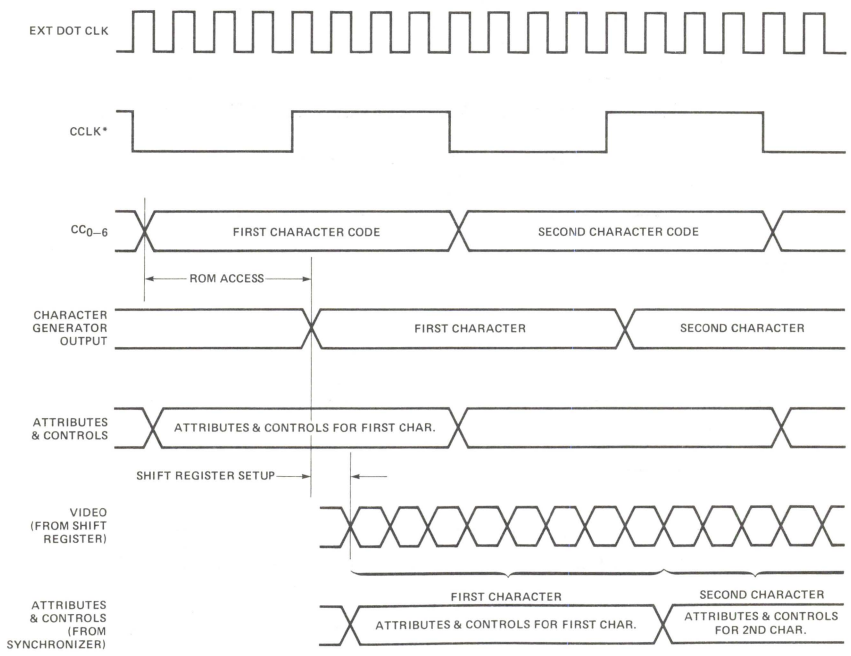
PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

Other Timing:

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
t_{CC}	Character Code Output Delay		150	ns	C_L = 50 pF
t_{HR}	Horizontal Retrace Output Delay		150	ns	C_L = 50 pF
t_{LC}	Line Count Output Delay		250	ns	C_L = 50 pF
t_{AT}	Control/Attribute Output Delay		250	ns	C_L = 50 pF
t_{VR}	Vertical Retrace Output Delay		250	ns	C_L = 50 pF
t_{IR}	IRQ↑ from CCLK↓		250	ns	C_L = 50 pF
t_{RI}	IRQ↓ from Rd↑		250	ns	C_L = 50 pF
t_{KQ}	DRQ↑ from CCLK↓		250	ns	C_L = 50 pF
t_{WQ}	DRQ↑ from WR↑		250	ns	C_L = 50 pF
t_{RQ}	DRQ↓ from WR↓		250	ns	C_L = 50 pF
t_{LR}	DACK↓ to WR↓	0		ns	
t_{RL}	WR↑ to DACK↑	0		ns	
t_{PR}	LPEN Rise		50	ns	
t_{PH}	LPEN Hold	100		ns	

Note: Timing measurements are made at the following reference voltages: Output "1" = 2.0V, "0" = 0.8V.

WAVEFORMS



*CCLK IS A MULTIPLE OF THE DOT CLOCK AND AN INPUT TO THE 8275.

Figure 25. Typical Dot Level Timing

PRELIMINARY
Motorola reserves the right to make changes to any products herein. This is not a final specification. Some parametric limits are subject to change.

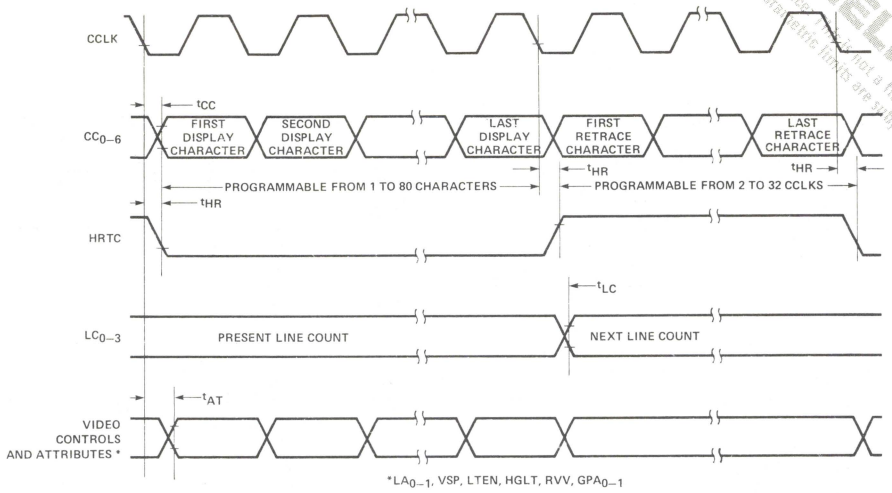


Figure 26. Line Timing

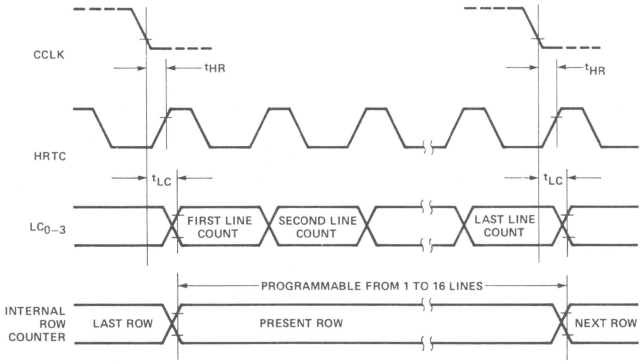


Figure 27. Row Timing

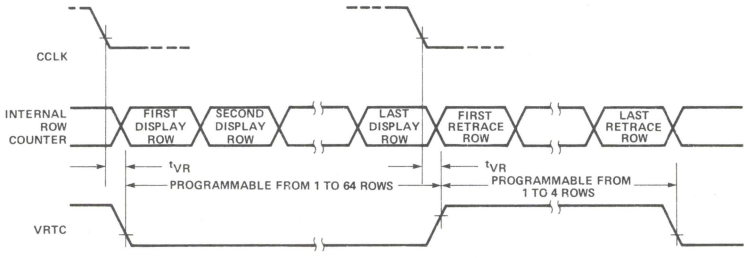


Figure 28. Frame Timing

MPU PERIPHERALS

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

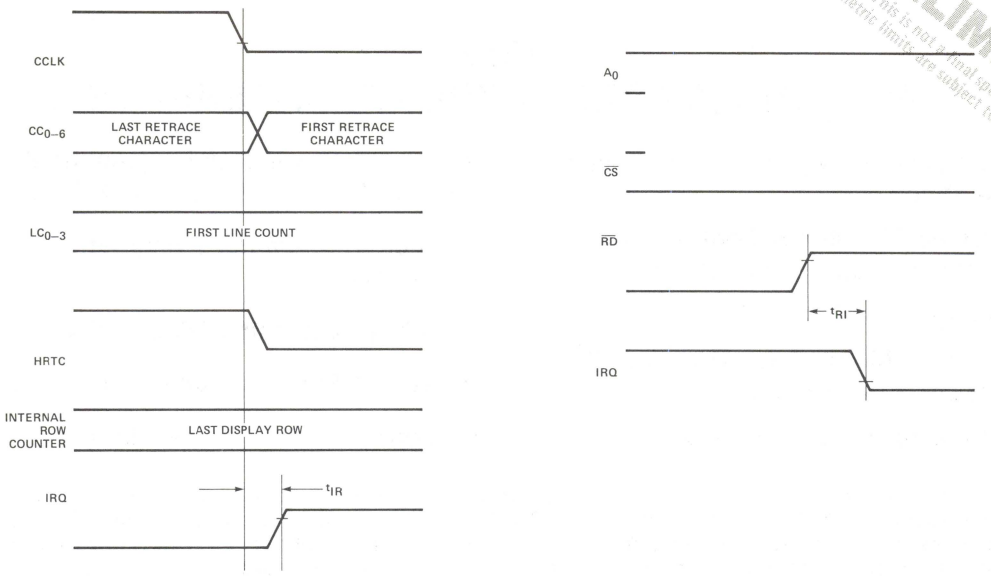


Figure 29. Interrupt Timing

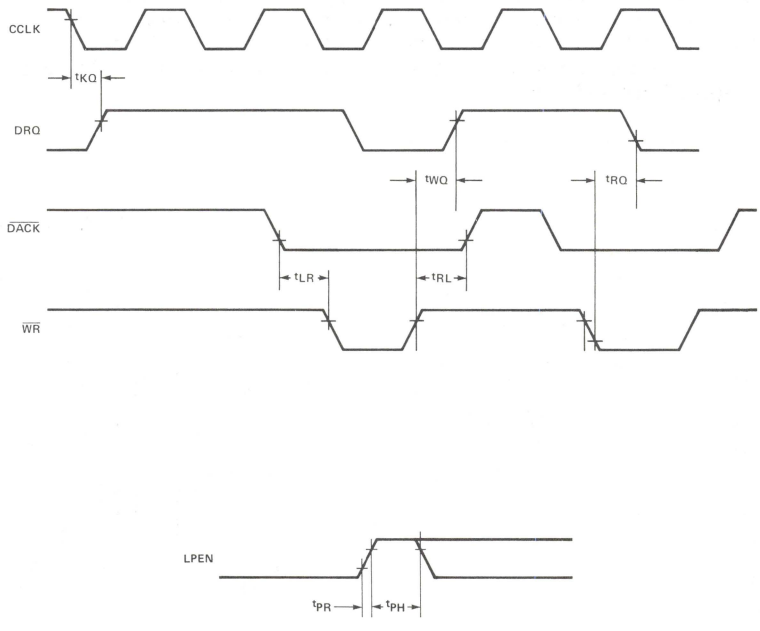


Figure 30. DMA Timing

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

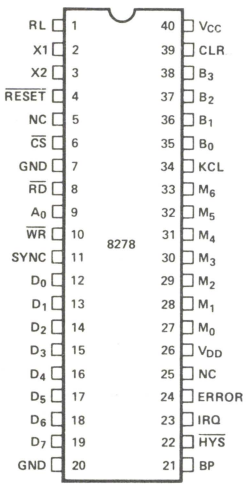
8278
PROGRAMMABLE KEYBOARD INTERFACE

- **Simultaneous Keyboard and Display Operations**
- **Interface Signals for Contract and Capacitive Coupled Keyboards**
- **128-Key Scanning Logic**
- **10.7 msec Matrix Scan Time for 128 Keys and 6 MHz Clock**
- **8-Character Keyboard FIFO**
- **N-Key Rollover with Programmable Error Mode on Multiple New Closures**
- **16- or 18-Character 7-Segment Display Interface**
- **Right or Left Entry Display RAM**
- **Depress/Release Mode Programmable**
- **Interrupt Output on Key Entry**

The Intel® 8278 is a general purpose programmable keyboard and display interface device designed for use with 8-bit microprocessors such the MDS-80™ and MCS-85™. The keyboard portion can provide a scanned interface to 128-key contact or capacitive-coupled keyboards. The keys are fully debounced with N-key rollover and programmable error generation on multiple new key closures. Keyboard entries are stored in an 8-character FIFO with overrun status indication when more than 8 characters are entered. Key entries set an interrupt request output to the master CPU.

The display portion of the 8278 provides a scanned display interface for LED, incandescent, and other popular display technologies. Both numeric displays and simple indicators may be used. The 8278 has a 16X4 display RAM which can be loaded or interrogated by the CPU. Both right entry calculator and left entry typewriter display formats are possible. Both read and write of the display RAM can be done with auto-increment of the display RAM address.

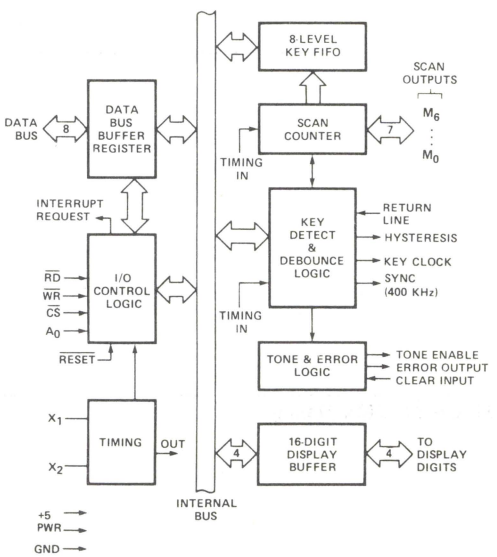
PIN CONFIGURATION



PIN NAMES

D_7-D_0	DATA BUS
$\overline{RD}$, $\overline{WR}$	READ, WRITE STROBES
$\overline{CS}$	CHIP SELECT
A_0	CONTROL/DATA SELECT
$\overline{RESET}$	RESET INPUT
X_1, X_2	FREQ. REFERENCE INPUT
SYNC	HIGH FREQUENCY OUTPUT CLOCK
RL	KEYBOARD RETURN LINE
CLR	CLEAR ERROR
KCL	KEY CLOCK
M_6–M_0	MATRIX SCAN LINES
B_3-B_0	DISPLAY OUTPUTS
ERROR	ERROR SIGNAL
$\overline{IRQ}$	INTERRUPT REQUEST
$\overline{HYS}$	HYSTERESIS
BP	TONE ENABLE

BLOCK DIAGRAM



MPU PERIPHERALS

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PIN DESCRIPTION

The 8278 is packaged in a 40-pin DIP. The following is a brief functional description of each pin.

Signal	Pin No.	Description
D_0-D_7	12-19	Three-state, bi-directional data bus lines used to transfer data and commands between the CPU and the 8278.
$\overline{WR}$	10	Write strobe which enables the master CPU to write data and commands between the CPU and the 8278.
$\overline{RD}$	8	Read strobe which enables the master CPU to read data and status from the 8278 internal registers.
$\overline{CS}$	6	Chip select input used to enable reading and writing to the 8278.
A_0	9	Address input used by the CPU to indicate control or data.
$\overline{RESET}$	4	A low signal on this pin resets the 8278.
X_1, X_2	2,3	Inputs for crystal, L-C or external timing signal to determine internal oscillator frequency.
IRQ	23	Interrupt Request Output to the master CPU. In the keyboard mode the IRQ line goes low with each FIFO read and returns high if there is still information in the FIFO or an ERROR has occurred.
M_0-M_6	27-33	Matrix scan outputs. These outputs control a decoder which scans the key matrix columns and the 16 display digits. Also, the Matrix scan outputs are used to multiplex the return lines from the key matrix.
RL	1	Input from the multiplexer which indicates whether the key currently being scanned is closed.
$\overline{HYS}$	22	Hysteresis output to the analog detector. (Capacitive keyboard configuration). A "0" means the key currently being scanned has already been recorded.
KCL	34	Key clock output to the analog detector (capacitive keyboard configuration) used to reset the detector before scanning a key.
SYNC	11	High frequency (400 KHz) output signal used in the key scan to detect a closed key (capacitive keyboard configuration).
B_0-B_3	35-38	These four lines contain binary coded decimal display information synchronized to the keyboard column scan. The outputs are for multiplexed digital displays.
ERROR	24	Error signal. This line is high whenever two new key closures are detected during a single scan or when too many characters are entered into the keyboard FIFO. It is reset by a system RESET pulse or by a "1" input on the CLR pin or by the CLEAR ERROR command.
CLR	39	Input used to clear an ERROR condition in the 8278.
BP	21	Tone enable output. This line is high for 10ms following a valid key closure; it is set high and remains high during an ERROR condition.
V_{CC}, V_{DD}	40,26	+5 volt power input: +5V ± 10%.
GND	20,7	Signal ground.

PRINCIPLES OF OPERATION

The following is a description of the major elements of the Programmable Keyboard/Display interface device. Refer to the block diagram in Figure 1.

I/O Control and Data Buffers

The I/O control section uses the $\overline{CS}$, A_0, $\overline{RD}$, and $\overline{WR}$ lines to control data flow to and from the various internal registers and buffers (see Table 1). All data flow to and from the 8278 is enabled by $\overline{CS}$. The 8-bits of information being transferred by the CPU is identified by A_0. A logic one means information is command or status. A logic zero means the information is data. $\overline{RD}$ and $\overline{WR}$ determine the direction of data flow through the Data Bus Buffer (DBB). The DBB register is a bi-directional 8-bit buffer register which connects the internal 8278 bus buffer register to the external bus. When the chip is not selected ($\overline{CS}$ = 1) the DBB is in the high impedance state. The DBB acts as an input when ($\overline{RD}$, $\overline{WR}$, $\overline{CS}$) = (1, 0, 0) and an output when ($\overline{RD}$, $\overline{WR}$, $\overline{CS}$) = (0, 1, 0).

$\overline{CS}$	A_0	$\overline{WR}$	$\overline{RD}$	Condition
0	0	1	0	Read DBB Data
0	1	1	0	Read STATUS
0	0	0	1	Write Data to DBB
0	1	0	1	Write Command to DBB
1	X	X	X	Disable 8278 Bus is High Impedance

Scan Counter

The scan counter provides the timing to scan the keyboard and display. The four MSB's (M_3-M_6) scan the display digits and provide column scan to the keyboard via a 4 to 16 decoder. The three LSB's (M_0-M_2) are used to multiplex the row return lines into the 8278.

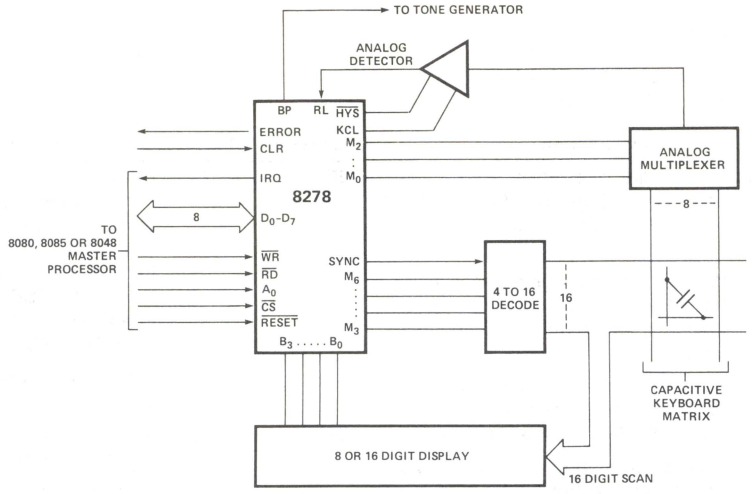


Figure 1. System Configuration for Capacitive-Coupled Keyboard

Keyboard Debounce and Control

The 8278 system configuration is shown in Figure 2. The rows of the matrix are scanned and the outputs are multiplexed by the 8278. When a key closure is detected, the debounce logic waits about 12 msec to check if the key remains closed. If it does, the address of the key in the matrix is transferred into a FIFO buffer.

FIFO and FIFO Status

The 8278 contains an 8X8 FIFO character buffer. Each new entry is written into a successive FIFO location and each is then read out in the order of entry. A FIFO status register keeps track of the number of characters in the FIFO and whether it is full or empty. Too many reads or key entries will be recognized as an error. The status can be read by a $\overline{RD}$ with $\overline{CS}$ low and A_0 high. The status logic also provides a IRQ signal to the master processor whenever the FIFO is not empty.

Display Address Registers and Display RAM

The Display Address registers hold the address of the word currently being written or read by the CPU and the two 4-bit nibbles being displayed. The read/write addresses are programmed by CPU command. They also can be set to auto increment after each read or write. The display RAM can be directly read by the CPU after the correct mode and address is set. Data entry to the display can be set to either left or right entry.

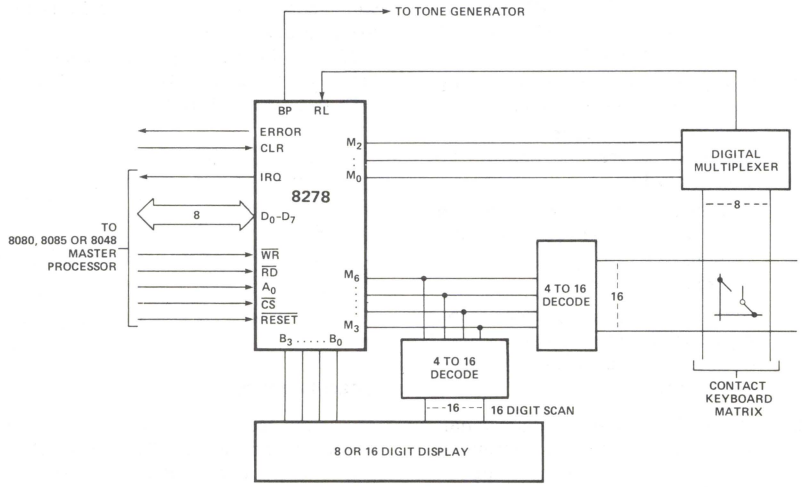
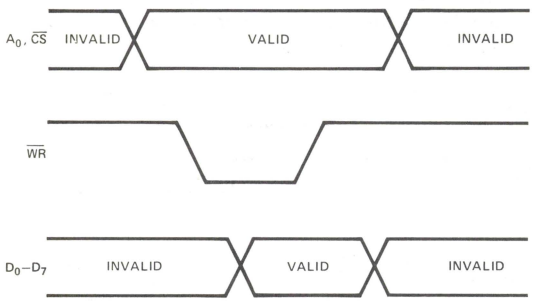


Figure 2. System Configuration for Contact Keyboard

8278 COMMANDS

The 8278 operating mode is programmed by the master CPU using the A_0, WR, and D_0-D_7 inputs as shown below:



The master CPU presents the proper command on the D_0-D_7 data lines with A_0=1 and then sends a $\overline{WR}$ pulse. The command is latched by the 8278 on the rising edge of the $\overline{WR}$ and is decoded internally to set the proper operating mode.

COMMAND SUMMARY

Keyboard/Display Mode Set

CODE	0	0	0	N	E	I	D	K

where the mode set bits are defined as follows:

K — the keyboard mode select bit
0 — normal key entry mode
1 — special function mode: Entry on key closure and on key release

D — the display entry mode select bit
0 — left display entry
1 — right display entry

I — the interrupt request (IRQ) output enable bit.
0 — enable IRQ output
1 — disable IRQ output

E — the error mode select bit
0 — error on multiple key depression
1 — no error on multiple key depression

N — the number of display digits select
0 — 16 display digits
1 — 8 display digits

NOTE: The default mode following a RESET input is all bits zero:

0	0	0	0	0	0	0	0

Read FIFO Command

CODE	0	1	0	0	0	0	0	0

Read Display Command

CODE	0	1	1	AI	A_3	A_2	A_1	A_0

Where AI indicates Auto Increment and A_3-A_0 is the address of the next display character to be read out.

AI=1 AUTO increment
AI=0 no AUTO increment

Write Display Command

CODE	1	0	0	AI	A_3	A_2	A_1	A_0

Where AI indicates Auto Increment and A_3-A_0 is the address of the next display character to be written.

Clear/Blank Command

CODE	1	0	1	UD	BD	CD	CF	CE

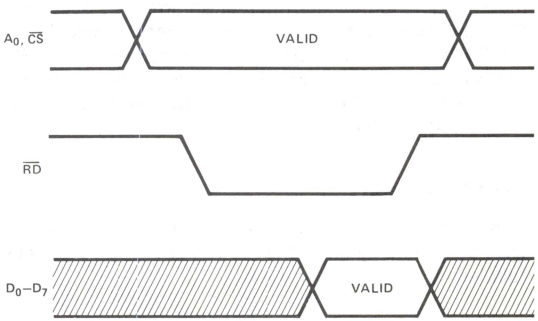
Where the command bits are defined as follows:

CE = Clear ERROR
CF = Clear FIFO
CD = Clear Display to all High
BD = Blank Display to all High
UD = Unblank Display

The display is cleared and blanked following a Reset.

8278 Status Read

The status register in the 8278 can be read by the master CPU using the A_0, $\overline{RD}$, and D_0-D_7 inputs as shown below:



The 8278 places 8-bits of status information on the D_0-D_7 lines following (A_0, $\overline{CS}$, $\overline{RD}$) = 1, 0 , 0 inputs from the master.

Status Format

S_3	S_2	S_1	S_0	B	KE	OBF	IBF
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Where the status bits are defined as follows:

IBF = Input Buffer Full Flag
OBF = Output Buffer Full Flag
KE = Keyboard Error Flag (multiple depression)
B = BUSY Flag
S_3-S_0 = FIFO Status

Status Description

The S_3-S_0 status bits indicate the number of entries (0 to 8) in the 8-level FIFO. A FIFO overrun will lock status at 1111. The overrun condition will prevent further key entries until cleared.

A multiple key closure error will set the KE flag and prevent further key entries until cleared.

The IBF and OBF flags signify the status of the 8278 data buffer registers used to transfer information (data, status or commands) to and from the master CPU.

The IBF flag is set when the master CPU writes Data or Commands to the 8278. The IBF flag is cleared by the 8278 during its response to the Data or Command.

The OBF flag is set when the 8278 has output data ready for the master CPU. This flag is cleared by a master CPU Data READ.

The Busy flag in the status register is used as a LOCK-OUT signal to the master processor during response to any command or data write from the master.

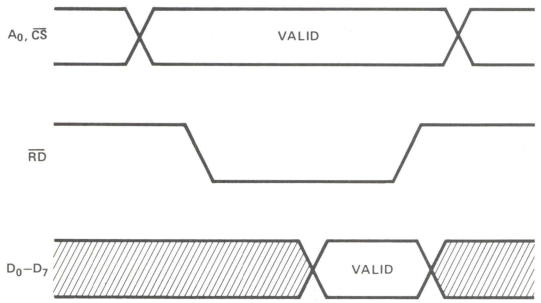
The master must test the Busy flag before each read (during a sequence) to be sure that the 8278 is ready with valid DATA.

The ERROR and TONE outputs from the 8278 are set high for either type of error. Both types of error are cleared by the CLR input, by the CLEAR ERROR command, or by a reset. The FIFO and Display buffers are cleared independently of the Errors.

FIFO status is used to indicate the number of characters in the FIFO and to indicate whether an error has occurred. Overrun occurs when the entry of another character into a full FIFO is attempted. Underrun occurs when the CPU tries to read an empty FIFO. The character read will be the last one entered. FIFO status will remain at 0000 and the error condition will not be set.

8278 Data Read

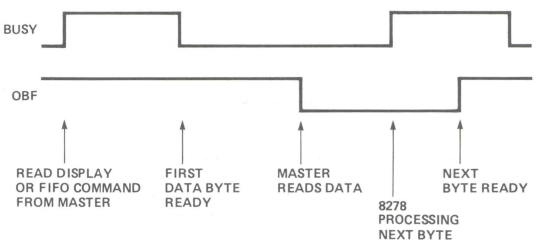
The master CPU can read DATA from the 8278 FIFO or Display buffers by using the A_0, $\overline{RD}$, and D_0-D_7 inputs as follows:



The master sends a $\overline{RD}$ pulse with A_0=0 and CS=0 and the 8278 responds by outputing data on lines D_0-D_7. The data is strobed by the trailing edge of $\overline{RD}$.

Data Read Sequence

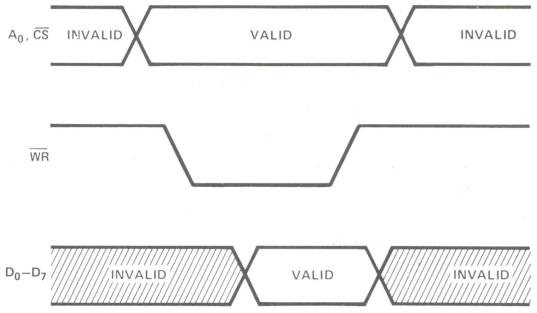
Before reading data, the master CPU must send a command to select FIFO or Display data. Following the command, the master must read STATUS and test the BUSY flag and the OBF flag to verify that the 8278 has responded to the previous command. A typical DATA READ sequence is as follows:



After the first read following a Read Display or Read FIFO command, successive reads may occur as soon as OBF rises.

8278 Data Write

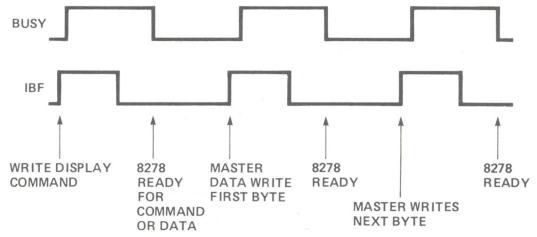
The master CPU can write DATA to the 8278 Display buffers by using the A_0, $\overline{WR}$ and D_0-D_7 inputs as follows:



The master CPU presents the Data on the D_0-D_7 lines with A_0=0 and then sends a $\overline{WR}$ pulse. The data is latched by the 8278 on the rising edge of $\overline{WR}$.

Data Write Sequence

Before writing data to the 8278, the master CPU must first send a command to select the desired display entry mode and to specify the address of the next data byte. Following the commands, the master must read STATUS and test the BUSY flag (B) and IBF flag to verify that the 8278 has responded. A typical sequence is shown below:



INTERFACE CONSIDERATIONS

Scanned Keyboard Mode

With N-key rollover each key depression is treated independently from all others. When a key is depressed the debounce logic waits for a full scan of 128 keys and then checks to see if the key is still down. If it is, the key is entered into the FIFO.

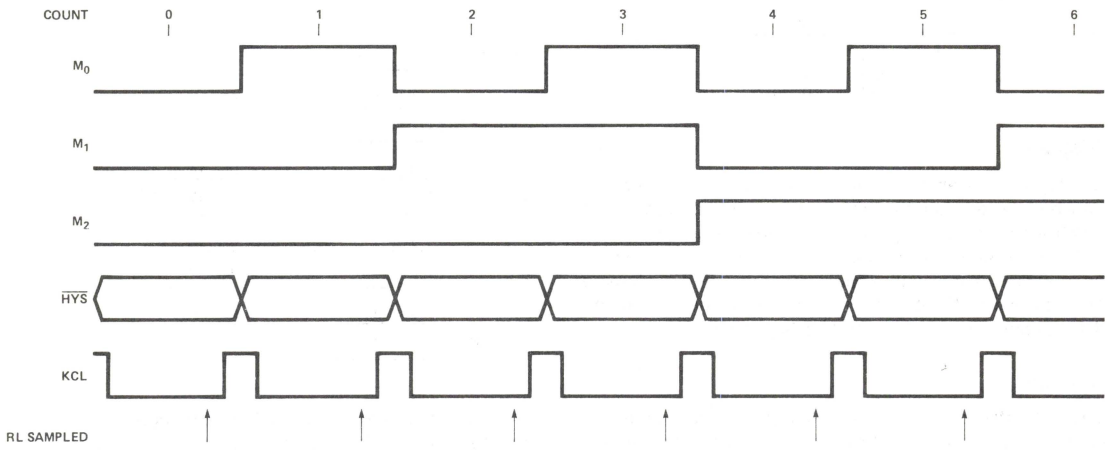


Figure 3. Keyboard Timing

If two key closures occur during the same scan the ERROR output is set, the KE flag is set in the Status word, the TONE output is activated and IRQ is set, and no further inputs are accepted. This condition is cleared by a high signal on the CLEAR input or by a system $\overline{RESET}$ input or by the CLEAR ERROR command.

In the special function mode both the key closure and the key release cause an entry to the FIFO. The release is entered with the MSB=1.

Any key entry triggers the TONE output for 10ms.

The $\overline{HYS}$ and KCL outputs enable the analog multiplexer and detector to be synchronized for interface to capacitive coupled keyboards.

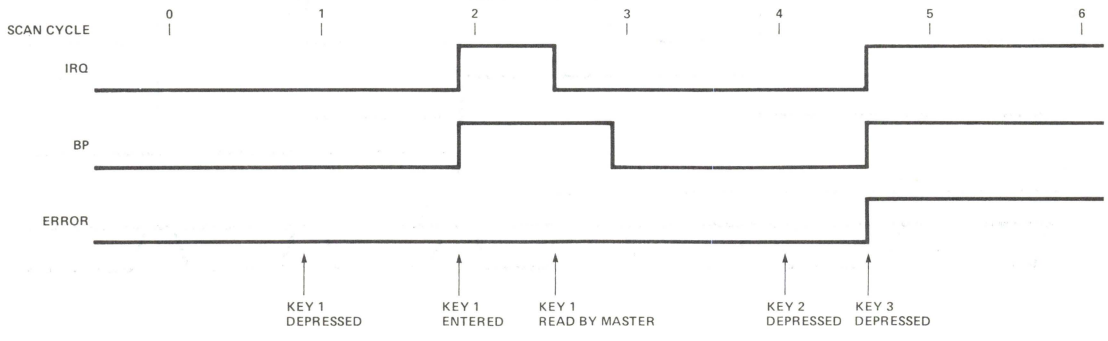


Figure 4. Key Entry and Error Timing

Data Format

In the scanned keyboard mode, the code entered into the FIFO corresponds to the position or address of the switch in the keyboard. The MSB is relevant only for special function keys in which code "0" signifies closure and "1" signifies release. The next four bits are the column count which indicates which column the key was found in. The last three bits are from the row counter.

KEY CODING

BIT	7	6	5	4	3	2	1	0
	SF	M_6	M_5	M_4	M_3	M_2	M_1	M_0

1 FOR SPECIAL FUNCTION MODE AND KEY RELEASED
0 FOR KEY DEPRESSED

Display

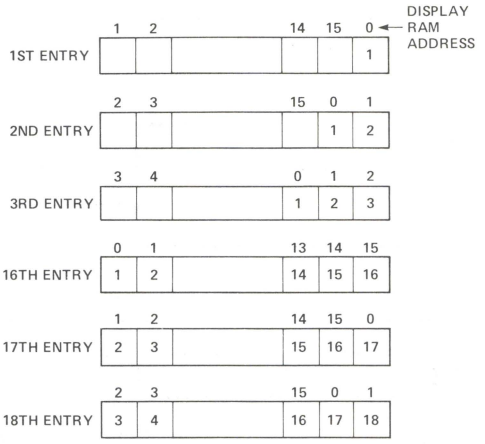
Display data is entered into a 16x4 display register and may be entered from the left, from the right or into specific locations in the display register. A new data character is put out on B_0-B_3 each time the M_6-M_3 lines change (i.e., once every 0.75ms with a 6 MHz crystal). Data is blanked during the time the column select lines change by raising the display outputs. Output data is positive true.

Left Entry

The left entry mode is the simplest display format in that each display position in the display corresponds to a byte (or nibble) in the Display RAM. Address 0 in the RAM is the left-most display character and address 15 is the right-most display character. Entering characters from position zero causes the display to fill from the left. The 17th character is entered back in the left-most position and filling again proceeds from there.

Right Entry

Right entry is the method used by most electronic calculators. The first entry is placed in the right-most display character. The next entry is also placed in the right-most character after the display is shifted left one character. The left-most character is shifted off the end and is lost.



Note that now the display position and register address do not correspond. Consequently, entering a character to an arbitrary position in the Auto Increment mode may have unexpected results. Entry starting at Display RAM address 0 with sequential entry is recommended. A Clear Display command should be given before display data is entered if the number of data characters is not equal to 16 (or 8) in this mode.

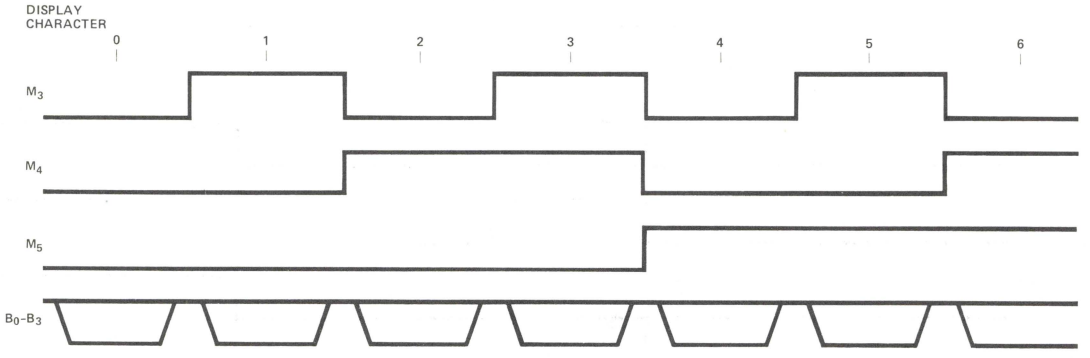
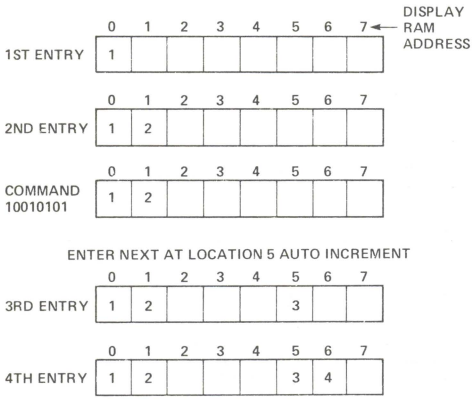


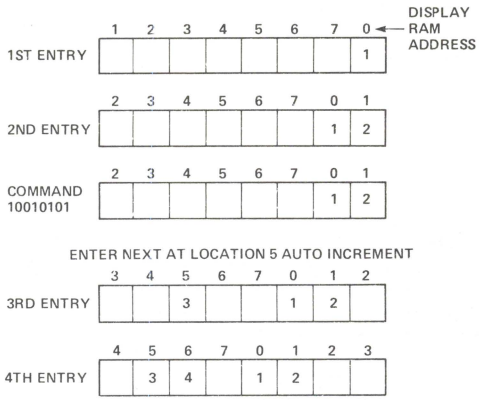
Figure 5. Display Timing

Auto Increment

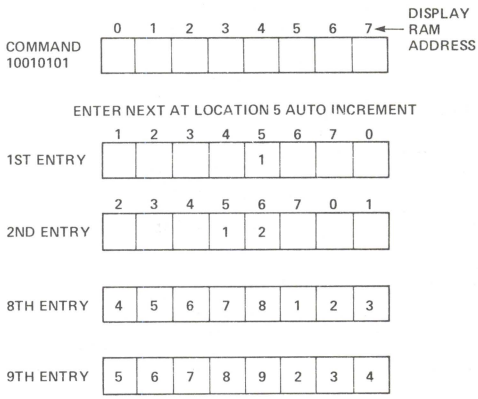
In the Left Entry mode, Auto Incrementing causes the address where the CPU will next write to be incremented by one and the character appears in the next location. With non-Auto Incrementing the entry is both to the same RAM address and display position. Entry to an arbitrary address in the Left Entry — Auto Increment mode has no undesirable side effects and the result is predictable:



In the Right Entry mode, Auto Incrementing and non Incrementing have the same effect as in the Left Entry except that the address sequence is interrupted:



Starting at an arbitrary location operates as shown below:



Entry appears to be from the initial entry point.

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin With Respect to Ground ..... 0.5V to +7V
Power Dissipation ..... 1.5 Watt

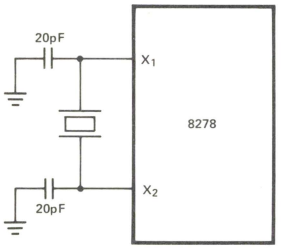
**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

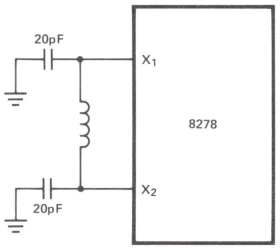
Commercial: $T_A = 0°C$ to $70°C$; $V_{CC} = +5V \pm 5\%$; $V_{SS} = 0V$

Symbol	Parameter	Min.	Max.	Units	Condition
V_{IL}	Input Low Voltage (All Inputs Except X_1, X_2	-0.5	0.8	V	
V_{IH1}	Input High Voltage (All Inputs Except X_1, X_2, $\overline{RESET}$	2.0	V_{CC}	V	
V_{IH2}	$\overline{RESET}$ High Voltage	3.0	V_{CC}	V	
V_{OL1}	Output Low Voltage (D_0-D_7)		0.45	V	$I_{OL} = 2.0mA$
V_{OL2}	Output Low Voltage (All Other Outputs)		0.45	V	$I_{OL} = 1.6mA$
V_{OH1}	Output High Voltage (D_0-D_7)	2.4		V	$I_{OH} = -400\mu A$
V_{OH2}	Output High Voltage (All Other Outputs)	2.4		V	$I_{OH} = -50\mu A$
I_{IL}	Input Leakage Current (All Inputs Except $\overline{RESET}$)		±10	μA	$V_{IN} = V_{CC}$
I_{OL}	Output Leakage Current (D_0-D_7)		±10	μA	$V_{IN} = V_{SS} + 0.45V$ or $V_{IN} = V_{CC}$
$I_{DD} + I_{CC}$	Total Supply Current		135	mA	$V_{CC} = 5.5V$
I_{DD}	V_{DD} Supply Current		25	mA	$V_{CC} = 5.5V$
I_{LI}	Low Input Source Current ($\overline{RESET}$)		0.2	mA	$V_{IL} = 0.8V$

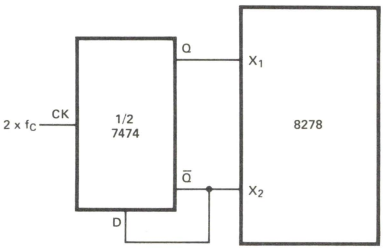
8278 FREQUENCY DIFFERENCE



1-6 MHz CRYSTAL



40 μh-130 μh INDUCTOR



EXTERNAL CLOCK

MPU PERIPHERALS

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

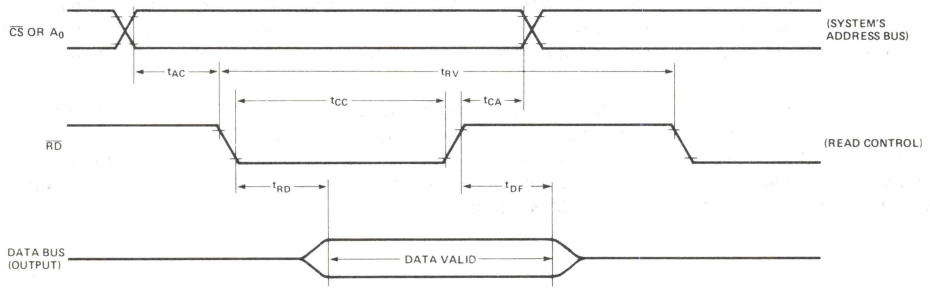
A.C. CHARACTERISTICS

T_A = 0°C to 70°C; V_{CC} = +5V ±10%; V_{SS} = 0V

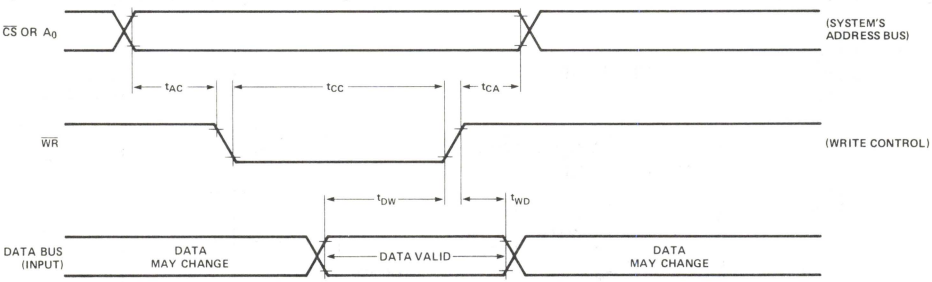
Symbol	Parameter	Min.	Max.	Units	Condition
t_{AC}	Address ($\overline{CS}$, A_0) Setup to Control ($\overline{RD}$, $\overline{WR}$)	0		ns	D_0-D_7, C_L = 150pF
t_{CA}	Address Hold from Control	0		ns	
t_{CC}	Control Pulse Width	250		ns	
t_{DW}	Data in Setup to $\overline{WR}$ T.E.	150		ns	
t_{WD}	Data in Hold After $\overline{WR}$ T.E.	0		ns	
t_{RD}	$\overline{RD}$ L.E. to Data Out Valid		150	ns	
t_{DF}	$\overline{RD}$ T.E. to Data Out Float	10	100	ns	
t_{MCY}	Matrix Cycle Time		10.7	ms	With 6MHz Crystal
t_{RV}	Recovery Time Between Reads and/or Writes	1		μs	

WAVEFORMS

Read Operation — Data Bus Buffer Register



Write Operation — Data Bus Buffer Register



MPU PERIPHERALS

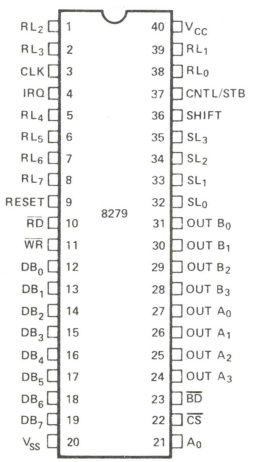
8279/8279-5
PROGRAMMABLE KEYBOARD/DISPLAY INTERFACE

- MCS-85™ Compatible 8279-5
- Simultaneous Keyboard Display Operations
- Scanned Keyboard Mode
- Scanned Sensor Mode
- Strobed Input Entry Mode
- 8-Character Keyboard FIFO
- 2-Key Lockout or N-Key Rollover with Contact Debounce
- Dual 8- or 16-Numerical Display
- Single 16-Character Display
- Right or Left Entry 16-Byte Display RAM
- Mode Programmable from CPU
- Programmable Scan Timing
- Interrupt Output on Key Entry

The Intel® 8279 is a general purpose programmable keyboard and display I/O interface device designed for use with Intel® microprocessors. The keyboard portion can provide a scanned interface to a 64-contact key matrix. The keyboard portion will also interface to an array of sensors or a strobed interface keyboard, such as the hall effect and ferrite variety. Key depressions can be 2-key lockout or N-key rollover. Keyboard entries are debounced and strobed in an 8-character FIFO. If more than 8 characters are entered, overrun status is set. Key entries set the interrupt output line to the CPU.

The display portion provides a scanned display interface for LED, incandescent, and other popular display technologies. Both numeric and alphanumeric segment displays may be used as well as simple indicators. The 8279 has 16X8 display RAM which can be organized into dual 16X4. The RAM can be loaded or interrogated by the CPU. Both right entry, calculator and left entry typewriter display formats are possible. Both read and write of the display RAM can be done with auto-increment of the display RAM address.

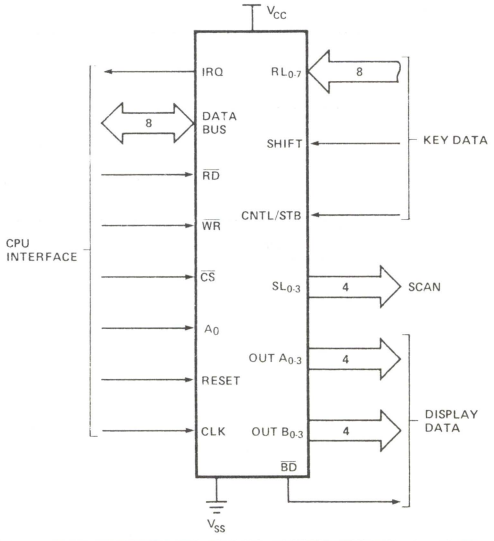
PIN CONFIGURATION



PIN NAMES

DB_{0-7}	I/O	DATA BUS (BI-DIRECTIONAL)
CLK	I	CLOCK INPUT
RESET	I	RESET INPUT
$\overline{CS}$	I	CHIP SELECT
$\overline{RD}$	I	READ INPUT
$\overline{WR}$	I	WRITE INPUT
A_0	I	BUFFER ADDRESS
IRQ	O	INTERRUPT REQUEST OUTPUT
SL_{0-3}	O	SCAN LINES
RL_{0-7}	I	RETURN LINES
SHIFT	I	SHIFT INPUT
CNTL/STB	I	CONTROL/STROBE INPUT
$OUT\ A_{0-3}$	O	DISPLAY (A) OUTPUTS
$OUT\ B_{0-3}$	O	DISPLAY (B) OUTPUTS
$\overline{BD}$	O	BLANK DISPLAY OUTPUT

LOGIC SYMBOL



MPU PERIPHERALS

FUNCTIONAL DESCRIPTION

Since data input and display are an integral part of many microprocessor designs, the system designer needs an interface that can control these functions without placing a large load on the CPU. The 8279 provides this function for 8-bit microprocessors.

The 8279 has two sections: keyboard and display. The keyboard section can interface to regular typewriter style keyboards or random toggle or thumb switches. The display section drives alphanumeric displays or a bank of indicator lights. Thus the CPU is relieved from scanning the keyboard or refreshing the display.

The 8279 is designed to directly connect to the microprocessor bus. The CPU can program all operating modes for the 8279. These modes include:

Input Modes

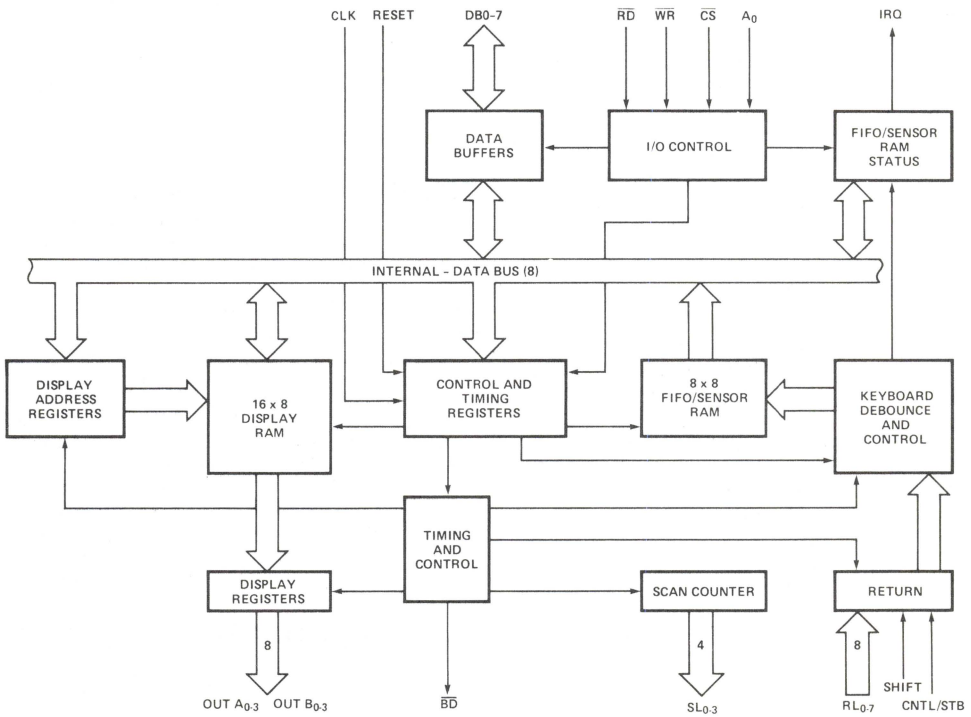
- Scanned Keyboard — with encoded (8 x 8 x 4 key keyboard) or decoded (4 x 8 x 4 key keyboard) scan lines. A key depression generates a 6-bit encoding of key position. Position and shift and control status are stored in the FIFO. Keys are automatically debounced with 2-key lockout or N-key rollover.
- Scanned Sensor Matrix — with encoded (8 x 8 matrix switches) or decoded (4 x 8 matrix switches) scan lines. Key status (open or closed) stored in RAM addressable by CPU.
- Strobed Input — Data on return lines during control line strobe is transferred to FIFO.

Output Modes

- 8 or 16 character multiplexed displays that can be organized as dual 4-bit or single 8-bit.
- Right entry or left entry display formats.

Other features of the 8279 include:

- Mode programming from the CPU.
- Programmable clock to match the 8279 scan times to the CPU cycle time.
- Interrupt output to signal CPU when there is keyboard or sensor data available.
- An 8 byte FIFO to store keyboard information.
- 16 byte internal Display RAM for display refresh. This RAM can also be read by the CPU.



HARDWARE DESCRIPTION

The 8279 is packaged in a 40 pin DIP. The following is a functional description of each pin.

No. Of Pins	Designation	Function
8	DB_0-DB_7	Bi-directional data bus. All data and commands between the CPU and the 8279 are transmitted on these lines.
1	CLK	Clock from system used to generate internal timing.
1	RESET	A high signal on this pin resets the 8279.
1	$\overline{CS}$	Chip Select. A low on this pin enables the interface functions to receive or transmit.
1	A_0	Buffer Address. A high on this line indicates the signals in or out are interpreted as a command or status. A low indicates that they are data.
2	$\overline{RD}$, $\overline{WR}$	Input/Output read and write. These signals enable the data buffers to either send data to the external bus or receive it from the external bus.
1	IRQ	Interrupt Request. In a keyboard mode, the interrupt line is high when there is data in the FIFO/Sensor RAM. The interrupt line goes low with each FIFO/Sensor RAM read and returns high if there is still information in the RAM. In a sensor mode, the interrupt line goes high whenever a change in a sensor is detected.
2	V_{SS}, V_{CC}	Ground and power supply pins.
4	SL_0-SL_3	Scan Lines which are used to scan the key switch or sensor matrix and the display digits. These lines can be either encoded (1 of 16) or decoded (1 of 4).
8	RL_0-RL_7	Return line inputs which are connected to the scan lines through the keys or sensor switches. They have active internal pullups to keep them high until a switch closure pulls one low. They also serve as an 8-bit input in the Strobed Input mode.
1	SHIFT	The shift input status is stored along with the key position on key closure in the Scanned Keyboard modes. It has an active internal pullup to keep it high until a switch closure pulls it low.
1	CNTL/STB	For keyboard modes this line is used as a control input and stored like status on a key closure. The line is also the strobe line that enters the data into the FIFO in the Strobed Input mode. (Rising Edge). It has an active internal pullup to keep it high until a switch closure pulls it low.
4 4	OUT A_0-OUT A_3 OUT B_0-OUT B_3	These two ports are the outputs for the 16 x 4 display refresh registers. The data from these outputs is synchronized to the scan lines (SL_0-SL_3) for multiplexed digit displays. The two 4 bit ports may be blanked independently. These two ports may also be considered as one 8 bit port.
1	$\overline{BD}$	Blank Display. This output is used to blank the display during digit switching or by a display blanking command.

PRINCIPLES OF OPERATION

The following is a description of the major elements of the 8279 Programmable Keyboard/Display interface device. Refer to the block diagram in Figure 1.

I/O Control and Data Buffers

The I/O control section uses the $\overline{CS}$, A_0, $\overline{RD}$ and $\overline{WR}$ lines to control data flow to and from the various internal registers and buffers. All data flow to and from the 8279 is enabled by $\overline{CS}$. The character of the information, given or desired by the CPU, is identified by A_0. A logic one means the information is a command or status. A logic zero means the information is data. $\overline{RD}$ and $\overline{WR}$ determine the direction of data flow through the Data Buffers. The Data Buffers are bi-directional buffers that connect the internal bus to the external bus. When the chip is not selected ($\overline{CS}$ = 1), the devices are in a high impedance state. The drivers input during $\overline{WR} \bullet \overline{CS}$ and output during $\overline{RD} \bullet \overline{CS}$.

Control and Timing Registers and Timing Control

These registers store the keyboard and display modes and other operating conditions programmed by the CPU. The modes are programmed by presenting the proper command on the data lines with A_0 = 1 and then sending a $\overline{WR}$. The command is latched on the rising edge of $\overline{WR}$.

The command is then decoded and the appropriate function is set. The timing control contains the basic timing counter chain. The first counter is a ÷ N prescaler that can be programmed to match the CPU cycle time to the internal timing. The prescaler is software programmed to a value between 2 and 31. A value which yields an internal frequency of 100 kHz gives a 5.1 ms keyboard scan time and a 10.3 ms debounce time. The other counters divide down the basic internal frequency to provide the proper key scan, row scan, keyboard matrix scan, and display scan times.

Scan Counter

The scan counter has two modes. In the encoded mode, the counter provides a binary count that must be externally decoded to provide the scan lines for the keyboard and display. In the decoded mode, the scan counter decodes the least significant 2 bits and provides a decoded 1 of 4 scan. Note than when the keyboard is in decoded scan, so is the display. This means that only the first 4 characters in the Display RAM are displayed.

In the encoded mode, the scan lines are active high outputs. In the decoded mode, the scan lines are active low outputs.

Return Buffers and Keyboard Debounce and Control

The 8 return lines are buffered and latched by the Return Buffers. In the keyboard mode, these lines are scanned, looking for key closures in that row. If the debounce circuit detects a closed switch, it waits about 10 msec to check if the switch remains closed. If it does, the address of the switch in the matrix plus the status of SHIFT and CONTROL are transferred to the FIFO. In the scanned Sensor Matrix modes, the contents of the return lines is directly transferred to the corresponding row of the Sensor RAM (FIFO) each key scan time. In Strobed Input mode, the contents of the return lines are transferred to the FIFO on the rising edge of the CNTL/STB line pulse.

FIFO/Sensor RAM and Status

This block is a dual function 8 x 8 RAM. In Keyboard or Strobed Input modes, it is a FIFO. Each new entry is written into successive RAM positions and each is then read in order of entry. FIFO status keeps track of the number of characters in the FIFO and whether it is full or empty. Too many reads or writes will be recognized as an error. The status can be read by an $\overline{RD}$ with $\overline{CS}$ low and A_0 high. The status logic also provides an IRQ signal when the FIFO is not empty. In Scanned Sensor Matrix mode, the memory is a Sensor RAM. Each row of the Sensor RAM is loaded with the status of the corresponding row of sensor in the sensor matrix. In this mode, IRQ is high if a change in a sensor is detected.

Display Address Registers and Display RAM

The Display Address Registers hold the address of the word currently being written or read by the CPU and the two 4-bit nibbles being displayed. The read/write addresses are programmed by CPU command. They also can be set to auto increment after each read or write. The Display RAM can be directly read by the CPU after the correct mode and address is set. The addresses for the A and B nibbles are automatically updated by the 8279 to match data entry by the CPU. The A and B nibbles can be entered independently or as one word, according to the mode that is set by the CPU. Data entry to the display can be set to either left or right entry. See Interface Considerations for details.

SOFTWARE OPERATION

8279 commands

The following commands program the 8279 operating modes. The commands are sent on the Data Bus with $\overline{CS}$ low and A_0 high and are loaded to the 8279 on the rising edge of $\overline{WR}$.

Keyboard/Display Mode Set

	MSB							LSB
Code:	0	0	0	D	D	K	K	K

Where DD is the Display Mode and KKK is the Keyboard Mode.

DD

0	0	8 8-bit character display — Left entry
0	1	16 8-bit character display — Left entry*
1	0	8 8-bit character display — Right entry
1	1	16 8-bit character display — Right entry

For description of right and left entry, see Interface Considerations. Note that when decoded scan is set in keyboard mode, the display is reduced to 4 characters independent of display mode set.

KKK

0	0	0	Encoded Scan Keyboard — 2 Key Lockout
0	0	1	Decoded Scan Keyboard — 2-Key Lockout
0	1	0	Encoded Scan Keyboard — N-Key Rollover
0	1	1	Decoded Scan Keyboard — N-Key Rollover
1	0	0	Encoded Scan Sensor Matrix
1	0	1	Decoded Scan Sensor Matrix
1	1	0	Strobed Input, Encoded Display Scan
1	1	1	Strobed Input, Decoded Display Scan

Program Clock

Code:	0	0	1	P	P	P	P	P

Where PPPPP is the prescaler value 2 to 31. The programmable prescaler divides the external clock by PPPPP to get the basic internal frequency. Choosing a divisor that yields 100 KHz will give the specified scan and debounce times. Default after a reset pulse (but not a program clear) is 31.

Read FIFO/Sensor RAM

Code:	0	1	0	AI	X	A	A	A	X = Don't Care

Where AI is the Auto-Increment flag for the Sensor RAM and AAA is the row that is going to be read by the CPU. AI and AAA are used only if the mode is set to Sensor Matrix. This command is used to specify that the source of data reads ($\overline{CS} \bullet RD \bullet \overline{A_0}$) by the CPU is the FIFO/Sensor RAM. No additional commands are necessary as long as

**Default after reset.*

data is desired from the FIFO/Sensor RAM. Another command is necessary if reading is desired from a different row than has been selected. If AI is a one, the row select counter will be incremented after each read so the next read will be from the next Sensor RAM row.

In the Auto Increment mode for reading data from the FIFO/Sensor RAM, each read advances the address by one so that the next read is from the next character. This Auto Incrementing has no effect on the display.

Read Display RAM

Code:

0	1	1	AI	A	A	A	A

Where AI is the Auto-Increment flag for the Display RAM and AAAA is the character that the CPU is going to read next. Since the CPU uses the same counter for reading and writing, this command also sets the next write location and Auto-Increment mode. This command is used to specify the display RAM as the data source for CPU data reads. If AI is set, the character address will be incremented after each read (or write) so that the next read (or write) will be from (to) the next character.

Write Display RAM

Code:

1	0	0	AI	A	A	A	A

Where AI is the Auto-Increment flag for the Display RAM and AAAA is the character that the CPU is going to write next. The addressing and Auto-Increment are identical to Read Display RAM. The difference is that Write Display RAM does not affect the source of CPU reads. The CPU will read from whichever RAM (Display or FIFO/Sensor) was last specified. This command will, however, change the location the next Display RAM read will be from if that source was specified.

Display Write Inhibit/Blanking

Code:

1	0	1	X	IW	IW	BL	BL
				A	B	A	B

Where IW is Inhibit Writing (nibble A or B) and BL is Blanking (nibble A or B). If the display is being used as a dual 4-bit display, then it is necessary to mask one of the 4-bit halves so that entries to the Display from the CPU do not affect the other half. The IW flags allow the programmer to do this. It is also useful to be able to blank either half when that half is not to be displayed. The BL flags blank the display. The next command sets the output code to be used as a "blank". Default after reset is all zeros. Note that to blank a display formatted as a single 8-bit output, it is necessary to set both BL flags to entirely blank the display. A "1" sets the flag. Reissuing the command with a "0" resets the flag.

Clear

Code:

1	1	0	C_D	C_D	C_D	C_F	C_A

Where C_D is Clear Display, C_F is Clear FIFO Status (including interrupt), and C_A is Clear All. C_D is used to clear all positions of the Display RAM to a programmable code. All ones, all zeros and hexadecimal 20 are possible. The 2 least significant bits of C_D are also used to specify the blanking code (see below).

C_D C_D C_D

0	X	All Zeros (X = Don't Care)
1	0	AB = Hex 20 (0010 0000)
1	1	All Ones

Enable clear display when = 1 (or by C_A = 1)

Clearing the display takes approximately 160 μs. During this time the CPU cannot write to the Display RAM. The MSB of the FIFO status word will be set during this time. C_F set the FIFO status to empty and resets the interrupt output line. After execution of a clear command with C_F set, the Sensor Matrix mode RAM pointer will be set to row 0.

C_A has the combined effect of C_D and C_F. C_A uses the C_D clearing code to determine how to clear the Display RAM. C_A also resets the internal timing chain to resynchronize it.

End Interrupt/Error Mode Set

Code:

1	1	1	E	X	X	X	X

X = Don't care.

For the sensor matrix modes this command lowers the IRQ line and enables further writing into RAM. (The IRQ line would have been raised upon the detection of a change in a sensor value. This would have also inhibited further writing into the RAM until reset).

For the N-key rollover mode — if the E bit is programmed to "1" the chip will operate in the special Error mode. (For further details, see Interface Considerations Section.)

Status Word

The status word contains the FIFO status, error, and display unavailable signals. This word is read by the CPU when A_0 is high and $\overline{CS}$ and $\overline{RD}$ are low. See Interface Considerations for more detail on status word.

Data Read

Data is read when A_0, $\overline{CS}$ and $\overline{RD}$ are all low. The source of the data is specified by the Read FIFO or Read Display commands. The trailing edge of $\overline{RD}$ will cause the address of the RAM being read to be incremented if the Auto-Increment flag is set. FIFO reads always increment (if no error occurs) independent of AI.

Data Write

Data that is written with A_0, $\overline{CS}$ and $\overline{WR}$ low is always written to the Display RAM. The address is specified by the latest Read Display or Write Display command. Auto-Incrementing on the rising edge of $\overline{WR}$ occurs if AI set by the latest display command.

INTERFACE CONSIDERATIONS

Scanned Keyboard Mode, 2-Key Lockout

There are three possible combinations of conditions that can occur during debounce scanning. When a key is depressed, the debounce logic is set. Other depressed keys are looked for during the next two scans. If none are encountered, it is a single key depression and the key position is entered into the FIFO along with the status of CNTL and SHIFT lines. If the FIFO was empty, IRQ will be set to signal the CPU that there is an entry in the FIFO. If the FIFO was full, the key will not be entered and the error flag will be set. If another closed switch is encountered, no entry to the FIFO can occur. If all other keys are released before this one, then it will be entered to the FIFO. If this key is released before any other, it will be entirely ignored. A key is entered to the FIFO only once per depression, no matter how many keys were pressed along with it or in what order they were released. If two keys are depressed within the debounce cycle, it is a simultaneous depression. Neither key will be recognized until one key remains depressed alone. The last key will be treated as a single key depression.

Scanned Keyboard Mode, N-Key Rollover

With N-key Rollover each key depression is treated independently from all others. When a key is depressed, the debounce circuit waits 2 keyboard scans and then checks to see if the key is still down. If it is, the key is entered into the FIFO. Any number of keys can be depressed and another can be recognized and entered into the FIFO. If a simultaneous depression occurs, the keys are recognized and entered according to the order the keyboard scan found them.

Scanned Keyboard — Special Error Modes

For N-key rollover mode the user can program a special error mode. This is done by the "End Interrupt/Error Mode Set" command. The debounce cycle and key-validity check are as in normal N-key mode. If during a single debounce cycle, two keys are found depressed, this is considered a simultaneous multiple depression, and sets an error flag. This flag will prevent any further writing into the FIFO and will set interrupt (if not yet set). The error flag could be read in this mode by reading the FIFO STATUS word. (See "FIFO STATUS" for further details.) The error flag is reset by sending the normal CLEAR command with $C_F = 1$.

Sensor Matrix Mode

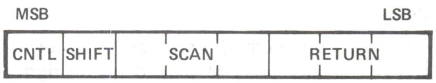
In Sensor Matrix mode, the debounce logic is inhibited. The status of the sensor switch is inputted directly to the Sensor RAM. In this way the Sensor RAM keeps an image of the state of the switches in the sensor matrix. Although debouncing is not provided, this mode has the advantage that the CPU knows how long the sensor was closed and when it was released. A keyboard mode can only indicate a validated closure. To make the software easier, the designer should functionally group the sensors by row since this is the format in which the CPU will read them.

The IRQ line goes high if any sensor value change is detected at the end of a sensor matrix scan. The IRQ line is cleared by the first data read operation if the Auto-Increment flag is set to zero, or by the End Interrupt command if the Auto-Increment flag is set to one.

Note: Multiple changes in the matrix Addressed by ($SL_{0-3} = 0$) may cause multiple interrupts. ($SL_0 = 0$ in the Decoded Mode). Reset may cause the 8279 to see multiple changes.

Data Format

In the Scanned Keyboard mode, the character entered into the FIFO corresponds to the position of the switch in the keyboard plus the status of the CNTL and SHIFT lines (non-inverted). CNTL is the MSB of the character and SHIFT is the next most significant bit. The next three bits are from the scan counter and indicate the row the key was found in. The last three bits are from the column counter and indicate to which return line the key was connected.



SCANNED KEYBOARD DATA FORMAT

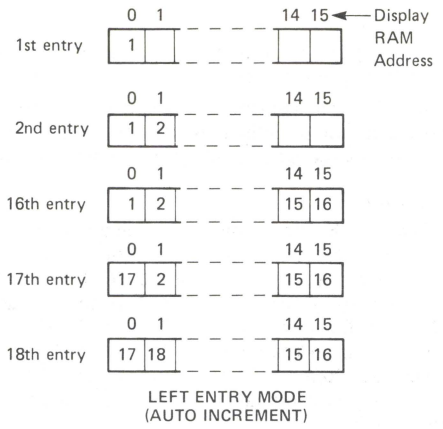
In Sensor Matrix mode, the data on the return lines is entered directly in the row of the Sensor RAM that corresponds to the row in the matrix being scanned. Therefore, each switch postion maps directly to a Sensor RAM position. The SHIFT and CNTL inputs are ignored in this mode. Note that switches are not necessarily the only thing that can be connected to the return lines in this mode. Any logic that can be triggered by the scan lines can enter data to the return line inputs. Eight multiplexed input ports could be tied to the return lines and scanned by the 8279.

In Strobed Input mode, the data is also entered to the FIFO from the return lines. The data is entered by the rising edge of a CNTL/STB line pulse. Data can come from another encoded keyboard or simple switch matrix. The return lines can also be used as a general purpose strobed input.

Display

Left Entry

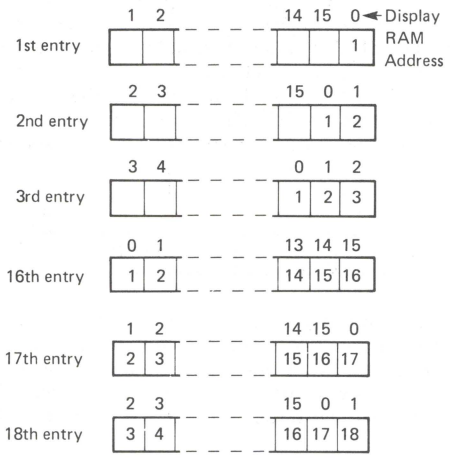
Left Entry mode is the simplest display format in that each display position directly corresponds to a byte (or nibble) in the Display RAM. Address 0 in the RAM is the left-most display character and address 15 (or address 7 in 8 character display) is the right most display character. Entering characters from position zero causes the display to fill from the left. The 17th (9th) character is entered back in the left most position and filling again proceeds from there.



LEFT ENTRY MODE
(AUTO INCREMENT)

Right Entry

Right entry is the method used by most electronic calculators. The first entry is placed in the right most display character. The next entry is also placed in the right most character after the display is shifted left one character. The left most character is shifted off the end and is lost.

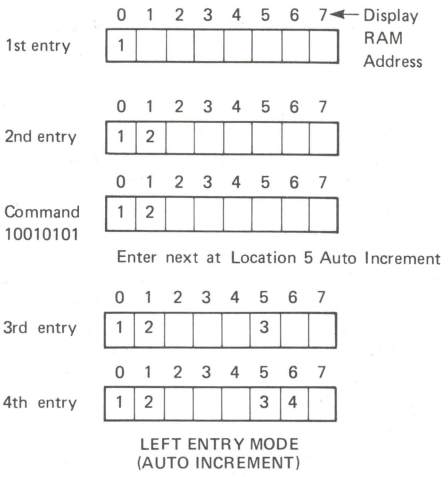


RIGHT ENTRY MODE
(AUTO INCREMENT)

Note that now the display position and register address do not correspond. Consequently, entering a character to an arbitrary position in the Auto Increment mode may have unexpected results. Entry starting at Display RAM address 0 with sequential entry is recommended.

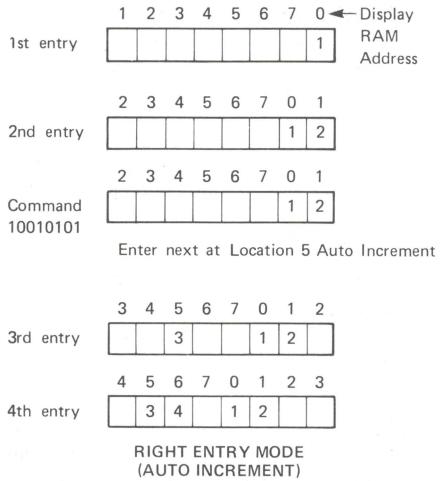
Auto Increment

In the Left Entry mode, Auto Incrementing causes the address where the CPU will next write to be incremented by one and the character appears in the next location. With non-Auto Incrementing the entry is both to the same RAM address and display position. Entry to an arbitrary address in the Auto Increment mode has no undesirable side effects and the result is predictable:



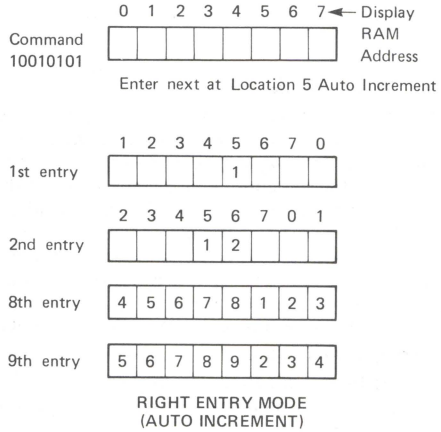
LEFT ENTRY MODE
(AUTO INCREMENT)

In the Right Entry mode, Auto Incrementing and non Incrementing have the same effect as in the Left Entry except if the address sequence is interrupted:



RIGHT ENTRY MODE
(AUTO INCREMENT)

Starting at an arbitrary location operates as shown below:



RIGHT ENTRY MODE
(AUTO INCREMENT)

PRELIMINARY
Notice: This is not a final specification. Some parameter limits are subject to change.

Entry appears to be from the initial entry point.

8/16 Character Display Formats

If the display mode is set to an 8 character display, the on duty-cycle is double what it would be for a 16 character display (e.g., 5.1 ms scan time for 8 characters vs. 10.3 ms for 16 characters with 100 kHz internal frequency).

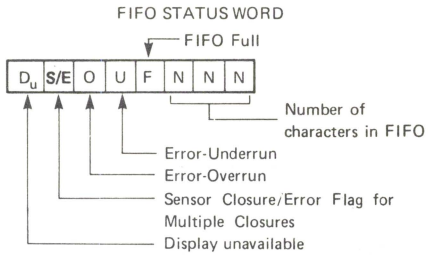
G. FIFO Status

FIFO status is used in the Keyboard and Strobed Input modes to indicate the number of characters in the FIFO and to indicate whether an error has occurred. There are two types of errors possible: overrun and underrun. Overrun occurs when the entry of another character into a full FIFO is attempted. Underrun occurs when the CPU tries to read an empty FIFO.

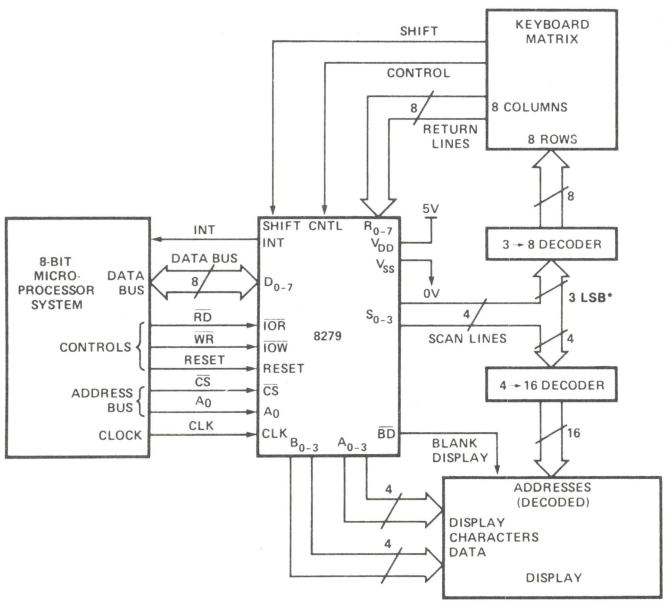
The FIFO status word also has a bit to indicate that the Display RAM was unavailable because a Clear Display or Clear All command had not completed its clearing operation.

In a Sensor Matrix mode, a bit is set in the FIFO status word to indicate that at least one sensor closure indication is contained in the Sensor RAM.

In Special Error Mode the S/E bit is showing the error flag and serves as an indication to whether a simultaneous multiple closure error has occurred.



APPLICATIONS



*Do not drive the keyboard decoder with the MSB of the scan lines.

PRELIMINARY

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature . . . . . 0°C to 70°C
Storage Temperature . . . . . -65°C to 125°C
Voltage on any Pin with
Respect to Ground . . . . . -0.5V to +7V
Power Dissipation . . . . . .1 Watt

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{SS} = 0V, Note 1

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{IL1}	Input Low Voltage for Return Lines	-0.5	1.4	V	
V_{IL2}	Input Low Voltage for All Others	-0.5	0.8	V	
V_{IH1}	Input High Voltage for Return Lines	2.2		V	
V_{IH2}	Input High Voltage for All Others	2.0		V	
V_{OL}	Output Low Voltage		0.45	V	Note 2
V_{OH}	Output High Voltage on Interrupt Line	3.5		V	Note 3
I_{IL1}	Input Current on Shift, Control and Return Lines		+10 -100	μA μA	$V_{IN} = V_{CC}$ V_{IN} = 0V
I_{IL2}	Input Leakage Current on All Others		±10	μA	$V_{IN} = V_{CC}$ to 0V
I_{OFL}	Output Float Leakage		±10	μA	$V_{OUT} = V_{CC}$ to 0V
I_{CC}	Power Supply Current		120	mA	

Notes:
1. 8279, V_{CC} = +5V ±5%; 8279-5, V_{CC} = +5V ±10%.
2. 8279, I_{OL} = 1.6mA; 8279-5, I_{OL} = 2.2mA.
3. 8279, I_{OH} = -100μA; 8279-5, I_{OH} = -400μA.

CAPACITANCE

SYMBOL	TEST	TYP.	MAX.	UNIT	TEST CONDITIONS
C_{in}	Input Capacitance	5	10	pF	$V_{in}=V_{CC}$
C_{out}	Output Capacitance	10	20	pF	$V_{out}=V_{CC}$

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{SS} = 0V, (Note 1)

Bus Parameters

Read Cycle:

Symbol	Parameter	8279 Min.	8279 Max.	8279-5 Min.	8279-5 Max.	Unit
t_{AR}	Address Stable Before $\overline{READ}$	50		0		ns
t_{RA}	Address Hold Time for $\overline{READ}$	5		0		ns
t_{RR}	$\overline{READ}$ Pulse Width	420		250		ns
t_{RD}[2]	Data Delay from $\overline{READ}$		300		150	ns
t_{AD}[2]	Address to Data Valid		450		250	ns
t_{DF}	$\overline{READ}$ to Data Floating	10	100	10	100	ns
t_{RCY}	Read Cycle Time	1		1		μs

Write Cycle:

Symbol	Parameter	8279 Min.	8279 Max.	8279-5 Min.	8279-5 Max.	Unit
t_{AW}	Address Stable Before $\overline{WRITE}$	50		0		ns
t_{WA}	Address Hold Time for $\overline{WRITE}$	20		0		ns
t_{WW}	$\overline{WRITE}$ Pulse Width	400		250		ns
t_{DW}	Data Set Up Time for $\overline{WRITE}$	300		150		ns
t_{WD}	Data Hold Time for $\overline{WRITE}$	40		0		ns

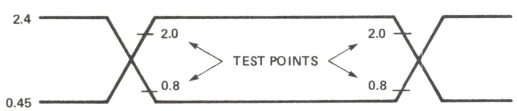
Notes:
1. 8279, V_{CC} = +5V ±5%; 8279-5, V_{CC} = +5V ±10%.
2. 8279, C_L = 100pF; 8279-5, C_L = 150pF.

Other Timings:

Symbol	Parameter	8279 Min.	8279 Max.	8279-5 Min.	8279-5 Max.	Unit
$t_{\phi W}$	Clock Pulse Width	230		120		nsec
t_{CY}	Clock Period	500		320		nsec

Keyboard Scan Time:	5.1 msec	Digit-on Time:	480 μsec
Keyboard Debounce Time:	10.3 msec	Blanking Time:	160 μsec
Key Scan Time:	80 μsec	Internal Clock Cycle:	10 μsec
Display Scan Time:	10.3 msec		

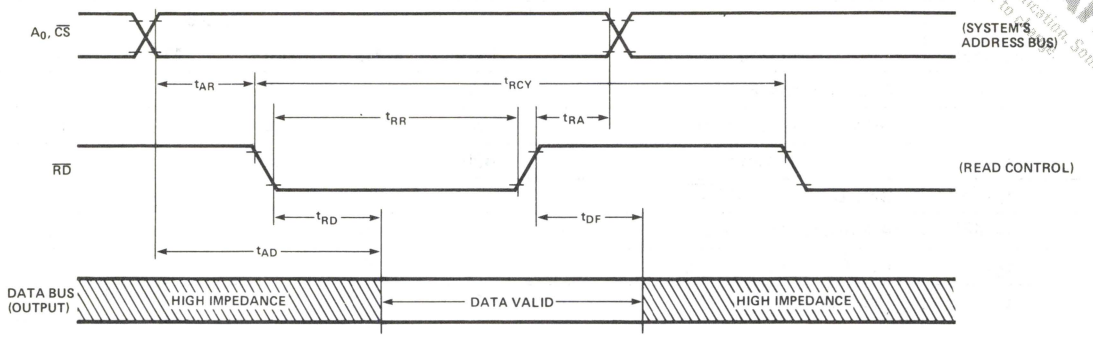
Input Waveforms For A.C. Tests



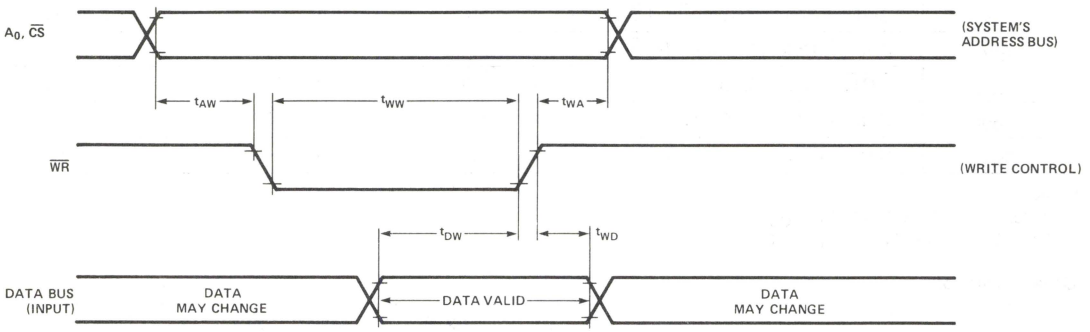
PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

WAVEFORMS

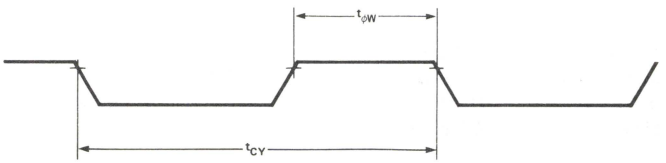
Read Operation



Write Operation



Clock Input



MPU PERIPHERALS

8294
DATA ENCRYPTION UNIT

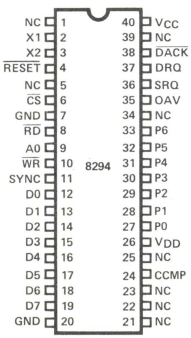
- 80-Byte/Sec Data Conversion Rate
- 64-Bit Data Encryption Using 56-Bit Key
- DMA Interface
- 3 Interrupt Output to Aid in Loading and Unloading Data
- 7-Bit User Output Port
- Single 5V ±10% Supply
- Peripheral to MCS-58™, MCS-80™, and MCS-48™ Processors
- Compatible with Algorithm Specified in Federal Information Processing Data Encryption Standard
- Encode and Decode Modes Available

The Intel® 8294 Data Encryption Unit (DEU) is a microprocessor peripheral device designed to encode and decode 64-bit blocks of data using the algorithm specified in the Federal Information Processing Data Encryption Standard. The DEU operates on 64-bit text words using a 56-bit user-specified key to produce 64-bit cipher words. The operation is reversible: if the cipher word is operated upon, the original text word is produced. The algorithm itself is permanently contained in the 8294; however, the 56-bit key is user-defined and may be changed at any time.

The 56-bit key and 64-bit message data are transferred to and from the 8294 in 8-bit bytes by way of the system data bus. A DMA interface and 3 interrupt outputs are available to minimize software overhead associated with data transfer. Also, by using the DMA interface, 2 or more DEUs may be operated in parallel to achieve effective system baud rates which are virtually any multiple of 80 bytes/second. The 8294 also has 7-bit TTL compatible output port for user-specified functions.

Because the 8294 is compatible with the NBS encryption standard it can be used in a variety of electronic funds transfer applications as well as other electronic banking and data handling applications where data must be encrypted.

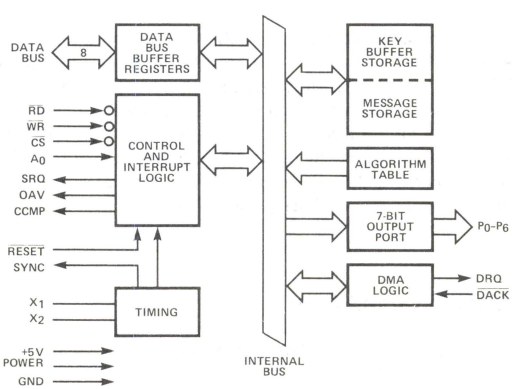
PIN CONFIGURATION



PIN NAMES

PIN NAME	FUNCTION
D_7-D_0	DATA BUS
$\overline{RD}$, $\overline{WR}$	READ, WRITE STROBES
$\overline{CS}$	CHIP SELECT
A_0	CONTROL/DATA SELECT
$\overline{RESET}$	RESET INPUT
X_1, X_2	FREQUENCY REFERENCE INPUT
SYNC	HIGH FREQUENCY OUTPUT
DRQ, $\overline{DACK}$	DMA REQUEST, DMA ACKNOWLEDGE
SRQ, OAV, CCMP	INTERRUPT REQUEST OUTPUTS
P_6-P_0	OUTPUT PORT LINES
V_{CC}, V_{DD}, GND	+5V POWER, GND

BLOCK DIAGRAM



MPU PERIPHERALS

COMMAND SUMMARY

Enter New Key

OP CODE:

0	1	0	0	0	0	0	0

MSB LSB

This command is followed by 8 data inputs which are retained in the key buffer (RAM) to be used in encrypting and decrypting data.

Encode Data

OP CODE:

0	0	1	1	0	0	0	0

MSB LSB

This command puts the 8294 into the encrypt mode.

Decode Data

OP CODE:

0	0	1	0	0	0	0	0

MSB LSB

This command puts the 8294 into the decrypt mode.

Set Mode

OP CODE:

0	0	0	0	A	B	C	D

MSB LSB

where:

A is the OAV (Output Available) interrupt enable
B is the SRQ (Service Request) interrupt enable
C is the DMA (Direct Memory Access) transfer enable
D is the CCMP (Conversion Complete) interrupt enable

This command determines which interrupt outputs will be enabled. A "1" in bits A, B, or D will enable the OAV, SRQ, or CCMP interrupts respectively. A "1" in bit C will allow DMA transfers. When bit C is set the OAV and SRQ interrupts should also be enabled (bits A,B = 1). Following the command in which bit C, the DMA bit, is set the 8294 will expect one data byte to specify the number of 8-byte blocks to be converted using DMA.

Write to Output Port

OP CODE:

1	P_6	P_5	P_4	P_3	P_2	P_1	P_0

MSB LSB

This command causes the 7 least significant bits of the command byte to be latched as output data on the 8294 output port.

FUNCTIONAL DESCRIPTION

In non-DMA mode, the conversion sequence is as follows:

1. A mode command is issued to enable the desired interrupt outputs.
2. A new key command is issued followed by 8 data inputs to initialize the key. Each byte must have odd parity.
3. The encrypt data or decrypt data command is issued to set the DEU in the desired mode.

After this, data conversions are made by writing 8 data bytes and then reading back 8 converted data bytes. Any of the above commands may be issued between data conversions to change the basic operation of the DEU; e.g., a decrypt data command could be issued to change the DEU from encrypt mode to decrypt mode without changing either the key or the interrupt outputs enabled.

COMMAND AND DATA TRANSFER

Four internal registers are addressable by the master: 2 for input, 2 for output. Access and function of these registers are described below.

$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	A_0	Register
1	0	0	0	Data input buffer
0	1	0	0	Data output buffer
0	1	0	1	Status output buffer
1	0	0	1	Command input buffer
X	X	1	X	Don't care

Data Input Buffer — Data written to this register is interpreted as part of a key, as data to be encrypted/decrypted, or as a DMA block count, depending on the command sequence preceding the write.

Data Output Buffer — Data read from this register will be the output of the encrypter/decrypter function.

Status Output Buffer — DEU status is available in this register at all times.

STATUS BIT:	7	6	5	4	3	2	1	0
FUNCTION:	XXX	XXX	XXX	KPE	HS	DEC	IBF	OBF

OBF — Output buffer full; OBF = 1 indicates that the output buffer contains encrypter/decrypter output data. It is set false when the data is read.

IBF — Input buffer full; IBF is set true when a command or data is written to the input buffer. The DEU sets this flag false when it has accepted the input byte. No data should be written when IBF = 1.

DEC — Decode; indicates whether the DEU is in encrypt or decrypt mode. Decrypt: DEC = TRUE; Encrypt: DEC = FALSE.

HS — Handshake flag; this flag is used in the data transfer protocol.

KPE — Key Parity Error; after a new key has been entered, the DEU will use this flag in conjunction with the HS flag to indicate correct or incorrect parity.

Command Input Buffer — Commands to the DEU are written to this register.

MASTER/SLAVE INTERFACE

Figures 1 through 4 illustrate four interface configurations used in Master/Slave data transfers. In all cases SRQ will be true (if enabled) and IBF will be false when the DEU is ready to accept data or commands.

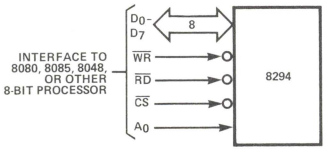


Figure 1. Polling Interface

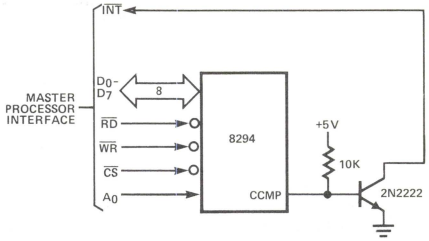


Figure 2. Single Interrupt Interface

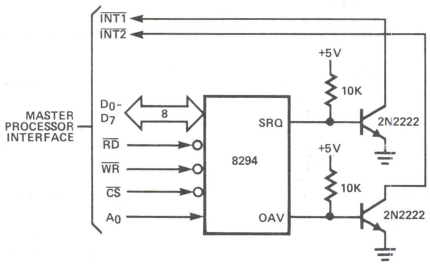
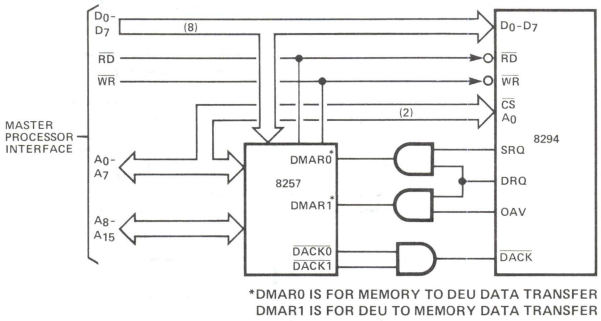


Figure 3. Dual Interrupt Interface



*DMAR0 IS FOR MEMORY TO DEU DATA TRANSFER
DMAR1 IS FOR DEU TO MEMORY DATA TRANSFER

Figure 4. DMA Interface

INTERFACE TIMING

Figures 5 through 8 illustrate recommended protocol sequences and timing for transferring commands and data between the master processor and the 8294.

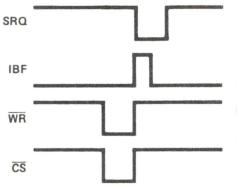


Figure 5. Single Byte Command

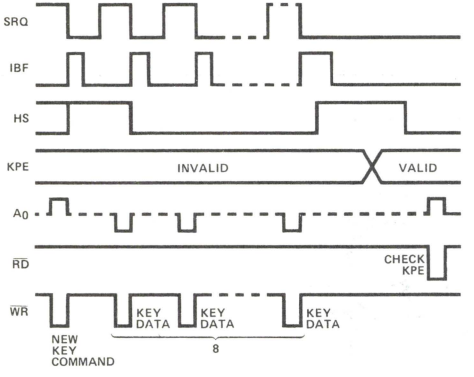


Figure 6. New Key Command

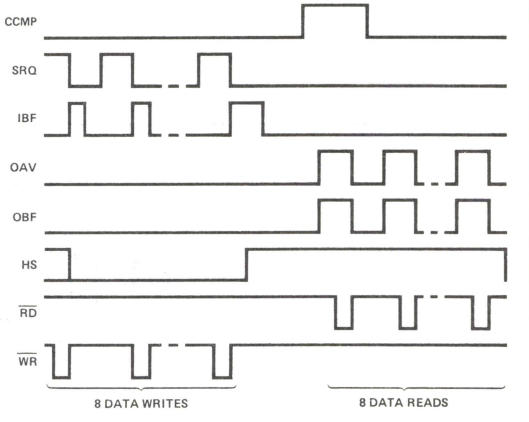


Figure 7. Encode/Decode data

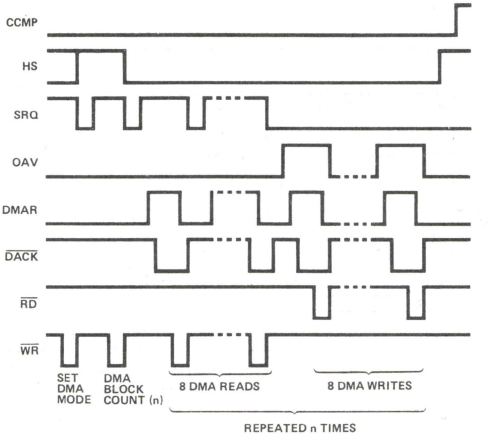
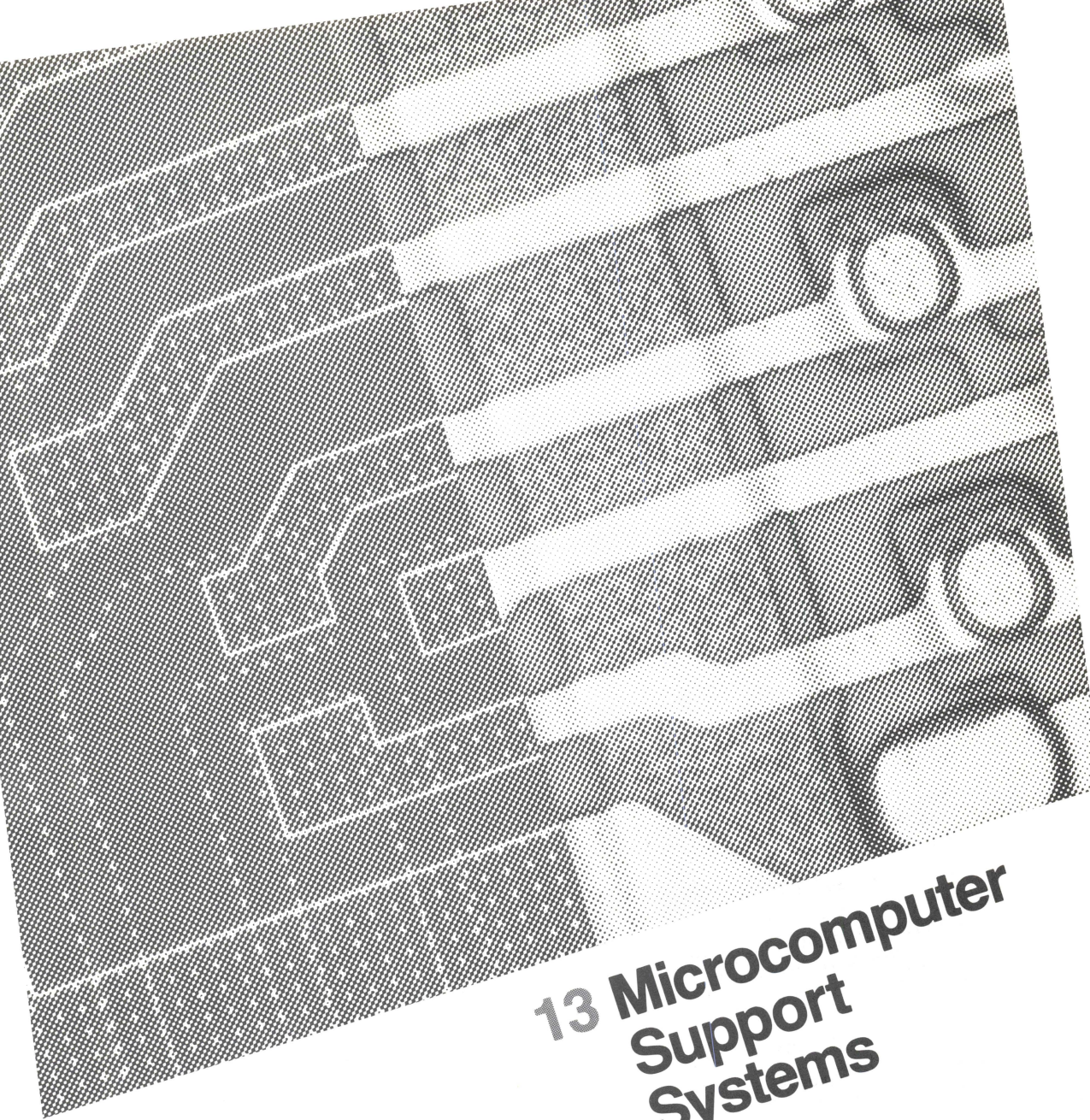


Figure 8. DMA Sequence



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MODEL 210
INTELLEC® SERIES II
MICROCOMPUTER DEVELOPMENT SYSTEM

Low-cost development system for MCS-80™, MCS-85™ and MCS-48™microprocessor families

Compact 4-slot chassis

Single LSI electronics board with CPU, 32K bytes RAM memory and 4K bytes ROM memory

Built-in interfaces for TTY, CRT, Printer, High-Speed Paper Tape Reader/Punch and Universal PROM Programmer

Eight-level nested, maskable priority interrupt system

ROM-based Monitor, Assembler and Editor

Self-Test Diagnostic capability

Standard MULTIBUS™ with multiprocessor and DMA capabilities

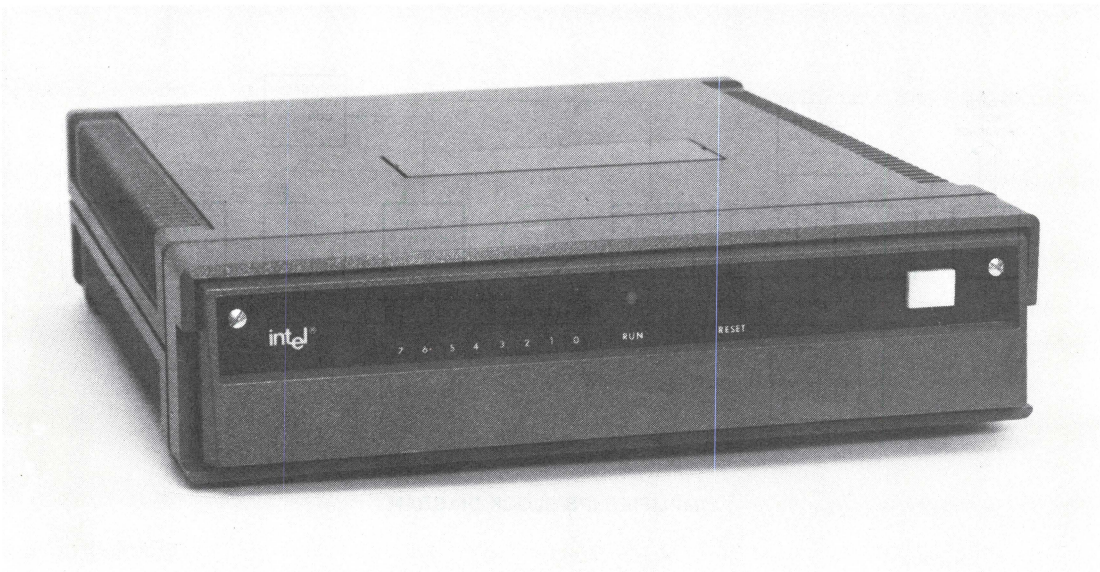
Easy upgrade to other Intellec Series II Systems

Compatible with standard Intellec/iSBC Expansion Modules

Software compatible with previous Intellec systems

The Intellec Series II Model 210 Microcomputer Development System is a low-cost, fully-supported development system providing basic hardware and software support for development of products based around Intel's MCS-80 or MCS-85 microprocessor families. Through optional software, this development capability can be extended to products based on the MCS-48 family of microprocessors.

Using the user-supplied system console (TTY or equivalent), the product designer may enter and correct his program's source code, then assemble and begin execution, all using the Model 210 ROM-resident Editor/Assembler. MCS-80 and MCS-85 debugging is accomplished through system monitor debug commands. Completed programs may be punched to paper tape for loading into the user's system or programmed into PROM using the optional Intellec Universal PROM Programmer.



MODEL 210 HARDWARE DESCRIPTION

The Intellec Series II Model 210 is a compact, 4" tabletop chassis with 4-slot cardcage, power supply, and two printed circuit cards. The CPU, interrupt, I/O and bus interface circuitry are all fashioned from Intel's high technology LSI components and located on one PC board. Known as the integrated processor board (IPB), it occupies the first slot in the cardcage. A second PC board (the parallel I/O board — PIO) containing additional I/O interface logic is mounted on the rear panel. The remaining 3 slots in the cardcage are available for system expansion.

The heart of the IPB is an Intel NMOS 8-bit microprocessor, the 8080A-2, running at 2.6 MHz. 32K bytes of RAM memory are provided on the board using Intel 16K RAMs. 4K of ROM is provided, preprogrammed with system bootstrap, "self-test" diagnostics and the Intellec Series II System Monitor. The 8-level vectored priority interrupt system allows interrupts to be individually masked. Using Intel's versatile 8259 interrupt controller, the interrupt system may be user-programmed to respond to individual needs.

The I/O subsystem in the Model 210 consists of two parts. Two serial channels are provided directly on the IPB itself. Each channel is RS232 compatible and is capable of running asynchronously from 110 to 9600 baud or synchronously from 150 to 56K baud. One channel contains current loop adapters for teletype compatibility. Both channels are implemented using Intel's 8251 USART. They can be programmatically selected to perform a variety of I/O functions.

Baud rate selection is accomplished programmatically through an Intel 8253 Interval Timer. The 8253 also serves as the real-time clock for the entire system. I/O activity is signaled to the system through a second 8259 interrupt controller, operating in a polled mode, nested to the primary 8259.

The second part of the I/O subsystem consists of the interface logic provided on the PIO board itself. Utilizing Intel's UPI-41 programmable peripheral controller, the PIO board provides device interfaces for:

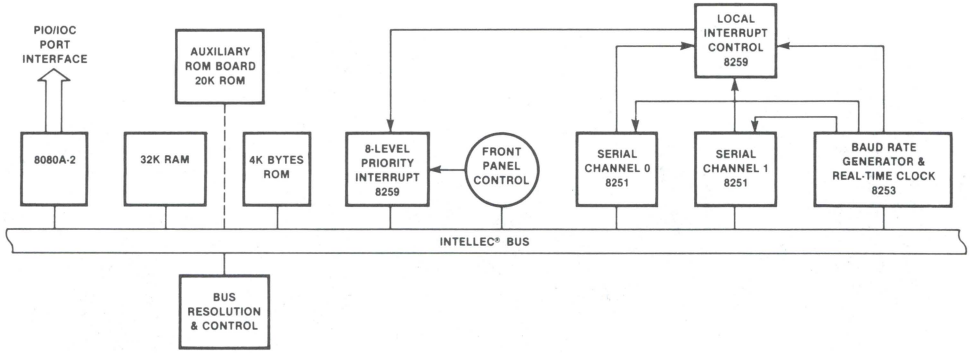
- Printer
- High-Speed Paper Tape Reader
- High-Speed Paper Tape Punch
- Universal PROM Programmer

Communication between the PIO and IPB is maintained over a separate 8-bit bidirectional data bus. Connectors for the 4 devices specified above, as well as the two serial channels, are mounted directly on the PIO.

User control is maintained through a front panel consisting of a power switch and indicator, reset/boot switch, run/halt light, and 8 interrupt switches and indicators. The front-panel circuit board is attached directly to the IPB, allowing the 8 interrupt switches to connect to the primary 8259, as well as the Intellec Series II Bus.

All Intellec Series II models implement the industry-standard MULTIBUS. It enables several bus masters, such as CPU and DMA devices, to share the bus and memory by operating at different priority levels. Resolution of bus exchanges is synchronized by a bus clock signal which is derived independently from processor clocks. Read/write transfers may take place at rates up to 5 MHz. The bus structure is suitable for use with any Intel microprocessor family.

All standard Model 210 software is ROM based to eliminate costly delays of loading paper tape. The capabilities of the System Monitor with its "self-test" diagnostics, Text Editor and MCS-80/MCS-85 or MCS-48 ROM Assemblers are described on pages 13-19 to 13-22 of this catalog.



SIMPLIFIED IPB BLOCK DIAGRAM

SPECIFICATIONS

PHYSICAL

Dimensions: 19.13" (48.59 cm) deep × 17.37" (44.12 cm) wide × 4.81" (12.22 cm) high

Weight: 45 lb (20.5 kg)

ELECTRICAL

DC Power Supply:

Volts Supplied	Amps Supplied	Typical System Requirements
+ 5 ±5%	24	3.5
+12 ±5%	2.0	0.1
−12 ±5%	0.3	0.05
−10 ±5%	1.0	0.1

AC Requirements: 50–60 Hz, 115/230 VAC

ENVIRONMENTAL

Operating Temperature: 0° to 35°C (95°F)

HOST PROCESSOR (IPB)

8080A-2 based, operating at 2.600 MHz.

RAM: 32K, expandable to 64K with SBC-032 RAM board (System Monitor occupies 62K through 64K).

ROM: 4K (2K in monitor, 2K in boot/diagnostic), expandable with addition of 20K auxiliary ROM board containing Text Editor and Assembler.

Bus: MULTIBUS, maximum transfer rate of 5 MHz.

Clocks: Host Processor, crystal controlled at 2.6 MHz. Bus Clock, crystal controlled at 9.8304 MHz.

I/O Interfaces:

2 Serial I/O Channels, RS232C, at 110–9600 baud (asynchronous) or 150–56K baud (synchronous). Baud rates and serial format fully programmable using Intel 8251 USARTs. Serial Channel 1 additionally provided with 20 mA current loop.

Parallel I/O interfaces provided for paper tape punch, paper tape reader, printer, and Universal PROM Programmer.

Interrupts:

8-level, maskable, nested priority interrupt network initiated from front panel or user-selected devces.

Direct Memory Access (DMA):

Standard capability on MULTIBUS; implemented for user-selected DMA devices through optional DMA module — maximum transfer rate of 2 MHz.

Memory Access Time:

RAM: 585 ns
PROM: 450 ns

EQUIPMENT SUPPLIED

Model 210 Chassis
Integrated Processor Board (IPB)
Parallel I/O Board (PIO)
ROM-Resident System Monitor
Auxiliary ROM Board with MCS-80/MCS-85 Assembler and Text Editor
PROM Programming Software (Paper Tape)
Assembler Cross Reference Program (Paper Tape)
A Guide to Microcomputer Development Systems (9800558)
Model 210 User's Guide (9800557)
Hardware Interface Manual (9800555)
8080/8085 Assembly Language Manual (9800301)
Monitor Source Listing (9800605)
Schematic Drawings (9800554)

ORDERING INFORMATION

PRODUCT CODE	DESCRIPTION
MDS-210	Intellec Series II Model 210 Microcomputer Development System

MODEL 220
INTELLEC® SERIES II
MICROCOMPUTER DEVELOPMENT SYSTEM

Complete Microcomputer Development System in one package for MCS-80™, MCS-85™ and MCS-48™ microprocessor families

Integral CRT with detachable upper/lower case "typewriter" style full ASCII keyboard

Integral 250K-byte floppy disk with total storage capacity expandable to over 2M bytes

Single LSI electronics board with CPU, 32K bytes RAM memory and 4K bytes ROM memory

Built-in interfaces for High-Speed Paper Tape Reader/Punch, Printer and Universal PROM Programmer

Eight-level nested, maskable priority interrupt system

Powerful ISIS-II Diskette Operating System with Relocating Macro Assembler, Linker and Locater

Self-Test Diagnostic capability

Standard MULTIBUS™ with multiprocessor and DMA capability

Compatible with standard Intellec/iSBC Expansion Modules

Software compatible with previous Intellec Systems

The Intellec Series II Model 220 is a complete microcomputer development system integrated into one compact package. It includes a CPU with 32K bytes of RAM memory, 4K bytes of ROM memory, a 2000-character CRT, detachable full ASCII keyboard with cursor controls and upper/lower case capability, and a 250K-byte floppy diskette drive.

Powerful ISIS-II Diskette Operating System software allows the Model 220 to be used quickly and efficiently for assembly and debugging of programs for Intel's MCS-80, MCS-85 or MCS-48 microprocessor families without the need for handling paper tape. ISIS-II performs all file handling operations for the user, leaving him free to concentrate on the details of his own application. When used in conjunction with an optional in-circuit emulator (ICE™) module, the Model 220 provides all the hardware and software development tools necessary for the rapid development of a microcomputer based product.

MODEL 220 HARDWARE DESCRIPTION

The Intellec Series II Model 220 is a packaged, highly integrated microcomputer development system consisting of a CRT chassis with 6-slot cardcage, power supply, fans, cables, single floppy diskette drive and two printed circuit cards. A separate, full ASCII keyboard is connected with a cable. The master CPU card contains its own microprocessor, memory, I/O, interrupt and bus interface circuitry, fashioned from Intel's high-technology LSI components. Known as the integrated processor board (IPB), it occupies the first slot in the cardcage. A second, slave CPU card, is responsible for all remaining I/O control, including the CRT and keyboard interface and floppy disk control. This card, mounted on the rear panel, also contains its own microprocessor, RAM and ROM memory and I/O interface, thus in effect creating a dual processor environment. Known as the I/O controller (IOC), the slave CPU card communicates with the IPB over an 8-bit bidirectional data bus, thus leaving the remaining 5 slots in the cardcage available for system expansion.

The heart of the IPB is an Intel NMOS 8-bit microprocessor, the 8080A-2, running at 2.6 MHz. 32K bytes of RAM memory are provided on the board using Intel 16K RAMs. 4K of ROM is provided, preprogrammed with system bootstrap, "self-test" diagnostics and the Intellec Series II System Monitor. The 8-level vectored priority interrupt system allows interrupts to be individually masked. Using Intel's versatile 8259 interrupt controller, the interrupt system may be user-programmed to respond to individual needs.

The I/O subsystem in the Model 220 consists of two parts: the IOC card and two serial channels on the IPB itself. Each serial channel is RS232 compatible and is capable of running asynchronously from 110 to 9600 baud or synchronously from 150 to 56K baud. Both may be connected to a user-defined data set or data terminal. One channel contains current loop adapters. Both channels are implemented using Intel's 8251 USART. They can be programmatically selected to perform a variety of I/O functions. Baud rate selection is accomplished programmatically through an Intel 8253 Interval Timer. The 8253 also serves as a real-time clock for the entire system. I/O activity through both serial channels is signaled to the system through a second 8259 interrupt controller, operating in a polled mode, nested to the primary 8259.

The remainder of system I/O activity takes place in the IOC. The IOC provides interfaces for the CRT, keyboard, integral floppy disk and standard Intellec peripherals, including printer, high-speed paper tape reader/punch and Universal PROM Programmer.The IOC contains its own independent microprocessor, also an 8080A-2. This CPU controls all I/O operations, as well as supervising communications with the IPB. 8K bytes of ROM contain all I/O control firmware. 8K bytes of RAM are used for CRT screen refresh storage and the floppy disk buffer. These do not occupy any space in Intellec Series II main memory since the IOC is a totally independent microcomputer subsystem.

The CRT is a 12-inch raster scan-type monitor with a 50/60 Hz vertical scan rate and 15.5 kHz horizontal scan rate. Controls are provided for brightness and contrast adjustments. The interface to the CRT is provided through an Intel 8275 single-chip, programmable CRT controller. The master processor on the IPB transfers a character for display to the IOC, where it is stored in RAM. The CRT controller reads a line at a time into its line buffer through an Intel 8257 DMA Controller and then feeds one character at a time to the character generator to produce the video signal. Timing for the CRT control is provided by an Intel 8253 Interval Timer. The screen display is formatted as 25 rows of 80 characters. The full set of ASCII characters are displayed, including lower-case alphas.

The keyboard interfaces directly to the IOC processor via an 8-bit data bus. The keyboard contains an Intel UPI-41 Universal Peripheral Interface which scans the keyboard, encodes the characters and buffers the characters to provide N-key rollover. The keyboard itself is a high quality typewriter-style keyboard containing the full ASCII character set. An upper/lower case switch allows the system to be used for document preparation. Cursor control keys are also provided.

The floppy disk drive is controlled by an Intel 8271 single-chip, programmable floppy disk controller. It transfers data via an Intel 8257 DMA Controller between an IOC RAM buffer and the diskette. The 8271 handles reading and writing of data, formatting diskettes and reading status, all upon appropriate commands from the IOC microprocessor.

A UPI-41 Universal Peripheral Interface on the IOC board performs similar functions to the UPI-41 on the PIO board in the Model 210. It provides interface for other standard Intellec peripherals, including:

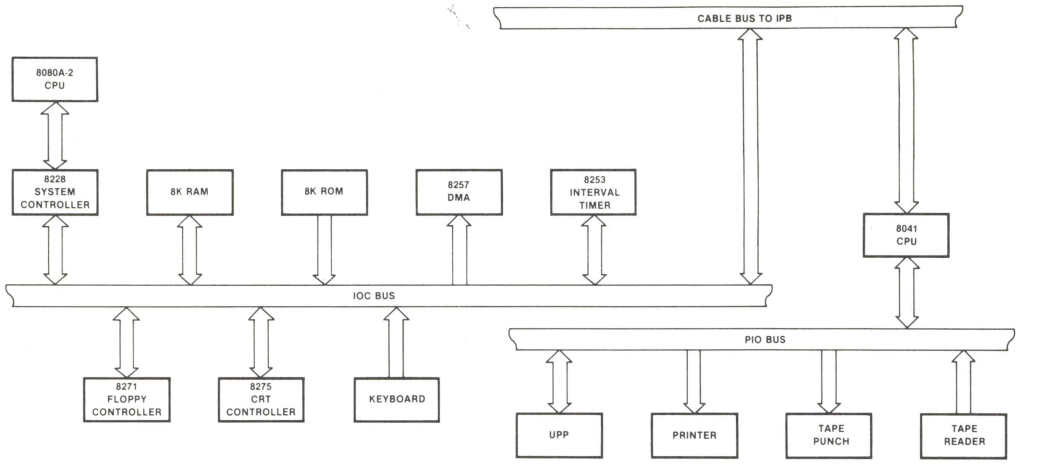
- Printer
- High-Speed Paper Tape Reader
- High-Speed Paper Tape Punch
- Universal PROM Programmer

Communication between the IPB and IOC is maintained over a separate, 8-bit bidirectional data bus. Connectors for the devices named above, as well as the two serial channels, are mounted directly on the IOC itself.

User control is maintained through a front panel consisting of a power switch and indicator, reset/boot switch, run/halt light, and 8 interrupt switches and indicators. The front-panel circuit board is attached directly to the IPB, allowing the 8 interrupt switches to connect to the primary 8259, as well as the Intellec Series II Bus.

All Intellec Series II models implement the industry-standard MULTIBUS. It enables several bus masters, such as CPU and DMA devices, to share the bus and memory by operating at different priority levels. Resolution of bus exchanges is synchronized by a bus clock signal which is derived independently from processor clocks. Read/write transfers may take place at rates up to 5 MHz. The bus structure is suitable for use with any Intel microcomputer family.

The Model 220 may be expanded to 64K of RAM and up to 2¼ million bytes of on-line diskette storage.



I/O CONTROLLER (IOC)

SPECIFICATIONS

PHYSICAL

Dimensions: 19.13" (48.59 cm) deep × 17.37" (44.12 cm) wide × 15.81" (40.16 cm) high

Weight: 86 lb (39 kg)

Keyboard: 9" (22 cm) deep × 17.37" (44.12 cm) wide × 3.0" (7.62 cm) high

Weight: 6 lb (3 kg)

ELECTRICAL

DC Power Supply:

Volts Supplied	Amps Supplied	Typical System Requirements
+ 5 ±5%	30	7.5
+12 ±5%	2.5	0.2
−12 ±5%	0.3	0.05
−10 ±5%	1.5	0.15
+15 ±5%	1.5	1.3*
+24 ±5%	1.7	1.2*

*Not available on bus.

AC Requirements: 50-60 Hz, 115/230 VAC

ENVIRONMENTAL

Operating Temperature: 0° to 35°C (95°F)

HOST PROCESSOR (IPB)

8080A-2 based, operating at 2.600 MHz.

RAM: 32K, expandable to 64K with SBC-032 RAM boards (System Monitor occupies 62K through 64K).

ROM: 4K (2K in monitor, 2K in boot/diagnostic).

Bus: MULTIBUS, maximum transfer rate of 5 MHz.

Clocks: Host Processor, crystal controlled at 2.6 MHz. Bus Clock, crystal controlled at 9.8304 MHz.

I/O Interfaces:

2 Serial I/O Channels, RS232C, at 110-9600 baud (asynchronous) or 150-56K baud (synchronous). Baud rates and serial format fully programmable using Intel 8251 USARTs. Serial Channel 1 additionally provided with 20 mA current loop.

Parallel I/O interfaces provided for paper tape punch, paper tape reader, printer, and Universal PROM Programmer.

Interrupts:

8-level, maskable, nested priority interrupt network initiated from front panel or user-selected devces.

Direct Memory Access (DMA):

Standard capability on MULTIBUS; implemented for user-selected DMA devices through optional DMA module — maximum transfer rate of 2 MHz.

Memory Access Time:

RAM: 585 ns
PROM: 450 ns

Diskette System Capacity: 250K bytes (Formatted)

Diskette Performance:

Diskette System Transfer Rate: 160K bits/sec.

Diskette System Access Time:

Track-to-Track: 10 ms
Average Random Positioning: 260 ms
Rotational Speed: 360 rpm
Average Rotational Latency: 83 ms
Recording Mode: FM

EQUIPMENT SUPPLIED

Model 220 Chassis
Integrated Processor Board (IPB)
I/O Controller Board (IOC)
CRT and Keyboard
250K-byte Floppy Disk Drive
ROM Resident System Monitor
ISIS-II System Diskette with MCS-80/MCS-85 Macro Assembler
A Guide to Microcomputer Development Systems (9800558)
Installation and Service Guide (9800559)
ISIS-II System User's Guide (9800306)
Hardware Reference Manual (9800556)
Hardware Interface Manual (9800555)
8080/8085 Assembly Language Programming Manual (9800301)
ISIS-II 8080/8085 Assembler Operator's Manual (9800692)
Monitor Source Listing (9800605)
Schematic Drawings (9800554)

ORDERING INFORMATION

PRODUCT CODE	DESCRIPTION
MDS-220	Intellec Series II Model 220 Microcomputer Development System (110V/60 Hz)
MDS-221	Intellec Series II Model 220 Microcomputer Development System (220V/50 Hz)

MODEL 230
INTELLEC® SERIES II
MICROCOMPUTER DEVELOPMENT SYSTEM

Complete Microcomputer Development Center for Intel MCS-80™, MCS-85™ and MCS-48™ microprocessor families

Integral CRT with detachable upper/lower case "typewriter-style " full ASCII keyboard

64K bytes RAM memory

1 million bytes (expandable to 2.5M bytes) of diskette storage

LSI electronics board with CPU, RAM, ROM, I/O and interrupt circuitry

Built-in interfaces for High-Speed Paper Tape Reader/Punch, Printer and Universal PROM Programmer

Powerful ISIS-II Diskette Operating System Software with Relocating Macro Assembler, Linker and Locater

"Self-Test" Diagnostic capability

Standard MULTIBUS™ with multiprocessor and DMA capability

Eight-level nested, maskable priority interrupt system

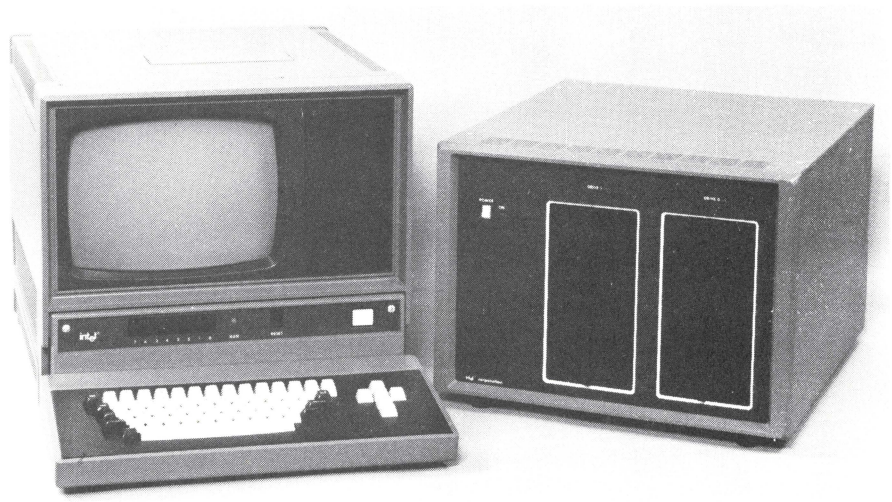
Compatible with standard Intellec/iSBC Expansion Modules

Software compatible with previous Intellec Systems

Supports PL/M and FORTRAN high level languages

The Intellec Series II Model 230 Microcomputer Development System is a complete center for the development of microcomputer-based products. It includes a CPU, 64K bytes of RAM, 4K bytes of ROM memory, a 2000-character CRT, detachable full ASCII keyboard and dual double-density diskette drives providing over 1 million bytes of on-line data storage.

Powerful ISIS-II Diskette Operating System software allows the Model 230 to be used quickly and efficiently for assembly and/or compilation and debugging of programs for Intel's MCS-80, MCS-85 or MCS-48 microprocessor families without the need for handling paper tape. ISIS-II performs all file handling operations for the user, leaving him free to concentrate on the details of his own application. When used in conjunction with an optional in-circuit emulator (ICE™) module, the Model 230 provides all the hardware and software development tools necessary for the rapid development of a microcomputer-based product.



MODEL 230 HARDWARE DESCRIPTION

The Intellec Series II Model 230 is a packaged, highly integrated microcomputer development system consisting of a CRT chassis with 6-slot cardcage, power supply, fans, cables, and five printed circuit cards. A separate, full ASCII keyboard is connected with a cable. A second chassis contains two floppy disk drives capable of double-density operation along with a separate power supply, fans and cables for connection to the main chassis.

The master CPU card contains its own microprocessor, memory, I/O, interrupt and bus interface circuitry fashioned from Intel's high technology LSI components. Known as the integrated processor board (IPB), it occupies the first slot in the cardcage. A second slave CPU card is responsible for all remaining I/O control including the CRT and keyboard interface. This card, mounted on the rear panel, also contains its own microprocessor, RAM and ROM memory, and I/O interface logic, thus, in effect, creating a dual processor environment. Known as the I/O controller (IOC), the slave CPU card communicates with the IPB over an 8-bit bidirectional data bus. In addition, 32K bytes of RAM (bringing the total to 64K bytes) is located on a separate card in the main cardcage. Fabricated from Intel's 16K RAMs, the board also contains all necessary address decoding and refresh logic. Two additional boards in the cardcage are used to control the two double-density floppy disk drives. Two remaining slots in the cardcage are available for system expansion. Additional expansion of 4 slots can be achieved through the addition of an Intellec Series II Expansion Chassis.

The heart of the IPB is an Intel NMOS 8-bit microprocessor, the 8080A-2, running at 2.6 MHz. 32K bytes of RAM memory are provided on the board using Intel 16K RAMs. 4K of ROM is provided, preprogrammed with system bootstrap, "self-test" diagnostics and the Intellec Series II System Monitor. The 8-level vectored priority interrupt system allows interrupts to be individually masked. Using Intel's versatile 8259 Interrupt Controller, the interrupt system may be user programmed to respond to individual needs.

The I/O subsystem in the Model 230 consists of two parts: the IOC card and two serial channels on the IPB itself. Each serial channel is RS232 compatible and is capable of running asynchronously from 110 to 9600 baud or synchronously from 150 to 56K baud. Both may be connected to a user-defined data set or terminal. One channel contains current loop adapters. Both channels are implemented using Intel's 8251 USART. They can be programmatically selected to perform a variety of I/O functions. Baud rate selection is accomplished programmatically through an Intel 8253 Interval Timer. The 8253 also serves as a real-time clock for the entire system. I/O activity through both serial channels is signaled to the system through a second 8259 interrupt controller, operating in a polled mode nested to the primary 8259.

The remainder of system I/O activity takes place in the IOC. The IOC provides interface for the CRT, keyboard, and standard Intellec peripherals including printer, high-speed paper tape reader/punch and Universal PROM Programmer. The IOC contains its own independent microprocessor, also an 8080A-2. The CPU controls all I/O operations as well as supervising communications with the IPB. 8K bytes of ROM contain all I/O control firmware. 8K bytes of RAM are used for CRT screen refresh storage. These do not occupy space in Intellec Series II main memory since the IOC is a totally independent microcomputer subsystem.

The CRT is a 12-inch raster scan type monitor with a 50/60 Hz vertical scan rate and 15.5 kHz horizontal scan rate. Controls are provided for brightness and contrast adjustments. The interface to the CRT is provided through an Intel 8275 Single Chip Programmable CRT Controller. The master processor on the IPB transfers a character for display to the IOC, where it is stored in RAM. The CRT controller reads a line at a time into its line buffer through an Intel 8257 DMA Controller and then feeds one character at a time to the character generator to produce the video signal. Timing for the CRT control is provided by an Intel 8253 Interval Timer. The screen display is formatted as 25 rows of 80 characters. The full set of ASCII characters are displayed, including lower case alphas.

The keyboard interfaces directly to the IOC processor via an 8-bit data bus. The keyboard contains an Intel UPI-41 Universal Peripheral Interface which scans the keyboard, encodes the characters and buffers the characters to provide N-key rollover. The keyboard itself is a high quality typewriter style keyboard containing the full ASCII character set. An upper/lower case switch allows the system to be used for document preparation. Cursor control keys are also provided.

A UPI-41 Universal Peripheral Interface on the IOC board performs similar functions to the UPI-41 on the PIO board in the Model 210. It provides interface for other standard Intellec peripherals including:

- Printer
- High-Speed Paper Tape Reader
- High-Speed Paper Tape Punch
- Universal PROM Programmer

Communication between the IPB and IOC is maintained over a separate 8-bit bidirectional data bus. Connectors for the 4 devices named above, as well as the two serial channels, are mounted directly on the IOC itself.

User control is maintained through a front panel, consisting of a power switch and indicator, reset/boot switch, run/halt light and 8 interrupt switches and indicators. The front panel circuit board is attached directly to the IPB, allowing the 8 interrupt switches to connect to the primary 8259, as well as the Intellec Series II Bus.

The Intellec Series II double-density diskette system provides direct access bulk storage, intelligent controller, and two diskette drives. Each drive provides 1/2 million bytes of storage with a data transfer rate of 500,000 bits/second. The controller is implemented with Intel's powerful Series 3000 Bipolar Microcomputer Set. The controller provides an interface to the Intellec Series II system bus, as well as supporting up to four diskette drives. The diskette system records all data in soft sector format.

The diskette controller consists of two boards, the Channel Board and the Interface Board. These two PC boards reside in the Intellec Series II system chassis and constitute the diskette controller.

The Channel Board receives, decodes and responds to channel commands from the 8080A-2 CPU in the Model 230. The Interface Board provides the diskette controller with a means of communication with the diskette drives and with the Intellec system bus. The Interface Board validates data during reads using a cyclic redundancy check (CRC) polynomial and generates CRC data during write operations. When the diskette controller requires access to Intellec system memory, the Interface Board requests and maintains DMA master control of the system bus, and generates the appropriate memory command. The Interface Board also acknowledges I/O commands as required by the Intellec bus.

The diskette system is capable of performing seven different operations: recalibrate, seek, format track, write data, write deleted data, read data, and verify CRC.

In addition to supporting a second set of double-density drives, the diskette controller may co-reside with the Intel single density controller to allow up to 2.5 million bytes of on-line storage.

All Intellec Series II models implement the industry standard MULTIBUS. It enables several bus masters such as CPU and DMA devices to share the bus and memory by operating at different priority levels. Resolution of bus exchanges is synchronized by a bus clock signal which is derived independently from processor clocks. Read/write transfers may take place at rates up to 5 MHz. The bus structure is suitable for use with any Intel microcomputer family.

SPECIFICATIONS

PHYSICAL

Dimensions:	19.13" (48.59 cm) deep × 17.37" (44.12 cm) wide × 15.81" (40.16 cm) high
Weight:	73 lb (33 Kg)
Keyboard:	9" (22.86 cm) deep × 17.37" (44.12 cm) wide × 3.0" (7.62 cm) high
Weight:	6 lb (3 Kg)
Dual Drive Chassis:	19.0" (48.26 cm) deep × 16.88" (42.88 cm) wide × 12.08" (30.68 cm) high
Weight:	64 lb (29 Kg)

ELECTRICAL

DC Power Supply:

	Volts Supplied	Amps Supplied	Typical System Requirements
	+5 ±5%	30	14.25
	+12 ±5%	2.5	0.2
	−12 ±5%	0.3	0.05
	−10 ±5%	1.5	15
*	+15 ±5%	1.5	1.3
*	+24 ±5%	1.7	

*Not available on bus.

AC Requirements: 50/60 Hz, 115/230 VAC

ENVIRONMENTAL

Operating Temperature: 0° to 35°C (95°F)

HOST PROCESSOR (IPB)

RAM: 64K (System Monitor occupies 62K through 64K).

ROM: 4K (2K in monitor, 2K in boot/diagnostic).

Diskette System Capacity (Basic Two Drives):

- Unformatted
  - Per Disk: 6.2 megabits
  - Per Track: 82.0 kilobits
- Formatted
  - Per Disk: 4.1 megabits
  - Per Track: 53.2 kilobits

Diskette Performance:

- Diskette System Transfer Rate: 500 kilobits/sec
- Diskette System Access Time
  - Track-to-Track: 10 ms
  - Head Settling Time: 10 ms
- Average Random Positioning Time: 260 ms
- Rotational Speed: 360 rpm
- Average Rotational Latency: 83 ms
- Recording Mode: M^2FM

EQUIPMENT SUPPLIED

Model 230 Chassis
Integrated Processor Board (IPB)
I/O Controller Board (IOC)
32K RAM Board
CRT and Keyboard
Double-Density Floppy Disk Controller (2 boards)
Dual-Drive Floppy Disk Chassis and Cables
2 Floppy Disk Drives (512K byte capacity each)
ROM-Resident System Monitor
ISIS-II System Diskette with MCS-80/MCS-85 Macro Assembler
A Guide to Microcomputer Development Systems (9800558)
Installation and Service Guide (9800550)
ISIS-II System User's Guide (9800306)
Hardware Reference Manual (9800556)
Hardware Interface Manual (9800555)
8080/8085 Assembly Language Programming Manual (9800301)
ISIS-II 8080/8085 Assembler Operator's Manual (9800292)
Monitor Source Listing (9800605)
Schematic Drawings (9800554)

ORDERING INFORMATION

PRODUCT CODE	DESCRIPTION
MDS-230	Intellec Series II Model 230 Microcomputer Development System (110V/60 Hz)
MDS-231	Intellec Series II Model 230 Microcomputer Development System (220V/50 Hz)

EXPANSION CHASSIS
INTELLEC® SERIES II
MICROCOMPUTER DEVELOPMENT SYSTEM

Four expansion slots for Intellec Series II Systems

Internal power supply

Fits snugly beneath all Intellec Series II Units

Cable connectable to main Intellec bus

Standard Intellec MULTIBUS™ with multiprocessor and DMA capability

Compatible with standard Intellec/iSBC Expansion Modules

The Intellec Series II Expansion Chassis provides 4 expansion slots for use with Intellec Series II Microcomputer Development Systems. With its own separate power supply, the expansion chassis may be fully loaded with any boards needed to expand a user's Intellec Series II System. With the addition of the expansion chassis, Intellec Series II Models 220 and 230 contain a total of 10 slots, sufficient for any configuration Intellec Series II system.

EXPANSION CHASSIS HARDWARE DESCRIPTION

The Intellec Series II Expansion Chassis is a compact chassis with 4-slot cardcage, power supply, fans and cable assemblies. It is designed to fit under any Intellec Series II System, connect directly to the system bus through an opening in the top of the chassis and provide additional slots for the system users.

The power supply is linked directly to the main chassis power supply, allowing power to flow to both chassis when the main system power is turned on.

SPECIFICATIONS

PHYSICAL

Dimensions: 19.13" (48.59 cm) deep × 17.37" (44.12 cm) wide × 4.81" (17.22 cm) high

Weight: 42 lb (19 Kg)

ELECTRICAL

DC Power Supply:

Volts Supplied	Amps Supplied	System Requirements
+5 ±5%	24	None
+12 ±5%	2.0	None
−12 ±5%	0.3	None
−10 ±5%	1.0	None

AC Requirements: 50–60 Hz, 115/230 VAC

ENVIRONMENTAL

Operating Temperature: 0° to 35°C (95°F)

EQUIPMENT SUPPLIED

Expansion Chassis
Cables
Interconnect Diagram
Schematic Drawings (9800554)
Installation and Service Guide (9800550)

ORDERING INFORMATION

PRODUCT CODE	DESCRIPTION
MDS-201	Intellec Series II Expansion Chassis

MODEL 210 ENHANCEMENT KIT INTELLEC® SERIES II MICROCOMPUTER DEVELOPMENT SYSTEM

Upgrades Model 210 System to Model 220 capability

Converts Model 210 chassis to MDS-201 expansion chassis

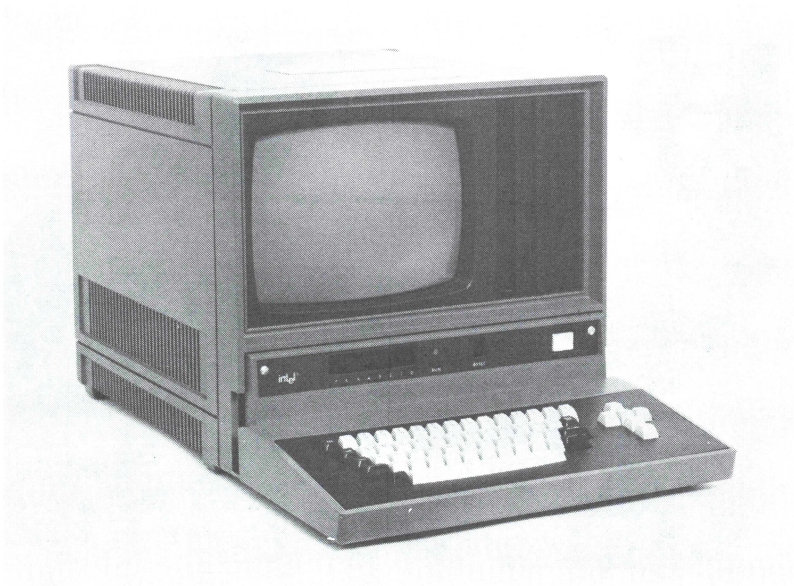
Includes full Model 220 capability including integral CRT and floppy disk

Eliminates the need to purchase an entire new system as development requirements increase

The Intellec® Series II Microcomputer Development System Enhancement Kit provides an easy, cost-effective way to expand the capability of a Model 210 system to the Model 220 level. The package includes a Model 220 chassis without the integrated processor board. The user simply removes the IPB from his Model 210, inserts it into his Model 220 chassis and is ready to go. The Model 210 chassis may then be used as an expansion chassis with the conversion kit provided in the upgrade package.

ORDERING INFORMATION

PRODUCT CODE	DESCRIPTION
MDS-217	Intellec Series II Model 210 Enhancement Kit (110V/60 Hz)
MDS-218	Intellec Series II Model 210 Enhancement Kit (220V/50 Hz)



MODEL 770 PRINTER
INTELLEC® SERIES II
MICROCOMPUTER DEVELOPMENT SYSTEM

Low-cost, hard-copy printer for CRT-based systems

Prints original plus 4 copies

Prints 60 cps (21-90 lines per minute)

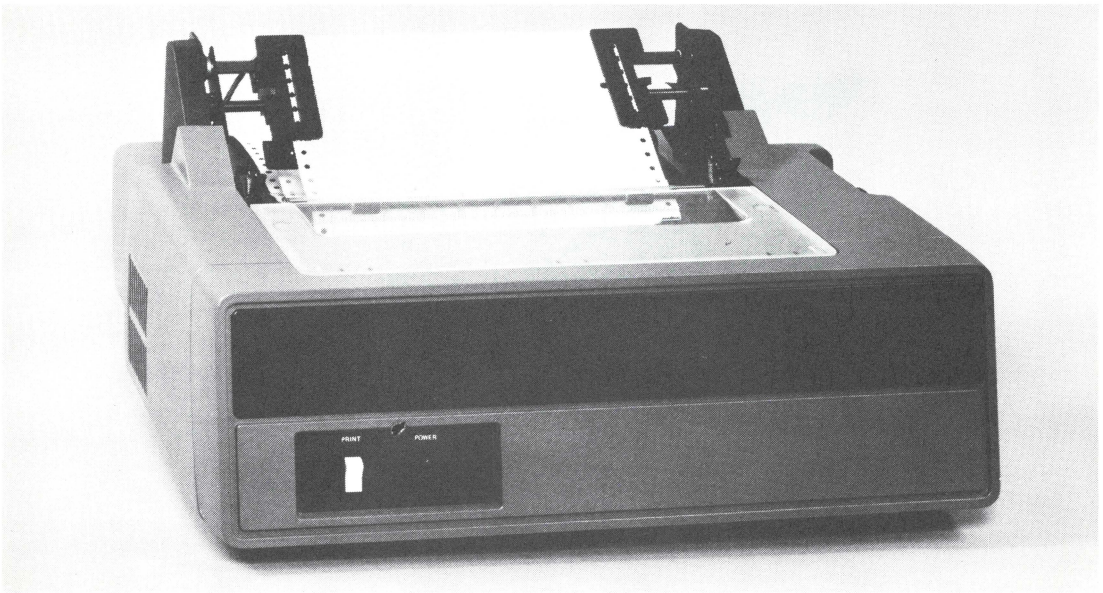
5 x 7 dot matrix character format

Tractor feed (rear or bottom feed)

Line width adjustable from 80 to 132 columns on 8½″ line

The Model 770 Printer is a low-cost, hard-copy printer designed for use with CRT-based Intellec Series II and Intellec Microcomputer Development Systems. Unidirectional printing at 60 cps makes the Model 770 an ideal printer for the microcomputer-based system designers with small-to-medium printing requirements. The 8½″ line width may be filled with 80 to 132 characters by varying the character size.

The printer uses standard fanfold paper through a tractor-feed mechanism to produce an original and up to four copies. Paper can be fed from the bottom or rear of the printer for versatility in any lab environment.



SPECIFICATIONS

PRINTING METHOD
Impact, character-by-character printing, one line character buffer.

PRINTING RATE
Characters: 60 characters per second.
Full Lines: 21 @ 80 characters/line.
90 @ 20 characters/line.

TRANSMISSION RATE
Parallel: Up to 75,000 characters per second.

CHARACTER STRUCTURE
5 × 7 dot matrix, 10 point type equivalent.

CODE
USASCII: 64 characters printed.

SWITCH CONTROLS
On-Off

INDICATORS
Paper Out

FORMAT
80 to 132 characters per line, variable.
10 to 165 characters per inch, operator adjustable.
6 lines per inch.

PAPER FEED
Tractor Feed: 5.5 ips slew.

PAPER
Standard sprocketed paper, 8½" to 9½" paper width.

NUMBER OF COPIES
Original plus up to four carbon copies.

DIMENSIONS
18" (45.7 cm) deep × 24.5" (62.2 cm) wide × 7" (17.8 cm) high

WEIGHT
60 lb (27 Kg)

ELECTRICAL REQUIREMENTS
50 – 60 Hz, 110/230 VAC ± 10%

TEMPERATURE
Operating: −40° to 100°F (5° to 40°C).
Storage: −40° to 160°F (−40° to 50°C).

HUMIDITY
Operating: 5% to 90% (no condensation).
Storage: 0% to 95% (no condensation).

ORDERING INFORMATION

PRODUCT CODE	DESCRIPTION
MDS-770	60 CPS Printer (110V/60 Hz)
MDS-771	60 CPS Printer (220V/50 Hz)

SYSTEM MONITOR
INTELLEC® SERIES II
MICROCOMPUTER DEVELOPMENT SYSTEM

Rom resident

I/O Interface Software Drivers for

- **TTY**
- **CRT**
- **High-Speed Paper Tape Reader**
- **High-Speed Paper Tape Punch**
- **Line/Character Printer**
- **Universal PROM Programmer**

Expandable I/O system allows easy inclusion of user-supplied device drivers

Bootstrap logic for all Intellec Series II Systems

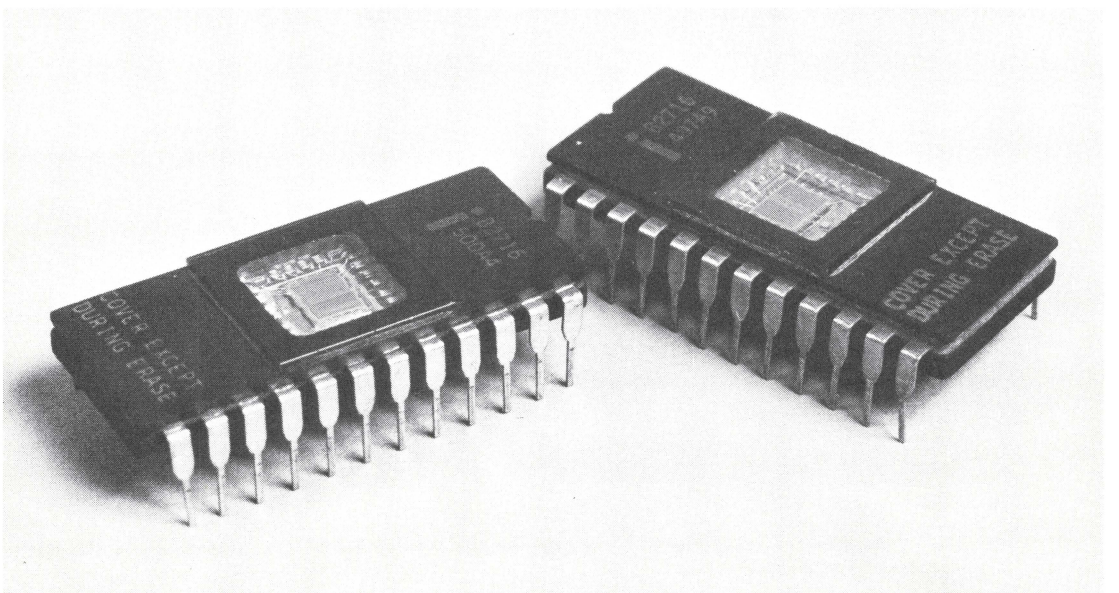
Self-Test Diagnostic for Intellec CPU and RAM memory

Occupies only 2K bytes of Intellec memory address space

Full Debug capability for Intellec resident program development

Commands for paper tape oriented system I/O

The Intellec Series II System Monitor is an 8080A program which provides basic control functions for all Intellec Series II Systems. These include bootstrap logic, system diagnostics, the I/O system, user interface logic for non-disk-based systems and complete debug and paper tape I/O commands.



The system monitor occupies 4K bytes of 8080A memory, although it only uses 2K bytes of Intellec Series II memory space. The remaining 2K bytes of memory contain bootstrap and diagnostic code and are "shadowed" (executed only upon system reset and then disabled in favor of RAM memory present at the same locations).

Upon system reset, the hardware enables the 2K code segment containing bootstrap and diagnostic logic, and forces a jump to the starting location. The bootstrap then determines if a diskette drive is present and ready, and transfers control either to the system monitor or ISIS-II diskette operating system. The bootstrap and diagnostic code segment is then disabled and removed from 8080A memory space.

The monitor accepts and executes user commands. These commands include:

- read paper tape into memory
- punch memory to paper tape
- execute programs in memory with breakpoints
- display/modify memory and CPU registers
- fill memory with a constant
- hexadecimal arithmetic
- execute user diagnostics

Together these commands provide powerful program loading and debug facilities for the non-disk-based user.

The monitor also provides a comprehensive I/O system, including drivers for all standard Intellec Series II devices, as well as linkage mechanism for easy inclusion of non-standard I/O devices. The monitor recognizes 4 logical I/O devices — a reader device, punch device, console device and list device.

Each logical device may be assigned to any one of 4 physical I/O devices by means of a monitor command. Device drivers are provided for each standard Intellec peripheral which may be selected by user command. Non-standard devices may be used by "linking" drivers through known absolute memory locations. The system is designed to operate, at a minimum, with a TTY as its sole I/O device.

ROM EDITOR / ASSEMBLER INTELLEC® SERIES II MICROCOMPUTER DEVELOPMENT SYSTEM

Reduces or eliminates paper tape handling for Model 210 users

Available in both MCS-80/MCS-85™ and MCS-48™ family versions

Provides total RAM-based program development capability for small programs

Assemblers offer optional cross reference listing

Editor provides powerful text entry and correction commands including String Search and Substitution

Assemblers accept standard Intel Assembly Language subset

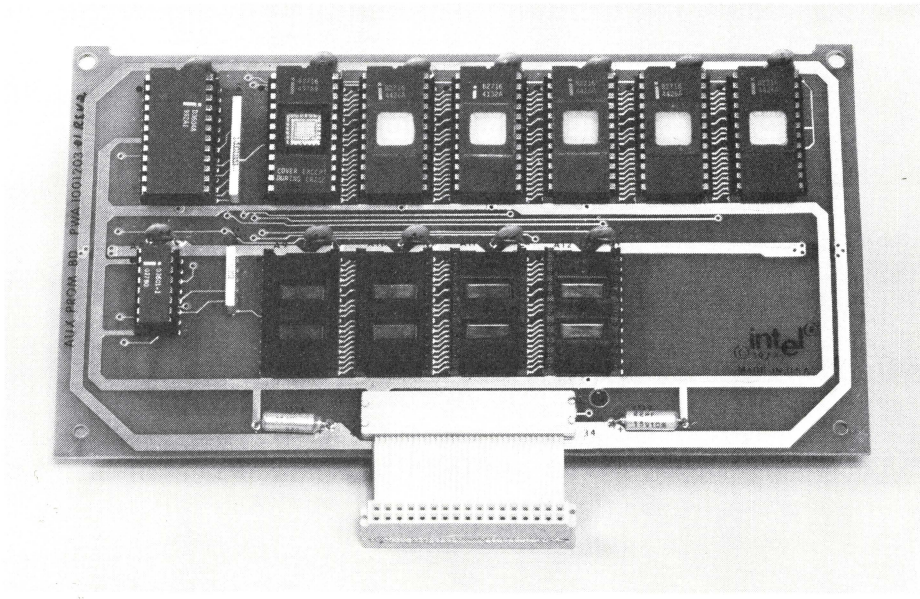
Assemblers produce absolute code for immediate execution or PROM programming

The ROM-based Editor/Assemblers for the Intellec Series II Model 210 Microcomputer Development System provide a rapid, efficient means of software development on Model 210 Systems by minimizing the handling of paper tape. The editor and assemblers may be invoked instantaneously by monitor command. Source code entered into the editor is stored in available RAM memory for easy modification. When editing is complete, the assemblers will assemble directly from RAM as long as source code size, symbol table size or object code size do not exceed available RAM storage. If they do, source code may be punched to paper tape and then re-read by the assembler. Object code produced by the assembler may be left in RAM memory for immediate execution or burned into an erasable PROM for execution in your prototype system. An optional, paper tape-based, cross reference program is provided to list the line numbers on which each symbol is referenced.

The ROM Editor/Assemblers are each provided on a printed circuit card designed to plug directly into the Intellec Series II's integrated processor board. Thus they do not use a slot in the system cardcage. The assembler/editor occupies 20K bytes of memory space, immediately below the monitor, starting at location B800 hexadecimal. All remaining memory space is available for RAM memory.

ORDERING INFORMATION

PRODUCT CODE	DESCRIPTION
	ROM Editor/Assembler for MCS-80/MCS-85 (Standard with Intellec Series II Model 210)
MDS-R48	ROM Editor/Assembler for MCS-48 Family of Microprocessors



MPU SYSTEM SUPPORT

ISIS-II
DISKETTE OPERATING SYSTEM
MICROCOMPUTER DEVELOPMENT SYSTEM

Supports up to four double density drives and two single density drives, providing up to 2.5 Megabytes of storage in one system with up to 200 files per diskette

Supports resident, high level programming languages, PL/M and FORTRAN

Relocating MCS-80/MCS-85™ macro assembler contains extended macro and conditional assembly capability

Linker automatically combines separately assembled or compiled programs into a single relocatable module

Library Manager™ creates and updates program libraries

Command file facility allows console commands to be submitted from a diskette file

Diskette system text editor provides string search, substitution, insertions, and deletion commands

Diskette operating system functions are callable from user programs

Access to all Intellec® monitor facilities provided

Dynamic allocation and de-allocation of diskette sectors for variable length files

Supports all standard Intellec® peripherals

The ISIS-II Diskette Operating System is a sophisticated, general purpose, high-speed data handler and file manipulation system. It provides the ability to edit, assemble, compile, link, relocate, execute and debug programs, and performs all file management tasks for the user.

The ISIS-II operating system resides on the system diskette and supports a broad range of user-oriented design aid software. Total file management and input editing features greatly reduce software development time. The ISIS-II Relocating Macro Assembler, Linker, Object Locator and Library Manager can be loaded from the diskette in seconds. All passes of the assembler can be executed without the need for user intervention. Object code and listings may be directed to any output device, or stored as diskette files.

Powerful system console commands are provided in an easy-to-use context. Monitor mode can be entered by a special prefix to any system command or program call.

ISIS-II FILES

A file is a user-defined collection of information of variable length. ISIS-II also treats each of the standard Intellec® system peripherals as files through pre-assignment of unique file names to each device. In this manner data can be copied from one device to another (i.e., tape reader to tape punch) using the same command required to copy one diskette data file to another. ISIS-II provides automatic implementation of random access disk files. Each file is identified by a user-chosen name unique on its diskette. Up to 200 files may be stored on each diskette.

ISIS-II SYSTEM COMMANDS

ISIS-II system commands are designed to provide the user with a powerful, easy-to-use program and file manipulation capability. Several commands have the capability of operating on several files at once via the wildcard file-naming convention. As an example, the command "DELETE ★.OBJ" deletes all files in the diskette directory with the suffix ".OBJ".

IDISK	Initializes a diskette for use by the system. Requires only one disk drive.
ATTRIB	Assigns specified attributes to a file, such as write-protect.
COPY	Creates copies of existing diskette files or transfers files from one device to another.
DELETE	Removes a file from the diskette, thereby freeing space for allocation of other files.
DIR	Lists name, size and attributes of files from a specified diskette directory.
RENAME	Allows diskette files to be renamed.
FORMAT	Initializes a diskette for use by the system. (Use with two or more drives.)
DEBUG	Loads a specified program from a diskette into memory and then transfers control to the Intellec monitor for execution and or debugging.
SUBMIT	Provides the capability to execute a series of ISIS-II commands which have been previously written to a diskette file.

ISIS-II SYSTEM CALL CAPABILITY

The DELETE, RENAME and ATTRIB system commands, along with a set of file I/O routines, are callable from user-written programs. This allows the user to open, close, read and write diskette files, access standard peripheral devices, write error messages and load other programs via simple program call statements.

ISIS-II TEXT EDITOR

The ISIS-II Text Editor is a comprehensive tool for the entry and correction of assembly language, PL/M and FORTRAN programs for Intel® microcomputers. Its command set allows manipulation of either entire lines of text or individual characters within a line.

Programs may be entered from the console keyboard or may be loaded directly. Text is stored internally in the editor's workspace, and may be edited with the following commands:

- string insertion or deletion
- string search
- string substitution

To facilitate the use of these editing commands, utility commands are used to change positions in the workspace. These include:

- move pointer by line or by character
- move pointer to start of workspace
- move pointer to end of workspace

The contents of the workspace are stored on diskette and can be immediately accessed by ISIS-II commands or other programs, such as the ISIS-II MCS-80/MCS-85 Macro Assembler.

ISIS-II MCS-80/MCS-85 RELOCATING MACRO ASSEMBLER

The ISIS-II MCS-80/MCS-85 Macro Assembler translates assembly language mnemonics into relocatable and/or absolute object code modules. In addition to eliminating the errors of hand translation, the ability to refer to program addresses with symbolic names makes it easy to modify programs by adding or deleting instructions. Extended macro capability eliminates the need to rewrite similar sections of code repeatedly and simplifies program documentation. Conditional assembly permits the assembler to include or delete sections of code which may vary from system to system, such as the code required to handle optional external devices.

In addition, the user is allowed complete freedom in assigning the location of code, data and stack segments.

The ISIS-II Assembler accepts diskette file input and produces a relocatable object file with corresponding symbol table and assembly listing file, including any error messages. A cross reference listing is also optionally produced. The list file may then be examined from the system console or copied to a specified list device.

The relocatable object file generated by the assembler may be combined with other object programs residing on the diskette to form a single relocatable object module or it can be converted to an absolute form for subsequent loading and execution.

ISIS-II LINKER

The ISIS-II LINKER provides the capability to combine the outputs of several independently compiled or assembled object modules (files) into a single relocatable object module. The LINKER automatically resolves all external program and data references during the linking process.

Object modules produced from previous link operations may be easily linked to a new module. ISIS-II also provides facilities to ease the generation of overlays.

An optional link map showing the contents and lengths of each segment in the output module can be requested. All unsatisfied external references are also listed.

If requested by the user, the ISIS-II LINKER can search a specified set of program libraries for routines to be included in the output module.

ISIS-II OBJECT LOCATOR

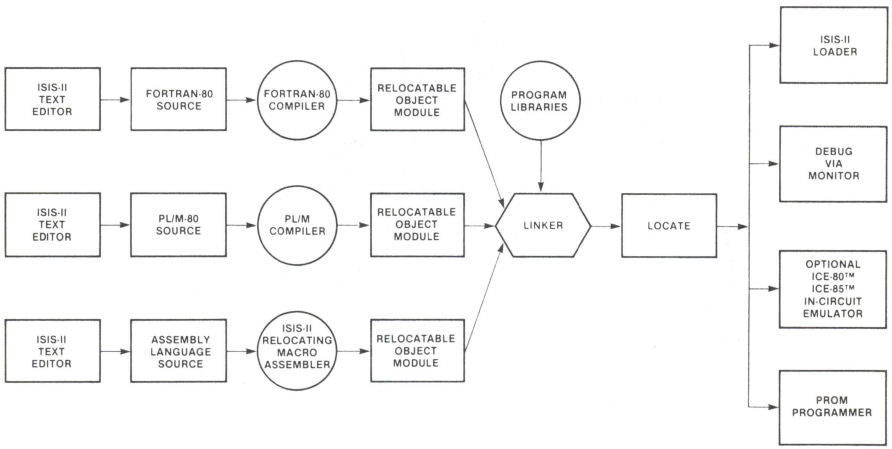
The ISIS-II LOCATE program takes output from either the resident FORTRAN or PL/M compilers, the macro assembler or the LINKER and transforms that output from a relocatable format to an absolute format which may then be loaded via the standard ISIS-II loader, or loaded into the appropriate In-Circuit Emulator (ICE) module.

During the LOCATE process, code, data and stack segments can be *separately* relocated, allowing code to be put in areas to be subsequently specified as ROM, while data and the stack can be directed to RAM addresses.

A LOCATE map showing absolute addresses for each code and data segment and a symbol table dump listing symbols, attributes and absolute address can also be requested.

ISIS-II LIBRARY MANAGER

The ISIS-II LIBRARY MANAGER program provides for the creation and maintenance of a program library containing Intel-provided and user-written programs and subroutines. These library routines can be linked to a program using the ISIS-II LINKER. Several libraries, each containing its own set of routines, can be created.



PROGRAM DEVELOPMENT FLOW USING ISIS-II DISK OPERATING SYSTEM

PL/M-80
HIGH LEVEL PROGRAMMING LANGUAGE
INTELLEC® RESIDENT COMPILER

Cuts software development and maintenance costs

Speeds project completion

Improves product reliability

Eases enhancements as system capabilities expand

Produces relocatable and linkable object code

Resident operation on Intellec® Microcomputer Development System and Intellec® Series II Microcomputer Development Systems

Sophisticated code optimization reduces application memory requirements

PL/M-80 is an advanced, high-level programming language for Intel® 8080 and 8085 Microprocessors, iSBC-80 OEM Computer Systems and Intellec® Microcomputer Development Systems. PL/M has been substantially enhanced since its introduction in 1973 and has become one of the most effective and powerful microprocessor systems implementation tools available. It is easy to learn, facilitates rapid program development and debugging, and significantly reduces maintenance costs.

PL/M is a powerful, high-level algorithmic language in which program statements can naturally express the algorithm to be programmed. This frees programmers to concentrate on their system development without having to deal with assembly language details (such as register allocation, meanings of assembler mnemonics, etc.).

The PL/M compiler efficiently converts free-form PL/M programs into equivalent 8080/8085 instructions. Substantially fewer PL/M statements are necessary for a given application than if it were programmed at the assembly language or machine code level.

Since PL/M programs are problem oriented and more compact, programming in PL/M results in a high degree of productivity during development efforts. This translates into significant reductions in software development and maintenance costs for the user.

FEATURES

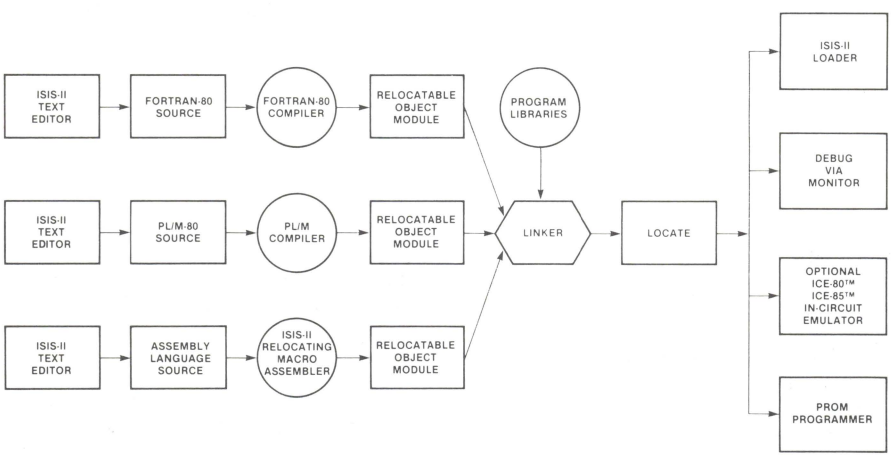
Major features of the Intel PL/M-80 Compiler and programming language include:

- Resident operation on the Intellec® Microcomputer Development System eliminates the need for a large in-house computer or costly timesharing system.
- Generation of relocatable and linkable object code permits PL/M programs to be developed and debugged in small modules. These modules can be easily linked with other modules and/or library routines to form a complete application.
- Extensive code optimization results in generation of short, efficient CPU instruction sequences. Major optimizations include compile time arithmetic, constant subscript resolution, and common subexpression elimination.
- The PL/M Compiler fully supports symbolic debugging with the ICE-80™ and ICE-85™ In-Circuit Emulators.
- Compile time options include general listing format commands, symbol table listing, cross reference listing, and "innerlist" of generated assembly language instructions.
- Block structure aids in utilization of structured programming techniques.
- High level PL/M statements provide access to hardware resources (interrupt systems, absolute addresses, CPU input/output ports).
- Complex data structures may be defined at a high level.
- Re-entrant procedures may be specified as a user option.

BENEFITS

PL/M is designed to be an efficient, cost-effective solution to the special requirements of microcomputer software development as illustrated by the following benefits of PL/M use:

- **Low Learning effort** — PL/M is very easy to learn even for the novice programmer.
- **Earlier Project Completion** — Critical projects are completed much earlier than otherwise possible because PL/M substantially increases programmer productivity.
- **Lower Development Cost** — Increases in programmer productivity translate into lower software development costs because less programming resources are required for a given function.
- **Increased Reliability** — PL/M is designed to assist in the development of reliable software (PL/M programs are simple statements of the program algorithm). This substantially reduces the risk of costly correction of errors in systems that have aleady reached full production status because a simply stated program is more likely to correctly perform its intended function.
- **Easier Enhancements and Maintenance** — Programs written in PL/M are easier to read and easier to understand. This means it is easier to enhance and maintain PL/M programs as system capabilities expand and future products are developed.
- **Simpler Project Development** — The Intellec® Microcomputer Development System, with resident PL/M-80, is all that is needed for development and debugging of software for 8080 and 8085 microcomputers. This reduces development time and cost because expensive (and remote) timesharing or large computers are not required.



The PL/M Compiler is an efficient multiphase compiler that accepts source programs, translates them into object code, and produces requested listings. After compilation, the object program may be linked to other modules, located to a specific area of memory, then executed. The diagram shown above illustrates a program development cycle where the program consists of three modules, one PL/M, one Fortran, and the other assembly language.

```
PL/M-80    COMPILER                FACTORIAL GENERATOR – PROCEDURE

                                   $OBJECT(:F1:FACT.OB2)
                                   $DEBUG
                                   $XREF
                                   $TITLE('FACTORIAL GENERATOR – PROCEDURE')
                                   $PAGEWIDTH(80)

   1                               FACT:
                                   DO;

   2       1                       DECLARE NUMCH BYTE PUBLIC;

   3       1                       FACTORIAL: PROCEDURE (NUM,PTR) PUBLIC;
   4       2                           DECLARE NUM BYTE, PTR ADDRESS;
   5       2                           DECLARE DIGITS BASED PTR (161) BYTE;
   6       2                           DECLARE (I,C,M) BYTE;

   7       2                           NUMCH=1; DIGITS(1)=1;
   9       2                           DO M = 1 TO NUM;
  10       3                               C=0;
  11       3                               DO I = 1 TO NUMCH;
  12       4                                   DIGITS(I) = DIGITS(I) * M + C;
  13       4                                   C = DIGITS(I)/10;
  14       4                                   DIGITS(I) = DIGITS(I) – 10 * C;
  15       4                               END;

  16       3                               IF C <> 0 THEN
  17       3                               DO;
  18       4                                   NUMCH = NUMCH+1;  DIGITS (NUMCH) = C;
  20       4                                   C = DIGITS(NUMCH)/10;
  21       4                                   DIGITS(NUMCH) = DIGITS(NUMCH) – 10 * C;
  22       4                               END
                                       END;

  24       2                       END FACTORIAL;

  25       1                       END;
```

SPECIFICATIONS

Operating Environment:

Required hardware
- Intellec® Microcomputer Development System
- 65K bytes of memory
- Dual diskette drives
- System console — teletype

Optional hardware
- CRT as system console
- Line printer

Required software
- ISIS-II Diskette Operating System

Documentation Package:
- PL/M Programming Manual
- ISIS-II PL/M-80 Compiler Operator's Manual

Shipping Media:
- Diskette

ORDERING INFORMATION

PRODUCT CODE	DESCRIPTION
MDS-PLM	High-Level Language Compiler Resident on Intellec System — Translates a Source Program written in PL/M-80 into 8080/8085 Machine Code

FORTRAN-80
8080/8085 ANS FORTRAN 77
INTELLEC® RESIDENT COMPILER

Meets and exceeds ANS FORTRAN 77 Subset Language Specification

Supports Intel Floating Point Standard

Resident operation on Intellec® Microcomputer Development System and Intellec® Series II Microcomputer Development System

Supports full symbolic debugging with ICE-80™and ICE-85™

Produces relocatable and linkable object code compatible with resident PL/M-80 and 8080/8085 Macro Assembler

Full FORTRAN 77 language I/O support when used with ISIS-II run-time library

Sophisticated code optimization insures efficient program implementation

FORTRAN-80 is a computer industry-standard, high-level programming language and compiler that translates FORTRAN statements into relocatable object modules. When the object modules are linked together and located into absolute program modules, they are suitable for execution on Intel® 8080/8085 Microprocessors, iSBC-80 OEM Computer Systems, and Intellec® Microcomputer Development Systems. FORTRAN-80 meets and exceeds the ANS FORTRAN 77 Language Subset Specification[1]. The compiler operates on the Intellec Microcomputer Development System under the ISIS-II Disk Operating Systems and produces efficient relocatable object modules that are compatible for linkage with PL/M-80 and 8080/8085 Macro Assembler modules.

The ANS FORTRAN 77 language specification offers many powerful extensions to the FORTRAN language that are especially well suited to Intel® 8080/8085 Microprocessor software development. Because FORTRAN-80 conforms to the ANS FORTRAN 77 standard, the user is assured of compatibility with existing FORTRAN software that meets the standard as well as a guarantee of upward compatibility to other computer systems supporting an ANS FORTRAN 77 Compiler.

[1]ANSI X3J3/90

FORTRAN-80 LANGUAGE FEATURES

Major ANS FORTRAN 77 features supported by the Intel® FORTRAN-80 Programming Language include:

- Structured Programming is supported with the IF . . . THEN . . . ELSE IF . . . ELSE . . . END IF constructs.
- CHARACTER data type permits alphanumeric data to be handled as strings rather than characters stored in array elements.
- Full I/O capabilities include:
  - — Sequential and Direct Access files
  - — Error handling facilities
  - — Formatted, Free-formatted, and Unformatted data representation
  - — Internal (in-memory) file units provide capability to format and reformat data in internal memory buffers
  - — List Directed Formatting
- Supports arrays of up to seven dimensions.
- Supports logical operators
  .EQV. — Logical equivalence
  .NEQV. — Logical nonequivalence

Major extensions to FORTRAN 77 in Intel FORTRAN-80 include:

- Direct 8080/8085 port I/O supported by intrinsic subroutines.
- Binary and Hexadecimal integer constants.
- User-defined INTEGER storage lengths of 1, 2 or 4 bytes.
- User-defined LOGICAL storage lengths of 1, 2 or 4 bytes.
- REAL STORAGE lengths of 4 bytes.
- Bitwise Boolean operations using logical operators on integer values.
- Hollerith data constants.
- Implicit extension of the length of an integer or logical expression to the length of the left-hand side in an assignment statement.
- A format descriptor to suppress carriage return on a terminal output device at the end of the record.

FORTRAN-80 COMPILER FEATURES

- Supports multiple compilation units in single source file.
- Optional Assembly Language code listing.
- Comprehensive cross-reference, symbol attribute and error listing.
- Compiler controls and directives are compatible with other Intel language translators.
- Optional Reentrancy.
- User-defined default storage lengths.
- Optional FORTRAN 66 Do Loop semantics.
- Source files may be prepared in free format.
- The INCLUDE control permits specified source files to be combined into a compilation unit at compile time.

FORTRAN-80 BENEFITS

FORTRAN-80 provides a means of developing application software for Intel® MCS-80/85 products in a familiar, widely accepted, and computer industry-standardized programming language. FORTRAN-80 will greatly enhance the user's ability to provide cost-effective solutions to software development for Intel microprocessors as illustrated by the following:

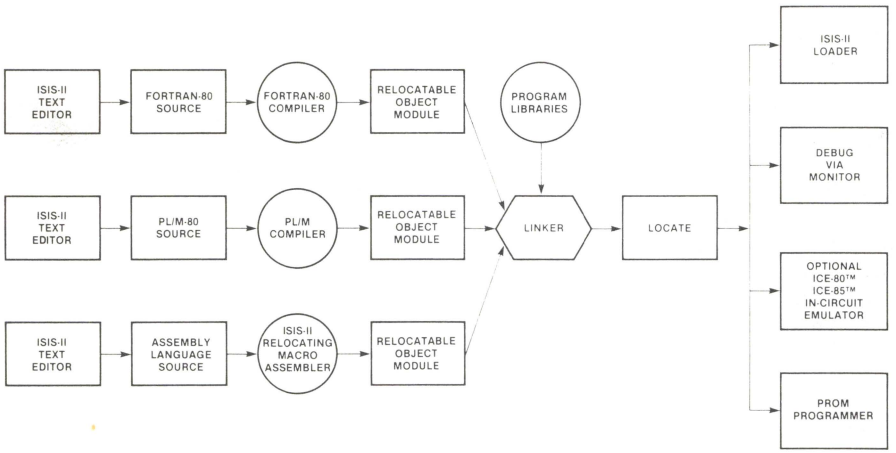
- *Completely Complementary to Existing Intel Software Design Tools* — Object modules are linkable with new or existing Assembly Language and PL/M Modules.
- *Incremental Runtime Library Support* — Runtime overhead is limited only to facilities required by the program.
- *Low Learning Effort* — FORTRAN-80, like PL/M, is easy to learn and use. Existing FORTRAN software can be ported to FORTRAN-80, and programs developed in FORTRAN-80 can be run on any other computer with ANS FORTRAN 77.
- *Earlier Project Completion* — Critical projects are completed earlier than otherwise possible because FORTRAN-80 will substantially increase programmer productivity, and is complementary to PL/M Modules by providing comprehensive arithmetic, I/O formatting, and data management support in the language.
- *Lower Development Cost* — Increases in programmer productivity translates into lower software development costs because less programming resources are required for a given function.
- *Increased Reliability* — The nature of high-level languages, including FORTRAN-80, is that they lend themselves to simple statements of the program algorithm. This substantially reduces the risk of costly errors in systems that have already reached production status.
- *Easier Enhancements and Maintenance* — Like PL/M, program modules written in FORTRAN-80 are easier to read and understand than assembly language. This means it is easier to enhance and maintain FORTRAN-80 programs as system capabilities expand and future products are developed.
- *Comprehensive, Yet Simple Project Development* — The Intellec Microcomputer Development System, with the 8080/8085 Macro Assembler, PL/M-80 and FORTRAN-80 is the most comprehensive software design facility available for the Intel MCS-80/85 Microprocessor family. This reduces development time and cost because expensive (and remote) timesharing or large computers are not required.

SAMPLE FORTRAN-80 SOURCE PROGRAM LISTING

```
C  THIS PROGRAM IS AN EXAMPLE OF ISIS-II FORTRAN-80 THAT
C  CONVERTS TEMPERATURE BETWEEN CELCIUS AND FARENHEIT
C
      PROGRAM CONVRT
      CHARACTER*1 CHOICE,SCALE
      PRINT 1
1     FORMAT (' TEMPERATURE CONVERSION PROGRAM',//,
     *' TYPE C FOR FARENHEIT TO CELCIUS OR',/,
     *' F FOR CELCIUS TO FARENHEIT',//)
10    PRINT 2
2     FORMAT (/,' CONVERSION? ',$)
      READ (5,3) SCALE
3     FORMAT (A1)
      IF (SCALE.EQ.'C') THEN
          PRINT 4
4         FORMAT (/,' ENTER DEGREES FARENHEIT? ',$)
          READ (5,*) DEGF
          DEGC=5./9.*DEGF-32.
          WRITE (6,5) DEGF,DEGC
5         FORMAT (/,F7.2,' DEGREES FARENHEIT = ',F7.2,' DEGREES CELCIUS',/)
11        PRINT 6
6         FORMAT (/,' AGAIN (Y OR N)? ',$)
          READ (5,3) CHOICE
          IF (CHOICE.EQ.'Y') THEN
              GOTO 10
          ELSE IF (CHOICE.EQ.'N') THEN
              CALL EXIT
          ELSE
              GOTO 11
          END IF
      ELSE IF (SCALE.EQ.'F') THEN
          PRINT 7
7         FORMAT (/,' ENTER DEGREES CELCIUS? ',$)
          READ (5,*) DEGC
          DEGF=9./5.*DEGC+32.
          WRITE(6,8) DEGC,DEGF
8         FORMAT (/,F7.2,' DEGREES CELCIUS = ',F7.2,' DEGREES FARENHEIT',/)
          GOTO 11
      ELSE
          WRITE (6,9) SCALE
9         FORMAT (/,1H ,A1,' NOT A VALID CHOICE - RETRY!',/)
          GOTO 10
      END IF
      END
```

FORTRAN-80

The FORTRAN-80 Compiler is an efficient, multiphase compiler that accepts source programs, translates them into relocatable object code, and produces requested listings. After compilation, the object program may be linked to other modules, located to a specific area of memory, then executed. The diagram shown below illustrates a program development cycle where the program consists of modules created by FORTRAN-80, PL/M-80 and the 8080/8085 Macro Assembler.



SPECIFICATIONS

OPERATING ENVIRONMENT

Required Hardware:

- Intellec® Microcomputer Development System
  - — MDS-800, MDS-888
  - — Series II Model 220, Model 230
- 64K bytes of RAM memory
- Dual diskette drives
  - — Single or Double Density
- System console
  - — CRT or hardcopy interactive device

Optional Hardware:

- Line Printer
- ICE-80™, ICE-85™

Required Software:

- ISIS-II Diskette Operating System
  - — Single or Double Density

DOCUMENTATION PACKAGE

FORTRAN-80 Programming Manual (9800481)

ISIS-II FORTRAN-80 Compiler Operator's Manual (9800480)

FORTRAN-80 Programming Reference Card (9800547)

SHIPPING MEDIA

Flexible Diskettes

- — Single and Double Density

ORDERING INFORMATION

PRODUCT CODE	DESCRIPTION
MDS-301	FORTRAN-80 Compiler for Intellec Microcomputer Development Systems

MCS-48™ DISKETTE-BASED SOFTWARE SUPPORT PACKAGE

Extends Intellec® Microcomputer Development System to support MCS-48™ development

Takes advantage of powerful ISIS-II file handling and storage capabilities

MCS-48 Assembler provides conditional assembly and macro capability

The MCS-48™ Diskette-based Software Support Package (MDS-D48) comes on an Intel® ISIS-II System Diskette and contains the MCS-48 Assembler (ASM48), and the diskette version of the Universal PROM Mapper.

The MCS-48 Assembler (ASM48) translates symbolic 8048 assembly language instructions into the appropriate machine operation codes. In addition to eliminating the errors of hand translation, the ability to refer to program addresses with symbolic names makes it easier to modify programs when adding or deleting instructions. Conditional assembly permits the programmer to specify portions of the master source document which should be included or deleted in variations on a basic system design, such as the code required to handle optional external devices.

Macro capability allows the programmer to define a routine through the use of a single label. ASM48 will assemble the code required by the reserved routine whenever the Macro label is inserted in the text.

Output from the ASM48 is in standard Intel® Hex format. It may be loaded directly to an ICE-48 module for integrated hardware/software debugging. It may also be loaded into the Intellec Development System for 8748 PROM programming using the Universal PROM Programmer.

SAMPLE MCS-48™ DISKETTE-BASED ASSEMBLEY LISTING

```
ISIS-II 8048 MACRO ASSEMBLER, V1.0                    PAGE 1

LOC   OBJ          SEQ          SOURCE STATEMENT

                     1  ;DECIMAL ADDITION ROUTINE.  ADD BCD NUMBER
                     2  ;AT LOCATION 'BETA' TO BCD NUMBER AT 'ALPHA' WITH
                     3  ;RESULT IN 'ALPHA.'  LENGTH OF NUMBER IS 'COUNT' DIGIT
                     4  ;PAIRS.  (ASSUME BOTH BETA AND ALPHA ARE SAME LENGTH
                     5  ;AND HAVE EVEN NUMBER OF DIGITS OR MSD IS 0 IF
                     6  ;ODD)
                     7  INIT      MACRO     AUGND,ADDND,CNT
                     8            MOV       R0, #AUGND
                     9  L1:       MOV       R1, #ADDND
                    10            MOV       R2, #CNT
                    11            ENDM
                    12  ;
0001E                13  ALPHA     EQU       30
0028                 14  BETA      EQU       40
0032                 15  COUNT     EQU       5
0100                 16            ORG       100H
                     17            INIT      ALPHA, BETA, COUNT
0100  B81E           18+           MOV       R0, #ALPHA
0102  B928           19+L1:        MOV       R1, #BETA
0104  BA32           20+           MOV       R2, #COUNT
0106  97             21            CLR       C
0107  F0             22  LP:       MOV       A, @R0
0108  71             23            ADDC      A, @R1
0109  57             24            DA        A
010A  A1             25            MOV       @R0, A
010B  18             26            INC       R0
010C  19             27            INC       R1
010D  EA07           28            DJNZ      R2, LP
                                   END

USER SYMBOLS
ALPHA 001E    BETA 0028    COUNT 0005    LP 0107
L1    0102

ASSEMBLY COMPLETE, NO ERRORS


ISIS-II ASSEMBLER SYMBOL CROSS REFERENCE, V1.0                PAGE 1

SYMBOL CROSS REFERENCE

ALPHA    13#   17
BETA     14#   17
COUNT    15#   17
INIT      7#   17
L1       19#
LP       22#   28
```

SPECIFICATIONS

MDS-D48

Operating Environment:
- Required Hardware
  - Intellec® Microcomputer Development System
  - System Console
  - Intellec Diskette Operating System
  - 32K RAM (non-Macro Assembler)
  - 48K RAM (Macro Assembler)
- Optional Hardware
  - Universal PROM Programmer

Documentation Package:
- MCS-48™ Assembly Language Manual
- Universal PROM Mapper Operator's Manual
- ISIS-II System User's Guide

Shipping Media:
- Diskette

ORDERING INFORMATION

PRODUCT CODE	DESCRIPTION
MDS-D48	Diskette-Based Assembler for MCS-48 Family of Microprocessors

INTELLEC SERIES II
AVAILABLE OPTIONS AND DOCUMENTATION

OPTIONS

EXPANSION MODULES

SBC-016	16K RAM Module
SBC-032	32K RAM Module
MDS-406	6K PROM Module using 1702A PROMs
MDS-416	16K PROM Module using 2708 PROMs
MDS-501	DMA Channel Controller
MDS-504	General Purpose I/O Module
SBC-310	High Speed Mathematics Unit

IN-CIRCUIT EMULATORS

ICE-80	8080A In-Circuit Emulator
ICE-85	8085 In-Circuit Emulator with External Trace Capability
ICE-48	8748/8048 In-Circuit Emulator
ICE-30	Series 3000 In-Circuit Emulator
MDS-EM1	8021 Emulation Board

PERIPHERALS

MDS-PTR	High Speed Paper Tape Reader
UPP-103	Universal PROM Programmer
MDS-PRN	165 Character per Second Dot Matrix Printer
MDS-770/771	60 Character per Second Dot Matrix Printer
MDS-701/702	Add-On Disk Drive for Intellec Series II Model 230
MDS-710/711	1/2 Million Byte Floppy Disk System
MDS-720/721	1 Million Byte Floppy Disk System
MDS-730/731	Add-On Drives to 720/721 with Addition al 1 Million Bytes

SOFTWARE

MDS-PLM	8080/8085 PL/M Compiler
MDS-301	8080/8085 ANS 1977 FORTRAN Compiler
MDS-R48	MCS-48 Family ROM Assembler/Editor*
MDS-D48	MCS-48 Family Diskette-Based Assembler
INSITE	Intel Microprocessor User's Library

DOCUMENTATION

MANUAL	DOC. #	PRICE
A Guide to Microcomputer Development Systems	9800558	$ 2.00
Intellec® Series II Model 210 User's Guide	9800557	15.00
ISIS-II User's Guide	9800306	15.00
Intellec® Series II Installation and Service Manual	9800559	15.00
Intellec® Series II Hardware Interface Manual	9800555	25.00
Intellec® Series II Hardware Reference Manual	9800556	25.00
Intellec® Series II Schematic Drawings	9800554	25.00
ISIS-II 8080/8085 Assembler Operator's Manual	9800292	10.00
8080/8085 Assembly Language Programming Manual	9800301	5.00
MCS-48/UPI-41 Assembly Language Programming Manual	9800255	5.00
PL/M-80 Programming Manual	9800268	5.00
FORTRAN-80 Programming Manual	9800481	5.00
ISIS-II PL/M Compiler Operator's Manual	9800300	15.00
ISIS-II 8080/8085 ANSI FORTRAN Compiler Operator's Manual	9800480	15.00
Universal PROM Mapper Operator's Manual	9800236	15.00
ICE-80 Operator's Manual	9800185	15.00
ICE-85 Operator's Manual	9800463	15.00
ICE-48 Operator's Manual	9800464	15.00
Universal PROM Programmer Hardware Reference Manual	9800133	25.00
Single Density Diskette Operating System Hardware Reference Manual	9800212	25.00
Double Density Diskette Operating System Hardware Reference Manual	9800422	25.00

Documentation may be ordered from:

Literature Department
Intel Corporation
3065 Bowers Avenue
Santa Clara, CA 95051

*For use with Model 210.

INTELLEC® PROMPT 48™
MCS-48™ MICROCOMPUTER DESIGN AID

Complete Design Aid and EPROM Programmer for revolutionary MCS-48™ Single Component Computers including:

CPUs	8-bit MCS-48™ : 8748, 8035
Program Memory	1K byte erasable, reprogrammable on-chip (8748), expandable. 1K byte RAM in PROMPT™ system.
Register Memory	64 bytes RAM on-chip, expandable
Data Memory	256 bytes RAM in PROMPT™ system, expandable
I/O	27 TTL compatible I/O lines on-chip, expandable
Control	On-chip clock, internal timer/event counter, two vectored interrupts, eight level stack
Power	Single +5 VDC system

Low Cost

Simplifies microcomputing — enter, run, debug, and save machine language programs with calculator-like ease

Complete with two removable MCS-48™ CPUs:

8748	CPU with erasable, reprogrammable program memory on-chip
8035	CPU program memory is off-chip

Integral keyboard and displays (no teletype-writer or CRT terminal required)

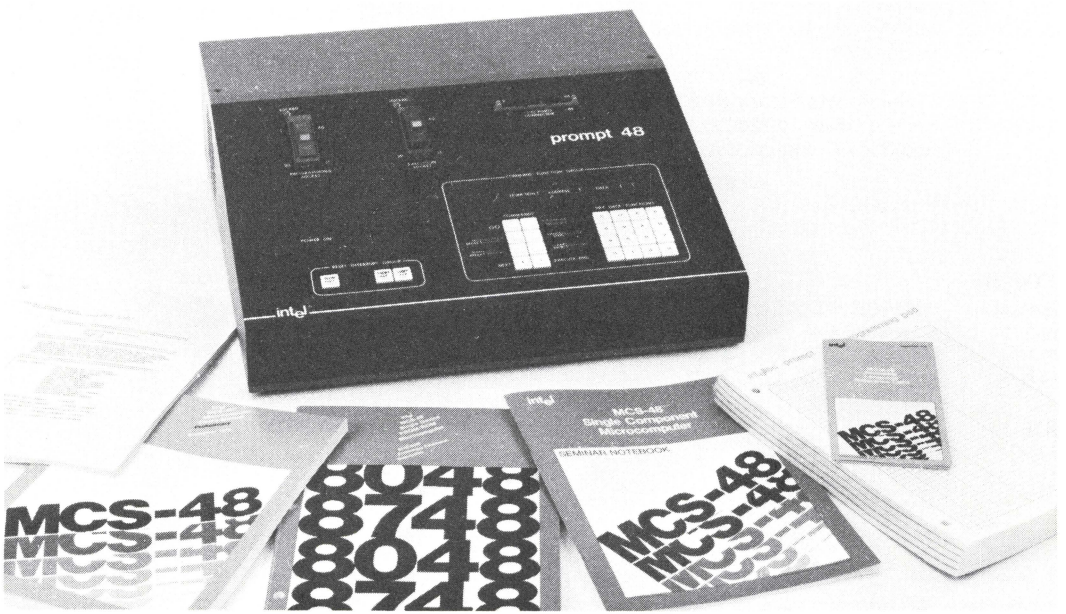
Extensive PROMPT 48™ monitor allows system I/O, bus and memory expansion

Intellec® Microcomputer Development System compatible

Comprehensive Design Library

Intellec PROMPT 48 is a low cost, fully-assembled design aid for the revolutionary 8748 single component microcomputer. PROMPT 48 simplifies the programming of MCS-48 systems — programs can be entered and debugged with calculator-like ease on the large, informative display and keyboard panel. The comprehensive design library with tutorial manual is ideal for newcomers to microcomputing.

PROMPT 48's panel connector allows easy access to I/O ports and system bus. Thus users can expand program memory beyond the 1k bytes provided internally. PROMPT 48 can serve as an economical 8748 Specialized PROM Programmer (SPP) peripheral in Intellec Microcomputer Development Systems.



PROMPT 48™ SIMPLIFIES MICROCOMPUTING

Intellec PROMPT 48 simplifies the programming of MCS-48 systems. Like the 8748 it is radically new, highly integrated, and expandable. Like the MCS-48 family, it is low cost, and ideal for small applications and programs. It is a design aid, not a development system with sophisticated software and peripherals.

"PROMPT" stands for PROgraMming Tool. It is a programmer for 8748 EPROMs, and a versatile aid for debugging MCS-48 programs. Programs can be entered via its integral panel keyboard, programming socket, or serial channel. Almost any terminal can be interfaced to the serial channel, including a teletypewriter, CRT, or the Intellec Microcomputer Development System.

Programs, written first in assembly language, are entered in machine language and debugged with calculator-like ease on the large, informative display and keyboard panel. Most MCS-48 operations can be specified with only two keystrokes.

Once entered, routines can be exercised one instruction (single step) or many instructions at a time. The principal MCS-48 register — the accumulator — is displayed while single-stepping. Programs can be executed in real-time (GO NO BREAK) or with as many as eight different breakpoints (GO WITH BREAK).

PROMPT 48 is a complete, fully assembled and powered microcomputer system including program memory, data memory, I/O and system monitor beyond that available on MCS-48 single component computers. 1K bytes of PROMPT system RAM serve as "writable program memory" — a ROM simulator for the program memory on each MCS-48 computer. 256 bytes of PROMPT system RAM serve as "external data memory," beyond the 64 register bytes on each MCS-48 computer. Users may further expand program or data memory via the panel I/O PORTS and BUS CONNECTOR.

The PROMPT 48 manual includes chapters for the reader with little or no programming experience. Topics treated range from number systems to microcomputer hardware design. A novel, unifying set of tutorial diagrams — MICROMAPs — simplify microcomputer concepts.

PROMPT's handy, pocket-sized reference cardlet can be affixed to the mainframe. Programming pads aid in the organization and documentation of programs. These features, plus a comprehensive design library of manuals, articles and application notes, make the Intellec PROMPT 48 ideal for the newcomer to microcomputing.

THE REVOLUTIONARY MCS 48™ SINGLE COMPONENT COMPUTER

Advances in n-channel MOS technology allow Intel, for the first time, to integrate into one 40-pin component all computer functions:

8-bit CPU
1K x 8-bit EPROM/ROM Program Memory
64 x 8-bit RAM Data Memory
27 Input/Output Lines
8-bit Timer/Event Counter

More than 90 instructions — each one or two cycles — make the single chip MCS-48 equal in performance to most multi-chip microprocessors. The MCS-48 is an efficient controller and arithmetic processor, with extensive bit handling, binary, and BCD arithmetic instructions. These are encoded for minimum program length: 70% are single byte operation codes, and none is more than two bytes.

Three interchangeable, pin-compatible devices offer flexibility and low cost in development and production:

- 8748 with user-programmable and erasable EPROM program memory for prototype and pre-production systems
- 8048 with factory-programmed mask ROM memory for low-cost, high volume production
- 8035 without program memory, for use with external program memories

Each MCS-48 processor operates on a single +5V supply, with internal oscillator and clock driver, and circuitry for interrupts and resets. Extra circuitry is in the 8048 ROM processor to allow low power standby operation: the 64 x 8 RAM data memory can be independently powered.

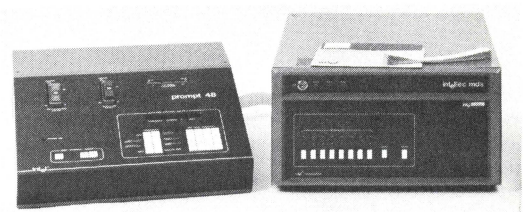
For systems requiring additional compatibility, the MCS-48 can be expanded with the new 8243 I/O expander, 8155 I/O and 256 byte RAM, 8755 I/O and 2K byte EPROM or 8355 I/O and 2K ROM devices. MCS-48 processors readily interface to MCS-80/85 peripherals and standard memories.

PROMPT 48 comes complete with two of these revolutionary MCS-48 processors — an 8748 and an 8035.

EXPANDING PROMPT 48™

PROMPT 48 may be expanded beyond the resources on the MCS-48 single component computer and those in the PROMPT system. External program and data memory may be interfaced and input/output ports added with the 8243 I/O Expander.

The PROMPT panel I/O Ports and Bus Connector allow easy access to all MCS-48 pins except those reserved for control by the PROMPT system, namely EA external access, SS single step, and X1, X2 clock inputs.

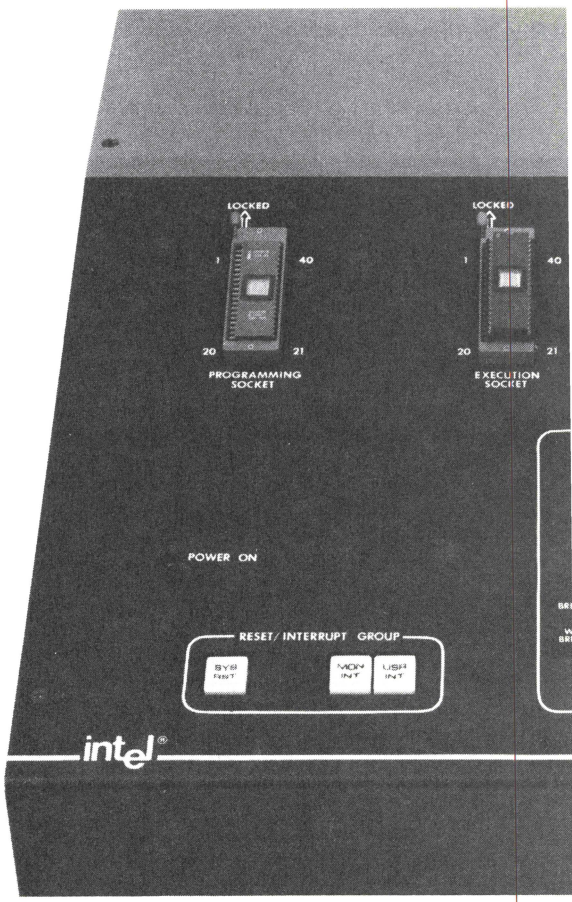


A Specialized PROM Programmer Kit, the PROMPT-SPP, allows PROMPT 48 to serve as an economical 8748 Specialized PROM Programmer peripheral in Intellec Microcomputer Development Systems. The PROMPT-SPP cable plugs directly into the rear panel of the Intellec Microcomputer Development System.

PROMPT 48 can be fully controlled either by the panel keyboard and displays, or remotely by a serial channel. Thus a teletypewriter or CRT can be used but neither is required. Full remote control by a serial channel means users can download and debug programs using the PROMPT 48 together with an Intellec Microcomputer Development System.

The 8748 is the first microcomputer fully integrated on one component. All elements of a computing system are provided, including CPU, RAM, I/O, timer, interrupts and erasable, reprogrammable non-volatile program memory.

PROMPT's **PROGRAMMING SOCKET** programs this revolutionary "smart PROM" – the 8748 – in a highly reliable, convenient manner. A fail-safe interlock ensures the device is properly inserted before applying programming pulses. Each location may be individually programmed, one byte at a time. A read-before-write programming algorithm prevents device damage by inadvertently programming unerased memory.



The **EXECUTION SOCKET** accepts an 8035 or an 8748. Both are supplied with each PROMPT 48, and either can serve as heart of the PROMPT system. There are no processors within the PROMPT 48 mainframe, which instead contains monitor ROM and RAM, user RAM, peripherals, drivers, and sophisticated control circuitry.

Once a processor is seated in the execution socket and power is applied the PROMPT system comes to life. One can select various access modes such as program execution from PROMPT system RAM, or from on-chip PROM. Thus programs can first be executed from PROMPT RAM with the 8035 processor. When debugging is complete, the 8035 (execution socket) processor can program the 8748 (programming socket) processor. Finally, a programmed 8748 processor can be exercised by itself from the execution socket. The execution socket processor runs either monitor or user programs.

SYSTEM RESET initializes the PROMPT system and enters the monitor. **MONITOR INTERRUPT** exits a user program gracefully, preserving system status and entering the monitor. **USER INTERRUPT** causes an interrupt only if the PROMPT system is running a user program.

A comprehensive system monitor resides in four 1K byte read-only memories. It drives the PROMPT keyboard and displays and responds to COMMANDS and FUNCTIONS.

The top 16 bytes of on-chip program memory must be used by the PROMPT system to switch between monitor and user programs. It requires one level of the MCS-48 eight-level stack.

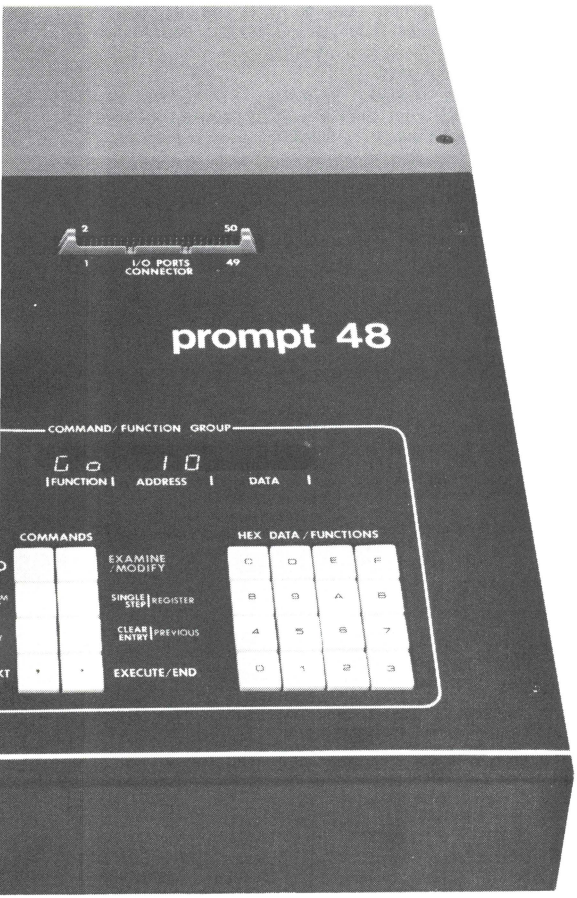
PROMPT 48's **COMMANDS** are grouped and color-coded to simplify access to the 8748's separate program and data memory. You can EXAMINE and MODIFY registers, data memory or program memory.

Then either the NEXT or PREVIOUS register and memory locations can be accessed with one keystroke.

Programs can be exercised in three modes. GO NO BREAK runs in real time. GO WITH BREAK is not real time – after each instruction the MCS-48 program counter is compared against pending breakpoints. If no break is encountered, execution resumes. GO SINGLE STEP exercises one instruction at a time.

Commands are like sentences, with parameters separated by [,] NEXT. Each command ends with [.] EXECUTE/END.

In addition to the PROMPT basic COMMANDs, thirteen functions simplify programming. Each is started merely by pressing a **HEX DATA/FUNCTIONs** key and entering parameters as required.



An optional cable, PROMPT-SER, directly connects the PROMPT system to virtually any terminal via a rear access slot. Another cable, PROMPT-SPP, allows programs and data to be downloaded from the Intellec Microcomputer Development System to the PROMPT system for debugging.

You enjoy easy access to the pins of the executing processor via this **I/O PORTS and BUS CONNECTOR**. Only the EA external access, SS single step and X1, X2 clock inputs are reserved for the PROMPT system.

Thus program or data memory may be expanded beyond that provided on-chip or in the PROMPT system. I/O ports can be expanded, as with the 8243, or peripheral controllers can be memory-mapped. The I/O ports and Bus connector allows the execution socket processor to be directly interfaced to your prototype system, yet be controlled from the PROMPT panel.

The **COMMAND/FUNCTION GROUP** panel keyboard and displays completely control PROMPT 48 – a teletypewriter or CRT terminal is not needed.

A hyphen prompting character appears whenever a command or function can be entered. Addresses and data are shown whenever EXAMINing registers and memory. Parameters for COMMANDs and FUNCTIONs are also shown.

[2] **Port 2 MAP** allows you to specify the direction of each pin on port 2. Port 2 is multiplexed to address external program memory and expand I/O. Thus it must be buffered; the P2 MAP command establishes the direction of buffering.

[3] **Program EPROM** programs 8748 EPROMs.

[4] **Byte Search with optional mask** sweeps through register, data or program memory searching for byte matches. Starting and ending memory addresses are specified.

[5] **Word Search with optional mask** sweeps through register, data or program memory searching for word matches. Starting and ending memory addresses are specified.

[6] **Hex Calculator** computes hexadecimal sums and differences.

[7] **8748 Program for Debug** is similar to Program EPROM, but ensures that the top of program memory contains monitor reentry code for debugging.

[8] **Compare** will verify any portion of EPROM program memory against PROMPT memory.

[9] **Move Memory** allows blocks of register, data or program memory to be moved.

[A] **Access** specifies one of six access modes for PROMPT 48. For example, EPROM, PROMPT RAM or external program memory, and a variety of input/output options may be selected.

[B] **Breakpoint** allows you to set and clear any or all of the eight breakpoints.

[C] **Clears** portions of register, data or program memory.

[D] **Dumps** register, data, or program memory to PROMPT's serial channel, for example a teletypewriter paper tape punch.

[E] **Enter** (reads) register, data or program memory from PROMPT's serial channel.

[F] **Fetches** programs from EPROM to PROMPT RAM.

SPECIFICATIONS

TIMING

Basic Instruction	2.5 μsec
Cycle Time	t_{CY} = 2.5 μsec
Clock	6 MHz ±0.1%

MEMORY BYTES

	Maximum	On Chip	In PROMPT 48
Register	64	64	0
Data	3328	0	256
Program	4096	1024 EPROM	1024 RAM

The 8748 contains 64 bytes of register memory, no external data memory, and 1024 bytes of EPROM program memory. The PROMPT system provides 256 bytes of external data memory, and 1024 bytes of RAM program memory. PROMPT RAM program memory can be used in place of the On-Chip EPROM program memory; thus programs less than 1024 bytes may be designed. For larger programs additional memory can be directly interfaced to the MCS-48 bus via the PROMPT panel I/O Ports and Bus Connector.

I/O PORTS

All MCS-48 I/O Ports are accessible on the PROMPT panel connector.

BUS is a true bidirectional 8-bit port with associated strobes. If the bidirectional feature is not needed, bus can serve as either a statically latched output port or a non-latching input port. Input and output lines cannot be mixed.

PORTS 1 AND 2 are each 8 bits wide. Data written to these ports is latched and remains unchanged until written. As inputs these lines are not latching. The lines of ports 1 and 2 are called quasibidirectional. A special output structure allows each line of port 1 and half of port 2 to serve as an input, an output, or both. Any mix of input, output, and both lines is allowed.

Three pins — T0, T1 and INT — can serve as inputs; T0 can be designated as a clock output. Input/Output can be expanded via the PROMPT panel connector with a special I/O expander (8243) or standard peripherals.

RESET and INTERRUPTS

RESET initializes the PROMPT system and enters the monitor. MONITOR INTERRUPT exits a user program gracefully, preserving system status and entering the monitor. USER INTERRUPT causes an interrupt only if the PROMPT system is running a user program. The processor traps to location 3_{16}. The MCS-48 timer/event counter is not used by the PROMPT system and is available to the user.

Either timer flag or interrupt will signal when overflow has occurred. The timer interrupt can be used only in the GO NO BREAK (real time) mode.

EPROM PROGRAMMING

PROMPT 48 provides a programming socket to directly program 8748s. Programs are loaded into the PROMPT RAM program memory via keyboard, EPROM, teletypewriter, or other serial interface.

A fail-safe interlock ensures programming pulses are applied only if the device is properly inserted. Inadvertent reprogramming is prevented by a read-before-write programming algorithm. Each location may be individually programmed, one byte at a time.

PANEL I/O PORTS and BUS CONNECTORS

All MCS-48 pins, except five, are accessible on the I/O Ports and Bus Connector. The five reserved for PROMPT system control are EA external access, SS single step, X1, X2 crystal inputs, and 5 V.

Due to internal buffering of the MCS-48 bus, access times will be negligibly degraded by the PROMPT system. Since MCS-48 processors do not communicate internal address gate status, bus data must be driven out if neither PSEN nor RD is asserted.

SYSTEM DEVICES

Both user programs and the PROMPT monitor enjoy access to system devices: serial I/O, panel displays and keyboard. These are memory-mapped to program memory addresses beyond 2K.

The SERIAL I/O port (data 820_{16}, control 821_{16}) is defined by software and jumpers for 110 baud, 20 mA current loop, but can easily be jumpered for other baud rates and RS232C levels. Asynchronous or synchronous transmission, data format, control characters, and parity can be programmed.

Software is used to debounce the PANEL KEYBOARD (data 810_{16}). The monitor's input routines (see SOFTWARE DRIVERS) provide this debouncing and can be called from user programs.

Eight display ports (data $810\text{-}817_{16}$) allow each of the PANEL DISPLAYS to be written from user programs. Data written on a display device will time out after a fixed interval. Displays must be refreshed on a polled or interrupt-driven basis. User programs can call SOFTWARE DRIVERS which provide this capability.

COMMANDS

☐ GO { ☐ Single Step / ☐ With Break / ☐ No Break } ☐ Examine/Modify { ☐ Register / ☐ Data / ☐ Program } Memory

☐ Open Previous/Clear Entry ☑ Next ⊡ Execute/End

FUNCTIONS

[2] Port 2 Map	[8] Compare EPROM with memory
[3] Program EPROM (8748)	[9] Move Memory (R, D or P)
[4] Search (R, D or P)* Memory for 1 byte, optional mask	[A] Access
[5] Search (R, D or P) Memory for 2 bytes, optional mask	[B] Breakpoint
[6] Hexadecimal Calculator +, –	[C] Clear Memory (R, D or P)
[7] 8748 Program EPROM for Debug	[D] Dump Memory (R, D or P)
	[E] Enter (Read) Memory (R, D or P)
	[F] Fetch EPROM Program Memory

*R, D or P is Register, Data or Program.

SOFTWARE DRIVERS

Panel Keyboard In: KBIN, KDBIN
Panel Display Out: DGS6, DGOUT, HXOUT, BLK, REFS, ENREF
Serial Channel: CI, CO, RI, PO, CSTS

CONNECTORS

Serial I/O: 3M 3462-0001 Flat Crimp/AMP 88106-1 Flat Crimp/TI H312113 Solder/AMP 1-583485-5 Solder.

Panel I/O Ports and Bus Connector: 3M 3425 Flat Crimp. A complete cable set including wirewrap header for prototyping is included with each PROMPT.

EQUIPMENT SUPPLIED

PROMPT 48 mainframe with two MCS-48 processors (8748, 8035), display/keyboard, EPROM Programmer, power supply, cabinet and ROM-based monitor.

110 VAC power cable, 110 or 220 VAC, fuse, Panel I/O Ports and Bus Connector cable set, PROMPT 48 User's Manual, PROMPT 48 Monitor Listing, Reference Cardlet, PROMPT 48 Programming Pads, MCS-48 Microcomputer User's Manuals, MCS-48 Assembly Language Manual, PROMPT 48 Schematics.

PHYSICAL CHARACTERISTICS

Maximum Height:	13.5 cm (5.3 in.)
Width:	43.2 cm (17 in.)
Maximum Depth:	43.2 cm (17 in.)
Weight:	9.6 kg (21 lb.)

ELECTRICAL REQUIREMENTS

Either 115 or 230 VAC (±10%) may be switch-selected on the mainframe. 1.8 amps max current (at 125 VAC).

Frequency is 47-63 Hz.

ENVIRONMENTAL

Operating Temperature:	0°C to +40°C
Non-Operating Temperature:	–20°C to +65°C

ORDERING INFORMATION

PROMPT-48 or PROMPT-48-220V	Intellec® PROMPT 48 MCS-48 Microcomputer Design Aid. Complete with two MCS-48 processors (8748 and 8305), EPROM programmer, integral keyboard, displays, and system monitor in ROM.
PROMPT-SER	Serial cable connects PROMPT to TTY, CRT
PROMPT-SPP	Specialized PROM Programmer Kit connects PROMPT 48 to Intellec Microcomputer Development System for EPROM programming

INTELLEC® PROMPT 80/85™
8080/8085 MICROCOMPUTER DESIGN AID

Simplifies microcomputing

Enter, run, debug and save machine language programs with calculator-like ease

Complete, fully-assembled microcomputer, including:

CPU	Standard 8080A on popular SBC 80/10 Single Board Computer
Memory	1K byte RAM, 3K byte ROM, and two spare 1K byte 8708 EPROMs
I/O	24 programmable parallel I/O (TTL) lines, including two: 8-bit ports, fully implemented switches, displays Programmable serial I/O interfaces directly with most terminals
Power	Only 110 or 230 VAC required

Low Cost

PROM Programmer for UV Erasable, Electrically Reprogrammable ROMs (EPROMs): 8708/2708/2704 standard, 8755 with adaptor

Integral keyboard and 16-digit display (no teletypewriter or CRT terminal required)

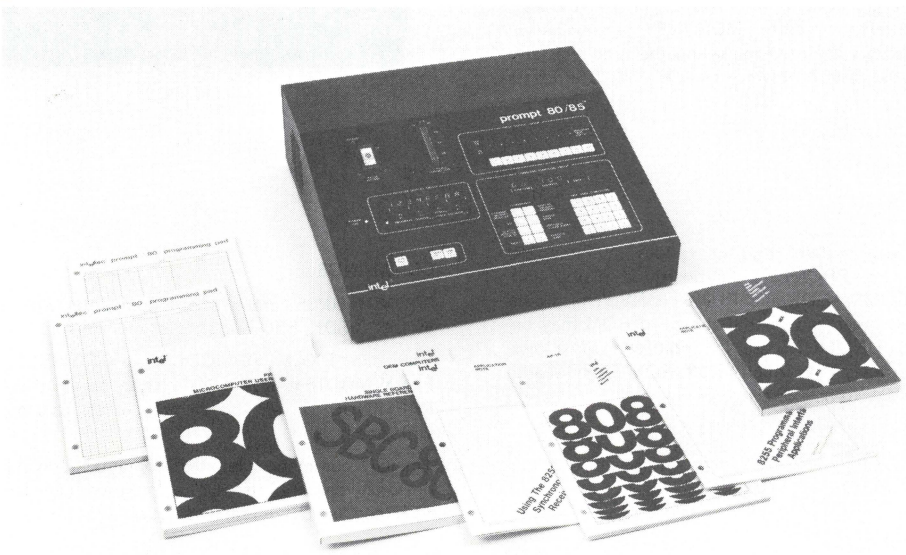
Extensive system monitor software in ROM:
- Examine/Display/Modify Registers and Memory
- Enter, Run, Test, Single-Step programs
- Hex Calculator
- Move, Search Memory Blocks

Self-programmable — user can add functions

Comprehensive design library

Intellec PROMPT 80/85 is a low-cost, fully assembled microcomputer design aid. PROMPT 80/85 simplifies the programming of SBC 80 and System 80 microcomputers, as well as 8080/8085 processors, 8708/2708/2704/8755 EPROMs and 8255/8251 programmable I/O devices. 8080 programs can be entered and debugged with calculator-like ease on the large, informative display and keyboard panel. The comprehensive design library with tutorial manual is ideal for newcomers to microcomputing.

PROMPT 80/85's SBC 80/10 can be expanded using the SBC modular cardcage. And PROMPT 80/85 can serve as an economical 8708/8755 Specialized PROM Programmer (SPP) peripheral in Intellec Microcomputer Development Systems.

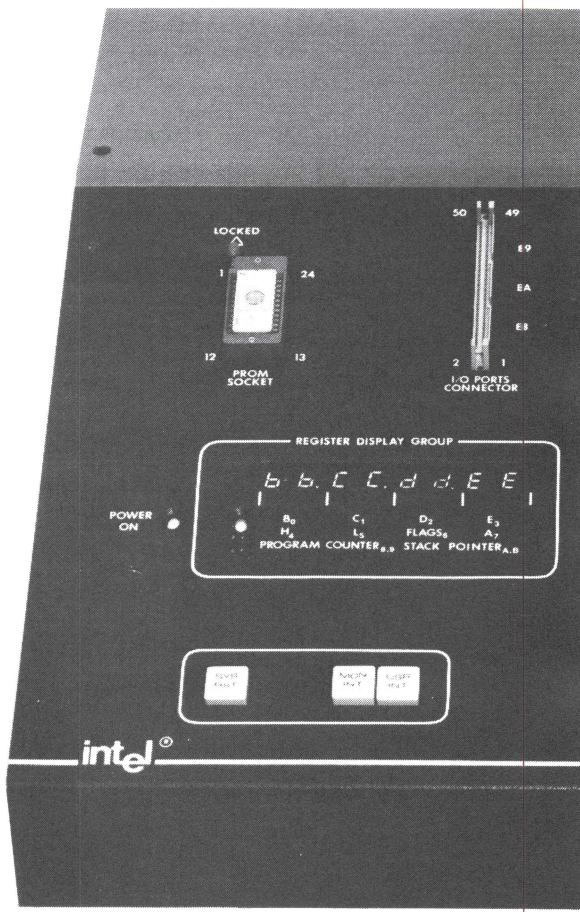


PROM PROGRAMMER

8708 UV Erasable, Electrically Reprogrammable ROMs (EPROMs) can be easily programmed, compared, and transferred to RAM using the zero-insertion force socket on the panel. A new technique allows 8708 to be partially programmed in multiple blocks of 16 bytes. Thus, small, modular routines can be entered, tested, and readily saved using EPROM.

EPROMs can also be conveniently duplicated. The master (original) device plugs into the SBC 80/10 inside PROMPT 80, and can be copied to the panel programming socket.

8755 EPROMs can also be programmed, compared and transferred over any address range using the optional adaptor PROMPT 875.



REGISTER/DISPLAY GROUP

All 8080 registers can be displayed, even while single-stepping programs. The registers are shown in three rows:

first row:	B	C	D	E
second row:	H	L	Flags	A
third row:	Program Counter		Stack Pointer	

One register row is visible at a time. Three small LEDs to the left of these rows indicate which row is displayed. The SCROLL REGISTER DISPLAY command displays the next row (first, second, third, etc.)

RESET, INTERRUPTS

SYS RST resets the system, initializes the PROMPT 80/85 registers and enters the monitor. MON INT interrupts a user program and enters the monitor saving the user registers. USR INT is a user interrupt which traps PROMPT 80/85 to location $3C02_{16}$.

MONITOR

A comprehensive system monitor resides in three 1K ROMs. It drives PROMPT's keyboard, displays, and responds to COMMANDS and FUNCTIONS. The monitor is modular, organized so that the third ROM may be removed if F FUNCTIONS are not required. This allows sizable user routines – as much as 2K ROM/EPROM and nearly 1K RAM – to be exercised.

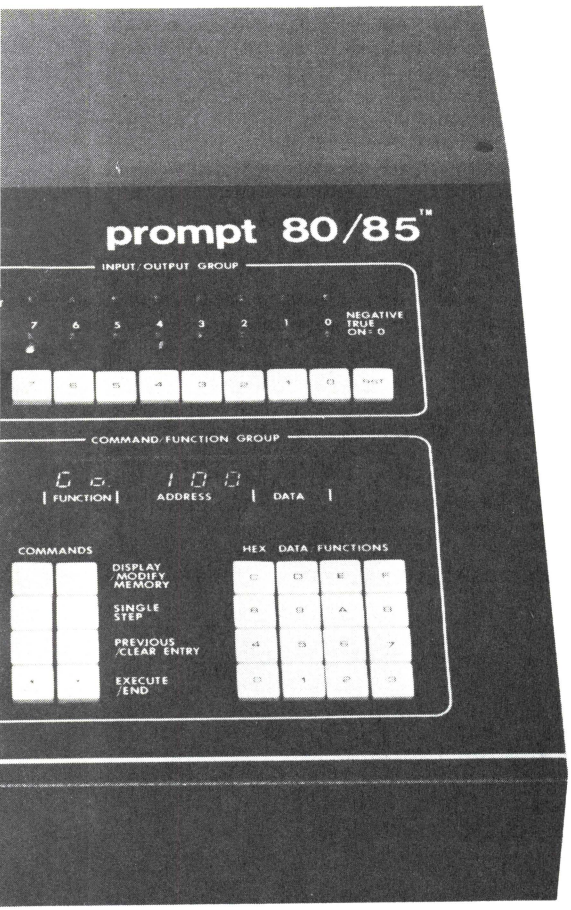
COMMANDS

PROMPT 80/85 commands are compatible with those used by Intel's SDK, SBC, and Intellec monitors.

You can EXAMINE/MODIFY a REGISTER, or DISPLAY/MODIFY MEMORY. Then either the NEXT or PREVIOUS register and memory locations can be opened with one button.

The GO command executes programs, allowing multiple, optional breakpoints. Or a program can be SINGLE STEPped, executed one instruction at a time.

The SCROLL REGISTER DISPLAY command displays the next row of the REGISTER/DISPLAY GROUP.



Commands are entered naturally, like phrases in a sentence: the NEXT parameters are separated bycommas [,] and command sentences end with [.] EXECUTE/END.

The commands do what makes sense. For example:

GO [ ] [1] [0] [0] [.] EXECUTE/END
starts the program at address 100.

GO [ ] [1] [0] [0] [,] NEXT [2] [0] [0] [.] EXECUTE/END
starts the program at 100, but stops if you get to 200, a breakpoint.

GO [ ] [.] EXECUTE/END
starts the program where you last stopped.

INPUT/OUTPUT GROUP

The INPUT/OUTPUT (I/O) GROUP features two fully implemented 8-bit ports, both with displays, and with latch switches for the input port E9. The port addresses are clearly marked E8 and E9. Those two ports and a third, at EA, are easily accessible on the I/O PORTS CONNECTOR. Negative true logic is used throughout the I/O GROUP and PORTS CONNECTOR to enhance noise immunity and allow wire-ANDing.

PARALLEL I/O

The I/O PORTS CONNECTOR provides easy access to 24 parallel, TTL-compatible lines. These lines are addressed as three ports (each 8 lines), port E8, E8, and EA.

These ports can be defined to be input or output by software. Defining control words, tabulated in "Specifications", are sent OUT to port EB, the control word register.

SERIAL I/O

PROMPT's programmable serial I/O readily interfaces with most terminals. Jumpers select either 20 mA teletypewriter (TTY) current loop or RS-232C operation, and the appropriate communications frequency. Asynchronous or synchronous transmission, data format, control characters, parity, and transmission rate can be programmed.

A serial cable kit, PROMPT-SER, connects PROMPT to either a teletypewriter or RS-232C standard (CRT) terminal through a rear chassis access slot. Teletypewriters may require minor reader control modifications.

COMMAND/FUNCTION DISPLAYS

The COMMAND/FUNCTION displays show addresses and data when DISPLAYing MEMORY, and parameters for COMMANDS and FUNCTIONS are entered.

FUNCTIONS

Eight FUNCTIONS are provided by PROMPT. Others may be added by the user. Pressing a HEX DATA/FUNCTIONS key (0–7) starts a function.

[0] is F0 Read Paper Tape
[1] is F1 Write Paper Tape
[2] is F2 Program 8708 EPROM, Compare
[3] is F3 Compare 8708 EPROM
[4] is F4 Transfer 8708 EPROM to RAM
[5] is F5 Move Block Memory
[6] is F6 Hexadecimal Calculator, +, –
[7] is F7 Byte Search Memory, optional mask
[8] is F8 Word Search Memory, optional mask

With the optional PROMPT-875 adaptor,

[9] is F9 Program 8755 EPROM, Compare
[A] is FA Compare 8755 EPROM
[B] is FB Transfer 8755 EPROM

PROMPT SIMPLIFIES MICROCOMPUTING

Intellec PROMPT 80/85 simplifies the programming of 8080/8085 processors, SBC 80 and System 80 microcomputers, as well as 8708/8755 EPROMs and 8255/8251 programmable I/O devices.

PROMPT is a low-cost programming tool. It is a microcomputer design aid – not a development system with sophisticated software and peripherals.

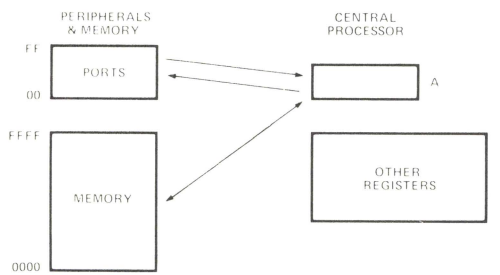
PROMPT encourages the preparation and verification of small, modular routines which together may comprise sizable programs. These are written in assembly language, then entered in machine language and debugged with calculator-like ease on the large, informative display and keyboard panel.

Many 8080 operations can be specified with only two key strokes. Once entered, programs can be exercised one instruction (single step) or many instructions at a time. And, any of the 8080 registers can be watched while single-stepping.

Programs are readily saved and instantly reloaded via UV Erasable, Electrically Reprogrammable ROMs (EPROMs). PROMPT 80/85 can program the popular 8708 EPROMs in small blocks, so routines can be debugged and saved incrementally. Several programs are pre-recorded as examples on PROMPT's spare 8708 EPROMs

PROMPT 80/85 is a complete, fully assembled and powered 8080 microcomputer, including RAM, I/O, and system monitor in ROM. Twenty-four lines of programmable, TTL-compatible, parallel I/O are easily accessed on a panel connector. Two 8-bit ports are fully implemented, one with displays for output, the other with displays and switches for input. PROMPT's programmable serial I/O interfaces directly with most terminals. A teletypewriter or CRT can be used, but neither is required because of PROMPT's built-in keyboard and display.

The PROMPT 80/85 manual includes chapters for the reader with little or no programming experience. Topics treated range from the number system to microcomputer hardware design. A novel, unifying set of tutorial diagrams – MICROMAPS™ – simplify microcomputer concepts.



Programming pads aid in the organization and documentation of programs. These features, plus a comprehensive design library of manuals, articles, and applications notes, make Intellec PROMPT 80/85 ideal for the newcomer to microcomputing.

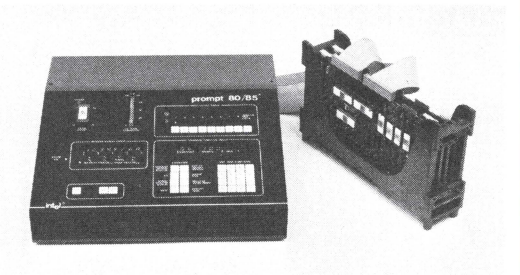
A COMPLETE COMPUTER

The heart of PROMPT 80/85 is the popular SBC 80/10 Single Board Computer, a complete computer on a single printed circuit board. The SBC 80/10 includes an 8080A, 1K bytes of static RAM memory, and sockets for 4K bytes of EPROM memory. Signals to the SBC 80/10 include 48 programmable, parallel I/O lines with sockets for interchangeable line drivers and terminators, a programmable serial channel, a multi-source single level interrupt network, and bus drivers for memory and I/O expansion. Read-only-memory may be added in 1K byte increments using Intel 8708 EPROMs or 8308 ROMs.

The central processor for PROMPT's SBC 80/10 is Intel's powerful 8-bit n-channel MOS 8080A CPU. The 8080A contains six 8-bit general-purpose registers and an accumulator. The six general-purpose registers may be addressed individually or in pairs, providing both single and double precision operations.

The 8080A has a 16-bit address bus which allows direct addressing of up to 64K bytes of memory. An external stack, located anywhere in read/write memory, may be used as a last-in/first-out store. The contents of the program counter, accumulator, flags, and all of the general-prupose registers are stacked using a 16-bit pointer. Subroutine nesting is bounded only by memory size.

EXPANDING PROMPT 80/85™



PROMPT 80/85's SBC 80/10 can be expanded via the SBC 604 Modular Cardcage. The cardcage houses the SBC 80/10 and up to three expansion boards. Memory and I/O can be added in various combinations. Additional power may be required.

A Specialized PROM Programmer kit, the PROMPT-SPP, allows PROMPT 80/85 to serve as an economical 8708/8755 Specialized PROM Programmer peripheral in Intellec Microcomputer Development Systems. The PROMPT-SPP cable plugs directly into the rear panel of the Intellec Microcomputer Development System.

SPECIFICATIONS

WORD SIZE

Instruction: 8, 16, or 24 bits
Data: 8 bits

TIMING

Basic Instruction: 1.95 μsec
Cycle Time: t_{CY} = 488 nsec
Clock: 2.058 MHz ± 0.1%

MEMORY BYTES

	Addressing	On Board	Monitor Uses
ROM/PROM	$0\text{-}0FFF_{16}$	4096	2048 or 3072
RAM	$3C00\text{-}3FFF_{16}$	1024	114

Up to 48K bytes may be added using optional RAM, ROM, or PROM expansion boards and the SBC 604 Cardcage.

I/O ADDRESSING

Ports E4 to E7 are dedicated to PROMPT's display/keyboard groups. Ports E8 to EB drive the panel I/O PORTS CONNECTOR and PROM SOCKET.

	Dedicated to Display/Keyboard				I/O Ports Connector PROM Socket				Serial I/O USART	
	A	B	C	Control	A	B	C	Control	Data	Control
PORT	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED

PARALLEL I/O

The panel I/O ports can be defined input or output by outputing control words to port address EB.

HEX Control Word (OUT this to EB)	Port E8 Bits 7–0	Port E9 Bits 7–0	Port EA Bits 7–4	Port EA Bits 3–0
80	OUTPUT	OUTPUT	OUTPUT	OUTPUT
81	OUTPUT	OUTPUT	OUTPUT	INPUT
82	OUTPUT	INPUT	OUTPUT	OUTPUT
83	OUTPUT	INPUT	OUTPUT	INPUT
84 or 85	OUTPUT	STROBED OUTPUT	OUTPUT	Bits 2, 1, 0 are strobes
86 or 8	OUTPUT	STROBED INPUT	OUTPUT	

All input ports are TTL-compatible. Ports E8 and EA are one-load fully TTL-compatible as output. Port E9 is ordinarily used as input. When used as output, E9 can sink at least one low-power TTL load.

SERIAL I/O

The serial I/O port is defined by software and jumper. PROMPT is configured at the factory for 20 mA current loop TTY interface, but can easily be jumpered for RS-232C levels.

Asynchronous or synchronous transmission, data format, control characters, parity and transmission rate can be programmed.

INTERRUPTS

PROMPT 80/85 provides a panel user interrupt to $3C02_{16}$. The SBC 80/10 supports single level vectoring to location 38_{16}. Requests may originate from user-specified I/O (2), the parallel ports (2), or serial port (2).

EPROM PROGRAMMING

8708/2708/2704 EPROMs can be programmed in multiple blocks of 16 bytes. Starting and ending memory address need only differ by a multiple of 16, and starting EPROM address end XX0 hexadecimal (X = don't care). Programming time is 115 sec for 1K byte, 3 sec for 16 bytes.

8755 EPROMs can be programmed at any addresses using the optional PROMPT 875 adaptor. Programming time is 52 sec for 1 1K byte.

EPROMs may be erased by exposure to high intensity short-wave ultraviolet light at a wavelength of 2537Å. The recommended integrated dose (UV intensity x exposure time) is 10W-sec/cm^2.

SYSTEM MONITOR

Resides in three 8308 ROMs, 0 to $3FF_{16}$, 400_{16} to $7FF_{16}$, and 800_{16} to BFF_{16}. The third ROM implements F FUNCTIONS, and can be removed. PROMPT has an unused ROM/EPROM socket at address $C00_{16}$ to FFF_{16}.

COMMANDS

Examine/Modify Register
Go (with optional breakpoints)
Scroll Register Display
Next □
Display/Modify Memory
Single Step
Open Previous/Clear Entry
□ Execute/end

FUNCTIONS

0 Read Tape
1 Write Tape
2 Program 8708, Compare
3 Compare 8708
4 Transfer 8708 to RAM
5 Move Block Memory
6 Hexadecimal Calculator, +, –
7 Byte Search Memory, optional mask
8 Word Search Memory, optional mask

With 875 adaptor:
9 Program 8755, Compare
A Compare 8755
B Transfer 8755

SOFTWARE DRIVERS

Panel Keyboard Input
Console Terminal Input
TTY Reader Input
Panel Display Output
Console Terminal Output
TTY Punch Output

CONNECTORS

PROMPT Panel I/O Ports	3M 3425 Flat
SBC 80/10 Parallel I/O	3M 3415 Flat
SBC 80/10 Serial I/O	3M 3462 Flat
SBC 80/10 Bus	CDC VPB01E43D00A1
SBC 80/10 Auxiliary Bus	TI H312130

EQUIPMENT SUPPLIED

PROMPT 80/85 mainframe with SBC 80/10, display/keyboard, PROM Programmer, power supply, cabinet, and ROM-based system monitor
(2) 8708 EPROMs with pre-recorded example programs
110 VAC power cable, 110 or 220 VAC fuse
PROMPT 80/85 User's Manual, PROMPT 80/85 Monitor Listing
PROMPT 80/85 Programming Pads
8080 Systems User'S Guide, 8080 Assembly Language Manual
System 80/10 Hardware Reference Manual
Design Library of Application Notes, Article Reprints
PROMPT 80 Schematics

PHYSICAL CHARACTERISTICS

Maximum Height:	13.5 cm	(5.3 in.)
Width:	43.2 cm	(17 in.)
Maximum Depth:	43.2 cm	(17 in.)
Weight:	9.6 kg	(21 lb)

ELECTRICAL REQUIREMENTS

Either 115 or 230 VAC (±10%) may be switch-selected on the mainframe. 1.8 amps max current (at 125 VAC).
Frequency is 47-63 Hz.

Voltage	Internal PROMPT 80/85 Supply	PROMPT 80/85 Requires
+26.5	0.1A	0.03A
+12	1.2A	0.5A
+ 5	6.0A	5.0A
– 5	0.3A	0.1A
–12	0.3A	0.2A

Fixed over-voltage protect on 5V supply 6.2-6.7 volts.

ENVIRONMENTAL

Operating Temperature: 10°C to 40°C
Non-Operating Temperature: –20°C to 65°C

ORDERING INFORMATION, COMPATIBLE EQUIPMENT

PROMPT-80 or PROMPT-80-220V	Intellec PROMPT 80/85 MCS80/85 Micro-Computer Design Aid. Complete with SBC 80/10 Single Board Computer (8080 CPU), integral keyboard, displays and EPROM programmer.
PROMPT-875	Optional 8755 programming adaptor.
PROMPT-SER	Serial Cable connects PROMPT to TTY, CRT.
PROMPT-SPP	Specialized PROM Programmer Kit connects PROMPT 80/85 to Intellec Microcomputer Development Systems for 8708/8755 EPROM programming.

ICE-30™
3001 MCU IN-CIRCUIT EMULATOR

Extends the Intellec® diagnostic capabilities into user configured systems, allowing in-circuit emulation of the user system's 3001 MCU

Direct Intellec® System connection to the user configured system is achieved via an external cable with 3001 compatible 40-pin connector

Provides for the display of all 3001 address, status, and control lines for the current micro-instruction executed.

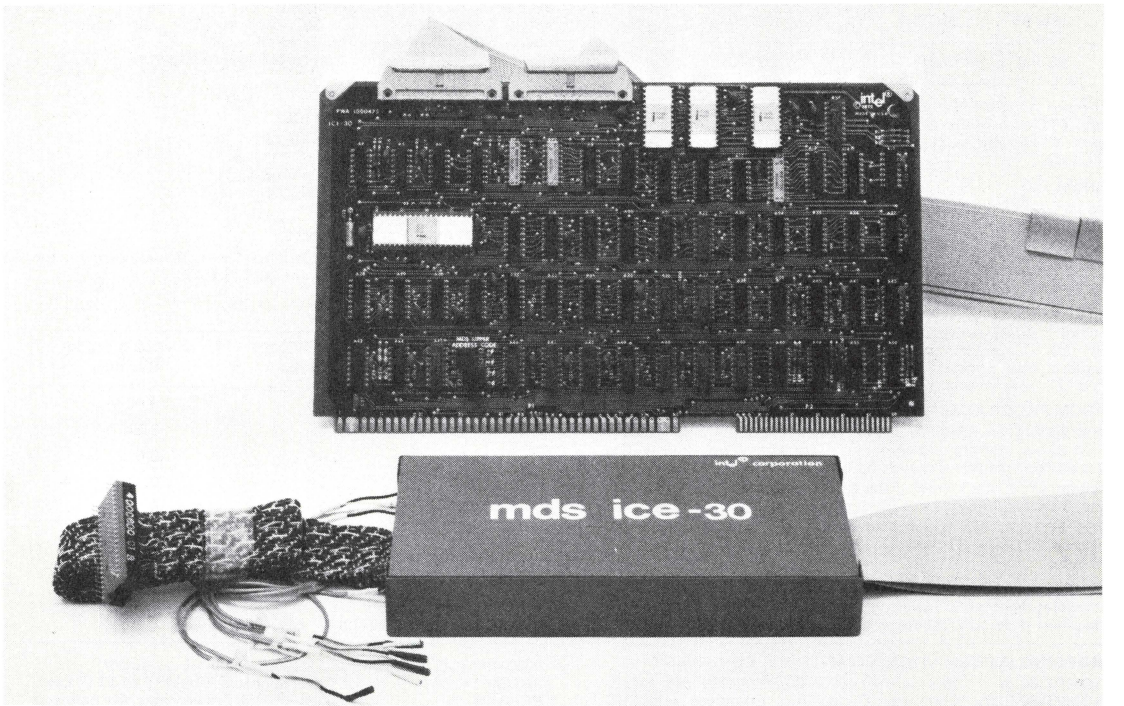
Allows for single-step microprogram execution

Presets the 9-bit 3001 Microprogram Address Register and sets two independent breakpoints on micro-instruction addresses generated by the 3001

Allows two independent breakpoints to be set on the logical combination of any three TTL compatible signals in the user system via three logic probes

Allows the microprogram word contents to be displayed and modified when used with the optional ROM-SIM modules

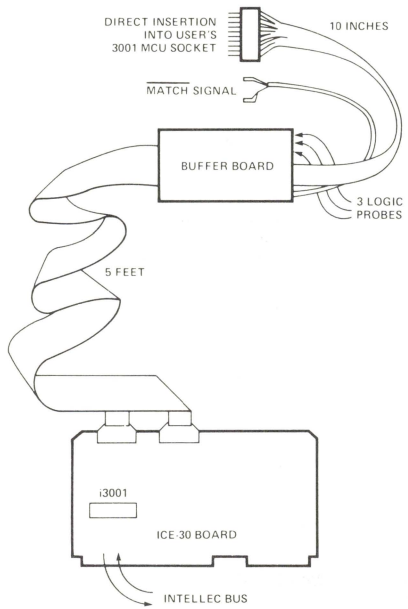
ICE-30 is an Intellec resident module that provides the user with direct in-circuit emulation of the 3001 Microprogram Control Unit (MCU) and complete control over the execution of user developed microprograms. Through in-circuit emulation, the designer is able to set microprogram address breakpoints, single-step microprogram execution, and monitor all of the address, status, and control lines of the 3001.



HARDWARE

ICE-30 consists of a single PC board that resides in the Intellec System. An external cable from the board, terminating in a 3001 compatible 40-pin connector, forms the interface to the user system. Through the 3001 compatible connector, ICE-30 plugs directly into the user system's 3001 socket and allows the user to completely monitor and control all the activities of the MCU.

The figure below shows the hardware supplied with the ICE-30 package.



ICE-30 MODULE HARDWARE

By inserting the board into the Intellec Bus inside a basic Intellec system, a 3001 MCU chip in the user's system may be emulated. The ICE-30 board contains a 3001 MCU and peripheral logic required to monitor the 3001 operation and store trace information. The external cable carries status and control lines to and from the 3001 compatible 40-pin connector and the three logic probe lines. In addition, a MATCH line is brought out on the external cable which allows ICE-30 to control the user system's master clock and perform microprogram halt and single-step functions.

SOFTWARE

The ICE-30 Software Driver, ICE30SD, is an Intellec Microcomputer Development System RAM-resident program which provides a user interface with the ICE-30 hardware. ICE30 recognizes a set of commands issued by the user, translates the commands, and places the encoded results into a control block for the hardware. In this fashion, the user can establish a dialogue with the 3001 Microcomputer Control Unit (MCU) which is connected to the system, thus providing the capability to monitor, control or alter its operation.

ICE30 is capable of operating in conjunction with a RAM-based microprogram in the optional ROM-SIM modules (see ROM-SIM Data Sheet #98-211A). The commands provided by ICE30SD may therefore be divided into three categories: (1) Those commands unique to the optional ROM simulator, (2) Those which support ICE30SD functions, and (3) Those commands which are common to both ROM-SIM and ICE30SD.

ICE30 FUNCTION COMMANDS

SET	Assign values to the two hardware breakpoint registers, the 9-bit microprogram address register, and the PR latch.
GO	Initiates real-time emulation which continues until an address encountered matches one of the two breakpoint values.
STEP	Causes execution to proceed in a non-real-time single-step micro-instruction mode.
CONTINUE	Resumes step mode execution following a break condition.
ENABLE	Activates or deactivates the two hardware breakpoint registers prior to issuing the 'GO' command.
TRAP	Used to set or remove any of the five-step mode software traps (software breakpoint registers).

COMMON COMMANDS

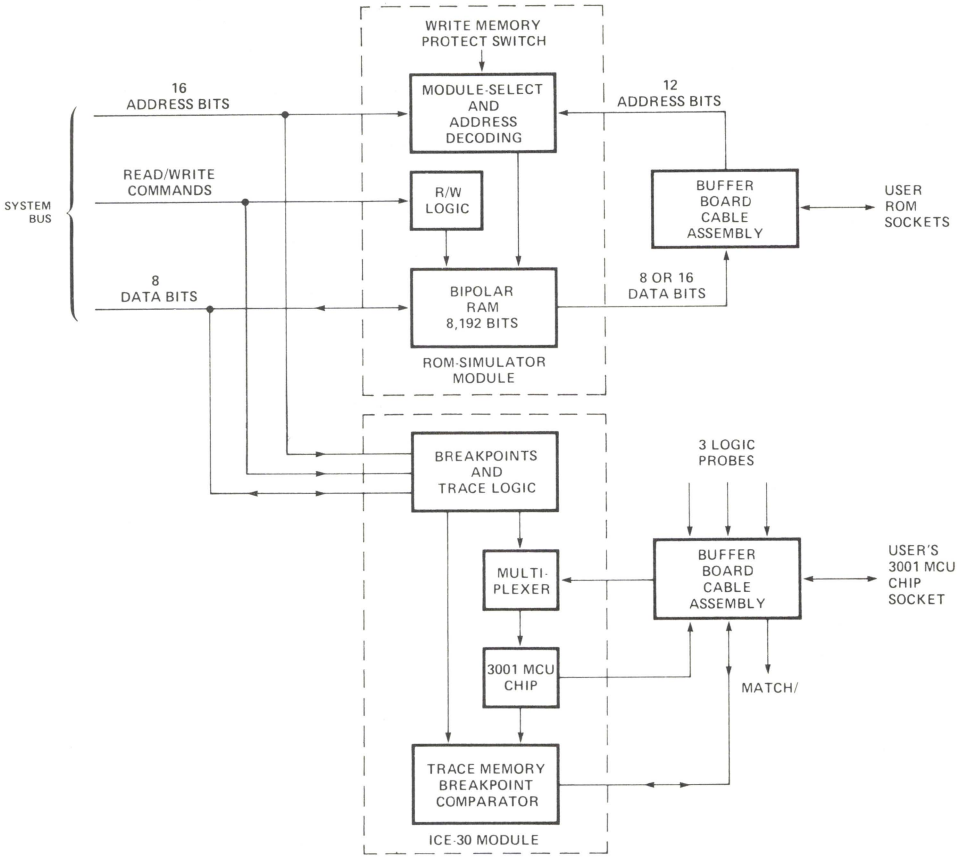
(Common to ICE30 and Optional ROM-SIM)

DISPLAY	Displays the contents of a specified address or address range in the simulated control storage.
BASE	Establishes a mode of display of all output data for the 'DISPLAY' command.
RESTART	Reinitializes all program variables, except the ROM-SIM configuration values, and starts execution at the point following the ROM-SIM configuration sequence.
EXIT	Causes ICE30SD to terminate.

ROM-SIM COMMANDS

ICE30SD provides commands necessary to drive the optional Intellec microprogram control storage simulation module, ROM-SIM. For a description of ROM-SIM capabilities, ask for the ROM-SIM Data Sheet #98-211A.

ICE30SD is written in Intel's high-level programming language PL/M and will execute in the minimum 16K RAM Intellec configuration.



FUNCTIONAL BLOCK DIAGRAM OF ICE-30 MODULE, OPERATING IN CONJUNCTION WITH ROM-SIMULATOR MODULE

SPECIFICATIONS

PHYSICAL CHARACTERISTICS

(Printed Circuit Board)

Width: 12.00 in.
Height: 6.75 in.
Depth: 0.50 in.

EQUIPMENT SUPPLIED

Printed Circuit Board
Interface Cables and
Buffer Enclosure Assembly
Reference Manual
Software Paper Tape

MPU SYSTEM SUPPORT

ORDERING INFORMATION

Part Number	Description
MDS-30-ICE	3000 Series In-Circuit Emulator

ICE-41™
UPI-41™ IN-CIRCUIT EMULATOR

Extends Intellec® Microcomputer Development System debug power to user configured system via an external cable and 40-pin plug, replacing the user UPI-41 device

Emulates user system UPI-41 device in real time

Allows user configured system to use static RAM memory for program debug

Provides hardware comparators for user designated break conditions

Eliminates the need for extraneous debugging tools residing in the user system

Collects address, data and UPI-41 status information on machine cycles emulated

Provides capability to examine and alter CPU registers, memory, flag values, and to examine pin and port values

Integrates hardware and software efforts early to save development time

The ICE-41™ Module is an Intellec® System resident module that interfaces to any user configured UPI-41 system. With an ICE-41 Module as a replacement for a prototype system UPI-41 device, the designer can emulate the system UPI-41 device in real time, single-step the system's program, and use internal static RAM memory for user system debugging. Powerful debug capability is extended into the UPI-41 system while ICE-41 debug hardware and software remain inside the Intellec System. Symbolic reference capability allows the designer to use meaningful symbols rather than absolute values when examining and modifying memory, registers, flags, and I/O ports in his system.

Attempting to mesh completed hardware and software in the final product can be costly and frustrating. The ICE-41 Module allows the designer to use his hardware and software to help debug each other as they are developed.

Hardware comparators provide the capability for breaking system emulation under specified conditions. An additional synchronization line allows the ICE-41 Module to break emulation on a condition outside the scope of the UPI-41 device, or, alternatively, allows the ICE-41 to signal an external device when a condition is recognized by the hardware comparators.

Static RAM memory is provided for program development. Programs can be easily altered during debug sessions without the need for program reassembly and the reprogramming of PROM memory. Internal UPI-41 registers and flags are accessible to the designer for checking program logic.

A trace buffer stores information on code executed, address, register, flag, and I/O operations during real time execution. The designer can examine this information after emulation is terminated to check the hardware/software interaction of his system.

The ICE-41 Module is a microcomputer system utilizing Intel's UPI-41 microprocessor as its nucleus. This system communicates with the Intellec System 8080 processor via direct memory access. Host processor commands and ICE-41 status are interchanged through a DMA channel. A parameter block resident in Intellec System main memory contains detailed configuration and status information transmitted in an emulation break.

ICE-41 hardware consists of two PC boards, which reside in the Intellec System chassis, and a cable assembly which interfaces to the user system. A 40-pin socket on the end of the cable assembly plugs directly into the socket provided for the user's UPI-41 device.

The ICE-41 software is an Intellec System program which provides the user with flexible, easy-to-use commands for defining breakpoints, initiating emulation, and interrogating and altering user system status recorded during emulation. A broad range of commands provides the user with maximum flexibility in describing the operation to be performed.

SPECIFICATIONS

ICE-41 OPERATING ENVIRONMENT

Required Hardware:
- Intellec® Microcomputer Development System
- System Console
- Intellec Diskette Operating System
- ICE-41 Module

Required Software:
- System Monitor
- ISIS-II
- ICE-41 Diskette-Based Software

EQUIPMENT SUPPLIED

Printed Circuit Boards
Interface Cables and Buffer Module
Operator's Manual
Schematic Diagram
ICE-41 Diskette-Based Software

ORDERING INFORMATION

Part Number	Description
MDS-41-ICE	UPI-41 In-Circuit Emulator, Cable Assembly and Interactive Diskette Software included

ICE-48™
MCS-48™ IN-CIRCUIT EMULATOR

Extends Intellec Microcomputer Development System debug power to user configured system via an external cable and 40-pin plug, replacing the system MCS-48 device

Emulates user system MCS-48 device in real time

Shares static RAM memory with user system for program debug

Provides hardware comparators for user designated break conditions

Eliminates the need for extraneous debugging tools residing in the user system

Collects bus, register and MCS-48 status information on instructions emulated

Provides capability to examine and alter MCS-48 registers, memory, flag values, and to examine pin and port values

Integrates hardware and software efforts early to save development time

The ICE-48 module is an Intellec-resident module that interfaces to any MCS-48 system. The MCS-48 family consists of the 8048, 8748, and 8035 microcomputers. The ICE-48 module interfaces with an MCS-48 system through a cable terminating in an MCS-48 pin-compatible plug which replaces the MCS-48 device in the system. With the ICE-48 plug in place, the designer has the capability to execute the system in real time while collecting up to 255 instruction cycles of real time trace data. In addition, he can single step the system program to monitor more closely the program logic during execution. Static RAM memory is available through the ICE-48 module to emulate MCS-48 program and data memory. The designer can display and alter the contents of data and replacement RAM control memory, internal MCS-48 registers and flags; and I/O ports. Powerful debug capability is extended into the MCS-48 system while ICE-48 debug hardware and software remain inside the Intellec System. Symbolic reference capability allows the designer to use meaningful symbols rather than absolute values when examing and modifying memory, registers, flags, and I/O ports in this system.

DEBUG CAPABILITY INSIDE USER SYSTEM

The ICE-48 module provides the user with the ability to debug a full prototype or production system without introducing extraneous hardware or software test tools.

The ICE-48 module connects to the user system through the socket provided for the MCS-48 device in the user system. Intellec memory is used for the execution of the ICE-48 software. The Intellec console and file handling capabilities provide the designer with the ability to communicate with the ICE-48 module and display information on the operation of the prototype system.

BATCH TESTING

In conjunction with the ISIS-II diskette operating system, the ICE-48 module can run extensive system diagnostics without operator intervention. The designer or test engineer can define a complete diagnostic exercise which is stored in a file on the diskette. When activated with an ISIS-II SUBMIT command, this file can instruct the ICE-48 module to execute the diagnostic routine and store the results in another file on the diskette. Results are available to the designer at his convenience. In this way, routine diagnostics and long term testing can be done without tying up valuable manpower.

INTEGRATED HARDWARE/SOFTWARE DEVELOPMENT

The user prototype need consist of no more than an MCS-48 socket and timing logic to begin integration of software and hardware development efforts. Through the ICE-48 module mapping capabilities, Intellec system resources can be accessed to replace prototype memory. Hardware designs can be tested using the system software which will drive the final product.

The system integration phase, which can be costly when attempting to mesh completed hardware and software products, becomes a convenient two-way debug tool when begun early in the design cycle.

REAL TIME TRACE

The ICE-48 module captures trace information while the designer is executing programs in real time. The instructions executed, program counter, port values for Port 0, Port 1, and Port 2, and the values of selected MCS-48 status lines are stored for the last 255 instruction cycles executed. When retrieved for display, code is disassembled for user convenience. This provides data for determining how the user system was reacting prior to emulation break. It is available whether the break was user initiated or the result of an error condition.

For detailed information on the actions of internal registers, flags, or other system operations, the user may operate in single or multiple-step sequences tailored to system debug needs.

MEMORY MAPPING

The 8748 and 8048 contain internal program and data memory. Both program and data memory can be expanded using external memory devices.

When the MCS-48 microcomputer is replaced by the ICE-48 socket in a system, the ICE-48 module supplies static RAM memory as a replacement for the internal microcomputer memory. The ICE-48 module has enough RAM memory available to emulate up to the total 4K control memory capability of the system. The ICE-48 module also provides for up to 320 bytes of data memory.

The ICE-48 module separates replacement control memory into 16 256-byte blocks. Replacement external data memory consists of one 256-byte block. Each block of memory can be defined separately as supplied by the user system or supplied by the ICE-48 module. The user may assign ICE-48 equivalent memory to take the place of external memory not yet supplied in his system.

During final debug stages when external or resident 8748 PROM is used for program execution, the designer can load the program back to ICE-48 memory to test out program changes before reassembly and reprogramming the PROM.

SYMBOLIC DEBUGGING

ICE-48 software provides symbolic definition of all MCS-48 registers, flags, and selected MCS-48 pins. Symbolically defined pseudo registers provide access to the sense of MCS-48 flipflops which enable time, counter, interrupt, and Flag 0/Flag 1 options.

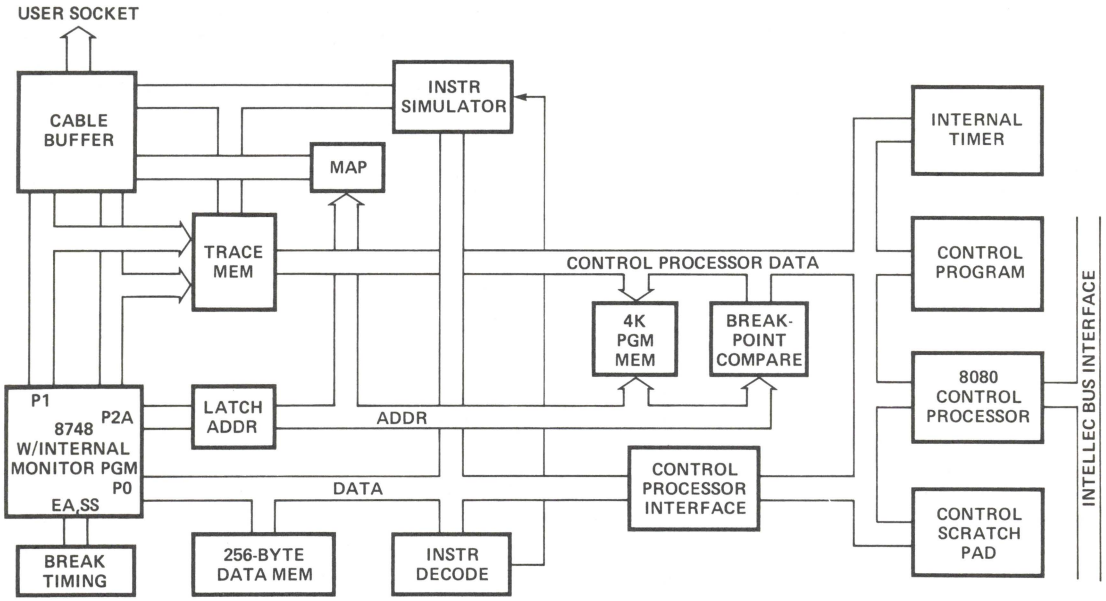
In addition, the user may reference locations in program and data memory, or their contents, symbolically. The user symbol table which is generated along with the object file during a program assembly may be loaded to Intellec memory for access during emulation. The user is encouraged to add to this symbol table any additional symbolic values for memory addresses, constants, or variables that he may find useful during system debugging. Symbols may be substituted for numeric values in any of the ICE-48 commands.

Symbolic reference is a great advantage to the system designer. He is no longer burdened with the need to recall or look up addresses of key locations in his program which can change with each assembly. Meaningful symbols from his source program can be used instead. For example, the command:

GO FROM . START TILL XDATA . RSLT WRITTEN

begins execution of the program at the address referenced by the label START in the designers assembly program. A breakpoint is set to occur the first time the microprocessor writes to the external data memory location referenced by RSLT. The designer does not have to be concerned with the physical locations of START and RSLT. The ICE-48 software driver supplies them automatically from information stored in the symbol table.

ICE-48 MODULE BLOCK DIAGRAM



HARDWARE

The ICE-48 module is a microcomputer system utilizing Intel's 8748 microcomputer as its nucleus. The 8748 provides the MCS-48 emulation characteristics. The ICE-48 module uses an Intel® 8080 to communicate with the Intellec host procesor via a DMA port. The 8080 also controls an internal ICE-48 bus for intramodule communication.

ICE-48 hardware consists of two PC boards, the Controller Board and the Emulator Board, which reside in the Intellec chassis. A cable interfaces the ICE-48 boards to the MCS-48 system. The cable terminates in a MCS-48 pin compatible plug which replaces any MCS-48 device in the user system.

REAL TIME TRACE

While the ICE-48 module is executing the user program, it is monitoring port, program counter, data and status lines. Values for each instruction cycle executed are stored in a 255 x 44 real time RAM trace buffer. A resetable timer resident on the Controller Board counts instruction cycles and provides timing for the trace monitor.

CONTROLLER BOARD

The ICE-48 module talks to the Intellec System as a peripheral device. The Controller Board receives commands from the Intellec System and responds through a DMA port.

Three 15-bit hardware breakpoint registers are available which can be loaded by the user. While in emulation mode, a hardware comparator is constantly monitoring address and status lines for a match which will terminate an emulation.

The breakpoint registers provide a signal when a match is detected. The user can disable the emulation break capability and use the signal to synchronize other debug tools.

The Controller Board returns real time trace data, MCS-48 register, flag, and pin values, and ICE-48 status information, to a control block in the Intellec System when emulation is terminated. This information is available to the user through the ICE-48 interrogation commands. Error conditions, when present, are automatically displayed on the Intellec System console.

The Controller Board also contains static RAM memory which can be used to emulate MCS-48 program and data memory in real time. 4K of memory is available in 16 256-byte pages to emulate MCS-48 PROM or ROM program memory. A 256-byte page of data memory is available to access in place of MCS-48 external data memory. The Controller Board address map directs the ICE-48 module to access either replacement ICE-48 memory or actual user system external memory in 256 byte segments based on information provided by the user.

EMULATOR BOARD

The Emulator Board contains the 8748 and peripheral logic required to emulate the MCS-48 device in the user system. A software selectable 6 MHz or 3 MHz clock drives the emulated MCS-48 device. This clock can be disabled and replaced with a user supplied TTL clock in the user system.

CABLE CARD

The Cable Card is included for cable driving. It transmits address and data bus information to the user system through a 40-pin connector which plugs into the user system in the socket designed for the MCS-48 device.

SOFTWARE

The ICE-48 software driver is a RAM-based program which provides the user with an easy-to-use command language for defining breakpoints, initiating real time emulation or single step operation, and interrogating and altering user system status recorded during emulation. The ICE-48 command language contains a broad range of modifiers which provide the user with maximum flexibility in defining the operation to be performed.

The ICE-48 software driver is available on diskette and operates in 32K of Intellec RAM memory.

ICE-48 COMMANDS

EMULATION COMMANDS:

ENABLE	Activates breakpoint and display registers for use with GO and STEP commands.
GO	Initiates real-time emulation and allows user to specify breakpoints, and data retrieval.
STEP	Initiates emulation in single instruction increments. Each step is followed by a register dump. The user may optionally tailor other diagnostic activity to his needs.
INTERRUPT	Emulates user system interrupt.

INTERROGATION COMMANDS:

DISPLAY	Print contents of memory, MCS-48 device registers, I/O ports, flags, pins, real time trace data, symbol table, or other diagnostic data on list device.
CHANGE	Alter contents of memory, register, output port, or flag. Set or alter breakpoints and display registers.
MAP	Define memory status.
BASE	Establish mode of display for output data.
SUFFIX	Establish mode of display input data.

UTILITY COMMANDS:

LOAD	Fetch user symbol table and object code from input device.
SAVE	Send user symbol table and object code to output device.
DEFINE	Enter symbol name and value to user symbol table.
MOVE	Move block of memory data to another area of memory.
LIST	Define list device.
EXIT	Return program control to ISIS II.
EVALUATE	Convert expression to equivalent values in binary, octal, decimal, and hex.
REMOVE	Delete symbols from symbol table.
RESET	Reinitialize ICE-48 program variables.

SPECIFICATIONS

ICE-48 OPERATING ENVIRONMENT

Diskette-Based ICE-48 Software
Required Hardware:
- Intellec® Microcomputer Development System
- System Console
- Intellec Diskette Operating System
- ICE-48 Module

Required Software:
- System Monitor
- ISIS-II

EQUIPMENT SUPPLIED

Printed Circuit Boards
Interface Cables and Buffer Module
Operator's Manual
Schematic Diagram
ICE-48 Software, diskette-based version

SYSTEM CLOCK

Crystal controlled 6.0 MHz internal, 3.0 MHz internal or user supplied TTL external: software selectable.

PHYSICAL CHARACTERISTICS

Width:	12.00 in. (30.48 cm)
Height:	6.75 in. (17.15 cm)
Depth:	0.50 in. (1.27 cm)
Weight:	8.00 lb. (3.64 kg)

ELECTRICAL CHARACTERISTICS

DC Power:
- V_{CC} = ±5V. ±5%
- I_{CC} = 10A maximum; 7.0A typical
- V_{DD} = +12V. ±5%
- I_{DD} = 79 mA maximum; 45 mA typical
- V_{BB} = -10V
- I_{BB} = 20 mA

ENVIRONMENTAL CHARACTERISTICS

Operating Temperature:	0°C to 40°C
Operating Humidity:	Up to 95% relative humidity without condensation

ORDERING INFORMATION

Part Number	Description
MDS-48-ICE	8048 CPU In-Circuit Emulator, Cable Assembly and Interactive Diskette Software included

MDS-EM1
8021 EMULATION BOARD

- EPROM functional equivalent of 8021 — single component 8-bit microcomputer
- Based on 8748 — user programmable/erasable EPROM 8-bit computer
- Operates with ICE-48™ to provide full in-circuit debugging of 8021 prototype system
- Connects to prototype system through 8021 pin compatible plug
- On-card 3.0 MHz or external TTL driven clock
- Portable 4" × 7" microcomputer circuit assembly

The MDS-EM1 emulator board is a ready-to-use 4" × 7" microcomputer circuit assembly that emulates the Intel 8021 microcomputer. A 12-inch flat-cable assembly connects the board to the 8021 socket in a prototype system. The board is designed so that it can be mounted either as a stand-alone unit, or within the prototype assembly.

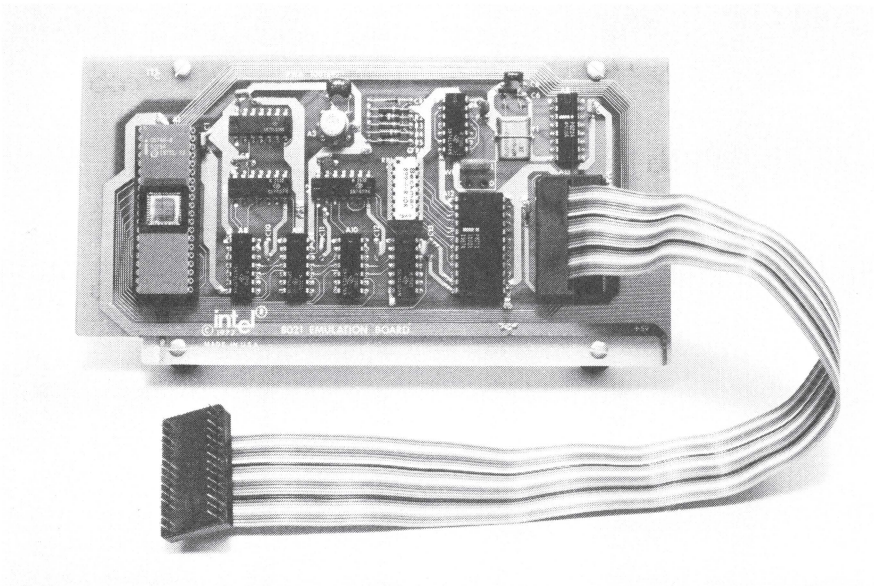
The 8021 microcomputer has 1K × 8 mask-programmable ROM program memory and 64 by 8 RAM data memory. The MDS-EM1 is controlled by an Intel 8748, with 1K of EPROM program memory and a 64 byte data memory. The EPROM can be programmed and erased repeatedly during hardware and software development. The MDS-EM1 has several ancillary circuits that perform the following functions which are specific to the 8021:

Zero crossing detector

Crystal controlled clock/buffer

Port Ø simulator

For prototype debugging, the 8748 can be removed from its socket and replaced with a cable to an INTEL ICE-48. When used with the MDS-EM1, ICE-48 emulates the 8021 in real-time, or single-steps the 8021 program at the user's command. A full range of capabilities for examining and modifying 8021 memory and status are supplied through ICE-48.



HARDWARE

The MDS-EM1 emulation board uses the 8748 to perform the emulation.

PØ SIMULATOR

Port Ø of the 8021 is a quasi*-bidirectional port. The PØ simulator converts the data bus of the 8748 into a quasi-bidirectional port.

CRYSTAL CONTROL CLOCK BUFFER

The MDS-EM1 allows user to select an on-board oscillator or a TTL clock driven from the 8021 user's prototype system via a Cambion Suitcase jumper.

Jumper	Position	State
W1	A – B	On-Board
	C – D	External TTL Clock

*A bidirectional port which serves as an input port, output port, or both even though outputs are statically latched.

ZERO CROSS DETECTION SIMULATOR

The zero cross detection simulator enables the 8748's T1 input to detect zero-crossings. The circuitry provides a high level signal on a positive crossing and a low level signal on a negative crossing of zero to the T1 input of the 8748.

RESET BUFFER

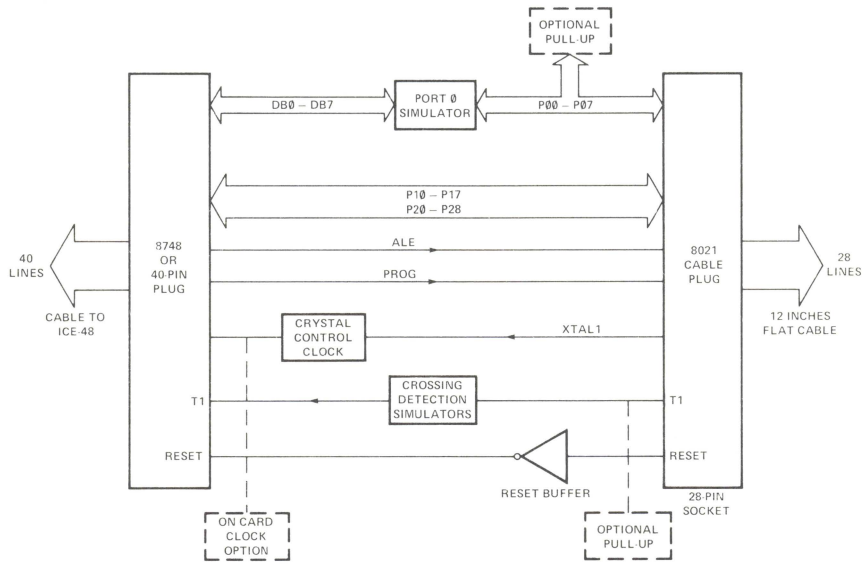
The 8021 resets on a logic HIGH level signal. However, the 8748 resets on a logic LOW level, thus an inverter is provided on the MDS-EM1 to make the two chips compatible.

OPTIONAL PULL-UPS

Resistors are provided to simulate the optional pull-up resistors on T1 input and Port Ø of the 8021. A removable resistor pack is used on Port Ø. The T1 input pull up can be installed by soldering in a 50K resistor.

SOFTWARE

When emulating the 8021 with MDS-EM1, the user must observe the 8021 instruction set.



MDS-EM1 FUNCTION DIAGRAM

SPECIFICATIONS

OPERATING ENVIRONMENT

Stand-Alone

Required Hardware:

MDS-EM1 emulation board

In-Circuit Emulation

Required Hardware:

MDS-EM1 emulation board

Intellec Microcomputer Development System configurated to support ICE-48

EQUIPMENT SUPPLIED

MDS-EM1 printed circuit board

12" long flat cable terminating in 28-pin plug, pin compatible with 8021

MDS-EM1 Operator's Manual

SYSTEM CLOCK

Crystal controlled 3.0 MHz on board or user supplied TTL external clock: hardware jumper selectable.

PHYSICAL CHARACTERISTICS

Width:	7.0 in. (17.78 cm)
Height:	4.0 in. (10.16 cm)
Depth:	0.75 in. (1.91 cm)
Weight:	<1.0 lbs. (0.45 kg)

ELECTRICAL CHARACTERISTICS

DC Power:

V_{CC} 5V ± 5%

I_{CC} 300 mA (max.)

ENVIRONMENTAL CHARACTERISTICS

Operating Temperature: 0 – 55°C

Operating Humidity: up to 95% relative humidity without condensation

ORDERING INFORMATION

Part Number	Description
MDS-EM1	8021 Emulation Board

ICE-80™
8080 IN-CIRCUIT EMULATOR

Connects Intellec® System to user configured system via an external cable and 40-pin plug, replacing the user 8080

Allows real-time (2 MHz) emulation of the user system 8080

Allows user configured system to share Intellec RAM, ROM and PROM memory and Intellec I/O facilities

Checks for up to three hardware and four software break conditions

Offers full symbolic debugging capabilities

Eliminates the need for extraneous debugging tools residing in the user system

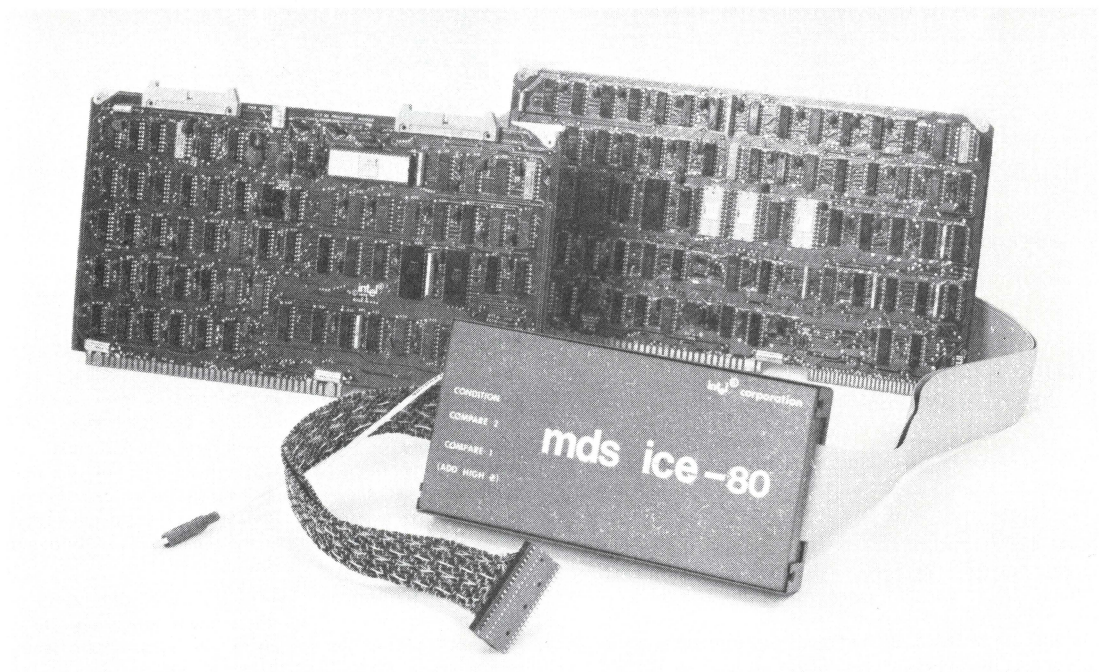
Provides address, data and 8080 status information on last 44 machine cycles emulated

Provides capability to examine and alter CPU registers, main memory, pin and flag values

Integrates hardware and software development efforts

Available in diskette or paper tape versions

The Intellec In-Circuit Emulator/80 (ICE-80) is an Intellec resident module that interfaces to any user configured 8080 system. With ICE-80 as a replacement for a prototype system 8080, the designer can emulate the system's 8080 in real time, single-step the system's program, and substitute Intellec memory and I/O for user system equivalents. Powerful Intellec debug functions are extended into the user system. For the first time the designer may examine and modify his system with symbolic references instead of absolute values.



INTEGRATED HARDWARE/ SOFTWARE DEVELOPMENT

The user prototype need consist of no more than an 8080 CPU socket and a user bus to begin integration of software and hardware development efforts. Through ICE-80 mapping capabilities, system resources can be accessed for missing prototype hardware. Hardware designs can be tested using the system software which will drive the final product.

The system integration phase, which can be so costly and frustrating when attempting to mesh completed hardware and software products, becomes a convenient two-way debug tool when begun early in the design cycle.

SYMBOLIC DEBUGGING

ICE-80 allows the user to make symbolic references to memory addresses and data in his program. Symbols may be substituted for numeric values in any of the ICE-80 commands. The user is relieved from looking up addresses of variables or program subroutines.

The user symbol table generated along with the object file during a PL/M compilation or a MAC80 or resident assembly, is loaded to memory along with the user program which is to be emulated. The user may add to this symbol table any additional symbolic values for memory addresses, constants, or variables that are found useful during system debugging. By referring to symbolic memory addresses, the user can be assured of examining, changing, or breaking at the intended location.

ICE-80 provides symbolic definition of all 8080 registers, flags, and selected pins. The following symbolic references are also provided for user convenience: TIMER, a 16-bit register containing the number of ϕ_2 clock pulses elapsed during emulation; ADDRESS, the address of the last instruction emulated; INTERRUPTENABLED, the user 8080 interrupt mechanism status; and UPPERLIMIT, the highest RAM address that can be occupied by user memory.

DEBUG CAPABILITY INSIDE USER SYSTEM

ICE-80 provides the user with the ability to debug a full prototype or production system without introducing extraneous hardware or software test tools.

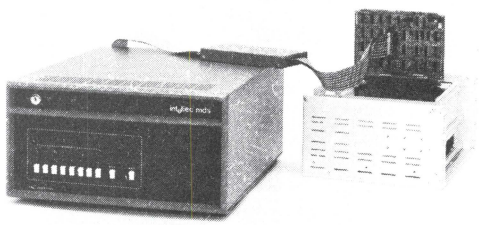
ICE-80 connects to the user system through the socket provided for the user 8080 in the user system. Intellec memory is used for the execution of the ICE-80 software, while I/O provides the user with the ability to communicate with ICE-80 and receive information on the operation of the user system.

MEMORY AND I/O MAPPING

Memory and I/O for the user system can be resident in the user system or "borrowed" from the Intellec System through ICE-80's mapping capability.

ICE-80 separates user memory into 16 4K blocks. User I/O is divided into 16 16-port blocks. Each block of memory or I/O can be defined independently. The user may assign system equivalents to take the place of devices not yet designed for the user system during prototyping. In addition, memory or I/O can be accessed in place of suspect user system devices during prototype or production checkout.

The user can also designate a block of memory or I/O as nonexistent. ICE-80 issues error messages when memory or I/O designated as nonexisting is accessed by the user program.



ICE-80 INSTALLED IN USER SYSTEM

REAL TIME TRACE

ICE-80 captures valuable trace information while the user is executing programs in real time. The 8080 status, the user memory or port addressed, and the data read or written (snap data), is stored for the last 44 machine cycles executed. This provides ample data for determining how the user system was reacting prior to emulation break. It is available whether the break was user initiated or the result of an error condition.

For detailed information on the actions of CPU registers, flags, or other system operations, the user may operate in single or multiple-step sequences tailored to system debug needs.

HARDWARE

The heart of ICE-80 is a microcomptuer system utilizing Intel's 8080 microprocessor as its nucleus. This system communicates with the Intellec® host processor via I/O commands. Host processor commands and ICE-80 status are interchanged through registers on the ICE-80 Trace Board. ICE-80 and the system also communicate through a Control Block resident in the Intellec® main memory which contains detailed configuration and status information transmitted at an emulation break.

ICE-80 hardware consists of two PC boards, the Processor and Trace Boards, residing in the Intellec® chassis, and a 6-foot cable which interfaces to the user system. The Trace and Processor Boards communicate with the system on the bus, and also with each other on a separate ICE-80 bus. ICE-80 connects to the user system through a cable that plugs directly into the socket provided for the user's 8080.

TRACE BOARD

The Trace Board talks to the system as a peripheral device. It receives commands to ICE-80 and returns ICE-80 responses.

While ICE-80 is executing the user program, the Trace Board collects data for each machine cycle emulated (snap data). The information is continuously stored in high-speed bipolar memory.

The Trace Board also contains two 24-bit hardware breakpoint registers which can be loaded by the user. While in emulation mode, a hardware comparitor is constantly monitoring address and status lines for a match which will terminate an emulation. A user probe is also available which can be attached to any user signal. When this signal goes true a break condition is recognized.

The Trace Board signals the Processor Board when a command to ICE-80 or break condition has been detected. The ICE-80 CPU then sends data stored on the Trace Board to the Control Block in memory. Snap data, along with information on 8080 registers and pin status, and the reason for the emulation break are then available for access during interrogation mode. Error conditions, if present, are transmitted and automatically displayed for the user.

PROCESSOR BOARD

An 8080 CPU resides on the Processor Board. During emulation it executes instructions from the user's program. At all other times it executes instructions from the control program in the Trace Module's ROM.

The Processor Board contains an internal Clock Generator that provides the clocks to the user emulation CPU at 2 MHz. The CPU can alternately be driven by a clock derived from user system signal lines. The clock source is selected by a jumper option on the board. A timer on the Trace Board counts the ϕ_2 clock pulses during emulation and can provide the user with the exact timing of the emulation.

The Processor Board turns on an emulation when ICE-80 has received a RUN command from the system. It terminates emulation when a break condition is detected on the Trace Board, or the user's program attempts to access memory or I/O ports designated as nonexistent in the user system, or the user 8080 is inactive for a quarter of a second.

The Address Map located on the Processor Board stores the assigned location of each user memory or I/O block. During emulation the Processor Board determines whether to send/receive information on the Intellec or User bus by consulting the Address Map. The Processor Board allows the ICE-80 CPU to gain access to the bus as a master to "borrow" Intellec facilities. At an emulation break, the Processor Board stores the status of specified 8080 input and output signals, disables all interaction with the user bus, and commands the Trace Board to send stored information to a Control Block in Intellec memory for access during interrogation mode.

CABLE CARD

The Cable Card is included for cable driving. It transmits address and data bus information to the user system through a 40-pin connector which plugs into the user system in the socket designed for the 8080 when enabled by the Processor Module's user bus control logic.

SOFTWARE

The ICE-80 software driver (ICE80SD) is a RAM-based program which provides the user with easy-to-use English language commands for defining breakpoints, initiating emulation, and interrogating and altering user system status recorded during emulation. ICE-80 commands are configured with a broad range of modifiers which provide the user with maximum flexibility in describing the operation to be performed.

ICE80SD is available in both paper tape and diskette-based versions. The diskette-based version, which is supplied on a System Diskette for operation with the Intellec Diskette Operating System, provides expanded capabilities for retrieving and storing user programs, as well as the standard peripherals available in the paper tape version.

EMULATION COMMANDS:

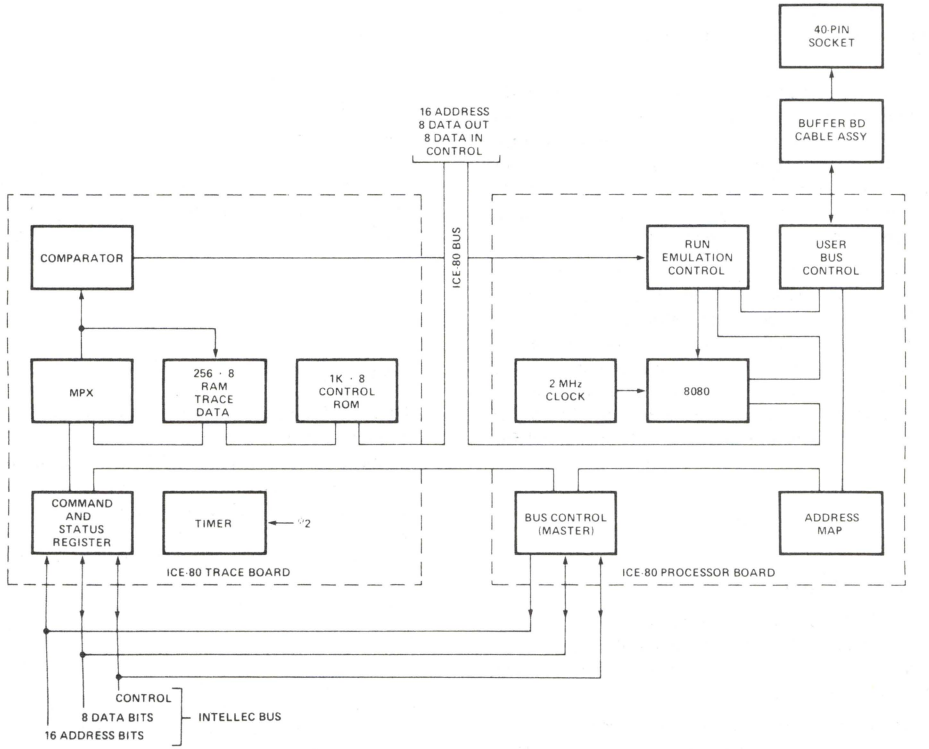
GO	Initiates real-time emulation and allows user to specify breakpoints, data retrieval, and conditions under which emulation should be reinitiated.
STEP	Initiates emulation in single or multiple instruction increments. User may specify a register dump or tailor diagnostic activity to his needs following each step, and define conditions under which stepping should continue.
RANGE	Delimits blocks of instructions for which register dump or tailored diagnostics are to occur.
CONTINUE	Resume real-time emulation.
CALL	Emulate user system interrupt.

INTERROGATION COMMANDS:

BASE	Establish mode of display for output data.
DISPLAY	Print contents of memory, 8080 registers, input ports, 8080 flags, 8080 pins, snap data, symbol table, or other diagnostic data on list device. Can also be used for base-to-base conversion, or addition or subtraction in any base.
CHANGE	Alter contents of memory, register, output port, or 8080 flag.
XFORM	Define memory and I/O status.
SEARCH	Look through memory range for specified value.

UTILITY COMMANDS:

LOAD	Fetch user symbol table and object code from input device.
SAVE	Send user symbol table and object code to output device.
EQUATE	Enter symbol name and value to user symbol table.
FILL	Fill memory range with specified value.
MOVE	Move block of memory data to another area of memory.
TIMEOUT	Enable/disable user CPU 1/4 second wait state timeout.
LIST	Define list device (diskette-based version only).
EXIT	Return program control to monitor.



FUNCTIONAL BLOCK DIAGRAM OF ICE-80 MODULE

SAMPLE, ICE-80 DEBUG SESSION

```
ISIS 8080 MACRO ASSEMBLER, V1.0                    PAGE 1

                ; USER PROGRAM TO OUTPUT A SERIES OF
                ; CHARACTERS TO SDK-80 CONSOLE DEVICE
                ;
1320                    ORG     1320H
01E3            C0      EQU     1E3H    ; SDK-80 CONSOLE OUT DRIVER
                ;
1320 0601       START:  MVI     B,1     ; SET UP B VALUE
1322 3A3613             LDA     DAT1    ; LOAD A WITH DAT1 VALUE
1325 4F         LOOP:   MOV     C,A
1326 CDE301             CALL    C0      ; SEND C VALUE TO CONSOLE
1329 79                 MOV     A,C     ; RESTORE A
132A 93                 SBB     B       ; SUBTRACT B FROM A
132B 323713             STA     RSLT    ; STORE RESULT IN RSLT
132E FE40               CPI     40H     ; LAST VALUE TO PRINT
1330 C22513             JNZ     LOOP    ; LOOP AGAIN IF A =40H
1333 C32013             JMP     START   ; ELSE RESTART WHOLE PROCEDURE
                ;
1336 5A         DAT1:   DB      5AH
1337            RSLT:   DS      1
0000                    END
```

```
ISIS, V1.0      INITIAL ICE-80 SESSION
-ICE80          (Note: The SDK-80 Monitor has already been used to initialize the SDK-80 Board)
ISIS ICE-80, V1.0
① **XFORM MEMORY 0 TO 1 U
  *XFORM IO 0FH U
② *LOAD PROG.HEX
  ERR=067
  STAT=11H TYPE=06H CMND=07H ADDR=1320H GOOD=06H BAD=04H
  *CHANGE MEMORY 1321H=FFH
  ERR=067
  STAT=11H TYPE=06H CMND=07H ADDR=1321H GOOD=FFH BAD=FDH
  *LOAD PROG.HEX
③ *GO FROM START UNTIL RSLT WRITTEN
  EMULATION BEGUN
④ ERR=067
  STAT=11H TYPE=07H CMND=02H
⑤ *DISPLAY CYCLES 5
  STAT=A2H ADDR=1326H DATA=CDH
  STAT=82H ADDR=1327H DATA=E3H
  STAT=82H ADDR=1328H DATA=01H
  STAT=04H ADDR=FFFFH DATA=13H
  STAT=04H ADDR=FFFEH DATA=29H
⑥ *CHANGE DOUBLE REGISTER SP=13FFH
  *BASE HEX
  *EQUATE STOP=1333H
⑦ *GO FROM START UNTIL STOP EXECUTED THEN DUMP
  EMULATION BEGUN
  B=01H C=41H D=00H E=00H H=00H L=00H F=56H A=40H P=1320H *=1333H S=13FFH
  EMULATION TERMINATED AT 1333H
⑧ *EXIT
  *FFFF
```

1. Set up user memory and I/O. The program is set up to execute in block 1 (1000H–1FFFH) of user memory, and requires access to the SDK-80 monitor (block 0) and I/O ports in block 0FH. Both ports and memory are defined as available to the user system. All other memory and I/O is initialized by ICE-80 as nonexistent (guarded).
2. A load command generates an error. The type and command numbers indicate that a data mismatch occurred on a write to memory command. The data to be written to address 1320H should have been 06H. When ICE-80 read the data after writing it, a 04H was detected. A change command to a different memory address hints that bit 1 does not go to 1 anywhere in this memory block. Examination indicates that a pin was shorted on the RAM located at 1300H–13FFH in the prototype system. The problem is fixed and a subsequent load succeeds.
3. A real-time emulation is begun. The program is executed *FROM* 'START' (1320H) and continues *UNTIL* 'RSLT' is written (in location 1328H, the contents of the accumulator is stored in (written into) 'RSLT').
4. An error condition results: TYPE 07, CMND 02 indicate the program accessed a guarded area.
5. The last 5 machine cycles executed are displayed. The last instruction executed was a call (CDH). The fourth and fifth cycles are a push operation (designated by status 04H) to store the program counter before executing the call. The stack pointer was not initialized in the program and is accessing memory location FFFFH.
6. After making a note to initialize the stack pointer in the next assembly, a temporary fix is effected by setting the stack pointer to the top of user available memory.
7. After setting the base for displays to hex and adding the symbol 'STOP' to the symbol table, emulation is started which will terminate when the instruction at 1333H ('STOP') is executed. When emulation terminates, a *DUMP* of the contents of user 8080 registers is requested. One can see that the value of the accumulator is set at 40H, the stack pointer is set at 13FFH, the last address executed (*) is 1333H, and the program counter has been set to 1320H.
8. *EXIT* returns control to the MDS monitor.

ICE80SD OPERATING ENVIRONMENT

Paper Tape-Based ICE80SD

Required Hardware:
- Intellec® System
- System console
- Reader device
- Punch device
- ICE-80

Required Software:
- System monitor

Diskette-Based ICE80SD

Required Hardware:
- Intellec® System
- 32K bytes RAM memory
- System console
- ISIS MOS Floppy Disk Drive
- ICE-80

Required Software:
- System monitor
- ISIS Diskette Operating System

EQUIPMENT SUPPLIED

Printed Circuit Modules (2)
Interface Cables and Buffer Board
Hardware Reference Manual
Operator's Manual
Schematic Diagram
ICE-80 Software Driver, paper tape version
(ICE-80 Software Driver, disketted-based version is supplied with Diskette Operating System)

SYSTEM CLOCK

Crystal controlled 2.185 MHz ±0.01%. May be replaced by user clock through jumper selection.

PHYSICAL CHARACTERISTICS

Width: 12.00 in. (30.48 cm)
Height: 6.75 in. (17.15 cm)
Depth: 0.50 in. (1.27 cm)
Weight: 8.00 lb (3.64 kg)

ELECTRICAL CHARACTERISTICS

DC Power:
- V_{CC} = +5V, ±5%
- I_{CC} = 9.81A maximum; 6.90A typical
- V_{DD} = +12V, ±5%
- I_{DD} = 79 mA maximum; 45 mA typical
- V_{BB} = -9V, ±5%
- I_{BB} = 1 mA maximum; 1 μA typical

ENVIRONMENTAL CHARACTERISTICS

Operating Temperature: 0°C to 40°C
Operating Humidity: Up to 95% relative humidity without condensation

CONNECTORS

Edge Connector: CDC VPB01E32A00A1

ORDERING INFORMATION

Part Number	Description
MDS-80-ICE	8080 CPU In-Circuit Emulator, cable assembly and interactive software included.

ICE-85™
MCS-85™ IN-CIRCUIT EMULATOR

Connects the Intellec® System Resources to the user-configured system via a 40-pin adaptor plug

Executes user system software in real-time

Allows user-configured system to share Intellec® memory and I/O facilities

Provides 1023 states of 8085 trace data plus 18 additional logic signals via an External Trace Module

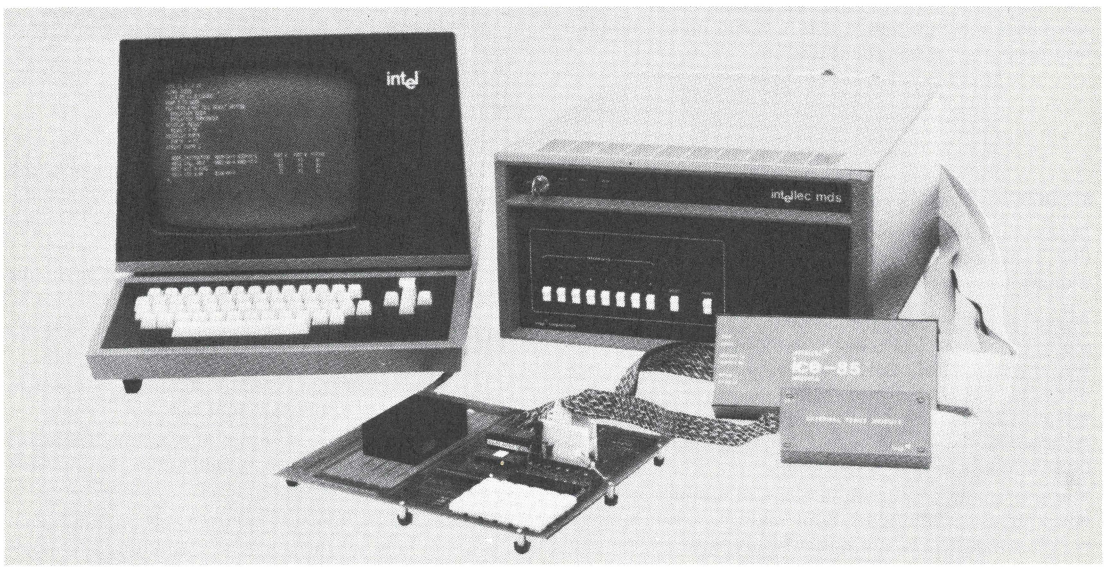
Offers full symbolic debugging capability for both assembly language and Intel's high-level compiler language, PL/M-80

Displays trace data from the user's 8085 in assembler mnemonics and allows personality groupings of data sampled by the external 18-channel trace module

Extends ICE capabilities to the rest of the prototype system peripheral circuitry by allowing the user to execute his own peripheral chip analysis routines

Provides ability to examine and alter MCS-85™ registers, memory, flag values, interrupt bits and I/O ports

The ICE-85 module resides in the Intellec® Microcomputer Development System and interfaces to the user system's 8085. In addition, an external trace module provides access to user system peripheral circuitry via a user-configured DIP clip for peripheral ICs or may be attached to as many as 18 separate prototype signal nodes via individual probe clips. Using the ICE-85 module, the designer can execute prototype software in real-time or single-step mode and can substitute Intellec® system memory and I/O for user system equivalent. ICE capability can be extended to the rest of the user system peripheral circuitry by allowing the user to create and execute a library of user-defined peripheral chip analyzer routines. All user access to the prototype system software may be done symbolically by assigning names to program locations and data, I/O ports and groups of external trace signals. For the first time, in-circuit emulation extends beyond the user's prototype CPU to the entire user's system, allowing In-System Emulation.



SYMBOLIC DEBUGGING CAPABILITY

ICE-85 allows the user to make symbolic references to I/O ports, memory addresses and data in his program. Symbols and PL/M statement number may be substituted for numeric values in any of the ICE-85 commands. The user is relieved from looking up addresses of variables or program subroutines.

The user symbol table generated along with the object file during a PL/M-80 compilation or by the ISIS-II 8080/8085 Macro Assembler is loaded into the Intellec® System memory along with the user program which is to be emulated. The user may add to this symbol table any additional symbolic values for memory addresses, constants, or variables that are found useful during system debugging. By referring to symbol memory addresses, the user can examine, change or break at the intended location.

ICE-85 provides symbolic definition of all 8085 registers, interrupt bits and flags. The following symbolic references are also provided for user convenience: TIMER, the low-order 16 bits of a register containing the number of 2 MHz clock pulses elapsed during emulation; HTIMER, the high-order 16 bits of the timer counter; PPC, the address of the last instruction emulated; BUFFERSIZE, the number of frames of valid trace data (between 0 and 1022).

PERSONALITY GROUPED DISPLAYS

Trace data in the 1023 by 42-channel real-time trace memory buffer is displayed in easy to read format. The user has the option to specify trace data displays in actual 8085 assembler instruction mnemonics. The data collected from the External Trace Module can be grouped and symbolically named according to user specifications and displayed in the appropriate number base designation. Simple ICE-85 commands allow the user to select any portion of the 42K-bit trace buffer for immediate display.

MEMORY AND I/O MAPPING

Memory and I/O for the user system can be resident in the user system or "borrowed" from the Intellec® System through ICE-85's mapping capability.

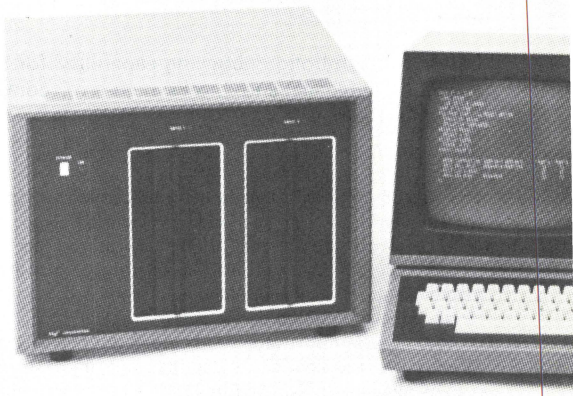
ICE-85 separates user memory into 32 2K blocks. Each block of memory can be defined independently. The user may assign Intellec® System equivalents to take the place of devices not yet designed for the user system during prototyping. In addition, Intellec® System memory or I/O can be accessed in place of suspect user system devices during prototyping or production checkout.

The user can also designate a block of memory or I/O as nonexistent. ICE-85 issues error messages when memory or I/O designated as nonexistent is accessed by the user program.

INTEGRATED HARDWARE/SOFTWARE DEVELOPMENT

The user prototype need consist of no more than an 8085 CPU socket and a user bus to begin integration of software and hardware development efforts. Through ICE-85 mapping capabilities, Intellec® System equivalents can be accessed for missing prototype hardware. Hardware designs can be tested using the system software which will drive the final product.

The system integration phase, which can be so costly when attempting to mesh completed hardware and software products, becomes a convenient two-way debug tool when begun early in the design cycle.



TYPICAL ICE INTERROGATION AND UTILITY COMMANDS

DISPLAY/ CHANGE	Display/Changes the values of symbols and the contents of 8085 registers, pseudo-registers, status flags, interrupt bits, I/O ports and memory.
EVALUATE	Displays the value of an expression in the binary, octal, decimal or hexadecimal.
SEARCH	Searches user memory between locations in a user program for specified contents.
CALL	*Emulates* a procedure starting at a specified memory address in user memory.
ICALL	*Executes* a user-supplied procedure starting at a specified memory address in the Intellec® System memory.
EXECUTE	Saves emulated program registers and emulates a user-supplied subroutine to access peripheral chips in the user's system.

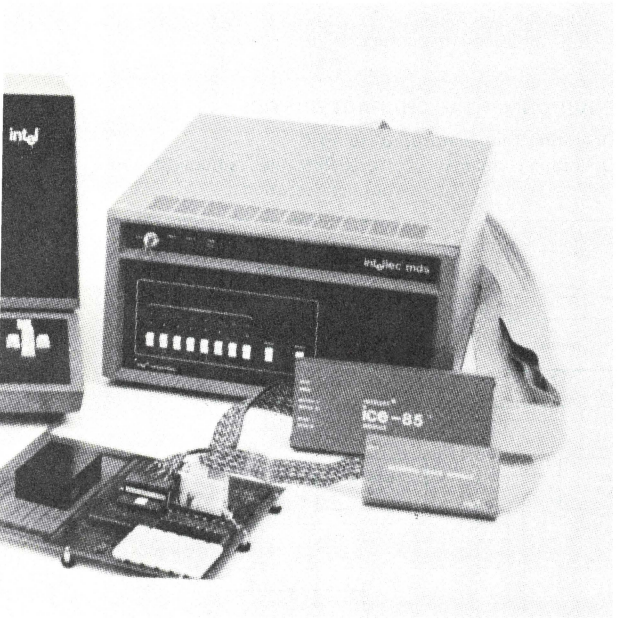
REAL TIME TRACE

ICE-85 captures valuable trace information from the emulating CPU and the External Trace Module while the user is executing programs in real time. The 8085 status, the user memory or port addressed, the data read or written, the serial data lines and data from 18 external signals, is stored for the last 1023 machine states executed (511 machine cycles). This provides ample data for determining how the user system was reacting prior to emulation break. It is available whether the break was user-initiated or the result of an error condition.

For detailed information on the actions of CPU registers, flags, or other system operations, the user may operate in single or multi-step sequences tailored to system debug needs.

EXTERNAL TRACE MODULE

TTL level signals from 18 points in the user system may be synchronously sampled by the External Trace Module and collected in ICE-85's trace buffer. The signals can be collected from a single peripheral chip via the supplied 40-pin DIP clip or may be placed by the user on up to 18 separate signal nodes using the supplied 18 individual probe clips. These signals are included in the 42-channel breakpoint comparisons and clock qualifiers. Also, data from these 18 channels may be displayed in each to read, user-defined groupings.



SYNCHRONOUS OPERATION WITH OTHER DESIGN AIDS

ICE-85 can be synchronized with other Intellec® design aids by means of two external synchronization lines. These lines are used to enable and disable ICE-85 trace data collection and to cause break conditions based on an external signal which may not be included in the ICE-85 breakpoint registers. In addition, ICE-85 can generate signals on these lines which may be used to control other design aids.

EMULATION CONTROLS AND COMMANDS

GROUP	Defines into a symbolically named group, a channel or combination of channels from the 8085 Microcprocessor and/or the External Trace Module.
GO	Initiates real-time emulation and controls emulation break conditions.
STEP	Initiates emulation in single instruction steps. User may specify the type and amount of information displayed following each step, and define conditions under which stepping should continue.
PRINT	Prints the user-specified portion of the trace memory to the selected list device.

BREAK REGISTERS/TRACE MEMORY

ICE-85 has two breakpoint registers which are used to break emulation, and two trace qualifier registers which are used to control the collection of trace data during emulation. Each register is 42 entries wide, one entry for each channel and each entry can take any one of the three values 0, 1 or "don't care".

The trace buffer, also 42 entries wide, collects data sampled from 24 8085 processor channels and 18 external channels sampled by the External Trace Module. The signals collected from the 8085 include address lines, data lines, status lines and serial input and output lines. The 18 channels extending from the External Trace Module synchronously sample and collect into the trace buffer any user-specified TTL compatible signal from the rest of the prototype system. "Break" and "trace qualification" may therefore occur as a result of a match of any combination of up to 42 channels of CPU and external circuitry signals.

SPECIFICATIONS

ICE-85 OPERATING ENVIRONMENT

Diskette-Based ICE-85 Software

Required Hardware:
- Intellec® Microcomputer Development System System Console
- Intellec®-Diskette Operating System
- ICE-85 Module

Required Software:
- System Monitor
- ISIS-II

EQUIPMENT SUPPLIED

18-Channel External Trace Module
Printed Circuit Boards (2)
Interface Cable and Emulation Buffer Module
Operator's Manual
ICE-85 Software, Diskette-Based Version

EMULATION CLOCK

User's system clock or ICE-85 adaptor socket (6.144 MHz Crystal)

PHYSICAL CHARACTERISTICS

Printed Circuit Boards:

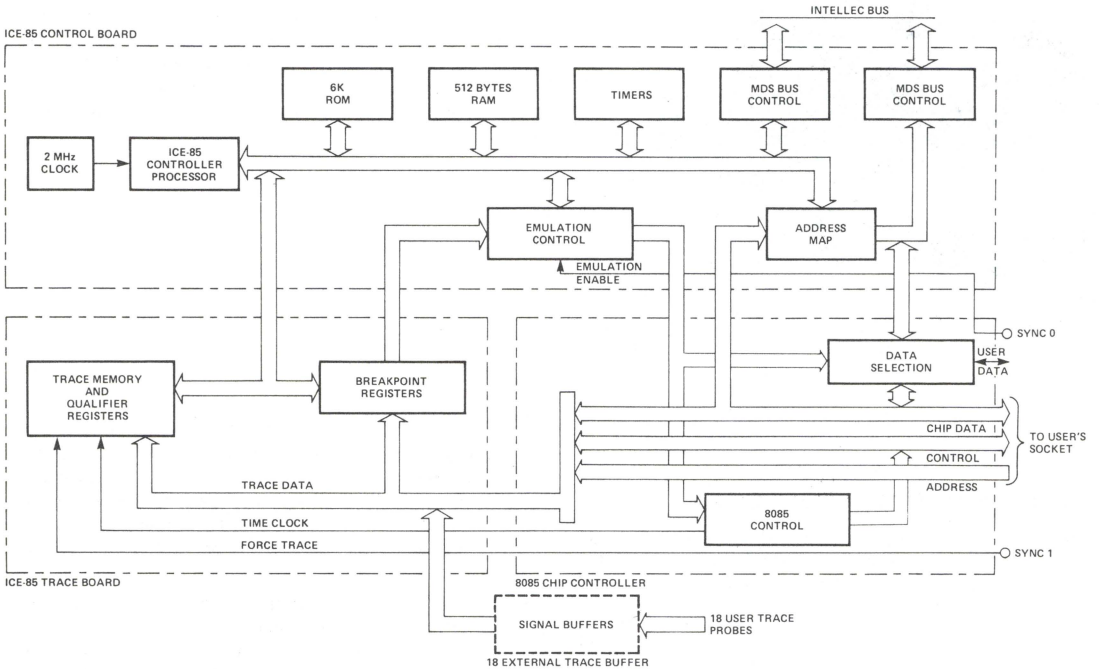
Width:	12.00 in.	(30.48 cm)
Height:	6.75 in.	(17.15 cm)
Depth:	0.50 in.	(1.27 cm)
Packaged Weight:	6.00 lb	(2.73 kg)

ELECTRICAL CHARACTERISTICS

DC Power:
- V_{CC} = +5V ±5%
- I_{CC} = 12A maximum; 10A typical
- V_{DD} = +12V ±5%
- I_{DD} = 80 mA maximum; 60 mA typical
- V_{BB} = −10V ±5%
- I_{BB} = 30 mA maximum; 10 μA typical

ENVIRONMENTAL CHARACTERISTICS

Operating Temperature: 0° to 40°C
Operating Humidity: Up to 95% relative humidity without condensation.



ICE-85 BLOCK DIAGRAM

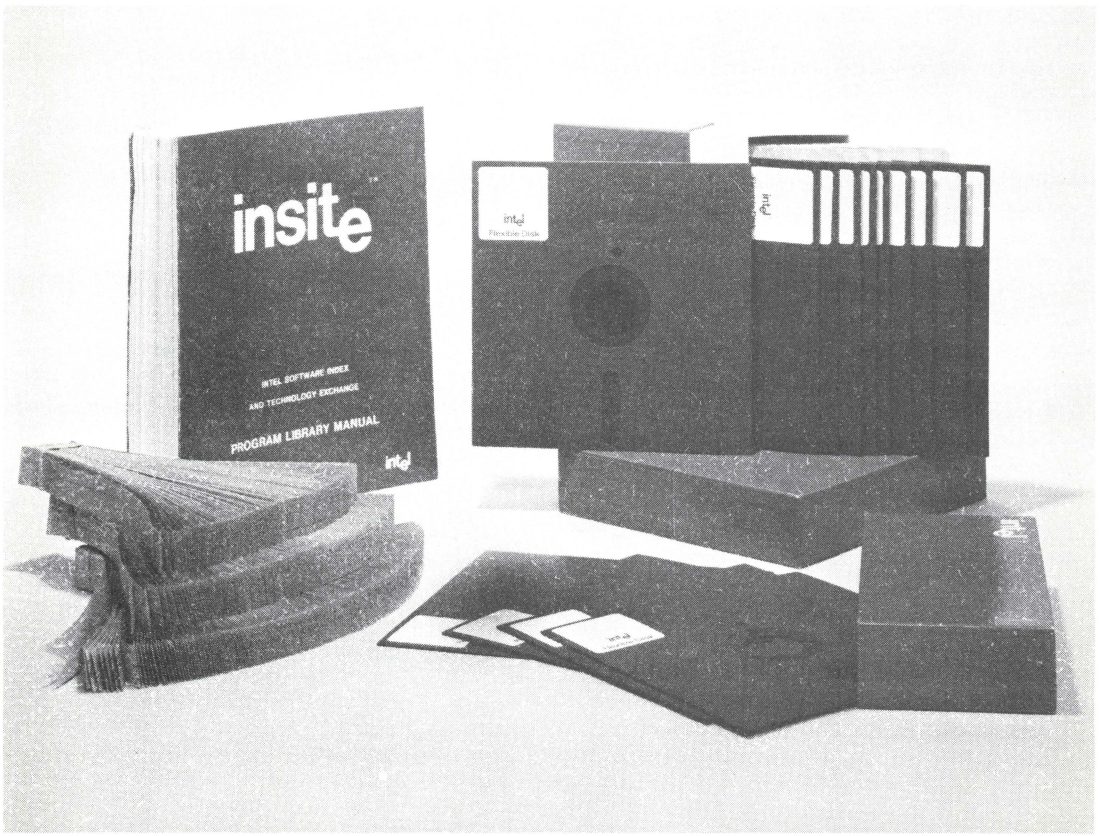
ORDERING INFORMATION

Part Number	Description
MDS-85-ICE	8085 CPU In-Circuit Emulator and 18-Channel External Trace Module

INSITE™
USER'S PROGRAM LIBRARY

- Programs for 8008, 8080, 8085 and 8048 Processors
- Updates of new programs sent every other month
- Diskette, Paper Tapes, and Listings available for Library programs
- Hundreds of programs
- For each accepted program submittal, Insite will provide either a one year free membership, five free paper tapes or free program diskette.
- 4004/4040 Library also available

Insite™ , Intel's Software Index and Technology Exchange, is a collection of programs, subroutines, procedures and macros written by users of Intel's 8008, 8080, 8085, and 8048 microcomputers, SBC 80 OEM computer systems, and Intellec® development systems. Thanks to customer contributions to Insite™, Intel is able to make these programs available to all users of Intel microcomputers. By taking advantage of the availability of these general-purpose routines, the microcomputer design engineer and programmer can save many hours of programming and debugging time. The library of programs also serves as a good learning tool for those unfamiliar with Intel assembly language or PL/M, Intel's high-level language for the 8008, 8080, and 8085 microcomputers.



LIBRARY PROGRAMS AVAILABLE ON PAPER TAPE AND DISKETTE

INSITE™ PROGRAM LIBRARY MANUAL

Each member will be sent the Program Library Manual which is a collection of source listings of library programs three pages and under. Longer programs are represented by an abstract which indicates the function of the routine, required hardware and software, and memory requirements.

User's Library members will be updated regularly with new programs submitted to Insit$_e$™ during the subscription period. Please refer to the Intel OEM Price List for yearly subscription fee.

PROGRAM LIBRARY SERVICES

PAPER TAPES AND LISTINGS are available for programs in Insit$_e$™. A handling fee will be charged for each paper tape and listing. Ordering information can be found in the Program Library Manual.

DISKETTE – Source of most User's Library programs are available on system diskettes. A three program minimum is required on all diskette orders, with the exception of Section 9.

4004/4040 PROGRAM LIBRARY MANUAL

4004/4040 User's Library members will be sent the 4004/4040 program library manual. Updates will be issued as new programs are contributed. Paper tapes and diskette are not available for 4004/4040 programs. Please refer to the Intel OEM Price List for yearly subscription fee.

MEMBERSHIP

Membership in Insit$_e$™ is available on an annual basis. Users may become a member through program contribution or membership fee. New members should use the membership form on the back of this data sheet.

PROGRAM SUBMITTAL

Programs submitted for our review must follow the guidelines listed below:

1. Programs must be written in a standard Intel Assembly Language or PL/M. These languages are documented in the following manuals:
   a. 8008 Assembly Programming Manual #98-019B
   b. 8080 Assembly Language Programming Manual #98-004C
   c. 4004/4040 Assembly Language Programming Manual #98-025A
   d. 8008/8080 PL/M Programming Manual #98-108A
   e. PL/M-80 Programming Manual #98-268
   f. MCS-48 Assembly Language Manual #98-255

PROGRAM SUBMITTAL (Cont)

2. A source listing of the program must be included. This must be the output listing of a compile or assembly. All accepted programs should assemble or compile correctly with no syntax errors. No consideration will be given to partial programs or duplication of existing programs.

3. A test program which assures the validity of the contributed program must be included. This must show the correct operation of the program.

4. A source paper tape or diskette of the contributed program is required. This will be used for the reproduction of tapes for other members.

Complete the Submittal Form as follows: (please type or print)

a. Processor (check appropriate box).

b. Program title: Name or brief description of program function.

c. Function: Detailed description of operations performed by the program. Attach additional pages if necessary.

d. Required hardware:

   For example: TTY or Port 0 and 1
   Interrupt Circuitry
   I/O Interface
   Machine line and configuration for cross products

e. Required software:

   For example: TTY Driver
   Floating Point Package
   Support software required for cross products

f. Input parameters: Description of register values, memory areas or values accepted from input ports.

g. Output results: Values to be expected in registers, memory areas or on output ports.

h. Program details: (for resident products only)
   (1) Register modified
   (2) RAM required (bytes)
   (3) ROM required (bytes)
   (4) Maximum subroutine nesting level

i. Assembler/Compiler used:

   For example: PL/M
   Intellec MDS Macro Assembler
   IBM 370 Fortran IV

j. Programmer company and address.

3-Byte Positive Fractional Multiply
8-Bit Multiply and Divide
8-Bit Random Number Generator
12 x 12 Multiply
16-Bit 2's Complement Signed Multiplication
16-Bit CRC for Polynomial X16+12+X5+1
16-Bit Division — 16-Bit Result
16-Bit Division — 16-Bit Result
16-Bit Multiply — 16-Bit Result
16-Bit Multiply — 16-bit Result
16-Bit Multiply — 32-Bit Result
16-Bit Random Number Generator
16-Bit Square Root Routine
32-Bit Binary to BCD Conversion, Leading Zero Blanking
32-Bit Divide Subroutine
4040 Cross Assembler for Intellec 8/MOD 80 and MDS-800
2708 PROM Programmer for Intellec 8/MOD 80
8080 Cross Assembler for Intel 8080/8085 Microprocessors
8008 Cross Inverse Assembler for HP 2100
8008 Disassembler
8008 MACRO Definition Set for Assembly on PDP-11
8008 MACRO Assembler Version 2.0
8080 MACRO Assembler 4.1
8080 CPU Exercise Routine
8080 Cross Assembler for Tektronics 4051
8080 Double Precision ARC Tangent
8080 Disassembler
8080 Disassembler
8080 Floating Point Extended Math Package
8080 Floating Point Package with BCD Conversion Routine
8080 Idle Analyzer for Approximating CPU Utilization
8080 I/O System Status Display
8080 Least Squares Quadratic Fitting Routine
8080 RAM Memory Test
8080 Symbol Table Dump
9600 Initialize CRT and Uart for Baud

ADCCP Remainder Routine
A/D Converter Routine
Adaptive Game Program
Algebraic Compare Subroutine
APL Graphic Display on a 5 X 7 Dot Matrix
Approximating Routine
Arctan 2 Subroutine
ASCII Display
Absorbance Calculation
ASCII to EBCDIC and EBCDIC to ASCII Converters
Assembler Oriented Centronics 306 Line Printer Handler and Error Only Assembler

Bandit Static Display
Banner Print and Punch
BASIC CPU State Vector Maintenance
Basic Digital Panel Meter Call
BASIC Interpreter
BASIC/M Translator and Interpreter
BCD to BIN Conversion Routine
BCD to/from Binary Conversion
BCD Input and Direct Conversion to Binary Routine
BCD Multiplication
BCD Sum for 8008
BCD Up/Down Counter
BIN to BCD Conversion Routine
Binary to BCD Subroutine
Binary to HEX Routine
Binary Loader for MDS
Binary Multiplication — 24-Bit
Binary Search
Binary Search Routine
Binary Tape Program
BINDECBIN — Binary to/from BCD
BINLB — 8080 System Loader
Blackjack
$BLPT
BOOT — Bootstrap Loading and Program Patching

Calendar Subroutine
Character Interpreted Memory Dump
Clock Subroutine
Compare
Compare Object Code Tape with Memory
Control Data Output
Conversion of Scientific to Easily Readable Notation
CRECH — Cyclic Redundancy Check
Cross Assembler ASM08
Cross Assembler for PDP-11
Cross Assembler for PDP-11
Cross Assembler for NOVA 1200
Cross Assembler for Nova 1220, IBM 360/40 and CDC 3000
Cross Assembler for Varian Data Machine
Cross Reference for PAS80 PASCAL Programs — XREF80
CRTBZ — GET
Cyclic Redundancy Character Generator
Cyclic Redundancy Check
Cyclic Redundancy Check for Data String of 2^{16} Bytes

Data Array Move
Data General to Intellec MDS Diskette Transport Package
Data I/O PROM Processor
Decrement H and L Registers
Delete Comments
Diagnostic 1003 — Memory Validity Check
Digital to Analog Conversion for Eight Outputs
Disable Hold — Screen Mode
Disassembler
Disk Dump Routine for ICOM F DOS-11/MOD 80 Floppy DOS
Double Precision Integer Arithmetic Package
Double Precision Multiply
Driver for Tektronix 4010 Grafic Screen

Elementary Function Package
Enable Hold — Screen Mode
ERLIST
Examin

Factorial of a Decimal Number
Fast Floating Point Square Root Routine
Fixed and Floating Point Arithmetic Routines
Fixed Point CHEBYSHEV Sine and Cosine for PL/M Users
Flag Processing Routine
Floating Point Decimal and HEX Format Conversion
Floating Point Format Conversion Package
Floating Point Interpreter
Floating Point Math Package
Floating Point Package for Intel 8008 and 8080 Microprocessors
Floating Point Procedures
Floating Point Square Root
Fly Reader Driver
Format
Format Intel Data

Gambol
Game of Life
Generalized Stepper Motor Drive Program
GLANCE
Gray to Binary Conversion

Handler for Tally PTP
HEX Convert — Convert Intel HEX to Prolog HEX File Converter
HEX to Decimal Conversion
HEX Format Paper Tape Dump for SDK
HEX Tape Loader for SDK
High Speed Paper Tape Reader with Stepper Motor Control
Histogram

IBM Selectric Output Program
ICE-80 Disassembler
I-Command — Insert Data in HEX Form from TTY into RAM

Input/Output Commands for MDS
Intellec 8/MOD 80 Monitor
Intellec 8/MOD 80 — Silent 700 Interface
Intellec MDS Diagnostic Confidence Test Version 1.0
Intellec MDS Monitor Version 2.0
Intellec 8 Text Editor
Interfacing the MDS and HP 2644
Interrupt Driven Clock Routine
Interrupt Handler (Re-Entrant)
Interrupt Service Routine
INVERT Data in RAM
I/O Routine for TI Silent 700 Terminal
I/O Simulation MACROS

Julian Data Routine

K, Program Trap and Dump Routine
Kalah
Keyboard Scanner
Kill the Rotating Bit

Leer
Legible Paper Tape
Lewthwaite's Game
List
List SCR
List Device Program
List 1 — High Speed List Program for Intellec 8
List/Print/Type "List SRC" on Diskette
LOAD
Log Base 2
LSORT

MACRO Assembler for DG NOVA
Main Routine DDUMP (Diskette DUMP Routines)
Mastermind
Match
Match Game
Maze
Maze
MBCD N1 x N2 Bytes Decimal Multiply Subroutine
Memory Compare
Memory Diagnostic Program
Memory Dump
Memory Test for the 8080
Memory Test Program
Model 101 Centronics Printer Handler
Mon256 — 256-Byte PROM Monitor
Morse Code Generator
MUL/DIV Multi-Precision Pack for 8080

Natural Logarithm
N-Byte Binary Multiplication and Leading Zero Blanking
Nim
Nim
Non-Encoded Key Board Subroutine
Nova Cross Assembler — Intel 8080
Numbers

Octal Code Conversion for PDP-11
Octal Debugging Program (ODT) for the MCS-80 Computer
Octal PROM Programming
OCTHEX

P2708 PROM Programming Routine
Page Break for Tektronix 4010 I/O Graphics Terminal
Page Listing Program
Paper Tape Reformatter for SDK
Paper Tape Leader I.D.
Pascall
Pass — Parameter Passing Routine
PDP-11 Bubart File to Intel HEX File Converter
PDP-11 Program Load to HEX, Dump, & Verify
PL/M 80 Pass 3
PL/M Floating Point Interface
PL/M Histogram Procedure and Random Number Generator
PROM Programmer for Intellec 8
Proportional Power Control Image Builder
Punch Binary Tape
Punch Test or TTY Reader/Punch Test

Quicksort Procedures

RAM Check
RAM Test Program
RANDOM$BITS
Random Number Generator — RINGEN

INSITE™ USER'S LIBRARY PARTIAL PROGRAM INDEX (Continued)

Read and Interrupt Modifications for Intellec 8/MOD 80
Reader Test
Read/Write Routines for Interchange Tapes
Real Time Executive
Real Time Monitor
React
Relative Jump Routine
RMSTF – Integration Routine
Run 0

Save/Restore CPU State on an Interrupt
SBC 80/10 Interactive Monitor
SBC 80/10 Port I/O Exerciser
SCAN
SDK-80 Keyboard Monitor
SDK-80 Paper Tape Punch Routine
Sets Horizontal Tabs on Terminet
Shellsorting Routine
Sin X, Cos X Subroutine
Slot Machine
SMAL: Symbolic Microcontroller Assembly Language
Snap Dump 8080
Software Stack Routines for 8008
Source Paper Tape to Magnetic Cassette
SQRTF – Calculates 8-Bit Root of 16-Bit Number
Stage 2
Statement Counter
Structured Assembler for 8080
Subroutine DMULT (Decimal Multiplication)
Subroutine Log – Common Logarithms
Subroutine SQRT
Symbol Table Dump for Intellec 8/MOD 80
Symbol Table List Routine

Tabs
Tally – User Tally 2200 Line Printer in Assembly Stage of Programming
Tally R2050 HSPTR Driver
Tape Duplicator
Tape Labeler for MDS
Teleprocessing Buffer Routine
Terminal Editor
Terminet 300
Terminet 1200
Text Storage Program
Thermocouple Linearization (Type J)
Tic-Tac-Toe
Time Sharing Communications
TIMIT – Interrupt Driven Real Time Clock Routine
T.I. Silent 700 Interface – Intellec MDS
T.I. Silent 700 – SBC 80 Monitor Interface
TRACE Version 7.0
TRACE – Program Trace and Debugger
Trace Routine
TTY Binary Dump Routine
TTY Binary Load Routine
Type
Type K.T.C. Linearizer

Utility Macros for 8080

Video Driver

Wipe
Word Game, The

4004/4040 USER'S LIBRARY PARTIAL PROGRAM INDEX

4 X 8 Keyboard Scanner
4 Digit BCD to Binary Converter
4 Digit Multiply
4040 Cross Assembler for Intellec 8/MOD 80 and MDS-800
8-Bit Binary to BCD Conversion
8 Digit Register Display

ASCII to EBCDIC Code Conversion
Automatic Digital Integration

Bit Manipulation Routine
BNPF Tape Generator for PDP-8
BNPF Tape Generator for PDP-8
Bowmar TP 3100 Printer Routine

Chebyshev Approximation Functions
Complement Decimal
Cross Assembler for PDP-8
Cross Assembler for NOVA
Cross Assembler and Test Program

Delay Subroutines
Data Compare Routine
Fast Binary Multiply: Selectable Bit Precision and Constant Execute Time
Fast Decimal Multiply Routine
Floating Point Arithmetic Subroutine Package

General Purpose ROM

High Speed Printer Interface
HEXBCD

Intel MCS-40 Cross Assembler and Text Editor
I/O Test
IOMEC Series 3 Cartritape to Intel MCS-4

John Conway's Solitaire Game of Life

MCS-4 Simulator for NOVA
MCS-4 Simulator for PDP-8
MCS-4/40 Disassembler
Mobile Mean Program
Mod 40/Silent 700 Interface
Multiply/Divide 8 Decimal Numbers
Paper Tape Conversion, 5 Level TTY to 8 Level ASCII
Paper Tape Edit Routine
Parity Checker/Generator
Parity Generator, ASCII Character
Peripheral Interface Routine for a Thermal Strip Printer
Pro Forma
PROM Utility Dump Program

Right Justified Hexadecimal Data Shifter
Random Number Generator

"SEL" Subroutine (Selector)

TOUCHTONE Keyboard Scanner
TP 3100
Translate HEX

Universal Logic Subroutine

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USER LIBRARY MEMBERSHIP FORM

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Enclosed is ☐ check, ☐ money order, ☐ purchase order*, ☐ Program Submittal

NAME: _____

COMPANY: _____

SHIP TO: _____

_____

☐ PLEASE SEND THE 4004/4040 LIBRARY *INSTEAD* OF INSITE™

SEND TO NEAREST LOCATION:

North America

Intel Corporation
User's Library
Microcomputer Systems
3065 Bowers Avenue
Santa Clara, California
95051

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Intel International
User's Library
51 Rue du Moulin a Papier
Boite 1
B-1160 Brussels

Orient

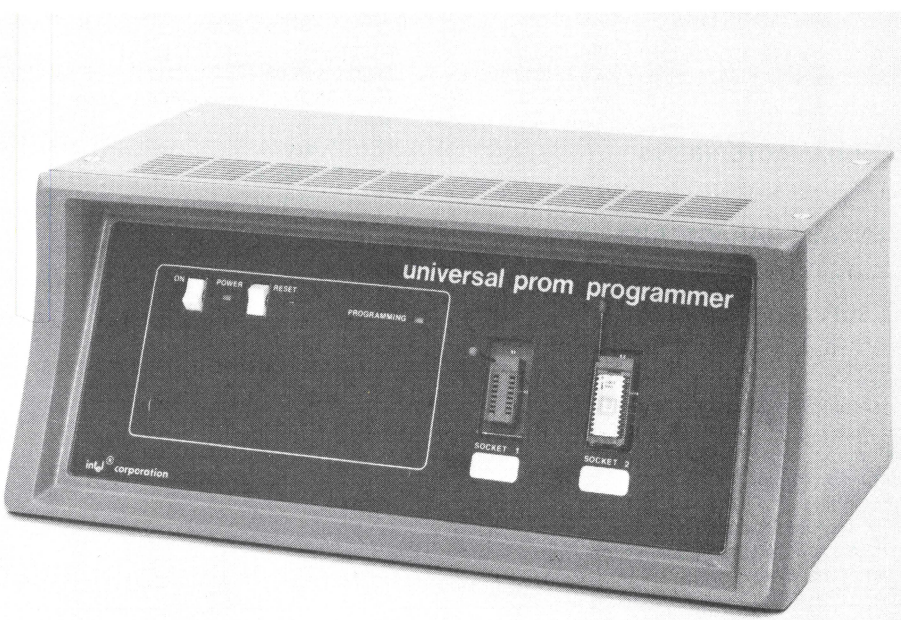
Intel Japan K.K.
User's Library
Flowerhill-Shinmachi, East Bldg.
1-23-9 Shinmachi, Setagaya-ku
Tokyo 154, Japan
Ph. 03-426-9261 (PME & FSE)
03-426-9267 (CS & Fin.)

*Please refer to the OEM Price List for membership fee.

UPP-103*
UNIVERSAL PROM PROGRAMMER

- Intellec® Development System Peripheral for PROM programming and verification
- Personality cards available for programming all Intel® PROM families
- Zero insertion force sockets for both 16-pin and 24-pin PROMs
- Universal PROM Mapper software provides powerful data manipulation and programming commands
- Flexible power source for system logic and programming pulse generation
- Holds 2 personality cards to facilitate programming operations using several PROM types

The Universal PROM Programmer (UPP) is an Intellec® System peripheral capable of programming and verifying the following Intel Programmable ROMs (PROMs): 1702A, 2704, 2708, 2716, 3601, 3602, 3602A, 3621, 3622, 3622A, 3604, 3604A, 3604AL, 3604L-6, 3605, 3608, 3624, 3624A, 3625, 3628, 8702A, 8704, and 8708. In addition, the UPP programs the PROM memory portions of the 8748 Microcomputer and the 8755 PROM and I/O chip. Programming and verification operations are initiated from the Intellec Development System console and are controlled by the Universal PROM Mapper (UPM) program.



*This UPP103 replaces the UPP101, UPP102.

FUNCTIONAL DESCRIPTION

The basic UPP consists of a controller module, two personality card sockets, front panel, power supplies, chassis and an Intellec Development System interconnection cable. An Intel 4040-based intelligent controller monitors the commands from the Intellec System and controls the data transfer interface between the selected PROM personality card and the Intellec memory. A unique personality card contains the appropriate pulse generation functions for each Intel PROM family. Programming and verifying any Intel PROM may be accomplished by selecting and plugging in the appropriate personality card. The front panel contains a power-on switch and indicator, reset switch, and two zero-force insertion sockets (one 16-pin and one 24-pin or two 24-pin). A central power supply provides power for system logic and for PROM programming pulse generation.

The Universal PROM Programmer may be used as a table top unit or mounted in a standard 19" RETMA cabinet.

The Universal PROM Mapper (UPM) is the software program which controls transfers of data between paper tape or diskette files and a PROM plugged into the Universal PROM Programmer. It uses Intellec System memory for intermediate storage. The UPM transfers data in 8-bit HEX, BNPF, or binary object format between paper tape or diskette files and the Intellec System memory. While the data is in Intellec System memory, it can be displayed and changed. In addition, word length, bit position, and data sense can be adjusted as required for the PROM to be programmed. PROMs can also be duplicated or altered by copying the PROM contents into the Intellec System memory. Easy-to-use PROGRAM and COMPARE commands give the user complete control over programming and verification operations. The UPM eliminates the need for a variety of personalized PROM programming routines because it contains the programming algorithms for all Intel PROM families.

There are two versions of the UPM: one that runs under Intellec System Monitor (paper tape system), and one that runs under ISIS-II, the Intellec Diskette Operating System (diskette-based system). The paper tape version is included with the Universal PROM Programmer. The diskette-based version of the UPM is available on all ISIS-II system diskettes.

HARDWARE INTERFACE

Data: Two 8-bit unidirectional buses
Commands: 3 Write Commands
2 Read Commands
Initiate Command

PHYSICAL CHARACTERISTICS

Dimensions: 6" x 7" x 17"
14.7 cm x 17.2 cm x 41.7 cm
Weight: 18 lb (8.2 kg)

ELECTRICAL CHARACTERISTICS

AC Power Requirements: 50-60 Hz; 115/230 VAC: 80 Watts

ENVIRONMENTAL CHARACTERISTICS

Operating Temperature: 0°C to 55°C

EQUIPMENT SUPPLIED

Cabinet
Power Supplies
4040 Intelligent Controller Module
Specified Zero Insertion Force Socket Pair
Intellec® Development System Interface Cable
Hardware Reference Manual
Reference Schematics
Universal PROM Mapper Operator's Manual
Universal PROM Mapper program (paper tape version — disk-based version available on ISIS-II diskettes)

OPTIONS

Personality Cards:
- UPP-361: 3601 Personality Card
- UPP-816: 2716 Personality Card
- UPP-848: 8748 Personality Card with 40-pin adaptor socket
- UPP-855: 8755 Personality Card with 40-pin adaptor socket
- UPP-865: 3602, 3622, 3602A, 3622A, 3621, 3604, 3624, 3604A, 3624A, 3604AL, 36046-6, 3605, 3625, 3608, 3628
- UPP-872: 8702A/1702A Personality Card
- UPP-878: 8708/8704/2708/2704 Personality Card

PROM Programming Sockets:
- UPP-501: 16-pin/24-pin socket pair
- UPP-502: 24-pin/24-pin socket pair
- UPP-562: Socket Adaptor for 3621, 3602, 3622, 3602A, 3622A
- UPP-555: Socket Adaptor for 3604AL, 36046-6, 3608, 3628
- UPP-565: Socket Adaptor for 3605, 3625

ORDERING INFORMATION

Universal PROM Programmer:
UPP-103 with 16-pin/24-pin socket pair and 24-pin/24-pin socket pair

INTELLEC® HIGH SPEED PAPER TAPE READER

Loads 16K Intellec® program memory in less than 3 minutes.

20 times faster than standard ASR-33 Teletype reader.

Data transfer at asynchronous rates in excess of 2000 characters per second

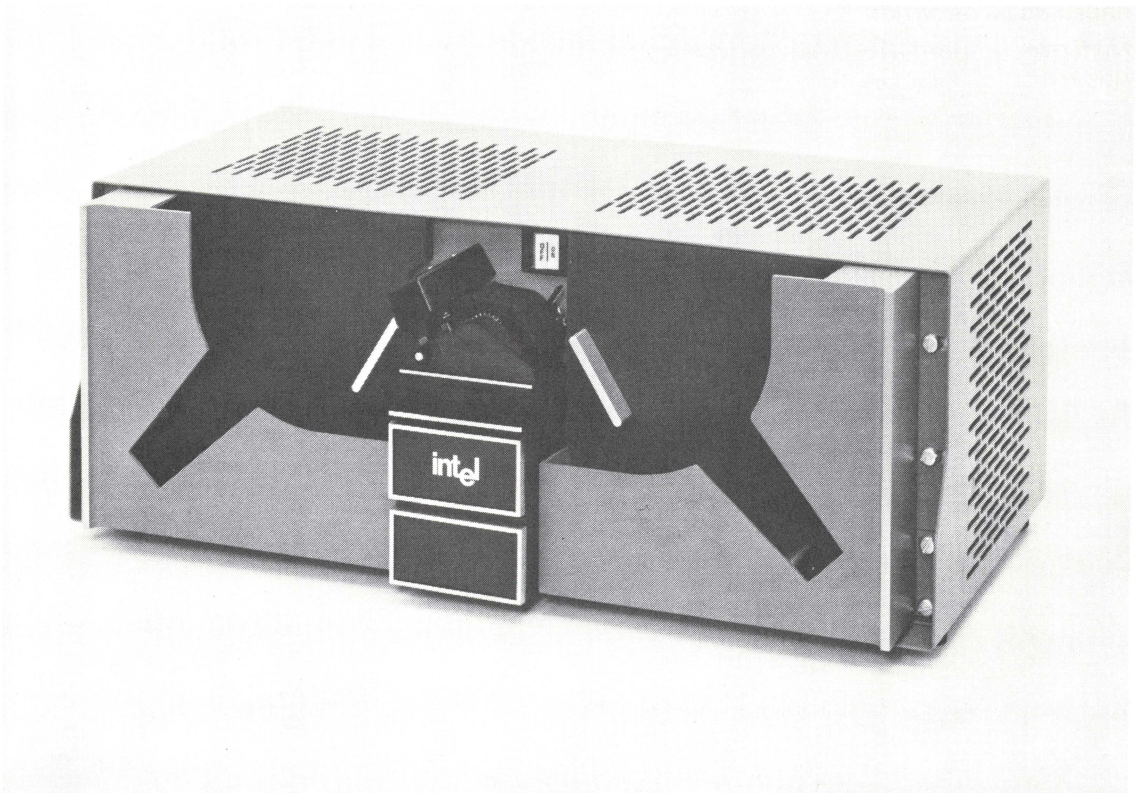
Rack-mountable or stand-alone

The Intellec® High-Speed Paper Tape Reader is an Intellec peripheral that reads paper tape over twenty times faster than the standard ASR-33 Teletype reader. This translates into a significantly faster development cycle due to a marked reduction in the time required for repetitive program loading, assembly, and editing operations.

The monitor software provides two key capabilities which significantly enhance the system's performance of the high-speed reader. A general-purpose paper tape reader driver is included in the Intellec Monitor which enables all system software or user-written application programs to utilize the high-speed reader features. The monitor also provides dynamic I/O reconfiguration, permitting reassignment of the high-speed reader to other logical input devices.

Reader data and command interface hardware is provided with the basic Intellec. A reader/Intellec system interface cable is included with the unit. A fanfold tape guide is also included to provide fanfold punch capability to the ASR-33 Teletype.

The high-speed reader may be used as a table-top unit or mounted in a standard 19" RETMA cabinet.



SPECIFICATIONS

TAPE MOVEMENT

Tape Reader Speed:
0 to 200 characters per second asynchronous
Tape Stopping:
Stops "On Character"

TAPE CHARACTERISTICS

Tape must be prepared to ANSI X 3.18 or EMCA 10 Standards for base materials and perforations.

Reads tape of any material with thickness between 0.0027" and 0.0045" with transmissivity less than or equal to 57% (oiled buff paper tape).

Tape loading: in line

Tape width: 1 inch

PHYSICAL CHARACTERISTICS

Height: 7.75 in. (19.69 cm)
Width: 19.25 in. (48.90 cm)
Depth: 11.62 in. (29.52 cm)
Weight: 13 lb (5.9 kg)

ELECTRICAL CHARACTERISTICS

AC Power Requirements:
3-wire input with center conductor (earth ground) tied to chassis. 100, 115, or 127 VAC, single phase at 3.0 amps or 220 or 240 VAC and 1.5 amps; 47 to 63 Hz.

ENVIRONMENTAL CHARACTERISTICS

Temperature:
Operating: 0 to 55°C (free air)
Non-operating: −55°C to +85°C

Humidity:
Operating: Up to 90% relative humidity without condensation.
Storage: All conditions without condensation of water or frost.

EQUIPMENT SUPPLIED

Paper Tape Reader
Reader Cable
Fanfold Tape Guide
Fanfold Paper Tape
Hardware Manual
Installation and Operations Guide
Fanfold Guide Installation Instructions

ORDERING INFORMATION

Part Number	Description
MDS-PTR	Paper Tape Reader

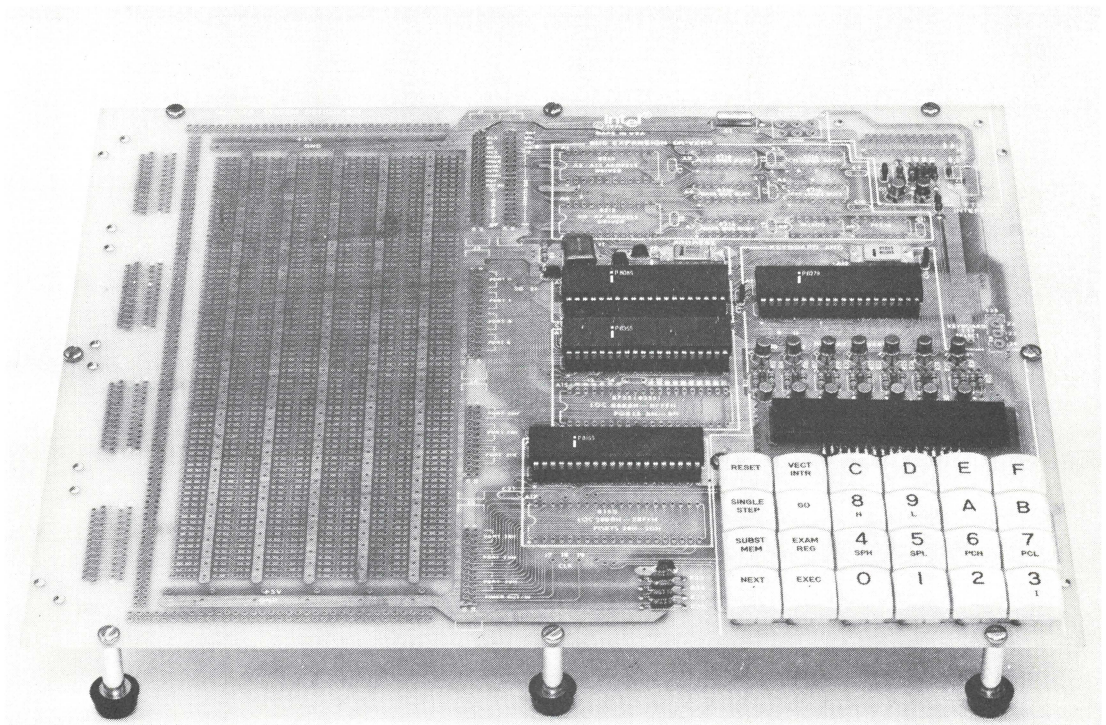
SDK-85
MCS-85™ SYSTEM DESIGN KIT

- **Complete Single Board Microcomputer System Including CPU, Memory and I/O**
- **Easy to Assemble Kit-Form**
- **High-Performance 3MHz 8085 CPU (1.3 μs Instruction Cycle)**
- **Popular 8080A Instruction Set**
- **Interfaces Directly With TTY**
- **Interactive LED Display and Keyboard**
- **Large Wire-Wrap area for Custom Interfaces**
- **Extensive System Monitor Software in ROM**
- **Comprehensive Design Library Included**
- **Low Cost**

The MCS-85 System Design Kit (SDK-85) is a complete, single board, microcomputer system in kit form. It contains all necessary components, including LED Display, Keyboard, resistors, caps, crystal and miscellaneous hardware to complete construction. Included is a preprogrammed ROM that contains the system monitor for general software utilities and system diagnostics.

The SDK-85 includes 6 digit LED display and 24 key-keyboard for a direct insertion, examination and execution of a user's program. In addition, it can be directly interfaced with a teletype terminal.

The SDK-85 is an inexpensive, high-performance prototype system that has designed-in flexibility for simple interface to the user's application.



General

The SDK-85 is a complete 8085 microcomputer system on a single board, in kit form. It contains all necessary components to build a useful, functional system. Such items as resistors, caps, and sockets are included. Assembly time varies from 3 to 5 hours, depending on the skill of the user.

A compact but powerful system monitor is supplied with the SDK-85 to provide general software utilities and system diagnostics. It comes in a pre-programmed ROM.

The SDK-85 communicates with the outside world through either the on-board LED Display/Keyboard combination or, the user's TTY terminal (Jumper Selectable). Both memory and I/O can be easily expanded by simply soldering in additional devices in locations provided for this purpose. A large area of the board (45 sq. in.) is laid out as general purpose wire-wrap for the user's custom interfaces.

Only a few simple tools are required for assembly; soldering iron, cutters, screwdriver, etc. The SDK-85 User's Manual contains step-by-step instructions that make assembly easy, and eliminate mistakes. Once construction is complete, the user connects his kit to a power supply and the SDK-85 is ready to go. The monitor starts immediately upon power-on or reset.

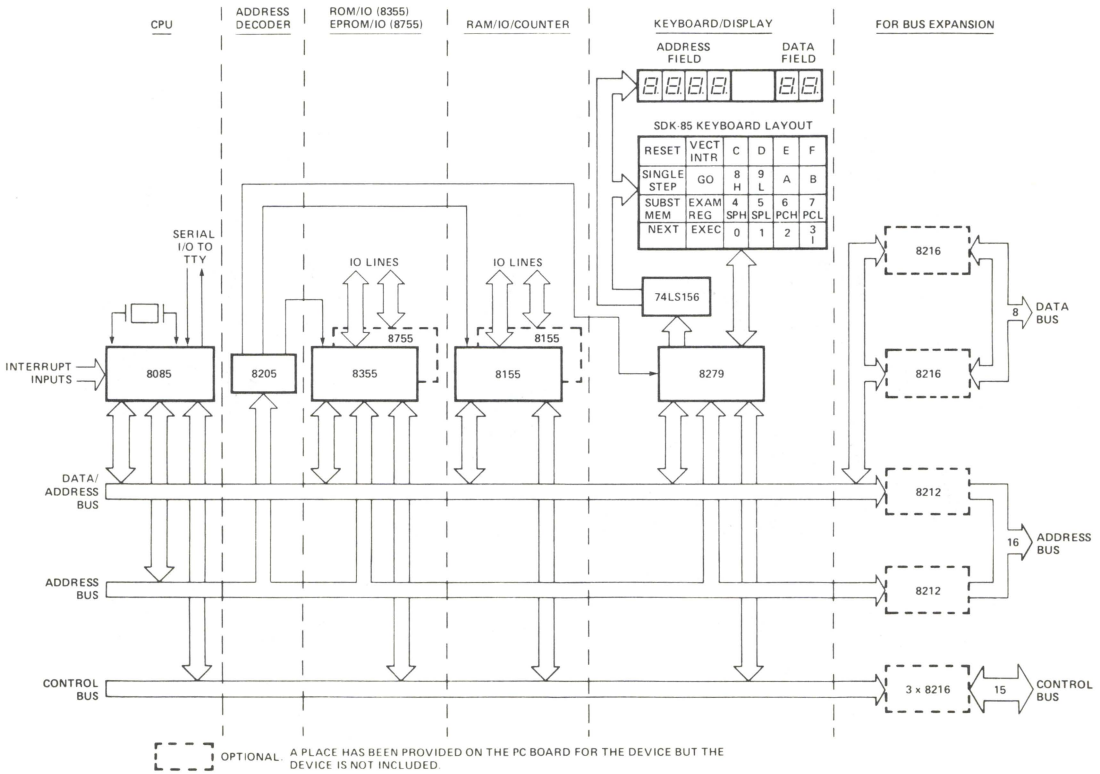
Keyboard Monitor Commands

- Reset — Starts the monitor
- GO — allows you to execute a user program
- Single Step — allows you to execute a user program one instruction at a time — useful for debugging
- Substitute Memory — allows you to examine and modify memory locations
- Examine Register — allows you to examine and modify the 8085's register contents
- Vector Interrupt — a user interrupt button

Teletype Monitor Commands

- Display Memory — displays multiple memory locations
- Substitute Memory — allows you to examine and modify memory locations one at a time
- Insert Instructions — allows you to store multiple bytes in memory
- Move Memory — allows you to move blocks of data in memory
- Examine Register — allows you to examine and modify the 8085's register contents
- GO — allows you to execute user programs

In addition to detailed information on using the monitors, the SDK-85 User's Manual provides circuit diagrams, a monitor listing, and a description of how the system works.



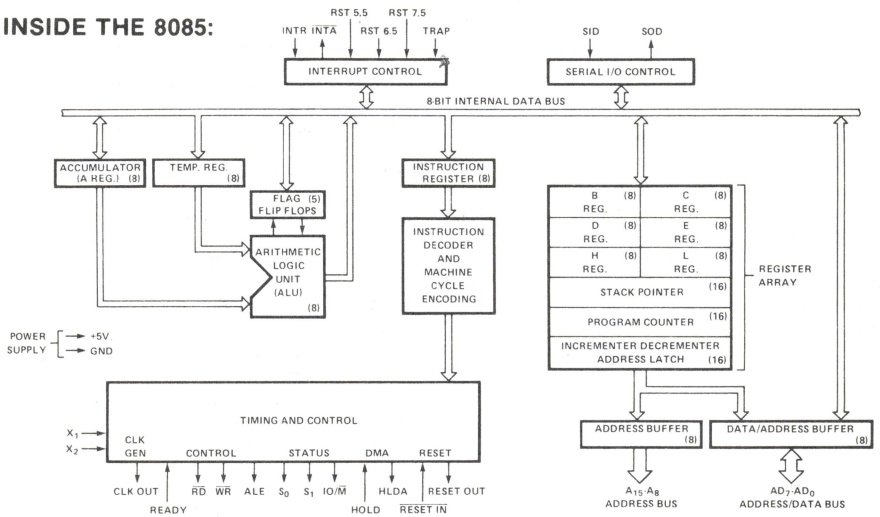
SDK-85 FUNCTIONAL BLOCK DIAGRAM

The SDK-85 is designed around Intel's 8085 Microprocessor. The Intel® 8085 is a new generation, complete 8-bit parallel central processing unit (CPU). Its instruction set is 100% software upward compatible with the 8080A microprocessor, and it is designed to improve the present 8080's performance by higher system speed. Its high level of system integration allows a minimum system of three IC's: 8085 (CPU), 8156 (RAM) and 8355/8755 (ROM/PROM).

The 8085 incorporates all of the features that the 8224 (clock generator) and 8228 (system controller) provided for the 8080, thereby offering a high level of system integration.

The 8085 uses a multiplexed Data Bus. The address is split between the 8-bit address bus and the 8-bit data bus. The on-chip address latches of 8155/8156/8355/8755 memory products allows a direct interface with 8085.

INSIDE THE 8085:



- SEVEN 8-BIT REGISTERS. SIX OF THEM CAN BE LINKED IN REGISTER PAIRS FOR CERTAIN OPERATIONS.
- 8-BIT ALU.
- 16-BIT STACK POINTER (STACK IS MAINTAINED OFFBOARD IN SYSTEM RAM MEMORY).
- 16-BIT PROGRAM COUNTER.

8085 INSTRUCTION SET Summary of Processor Instructions

Mnemonic	Description	Instruction Code[1] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock[2] Cycles
MOVE, LOAD, AND STORE										
MOVr1,r2	Move register to register	0	1	D	D	D	S	S	S	4
MOV M,r	Move register to memory	0	1	1	1	0	S	S	S	7
MOV r,M	Move memory to register	0	1	D	D	D	1	1	0	7
MVI r	Move immediate register	0	0	D	D	D	1	1	0	7
MVI M	Move immediate memory	0	0	1	1	0	1	1	0	10
LXI B	Load immediate register Pair B & C	0	0	0	0	0	0	0	1	10
LXI D	Load immediate register Pair D & E	0	0	0	1	0	0	0	1	10
LXI H	Load immediate register Pair H & L	0	0	1	0	0	0	0	1	10
STAX B	Store A indirect	0	0	0	0	0	0	1	0	7
STAX D	Store A indirect	0	0	0	1	0	0	1	0	7
LDAX B	Load A indirect	0	0	0	0	1	0	1	0	7
LDAX D	Load A indirect	0	0	0	1	1	0	1	0	7
STA	Store A direct	0	0	1	1	0	0	1	0	13
LDA	Load A direct	0	0	1	1	1	0	1	0	13
SHLD	Store H & L direct	0	0	1	0	0	0	1	0	16
LHLD	Load H & L direct	0	0	1	0	1	0	1	0	16
XCHG	Exchange D & E, H & L Registers	1	1	1	0	1	0	1	1	4

Mnemonic	Description	Instruction Code[1] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock[2] Cycles
STACK OPS										
PUSH B	Push register Pair B & C on stack	1	1	0	0	0	1	0	1	12
PUSH D	Push register Pair D & E on stack	1	1	0	1	0	1	0	1	12
PUSH H	Push register Pair H & L on stack	1	1	1	0	0	1	0	1	12
PUSH PSW	Push A and Flags on stack	1	1	1	1	0	1	0	1	12
POP B	Pop register Pair B & C off stack	1	1	0	0	0	0	0	1	10
POP D	Pop register Pair D & E off stack	1	1	0	1	0	0	0	1	10
POP H	Pop register Pair H & L off stack	1	1	1	0	0	0	0	1	10
POP PSW	Pop A and Flags off stack	1	1	1	1	0	0	0	1	10
XTHL	Exchange top of stack, H & L	1	1	1	0	0	0	1	1	16
SPHL	H & L to stack pointer	1	1	1	1	1	0	0	1	6
LXI SP	Load immediate stack pointer	0	0	1	1	0	0	0	1	10
INX SP	Increment stack pointer	0	0	1	1	0	0	1	1	6
DCX SP	Decrement stack pointer	0	0	1	1	1	0	1	1	6

8085 INSTRUCTION SET Summary of Processor Instructions (Cont.)

Mnemonic	Description	Instruction Code[1] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock[2] Cycles
JUMP										
JMP	Jump unconditional	1	1	0	0	0	0	1	1	10
JC	Jump on carry	1	1	0	1	1	0	1	0	7/10
JNC	Jump on no carry	1	1	0	1	0	0	1	0	7/10
JZ	Jump on zero	1	1	0	0	1	0	1	0	7/10
JNZ	Jump on no zero	1	1	0	0	0	0	1	0	7/10
JP	Jump on positive	1	1	1	1	0	0	1	0	7/10
JM	Jump on minus	1	1	1	1	1	0	1	0	7/10
JPE	Jump on parity even	1	1	1	0	1	0	1	0	7/10
JPO	Jump on parity odd	1	1	1	0	0	0	1	0	7/10
PCHL	H & L to program counter	1	1	1	0	1	0	0	1	6
CALL										
CALL	Call unconditional	1	1	0	0	1	1	0	1	18
CC	Call on carry	1	1	0	1	1	1	0	0	9/18
CNC	Call on no carry	1	1	0	1	0	1	0	0	9/18
CZ	Call on zero	1	1	0	0	1	1	0	0	9/18
CNZ	Call on no zero	1	1	0	0	0	1	0	0	9/18
CP	Call on positive	1	1	1	1	0	1	0	0	9/18
CM	Call on minus	1	1	1	1	1	1	0	0	9/18
CPE	Call on parity even	1	1	1	0	1	1	0	0	9/18
CPO	Call on parity odd	1	1	1	0	0	1	0	0	9/18
RETURN										
RET	Return	1	1	0	0	1	0	0	1	10
RC	Return on carry	1	1	0	1	1	0	0	0	6/12
RNC	Return on no carry	1	1	0	1	0	0	0	0	6/12
RZ	Return on zero	1	1	0	0	1	0	0	0	6/12
RNZ	Return on no zero	1	1	0	0	0	0	0	0	6/12
RP	Return on positive	1	1	1	1	0	0	0	0	6/12
RM	Return on minus	1	1	1	1	1	0	0	0	6/12
RPE	Return on parity even	1	1	1	0	1	0	0	0	6/12
RPO	Return on parity odd	1	1	1	0	0	0	0	0	6/12
RESTART										
RST	Restart	1	1	A	A	A	1	1	1	12
INCREMENT AND DECREMENT										
INR r	Increment register	0	0	D	D	D	1	0	0	4
DCR r	Decrement register	0	0	D	D	D	1	0	1	4
INR M	Increment memory	0	0	1	1	0	1	0	0	10
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10
INX B	Increment B & C registers	0	0	0	0	0	0	1	1	6
INX D	Increment D & E registers	0	0	0	1	0	0	1	1	6
INX H	Increment H & L registers	0	0	1	0	0	0	1	1	6
DCX B	Decrement B & C	0	0	0	0	1	0	1	1	6
DCX D	Decrement D & E	0	0	0	1	1	0	1	1	6
DCX H	Decrement H & L	0	0	1	0	1	0	1	1	6
ADD										
ADD r	Add register to A	1	0	0	0	0	S	S	S	4
ADC r	Add register to A with carry	1	0	0	0	1	S	S	S	4
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7
ADI	Add immediate to A	1	1	0	0	0	1	1	0	7
ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0	7
DAD B	Add B & C to H & L	0	0	0	0	1	0	0	1	10
DAD D	Add D & E to H & L	0	0	0	1	1	0	0	1	10
DAD H	Add H & L to H & L	0	0	1	0	1	0	0	1	10
DAD SP	Add stack pointer to H & L	0	0	1	1	1	0	0	1	10
SUBTRACT										
SUB r	Subtract register from A	1	0	0	1	0	S	S	S	4
SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S	4
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7
SUI	Subtract immediate from A	1	1	0	1	0	1	1	0	7
SBI	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7
LOGICAL										
ANA r	And register with A	1	0	1	0	0	S	S	S	4
XRA r	Exclusive Or register with A	1	0	1	0	1	S	S	S	4
ORA r	Or register with A	1	0	1	1	0	S	S	S	4
CMP r	Compare register with A	1	0	1	1	1	S	S	S	4
ANA M	And memory with A	1	0	1	0	0	1	1	0	7
XRA M	Exclusive Or memory with A	1	0	1	0	1	1	1	0	7
ORA M	Or memory with A	1	0	1	1	0	1	1	0	7
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7
ANI	And immediate with A	1	1	1	0	0	1	1	0	7
XRI	Exclusive Or immediate with A	1	1	1	0	1	1	1	0	7
ORI	Or immediate with A	1	1	1	1	0	1	1	0	7
CPI	Compare immediate with A	1	1	1	1	1	1	1	0	7
ROTATE										
RLC	Rotate A left	0	0	0	0	0	1	1	1	4
RRC	Rotate A right	0	0	0	0	1	1	1	1	4
RAL	Rotate A left through carry	0	0	0	1	0	1	1	1	4
RAR	Rotate A right through carry	0	0	0	1	1	1	1	1	4
SPECIALS										
CMA	Complement A	0	0	1	0	1	1	1	1	4
STC	Set carry	0	0	1	1	0	1	1	1	4
CMC	Complement carry	0	0	1	1	1	1	1	1	4
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4
INPUT/OUTPUT										
IN	Input	1	1	0	1	1	0	1	1	10
OUT	Output	1	1	0	1	0	0	1	1	10
CONTROL										
EI	Enable Interrupts	1	1	1	1	1	0	1	1	4
DI	Disable Interrupt	1	1	1	1	0	0	1	1	4
NOP	No-operation	0	0	0	0	0	0	0	0	4
HLT	Halt	0	1	1	1	0	1	1	0	5
NEW 8085 INSTRUCTIONS										
RIM	Read Interrupt Mask	0	0	1	0	0	0	0	0	4
SIM	Set Interrupt Mask	0	0	1	1	0	0	0	0	4

NOTES: 1. DDD or SSS: B=000, C=001, D 010, E 011, H 100, L 101, Memory=110, A=111.
2. Two possible cycle times, (6/12) indicate instruction cycles dependent on condition flags.

*All mnemonics copyright ©Intel Corporation 1977

SDK-85 SPECIFICATIONS

Central Processor

CPU: 8085
Instruction Cycle: 1.3 microsecond
Tcy: 330 ns

Memory

ROM: 2K bytes (expandable to 4K bytes) 8355/8755
RAM: 256 bytes (expandable to 512 bytes) 8155
Addressing:
ROM 0000-07FF (expandable to 0FFF with an additional 8355/8755)
RAM 2000-20FF (2800-28FF available with an additional 8155)

Note: The wire-wrap area of the SDK-85 PC board may be used for additional custom memory expansion up to the 64K byte addressing limit of the 8085.

Input/Output

Parallel: 38 lines (expandable to 76 lines).
Serial: Through SID/SOD ports of 8085. Software generated baud rate.
Baud Rate: 110

Interfaces

Bus: All signals TTL compatible.
Parallel I/O: All signals TTL compatible.
Serial I/O: 20 mA current loop TTY

Note: By populating the buffer area of the board, the user has access to all bus signals which enable him to design custom system expansions into the kit's wire-wrap area.

Interrupts

Three Levels: (RST 7.5) — Keyboard Interrupt.
(RST 6.5) — TTL Input
(INTR) — TTL Input

DMA

Hold Request: Jumper selectable. TTL compatible input.

Software

System Monitor: Pre-programmed 8755 or 8355 ROM
Addresses; 0000-07FF.
Monitor I/O: Keyboard/Display or TTY (serial I/O)

Literature

Design Library (Provided with kit):

- SDK-85 User's Manual
- MCS-85 User's Manual
- 8080/8085 Assembly Language Programming Manual
- Intellec® MDS Brochure
- ICE-85 Data Sheet
- PL/M-80 Data Sheet
- 8085/8080 Assembly Language Reference Card

Physical Characteristics

Width: 12.0 in.
Height: 10 in.
Depth: 0.50 in.
Weight: approx. 12 oz.

Electrical Characteristics (DC Power Required — Power Supply Not Included in Kit)

V_{CC} 5V ±5%	1.3 Amps	
V_{TTY} -10V ± 10%	0.3 Amps	(V_{TTY} required only if teletype is connected)

Environmental

Operating Temperature: 0-55°C

μSCOPE™ 820
MICROPROCESSOR SYSTEM CONSOLE

- Provides an interface to microcomputer systems for troubleshooting system problems
- Monitors, displays, and alters register, memory and I/O values for system under test
- Executes diagnostic routines from μScope 820 console overlay memory
- Executes instrument resident software patch routines even when microcomputer system is ROM-based
- Provides a 32-bit hardware breakpoint with bit masking and a 256-word trace memory
- Is a stand-alone, self-contained, rugged portable unit
- Human engineered with easy to read 9-segment hexadecimal displays and extensive operator prompting
- Gives complete control over microprocessor including single step, run with display, or run real-time capability
- Designed to support many different microprocessors
- Has built-in, self-test operation

The μScope™ 820 Microprocessor System Console is a portable, self-contained instrument designed to provide the control, monitoring, and interaction necessary to effectively and quickly evaluate and debug 8-bit microcomputer-based systems in the lab, on the production line, or in the field. Connection to the user's system is through a personality probe that is plugged into the microprocessor socket. Each personality probe is unique to each microprocessor type. The instrument features many different operating and control modes which allow the operator to carry out a number of functional checks on the microcomputer System Under Test (SUT).

The unit has been specificially designed to ease the task of microcomputer system check-out for the lab, production line, and field technician. It also provides the more powerful analytical capabilities necessary to troubleshoot difficult problems by the more experienced, sophisticated user. Preprogrammed test routines resident in front panel PROMs, dedicated high level command keys, visual prompting, and simplified data entry sequences all ease the check-out of microcomputer hardware. For more rigorous diagnostic tasks, the unit provides a 32-bit maskable hardware breakpoint with optional course of action after a breakpoint match, a 256 X 32-bit trace memory and a 128 X 8 overlay RAM that allows real-time entry of test routines via the μScope 820 Microprocessor System Console keyboard.

CHARACTERISTICS

COMMANDS

Reset
Self Test
CPU Reset
Run Real Time
Run with Display
Halt
Single Step
Enable/Disable Breakpoint
Enable/Disable Overlay
Enable Trace All Cycles
Enable Trace at Breakpoint
Examine/Modify Value
- Single Registers
- Double Registers
- CPU States
- Breakpoint Pass Count

Examine/Modify Memory
Examine/Modify I/O
Examine/Modify Overlay Memory
Examine/Modify Next Location
Examine/Modify Last Location
Examine/Modify Breakpoint Condition
Examine/Modify Breakpoint Mask
Examine/Modify Breakpoint Action
Examine/Modify Overlay Origin
Display Trace Data
Clear Entry
Continue
End/Execute
Subroutine Select

CPU CONTROLS

User-selectable commands permit one of four possible CPU operating modes:

1. *Run Real Time* — User's CPU runs at full speed set by user clock. No wait states or cycle stealing are required.
2. *Run with Display* — User's CPU runs at full speed, except that 10 times/sec the instrument halts user's CPU temporarily to acquire display data. Worse case throughput is 95% of real time operation.
3. *Halt* — User CPU halted at next opcode fetch. DMA activity is permitted during HALT.
4. *Single Step* — User CPU executes one instruction then halts.

BREAKPOINT

The breakpoint condition is set by a 32-bit word (16-bit address, 8-bit data, 8-bit status). The breakpoint mask is also set by a 32-bit word which is bit-selectable. There are three courses of action following a breakpoint match:

1. Halt on first opcode fetch following breakpoint match.
2. Halt on first opcode fetch following Nth breakpoint match $1 \leqslant N \leqslant 256$.
3. Execute subroutine beginning at first opcode fetch following breakpoint match.

All breakpoint actions following a match are controlled by the breakpoint enable/disable switch except for trace recording and the Sync Trigger Output. The Sync Output is a negative true TTL output that occurs whenever a breakpoint match occurs.

Pulse Width = 180 nsec typ
Output High = 2.5 V min, –1.2 mA
Output Low = 0.5 V max, 24.0 mA

TRACE

The trace memory is a 256-word memory with each word consisting of 16 address bits, 8 data bits and 8 status bits. The memory is a circular buffer which records the last 256 cycles (words) prior to a user CPU halt or DISPLAY TRACE command. Trace data can be recorded on all CPU cycles or only when breakpoint matches occur (independent of breakpoint enable/disable status). In addition, the operator can initiate a panel freeze which temporarily stops all trace data recording, and allows display of previously recorded data without halting the user CPU.

DATA ENTRY

All single and double byte items can be entered via the front panel hexadecimal keypad. In addition, all single byte items can be optionally entered via eight binary input keys.

MEMORY OVERLAY

The μScope™ 820 Microprocessor System Console allows memory read/writes of the user CPU in any assigned 1K or 2K block to be made to the instrument's overlay memory. For 1K block assignments, the first 128 bytes reside in the instrument's RAM memory while the remaining 896 bytes reside in the interchangeable front panel ROM/EPROM (either Intel's 2716 EPROM or Intel's 2316E ROM). For 2K block assignments, again the first 128 bytes are from RAM and the remaining 1920 bytes are from the front panel 2716/-2316E.

DATA DISPLAY

Eight hexadecimal 0.5 in. LEDs are provided for the simultaneous display of 4 bytes of information. The displays are physically separated into two groups. The first group displays 2 bytes of address, while the second group displays CPU data, status, single and double byte register values, or single and double byte breakpoint values. In addition, eight binary displays are used to provide quick recognition of single byte binary data patterns.

SELF TEST

The necessary hardware and software have been incorporated into the instrument to facilitate the self-checking of the majority of its operations. Included in these self tests are:

- Bit tests of all breakpoint condition and mask latches.
- Bit tests of all RAM.
- Verifies checksum on all operating system ROMs.
- Clears trace memory and performs bit test on trace RAM.
- Checks miscellaneous I/O ports and peripheral components.
- Lights all front panel displays for user verification.

CONNECTION

Four external connections to the μScope 820 Microprocessor System Console are provided:

- 1.2 m (4 ft), 50 conductor flat cable for connection to the microprocessor probe.
- 20-pin board edge connector for the probe personality PROM.
- 24-pin zero force insertion sockets for overlay EPROM/ROM.
- One recessed pin for breakpoint sync output.

PHYSICAL CHARACTERISTICS

Width:	479 mm	(18-7/8 in.)
Length:	394 mm	(15-1/2 in.)
Height (top closed):	168 mm	(6-5/8 in.)
Height (top removed):	117 mm	(4-5/8 in.)
Weight:	9.1 kg	(20 lb)

ELECTRICAL REQUIREMENTS

Voltage: 100, 120, 220, 240 — 10% +5%, 110VA max
Frequency: 48–63 Hz

ENVIRONMENTAL CONDITIONS

Operating Temperature: 0°C to 55°C (32°F to 130°F)
Storage Temperature: -40°C to 75°C (-40°F to 167°F)
Humidity: 95% RH, 15°C to 40°C (59°F to 104°F) non condensing

ACCESSORIES SUPPLIED

Two keys
One fuse for 220/240 V operation
One 2.3 m (7.5 ft) power cord
One Operator's Manual
One Hardware Reference Manual

ORDERING INFORMATION

Part Number	Description
USC-820	Microprocessor System Console

CPU CONTROL

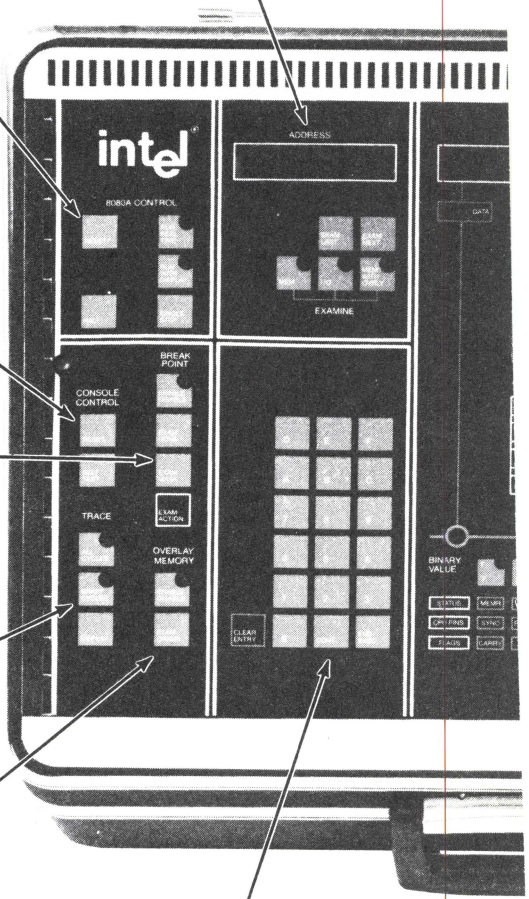
The instrument provides complete control over the operation of the microprocessor in the System Under Test (SUT). The user CPU can be forced to HALT, SINGLE STEP, RESET, RUN REAL TIME, or RUN WITH DISPLAY. All of the above CPU commands can be issued without impacting other operational parameters or diagnostic sequences that have been set up.

ADDRESS DISPLAY/SELECT

A dedicated, 4-digit hexadecimal address display allows the following address information to be displayed:

- The address of any memory location.
- The I/O port number of any I/O port.
- The address of any overlay memory location.
- The address of the overlay memory origin assignment.
- The address at which the breakpoint is to occur.
- The address portion of the breakpoint mask.
- The address of the given trace record element.

An additional feature of the address display/select logic is that once the operator has initiated a given memory, trace, or I/O examination, it is possible to continue the examination in a sequential fashion either in an ascending or descending address value.



BREAKPOINT CONTROL

The hardware breakpoint of the instrument allows the operator to alter the normal program flow of the SUT. Breakpoint logic is implemented in hardware, thereby eliminating any throughput degradation of the SUT. All 32 bits of the breakpoint condition word are maskable in order to allow the breakpoint condition to be as specific or as general as may be desired.

The occurrence of a breakpoint match can cause an unconditional halt, incrementing of the pass counter, calling of a subroutine, or the recording of a single cycle of trace data. All of these options are selectable via the EXAM ACTION key prior to enabling the breakpoint.

TRACE MEMORY

The console has a full 32-bit word trace memory that records 256 cycles of SUT operation without causing any delays. The trace memory provides information about CPU operation just prior to a CPU halt or just prior to the initiation of a panel freeze via the trace DISPLAY key.

The operator can alternatively elect to have data recorded on all SUT microprocessor cycles or only when program execution of the SUT microprocessor generates a breakpoint match. Once the data is recorded, sequential examination of the data can be accomplished simply by depressing the EXAM NEXT or EXAM LAST keys.

OVERLAY MEMORY

A unique feature of the unit is the ability to map its memory onto the SUT memory space. Using the overlay memory allows the operator to insert patch, exercise, or diagnostic subroutines at any location or point of execution in the SUT program. The subroutine can either be entered via the front panel hexadecimal keypad or via the front panel's ROM/PROM socket.

By using the unit's overlay memory, the operator can quickly set up the SUT to execute special maintenance or troubleshooting programs that permit rapid evaluation of system operation.

ADDRESS, DATA, AND CONTROL ENTRY

The address, data, and control variable entry into the instrument is accomplished via the conveniently located hexadecimal keypad.

For selection of the information to be displayed or modified the operator enters the hexadecimal value of the desired address, I/O port number or label assigned to each of the registers. Once this entry is made, the operator can then elect to either CONTINUE data entry if modification is desired or press the END/EXECUTE key if examination only is desired. For all data entry sequences that potentially require multiple value entry, the μScope™ 820 Microprocessor System Console provides operator prompting to indicate the specific information expected.

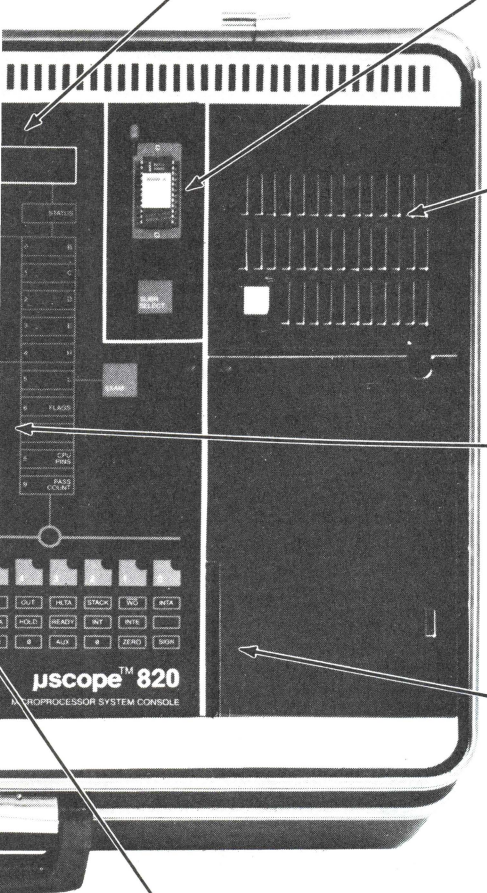
VALUE DISPLAY/SELECT

The value displays provide clear and easy to use information. Together with the address display, they provide simultaneous readout of trace vectors, breakpoint conditions and breakpoint mask values, memory contents and I/O port contents. In addition, the display allows readout of all single and double byte register values, the state of CPU pins and flags, information regarding the course of action following the occurrence of a breakpoint, as well as information regarding the breakpoint pass count.

The information displayed by the 4-digit hexadecimal value readouts is selected via the hexadecimal keypad in conjunction with any of the instrument's 11 dedicated examine keys. Further, the information is either displayed statically or is continually updated 10 times/sec if the unit is in the run with display mode.

PROM/ROM SOCKET

A front panel socket is provided for mounting 2K PROMs or ROMs that serve as storage for preprogrammed test subroutines. The actual useable program space of the PROM/ROM is 1920 bytes. The remaining 128 bytes of storage, shadowed by RAM, are used by the unit to identify up to 16 separate subroutines in the PROM/ROM and to define the specific instrument states and conditions under which the subroutine will be called. Each of the separate subroutines is uniquely enabled by the SUBR SELECT key and the hex keypad.



POWER SUPPLY

The system console is complete with its own fully regulated DC power supply that provides all the DC power required by the unit itself, as well as that which is required by the associated microprocessor probe. The supply is completely self-contained, including its own AC on/off switch, line fuse, line filter and power cord. An additional feature of the power supply is that it has been designed to permit line voltage selection in the field to facilitate operation with a wide range of AC line voltages and frequencies.

BREAKPOINT ACTION

Following the occurrence of a breakpoint match, the operator has the flexibility to execute a number of different diagnostic operations. The selection of these alternate courses of action is accomplished by pushing the EXAM ACTION key and then entering the assigned value of the specific action desired via the hex keypad. Further keypad entries specify the parametric value of the action selected such as the number of breakpoint pass counts or the start address of a subroutine call following a breakpoint.

PROBE CONNECTION

The instrument is intended to work with many of the microprocessors that are available today. This is accomplished by standardized interface logic which transmits and receives various address, data, and control signals between the system console and the circuitry of the particular probe. The interconnect circuitry between the instrument and probe has been designed to drive a 4-foot cable that permits convenient positioning of the panel and the SUT.

In addition, a board edge connector has been provided for a personality ROM that provides front panel definition and interpretation of specific control signals for different types of microprocessors. This personality ROM is supplied with each probe kit.

BINARY DATA DISPLAY/MODIFICATION

All 8-bit values can be displayed in binary format on the instrument. The binary display operates in parallel with the hexadecimal display and it is provided for those instances where operator recognition is enhanced by binary presentation. The selection procedure for the binary data display is identical to that for the hexadecimal value display. Once the selection has been made, the operator can alter the value by means of further hex keypad entries or by changing the binary state of any of the data bits via the 8 binary data switches.

FRONT PANEL

The front panel of the μScope™ 820 Microprocessor System Console has been designed to be rugged and durable as well as easy to use and understand. A plastic overlay that employs membrane switch contacts provides long lasting durability as well as protection from accidental spills. Audio and tactile feedback for the membrane switches is provided for operator convenience.

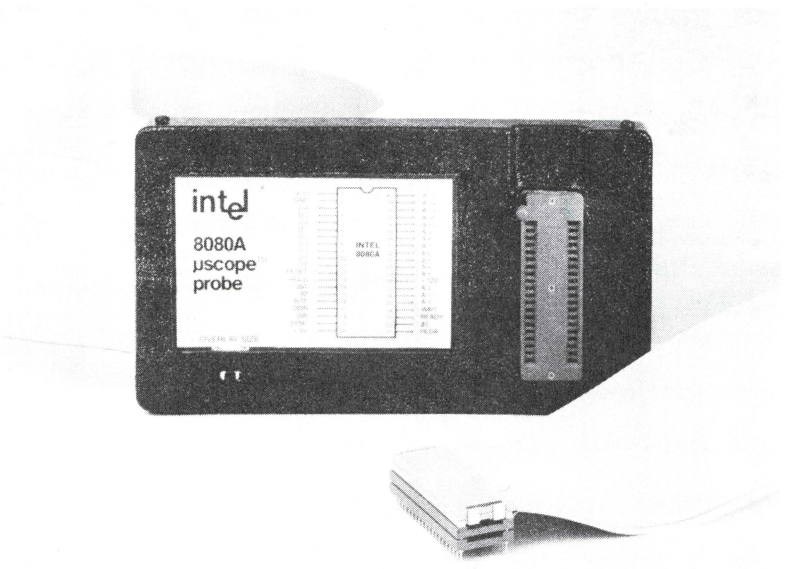
Ease of use of the front panel has been further enhanced by human engineering with functional grouping of switches as well as LEDs that prompt the operator during data entry sequences. Graphics have also been added to reinforce the functional switch groupings as well as data entry procedures.

μSCOPE™ PROBE 8080A

- Provides interconnection for 8080A Microprocessor-based Systems to the μScope™ 820 Microprocessor System Console
- Comes complete with cable, buffer box, personality ROM, and μScope 820 system console overlay
- Has user system interconnect cable with integral ground plane for low noise operation
- Connects via a 4 foot cable to the μScope 820 Console
- Operates over a broad range of environmental conditions
- Provides complete control over the system under test, yet causes minimal interference with system under test operation
- Fits securely in the console carrying case during transit
- Provides complete protection for plug pins during transit

The probe 8080A provides the μScope 820 console with the ability to interact with 8080A Microcomputer-based Systems. The purpose of the probe is to interface the μScope 820 console to the CPU of the System Under Test (SUT). All of the interface signals and the associated circuitry have been designed to be effectively transparent to the SUT. CPU data, address, and clock lines are sensed by the probe 8080A, with only the CPU control lines being switched. In addition, all SUT loading and timing degradations have been minimized by specially designed buffer circuitry.

The mechanical design of the probe is compact, rugged, and allows proper operation of the probe and the console over the full ambient range specified. The buffer circuitry and the ground plane design of the interconnect cable provide low noise electrical signals while allowing the SUT to be 4 feet from the system console.



GENERAL

μSCOPE 820 CONSOLE INTERCONNECT

The probe interconnection to the μScope 820 console is accomplished via a 1.2 m (4 ft) flat cable. 50-pin mating connectors plug into a board edge connector in the power cord compartment of the instrument and into a flat cable connector on the buffer box.

SYSTEM UNDER TEST (SUT) INTERCONNECT

Interconnection from the buffer box to the SUT is accomplished with a 406 mm (16 in.) flat cable, complete with an integral ground plane, which is terminated with a low profile 40-pin DIP connector. The DIP connector is inserted into the SUT 8080A socket and the 8080A itself is plugged into the 40-pin socket provided on the probe buffer box.

μSCOPE 820 CONSOLE CONFIGURATION

Several features of the console are directly determined by the probe being used with it. The instrument features that are determined by the 8080A interface probe are:

- Single Registers: A, B, C, D, E, H, L
- Double Registers: BC, DE, HL, PC, SP
- CPU States: Flags, CPU pins (SYNC, RESET, HLDA, HOLD, READY, INT, INTE)
- Trace/Breakpoint Word Size: 32 bits with 16 bits of address, 8 bits of data and 8 bits of CPU status.

ELECTRICAL SPECIFICATIONS

All DC specifications are in addition to user system parameters. All capacitance values include cables and connectors.

Non-Intercepted Signals

$\phi 1$, $\phi 2$	±10 μA max; 55 pF typical
A_{15}–A_0, D_7–D_0	–0.25 mA max @ 0.45V; 30 μA max @ 5.25V; 49 pF typical
+12V Supply	15 μA max
WAIT	35 pF typical (capacitive loading only)

Intercepted Signals

Outputs to user system:

SYNC	20 mA min @ 0.5V; –1 mA min @ 2.7V; 40 pF typical
HOLDA, INTE, DBIN, and $\overline{WR}$	4 mA min @ 0.4V; –0.2 mA min @ 2.7V; 40 pF typical

Inputs from user system:

INT, READY, RESET	40 μA max @ 2.7V; –0.72 mA max @ 0.4V; 50 pF typical
HOLD	60 μA max @ 2.7V; –1.08 mA max @ 0.4V; 50 pF typical

CONNECTIONS

Three external connections to the probe are provided:

- 50-pin flat cable connector on buffer box
- 40-pin zero insertion socket for the 8080A
- 40-pin low profile replaceable IC DIP connector for connection to SUT

CHARACTERISTICS

PHYSICAL CHARACTERISTICS

Probe Buffer Box:

Height:	19 mm	(3/4 in.)
Length:	184 mm	(7-1/4 in.)
Width:	95 mm	(3-3/4 in.)

User System Interconnect Cable:

Width:	57 mm (2-1/4 in.)
Length:	406 mm (16 in.) flat cable

μScope 820 Console Personality ROM PC Card:

Height:	19 mm (3/4 in.)
Width:	57 mm (2-1/4 in.)
Length:	83 mm (3-1/4 in.)

POWER REQUIREMENTS

Power supplied by μScope™ 820 Microprocessor System Console.

ENVIRONMENTAL CONDITIONS

Operating Temperature:	0° to 55°C (32° to 130°F)
Storage Temperature:	–40°C to 75°C (–40° to 167°F)
Humidity:	95% RH, 15° to 40°C (59° to 104°F) noncondensing

ACCESSORIES SUPPLIED

One μScope 820 System Console Overlay
One Personality ROM
One Hardware Reference Manual

ORDERING INFORMATION

Part Number	Description
PRB-80	8080A Interface Probe

MICROCOMPUTER TRAINING PROGRAMS

Courses presented at training centers and customer facilities.

Training Centers
- Boston
- Chicago
- Santa Clara

Scheduled on a continuing basis throughout the year.

On-site courses tuned to customer requirements.

System demonstrations.

Hands-on laboratory sessions reinforce lecture.

Training center classes limited to 14 attendees.

Intellec® Microcomputer Development Systems with In-Circuit Emulators in laboratory.

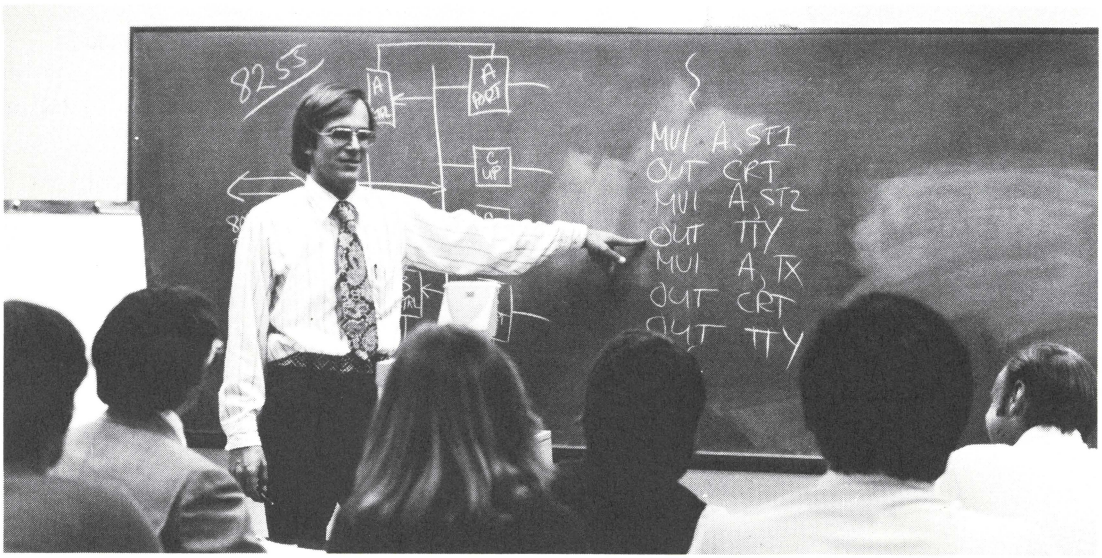
Microcomputers are being used in hundreds of applications from simple controllers to complex data processing systems. To enable users to bring microcomputers into their applications, Intel offers a selection of workshops that are designed to provide you with the "tools" for making optimum use of Intel microcomputers in system development.

COURSE PREREQUISITES:

MCS-80/85™ System, MCS-48™ System, PL/M-80 Language/Software Design, General Purpose Peripherals, Dedicated Function Peripherals Workshops. The course prerequisites are a knowledge of binary and hexadecimal number systems and basic logic functions. To attain maximum benefit from course presentation, some background in logic design or computer programming is recommended.

RMX-80™ System Workshop. A working knowledge of the 8080 (or 8085) and the Intellec Microcomputer Development System, or attendance at the MCS-80/85 System Workshop is required. For those that are unfamiliar with the concepts and implementation of modular program design, we recommend attendance at the PL/M-80 Language/Software Design Workshop.

REGISTRATION AND ADDITIONAL INFORMATION: Contact MCSD Training at Intel Corporation, Santa Clara, California 95051, (408) 987-8003 or 987-8004 or your local Intel sales office.



MCS-80/85 System Workshop

This workshop will prepare the student to design and develop a system using the Intel® 8080/8085 microprocessors through the use of lecture, demonstration, and laboratory "hands-on" experience with the Intellec® Microcomputer Development System and In-Circuit Emulator.

COURSE OUTLINE:

Day 1

Introduction
a. Microprocessor System
   1. Function
   2. Organization
   3. Programming
b. Central Processor Overview
   1. Functional Sections
   2. Programming Model
   3. Execution Sequence

Assembly Language Instructions
a. Input/Output
b. Register/Memory Reference
c. Arithmetic, Logical, Rotates

Programmed Input/Output
a. Status Request
b. Command
c. Data Transfer

Development System
a. Function
b. System Monitor
c. Disk Operating System

Debugging With the System Monitor
a. Break Points
b. Examine Registers

Laboratory
a. Using the System Monitor
b. Program Instruction Sequences
c. Debugging and Break Points

Day 2

Disk Operating System Modules
a. Macro Assembler
b. Text Editor
c. File Utility Commands

System Timing
a. Instructions
b. State Transition
c. Signal Relationships
d. Specifications

Subroutines
a. Invocation
b. Stack Memory
c. Parameters

Interrupt System
a. Description
b. RST Instruction
c. Service Subroutines

Laboratory
a. Using the Disk Operating System
b. Program Assembly and Execution

Day 3

Branch Tables
a. Application
b. Construction

Direct Load/Store Instructions

Special Purpose Instructions

Macros
a. Definition
b. Reference
c. Expansion

8080A CPU Set
a. 8228/8238 System Controller
b. 8224 Clock Generator
c. RAM/ROM/PROM Address Decoding
d. Memory Mapped I/O

8085 CPU Set
a. 8085 Bus Structure
b. 8355/8755 ROM/EPROM and I/O
c. 8155 RAM/Timer and I/O

Laboratory
a. Monitor Subroutines
b. Program DEBUG Under Disk Operating System

Day 4

Family Peripherals
a. Memory Design
   1. 8708 PROM
   2. 2114 RAM
b. I/O Design
   1. 8255 Parallel Interface
   2. 8251 Serial Interface

In-Circuit Emulator
a. Prototype Development
b. Resource Sharing
c. Mapping Commands
d. Utility Commands
e. Debug Commands
f. Emulation Syntax

Laboratory
a. Use of the In-Circuit Emulator for System Debugging

Day 5

Single Board Computers
a. Use as a System Component
b. Parallel I/O Options
c. Serial I/O Options
d. Interrupt System
e. Family Boards

Relocation and Linkage
a. ISIS-II LINK and LOCATE Commands
b. Relocatable Libraries
c. Parameter Passing
d. System Design

RMX-80 Real-time Multi-tasking Executive System Workshop

This workshop will cover the concepts of multi-tasking, i.e., what a task is, concurrency of tasks, asynchronous events, priorities and scheduling, resource sharing, interrupts and inter-task communication. Also included will be discussions on system design, writing tasks, system generation and debugging.

COURSE OUTLINE:

Day 1

Introduction

a. Preview of Workshop

What is RMX/80

a. Constituent Parts of the RMX/80 Product
b. Overview of the RMX/80 Development Process

Review of the Development Process

a. Intel 8080/8085 Translators
   1. Assembler
   2. PL/M-80 Compiler
   3. Translator DEBUG option (In-Circuit Emulator)
b. ISIS-II Commands
c. LINKing Task Modules with the RMX/80 Nucleus and Intel Provided Tasks
d. LOCATEing the Final Module in an End Product Environment (Single Board Computer Modules)
e. Debugging the Task Environment

Real Time Asynchronous Event Processing

a. Definition of Terminology
b. Recognition of Asynchronous Events
   1. Polling (Status Loop)
   2. Preemption (Interrupt)
c. The Single Unit Program
   1. Status Environment
   2. Interrupt Environment
d. Program Execution
   1. Sequential Processing
   2. Concurrent Processing

Day 2

RMX/80 Model

a. Task
   1. Single Unit Program
b. Exchanges and Messages
   1. SEND Function
   2. WAIT Function
c. Context Switching and Dispatching of Tasks
   1. Task States
d. A Sequential Model
e. A Concurrent Model
f. The Interrupt Exchange/Message
   1. Interrupt Levels

RMX/80 Terminal Handler

a. Message Formats
b. Service Request Exchanges
   1. Terminal Input (Line Edited)
   2. Terminal Output
c. Service Response Exchanges

Implementing an RMX Task(s) Module

a. Translator INCLUDE option
b. Creating a Task(s) Module
c. RMX/80 System Creation
d. Configuration Module
e. System Generation

Laboratory

a. Implementation of Two Modules

Day 3

Laboratory

a. Implement Configuration Module and System Generation

Use of In-Circuit Emulator to Emulate Task System

a. Hardware Considerations

Terminal Handler

a. Line Edit Input
b. Control Character Table
c. Alarm Exchange — Alarm Message Type
d. DEBUGGER and Wakeup Exchange

DEBUGGER Task

a. Configuration
b. Invoking the DEBUGGER
c. DEBUGGER Commands

Day 4

RMX/80 Interrupt Processing

a. Interrupt Exchanges
b. Enabling and Disabling Interrupt Levels
c. Software Priorities and Interrupt Masking
d. SBC 80/10 User Required Interrupt Services
   1. Interrupt Poll Routines
   2. Clock Control Routines
e. User Defined Interrupt Handling

Line Printer Driver Task Example

a. Interrupt Handling
   1. Using RMX/80 Model
   2. User Defined Handler

Analog I/O Tasks

High Speed Math Unit Tasks

Laboratory

a. Interrupt Handling

Day 5

Disk File System

a. Disk File System Services
   1. File Access
   2. File Read/Write
   3. File Seek
   4. Disk I/O
b. Add-on ISIS-II Services
   1. File Attributes
   2. File Rename
   3. File Delete
c. Configuration
   1. Free Space Manager
   2. Concurrent Operation
d. File System Structure
   1. Directory Format
   2. File Data Format

Laboratory

a. Disk File System

MCS - 48™ System Workshop

This workshop will prepare the student to design and develop a system using the Intel 8048 microprocessor through the use of lecture, demonstration and laboratory "hands-on" experience with the Intellec® Development System, PROMPT-48, and In-Circuit Emulator.

COURSE OUTLINE:

Day 1

Orientation

Introduction

a. Microprocessor System
   1. Function
   2. Organization
   3. Programming
b. 8048 Overview
   1. Functional Sections
   2. Programming Model
   3. Execution Sequence

Assembly Language Instructions

a. I/O Instructions
b. Data Move Instructions
c. Increment/Decrement Instructions
d. Branch Instructions
e. Worksession No. 1
f. Accumulator Group Instructions
   1. ADD/ADDC
   2. Logicals

PROMPT-48

a. Function
b. Operation

Laboratory Exercise

a. Program Entry and Execution Using PROMPT-48

Day 2

Assembly Language Instructions

a. Accumulator Group Instructions
   1. Flags
   2. Rotates
b. Specials (XCH, DA, SWAP)
c. Worksession No. 2
d. Subroutines
   1. Invocation
   2. Stack Operation
e. Interrupt System
   1. Description
   2. Service Subroutines
   3. Multiple Source Systems

Development System

a. Function
b. Disk Operating System

Text Editor and Macro Assembler

a. Function
b. Operation

Laboratory Exercise

a. Bootstrap Procedures
b. Create, Edit, and Assemble Source Program
c. Execute Program

Day 3

System Timing

a. Basic Timing and Timer
b. Bus Timing for Peripheral Devices

Peripherals and Design

a. Expanding Memory*
   1. Program Memory (1, 2K ROMs)
   2. Data Memory (RAMs)
b. Expanding Ports (8243)*
   1. Device Characteristics
   2. Software Control of Ports
c. Combination Chips*
   1. 8155 RAM and I/O Chip
   2. 8355, 8755 ROM and I/O Chip
d. Peripheral Interfacing (Parallel)*
   1. 8255 Parallel I/O
   2. 8279 Keyboard and Display Interface
      —Keyboard Scanning Techniques
      —Display Refresh

Laboratory Exercise

a. Edit and Assemble Using DOS
b. Execute Using PROMPT-48

Day 4

Peripherals and Design

a. Peripheral Interfacing (Serial)*
   1. Transmission Formats
   2. Asynchronous Operation
   3. RS232C Interface
b. A/D and D/A Interfacing*
   1. Successive Approximation A/D
   2. A/D, D/A Chips
   3. A/D Design

Laboratory Exercise

a. Edit and Assemble Programs
b. Execute Programs

Day 5

8048 Family

a. 8041 Overview
   1. 8041/8048 Difference
   2. 8041 Slave/Master Protocol
b. 8021 Overview
c. 8049 Overview

In-Circuit Emulator

a. Prototype Development
b. Resource Sharing
c. Commands
   1. Mapping
   2. Utility
   3. Interrogation
   4. Emulation

Laboratory

a. Use of the In-Circuit Emulator for System Debugging

*Each section will consist of a design example including schematic, bus loading calculations, software, and timing.

PL/M-80 Language/Software Design Workshop

This workshop will prepare the student for designing, developing and debugging modular PL/M-80 programs using lecture, demonstration, and laboratory "hands-on" experience with the Intellec® Microcomputer Development System and In-Circuit Emulator.

COURSE OUTLINE:

Day 1
Introduction
a. Preview of Course
b. Overview of PL/M, Linking and Relocation
c. Why use a High Level Language

Definitions
Symbols, Identifiers, Reserved Words, Comments, Data Elements, Expressions, Statements, Declarations

Data Elements
Variables, Subscripted Variables, Data Type, Constants

Operators, Operations and Priorities
Arithmetic and Boolean

Evaluating Expressions

Statements
Redefine, Basic, Conditional

Assignment
a. Implement a Given Algorithm in PL/M

Day 2
ISIS-II Disc Operating System
a. Components of System

ISIS-II File Structure
a. System Files
b. User Files
c. Device Files
d. Directory and File Attributes

ISIS-II Commands
a. CUSPS — Commonly Used System Programs
b. Directory and Attribute Commands
c. Rename and Delete Commands
d. Creating System and User Discs

ISIS-II Editor
a. Definition of Terminology
b. Invoking the Editor
c. Editor Commands
d. Editing Existing Files

ISIS-II PL/M 80 Compiler
a. Invoking PL/M
b. Compiler Options

ISIS-II Locate
a. Invoking Locate

Laboratory
a. Introduction to ISIS-II Disc Operating System
b. Creating a PL/M Source File
c. Compiling a PL/M Program
d. Locating and Executing a PL/M Program

Day 3
Review

Procedures
a. Declaration
b. Invocation
c. Program Construction

Data References
a. Based Variables
b. Variable Equivalencing

Statement Labels

Unconditional Transfers

Blocks
a. Concept and Use
b. Scope of Declarations
c. Modular Compilation
d. Modular Program

ISIS-II Link
a. Invoking Link
b. Link Options
c. Assembly Object Modules

Laboratory
a. Compile Program Modules
b. Link and Locate Modules
c. Execute Program

Day 4
Review

ISIS-II Librarian
a. Creating a Library
b. Managing a Library
1. Adding Modules
2. Deleting Modules

ISIS-II System Interfaces
a. System Library

In-Circuit Emulator
a. Definition
b. System Overview
1. Memory and I/C Mapping
2. Breakpoint Capability
3. Dynamic Tracing
4. Control Block

In-Circuit Emulator Software Driver
a. Modes
b. Commands

System Debugging Examples

System Demonstration

Laboratory
a. Create a Library
b. Link Object to a Library
c. Locate
d. Load and Emulate Using In-Circuit Emulator

Day 5
Review

Interrupt Procedures

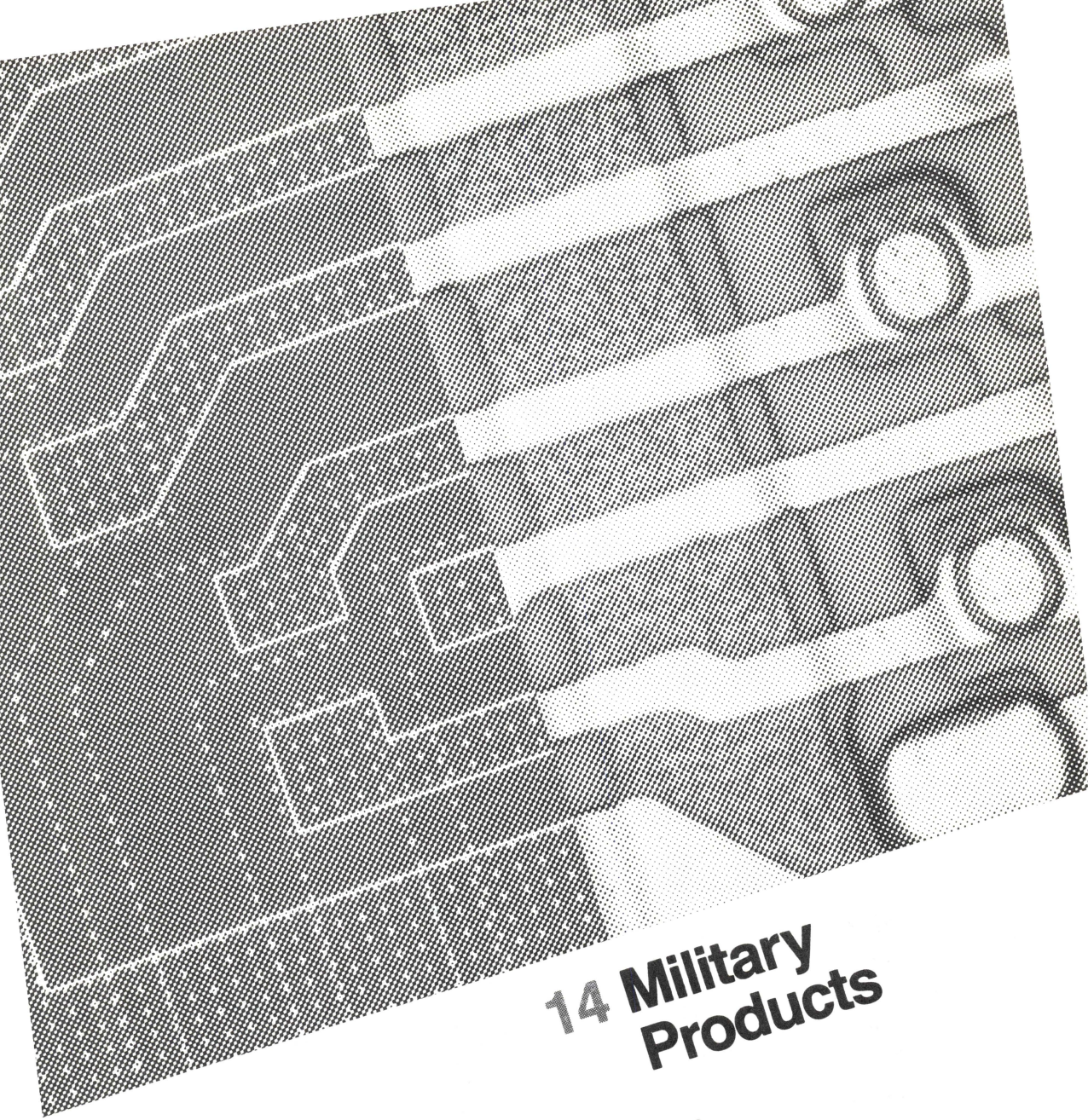
Reentrant Procedures

Predeclared Procedures
a. TIME, MOVE, LENGTH, LAST and SIZE Procedures
b. Type Transfers
c. Shifts and Rotates

The Memory Array and STACKPTR Variables

Discussion of Selected Programs

Laboratory
a. Execution and Debugging of Selected Programs



14 Military Products

INTEL MILITARY PRODUCTS
IC 38510 PROGRAM

In 1977, Intel qualified the first military microprocessor to JAN MIL-M-38510. The JAN version of the 8080A, designated JM38510/420, is manufactured on Intel's DESC-certified production line.

Intel also offers other selected products for high reliability military applications. The in-house IC38510 Program emulates the anticipated JAN processing and lot acceptance requirements and is in full compliance with the testing and screening requirements of MIL-M-38510D and MIL-STD-883B.

Intel Specifications are available which document general and detailed requirements for each of the military products. Detail specifications are organized by generic family and provide all information necessary for non-standard parts submissions in accordance with MIL-STD-749, Step I, Step II, and Step III. These documents are available from your local Intel Sales Office or authorized Intel Distributor.

Three levels of product assurance are offered: Level B, Level C, and Military Temperature Only.

The Military Temperature level products have guaranteed operating characteristics over the specified temperature range and have undergone Intel's rigid product assurance requirements.

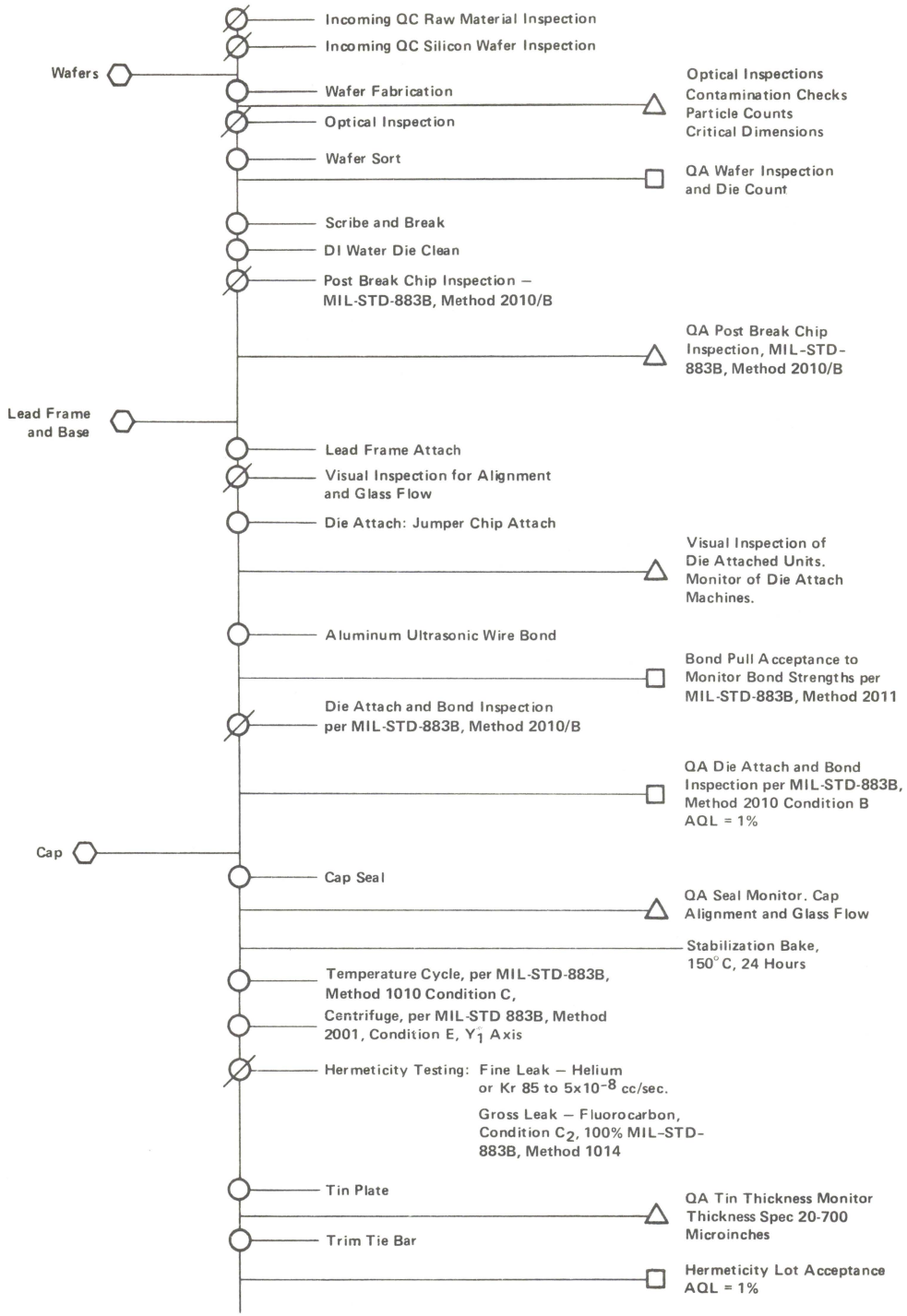
Level B and Level C products are in conformance with MIL-STD-883, Method 5004 requirements, and in addition, have a specified maximum rebond criteria (10%) and a specified burn-in PDA (10%), all documented in the detail specifications, consistent with 38510 requirements. Lot conformance tests are performed in accordance with MIL-STD-883, Method 5005.

INTEL MILITARY PRODUCTS

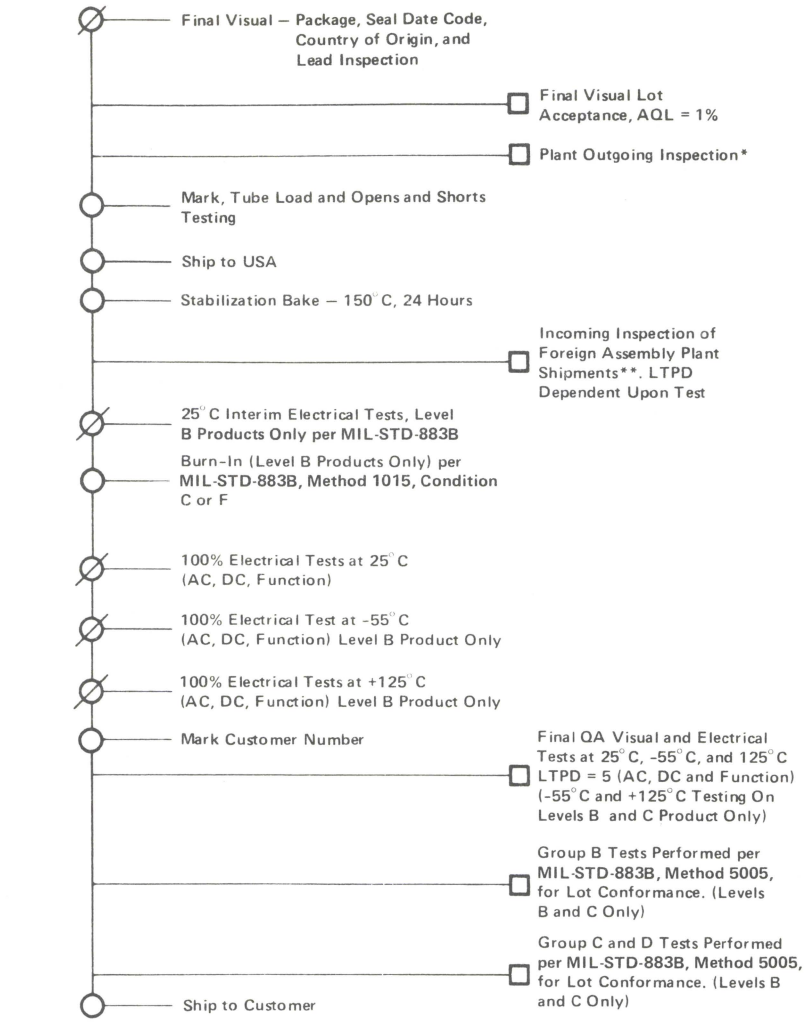
MCS-80™	3000 Series	PROMs	RAMs
M8080A	M3001	M1702A	M2111A
M8212	M3002	M2708	M2102A-4
M8214	M3003	M2716*	M2114*
M8216		M3604A	M2115A
M8224		M3624A	M2115AL
M8226			M2125A
M8228			M2125AL
M8251			M2147*
M8255A			M5101L-4

*New Product to be released by mid-year 1978. Contact Intel representative for details.

LEVEL B AND C
MILITARY PRODUCTS MANUFACTURING FLOW



LEVEL B AND C
MILITARY PRODUCTS MANUFACTURING FLOW (Cont'd)



PIECE PARTS	MANUFACTURING OPERATION	QA MONITOR
⬡	○ MANUFACTURING INSPECTION OR TEST	△ QA LOT ACCEPTANCE

*Outgoing Acceptance (Plant Clearance) Inspections:

Test	LTPD	ACC
1. Hermeticity	5	2
2. Centrifuge	5	2
3. X-Ray	7	1
4. Lead Fatigue	20	0
5. Acoustic (Loose Particles) AQL = .04%		

**Incoming Inspection Testing:

Test	LTPD	ACC
1. X-Ray, Die Attach and Seal Quality	7	1
2. External Visual	7	1
3. Opens and Shorts	7	1
4. Hermeticity	7	1
5. Lead Fatigue	20	0
6. Internal Visual	10	0
7. Bond Pull	7	1
8. Acoustic (1000 Particles) AQL = .04%		

NOTES

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